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A High Step-Up Partial Power Processing DC/DC T-Source Converter for UPS Application

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Abstract: In this paper, a new modified structure of a DC/DC T-source converter is proposed. Since the proposed converter provides high voltage gain, it is suitable for photovoltaic integration into uninterruptible power supply (UPS) systems. The proposed structure employs partial power processing technique to increase the output voltage as well as efficiency without requiring new hardware. Partial power converters (PPCs) process only a fraction of flowing power while the remaining power directly flows through output. This generally causes an improvement in efficiency and output voltage. A total of two structures are presented: conventional partial power T-source converters and improved partial power T-source converters. The key advantage of the improved partial power converter is a higher voltage gain. Furthermore, it reduces the voltage and the current stresses on switches and diodes. The steady-state operation principles are described for both converters and the governed rules and equations are derived. The PPCs and full power converter are compared in terms of efficiency, voltage gain, voltage stress, and current stress of converter elements. The converter performance is evaluated through experimental and simulation studies. The presented results show good consistency with the theoretical analysis.

Keywords: DC/DC converter; partial power processing converter; T-source converter; high voltage gain; uninterruptible power supply (UPS)

1. Introduction

Uninterruptible power supply (UPS) systems have been extensively used in the infrastructure of data centers, communication networks, and IT servers [1,2]. Recently, several studies focused on integrating multiple energy sources into the UPS systems to enhance the performance under all operation modes [3]. As a promising solution, integrating the photovoltaic (PV) system as an eco-friendly generation system into UPS (Figure 1) helps to reduce the cost of the electricity from the grid [4]. The ordinary solution is the connection of several PV arrays in series, but this method is not optimal mainly because of partial shading conditions and mismatched parameters [5–7]. Employing step-up DC/DC converters is the other method to build up DC link voltage [8,9] (blue converter in Figure 1). Output characteristics of PV are nonlinear and depend on the temperature, irradiance intensity, and angle; therefore, the maximum power can be extracted only at one operation point [10–12]. The PV-side converter should be able to execute the maximum power point tracking (MPPT) algorithm to extract the maximum available power [13,14].

Boosting the capability of the classical boost converter is limited due to the practical constraints; hence, the following structures and techniques are presented in the literature to provide high voltage gain [15,16]:

- Structures based on a high-frequency transformer and coupled inductors;
- Employing voltage lift techniques;
- Employing voltage multiplier circuits;
- Impedance source converters;
- Partial power converters (PPCs).

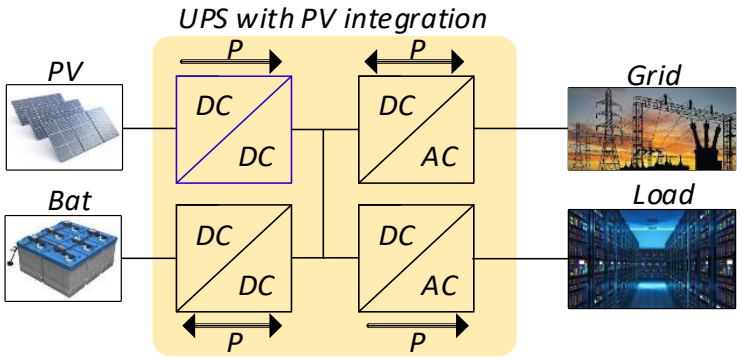


Figure 1. Online uninterruptible power supply (UPS) with photovoltaic (PV) connection.

Impedance-source converters are single-stage buck-boost converters, which can work for DC/AC, AC/DC, AC/AC, and DC/DC energy conversions [17,18]. The following advantages of these topologies make them suitable for low-voltage photovoltaic applications: high boosting capability; higher efficiency due to single-stage operation; lower number of active switches; immunity to switching transient short circuits.

A front-end switching system in impedance-source DC/DC conversion systems includes a conventional single switch, a full-bridge, and a push-pull structure, as shown in Figure 2 [19]. Using full-bridge and push-pull switching systems provides input to output voltage isolation, which is preferred for some applications. As described below, voltage isolation proves the ability to apply the partial power processing technique, which results in performance improvement.

Several structures of impedance networks are presented, such as Z-source, T-source, Y-source, and A-source [20–22]. Compared to a traditional structure (Z-source), T-source requires a lower number of passive elements and coupling inductors, which provides higher voltage gain for the converter [22]. A total of two types of T-source converters, non-isolated and isolated, are depicted in Figure 3. In the isolated type, a voltage multiplier is connected to the output of the isolated winding of the transformer (Figure 3b).

The partial power processing technique is a technique which can be used to improve the voltage gain and efficiency of a converter. A DC/DC converter can be considered a DC transformer with a turns ratio of $M_{(D)}$, which is the converter voltage gain. Similar to the winding connection of an AC autotransformer, an isolated DC/DC converter can be changed to a PPC. In a PPC, a part of the energy is directly transferred to the output and only a fraction of power is processed by the converter; therefore, the converter performance can be improved. There are two main types of PPC structures [23]: input parallel output series (Figure 4a) and input series, output parallel (Figure 4b).

Using the partial power processing technique for non-isolated converters was investigated [23–28]. In this paper, this technique is applied to an isolated T-source DC/DC converter to improve the converter voltage gain. A total of two structures of this converter are proposed and compared for possible applications, including UPS systems. In Section 2, the proposed structures are presented and the main relations for steady-state operation of the converter are derived. In Section 3, conventional PPC and improved PPC and full-power converter (FPC) are compared. The simulation and experimental results of the presented converter are provided in Section 4.

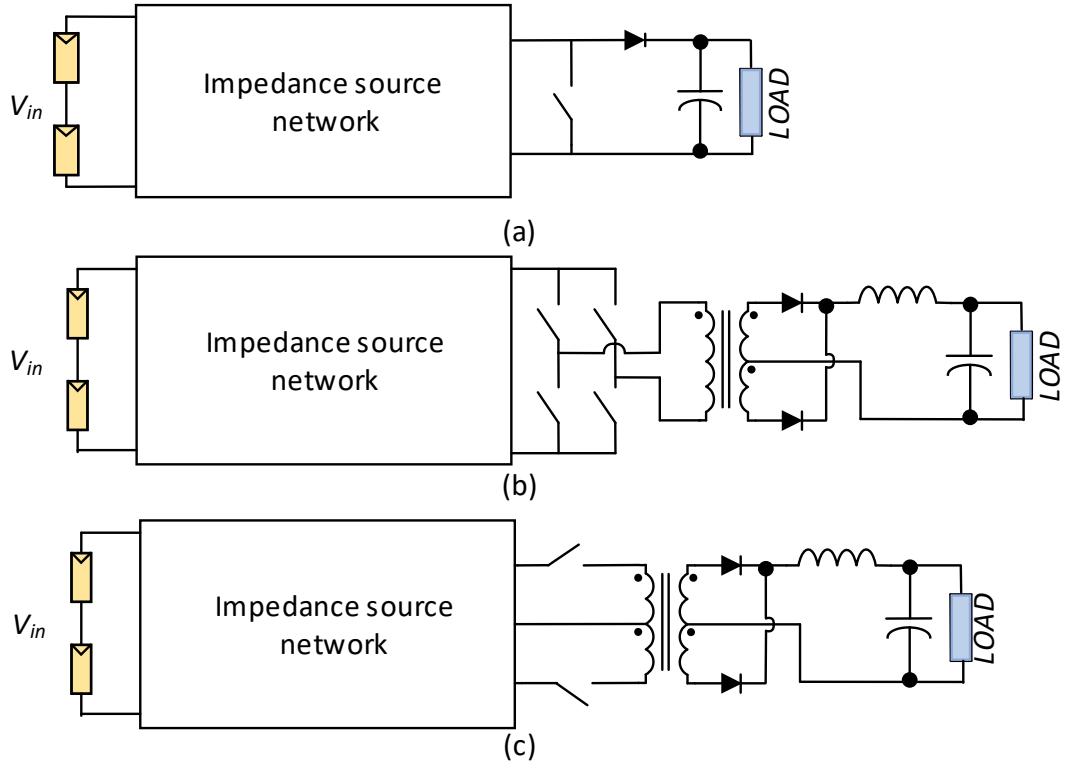


Figure 2. Different configuration of the front-end switching system in DC/DC impedance source converter. (**a**) single switch switching system, (**b**) full-bridge switching system, and (**c**) push-pull switching system.

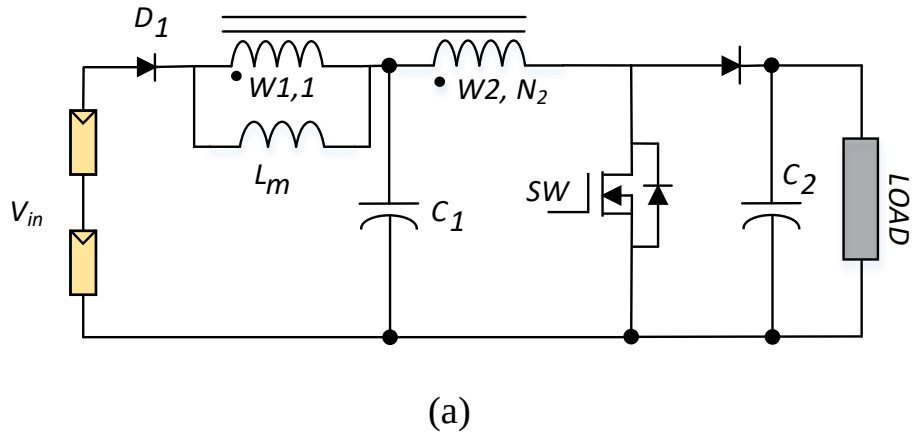
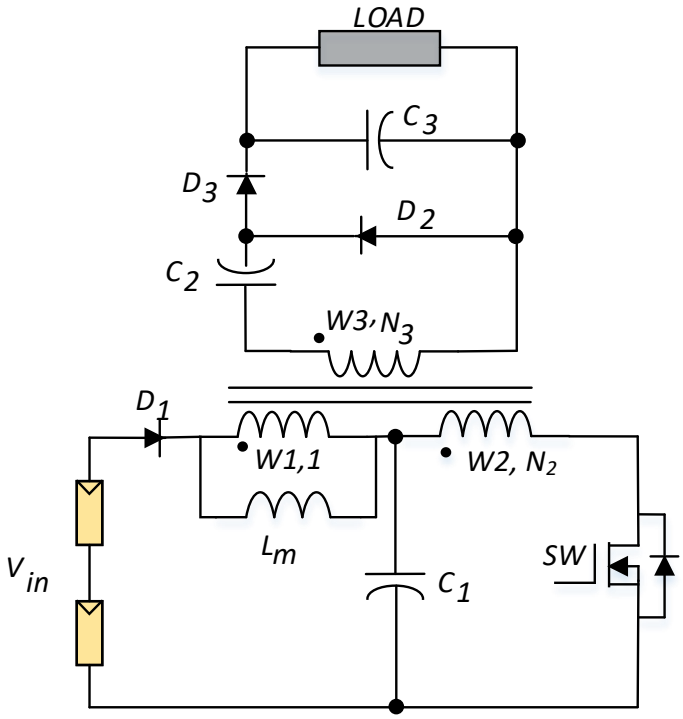
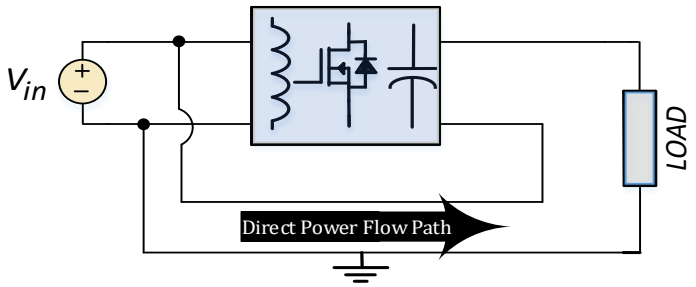


Figure 3. *Cont.*

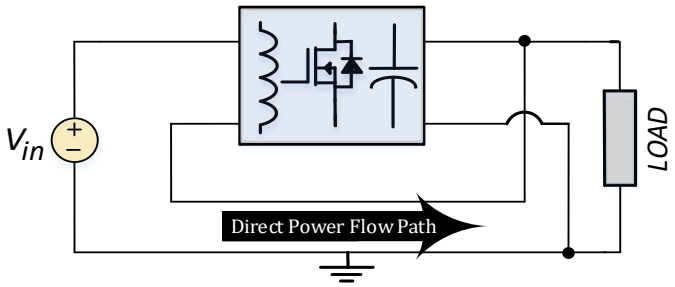


(b)

Figure 3. Configuration of T-source impedance network. (**a**) non-isolated and (**b**) isolated structures.



(a)



(b)

Figure 4. Schematic diagram of PPC structures: (**a**) input parallel, output series, (**b**) input series, output parallel.

2. Operation Principles

A total of two configurations of partial power for a T-source converter are presented here: conventional partial power T-source converter (PPTSC) and improved PPTSC. The schematics of the converters are shown in Figure 5a,b, respectively. As shown in Figure 5, in the conventional form, the series connection of input voltage and the voltage on the C_3 capacitor creates the output voltage. In the improved form, C_3 and C_1 are in series in the output. As the C_1 voltage is greater than the input voltage, higher voltage gain and improved performance are expected.

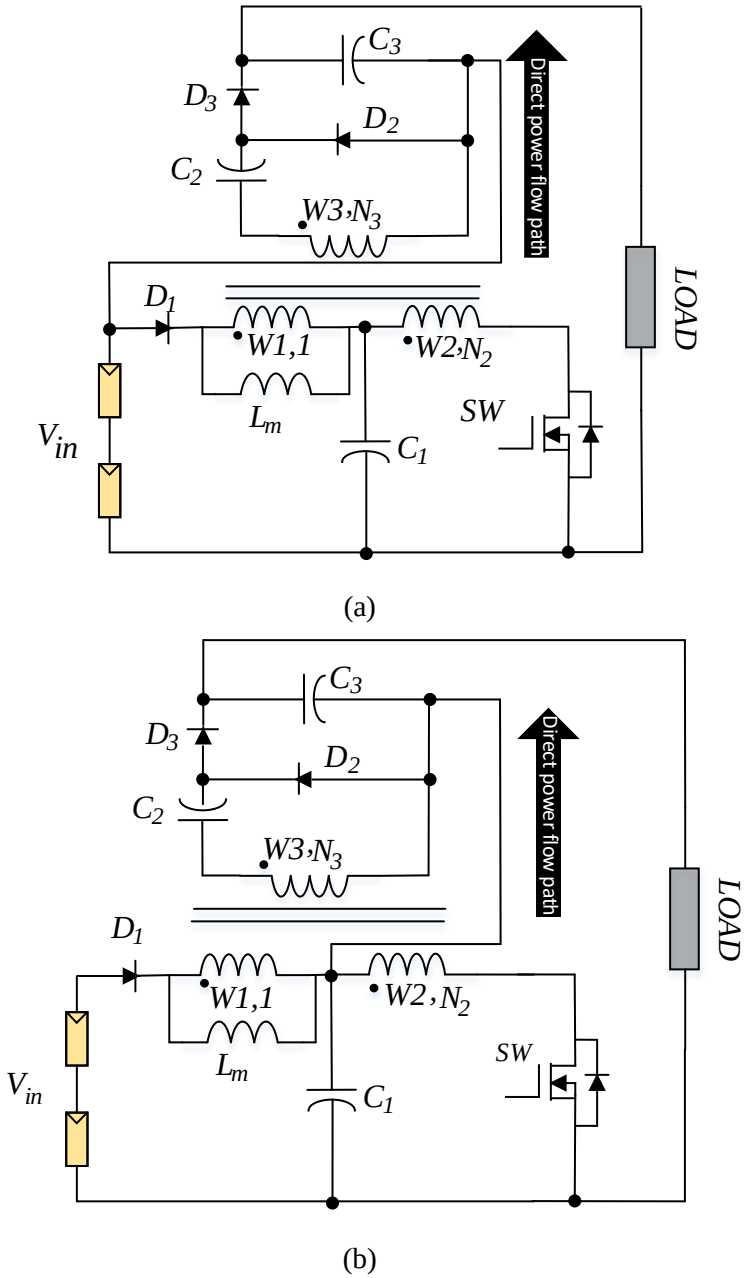


Figure 5. Schematic of the proposed PPC: (**a**) conventional partial power processing T-source converter (PPTSC) and (**b**) improved PPTSC.

The converter circuit and current paths for two switching states are shown in Figure 6. During the ON state operation (Figure 6a), the voltage across the second winding (W_2) (with a turns ratio of N_2) is equal to C_1 voltage (V_{C1}) and the current goes through it; therefore, the current induces in the first

and third windings (W_1 and W_3, respectively). This causes D_1 and D_2 to be turned off and D_3 to be turned on. Magnetizing the current (I_{lm}), which is modelled in parallel with W_1, decreases during this state. The W_1 current (I_{W1}) is equal to I_{lm}. The converter relationships during this switching state are as follows:

$$I_{lm} + N_2 I_{W2} + N_3 I_{W3} = 0, \tag{1}$$

$$V_L = \frac{V_{C_1}}{N_2} = \frac{V_{C_2} + V_{C_3}}{N_3}, \tag{2}$$

$$I_{C_1} = I_{W2} - I_o, \tag{3}$$

$$I_{C_2} = I_{W3}, \tag{4}$$

$$I_{C_3} = I_{W3} - I_o. \tag{5}$$

where I_{W2} and I_{W3} are the currents of W_2 and W_3 windings, respectively; I_o is the output current of the converter in Figure 6; N_3 is the turns ratio of W_3; and V_L is the voltage across magnetizing inductance. During the OFF state operation (Figure 6b), I_{lm} increases and D_1 and D_2 are ON while D_3 is OFF. The converter relationships during this switching state are as follows:

$$V_L = V_{in} - V_{C_1} = \frac{V_{C_2}}{N_3}, \tag{6}$$

$$I_{C_1} = I_{W1} + I_{lm} - I_o, \tag{7}$$

$$I_{C_2} = \frac{I_{W1}}{N_3}, \tag{8}$$

$$I_{C_3} = -I_o. \tag{9}$$

Employing (1)–(9) and using the inductor volt second balance and capacitor charge balance rules, the steady-state relations are derived.

$$D\left(\frac{V_{C_1}}{N_2}\right) + D'\left(V_{in} - V_{C_1}\right) = 0 \Rightarrow \frac{V_{C_1}}{V_{in}} = \frac{N_2(D-1)}{D + N_2(D-1)} \tag{10}$$

$$\frac{D(V_{C_2} + V_{C_3})}{N_3} + \frac{(1-D)V_{C_2}}{N_3} = 0 \Rightarrow V_{C_3} = \frac{V_{C_2}}{D} \tag{11}$$

$$(V_{in} - V_{C_1})N_3 = V_{C_2} \Rightarrow \frac{V_{C_3}}{V_{in}} = \frac{-N_3}{D + N_2(D-1)} \tag{12}$$

$$\frac{V_{out}}{V_{in}} = \frac{V_{C_1} + V_{C_3}}{V_{in}} = \frac{N_1(1-D) - N_2}{D + N_1(D-1)} = \frac{N_2 - N_1(1-D)}{(1-D)N_1 - D} \tag{13}$$

$$D(I_{W3} - I_o) - (1-D)I_o = 0 \Rightarrow I_{W3} = \frac{I_o}{D} \tag{14}$$

$$D(I_{W3}) + (1-D)\frac{I_{W1}}{N_3} = 0 \Rightarrow I_{W1} = \frac{-I_o N_3}{1-D} \tag{15}$$

$$(I_{W2} - I_o)D + (I_{W1} + I_{lm} - I_o)(1-D) = 0 \tag{16}$$

$$I_{lm} + N_2 I_{W2} + N_3 I_{W3} = 0 \tag{17}$$

$$I_{lm} = \frac{(1+N_3)N_2 + N_3}{(1-D)N_2 - D} I_o \tag{18}$$

$$I_{W2} = \frac{-\frac{(1-D)N_3}{D} - (1+N_3)}{(1-D)N_2 - D} I_o \tag{19}$$

where D is the duty cycle of the switch.

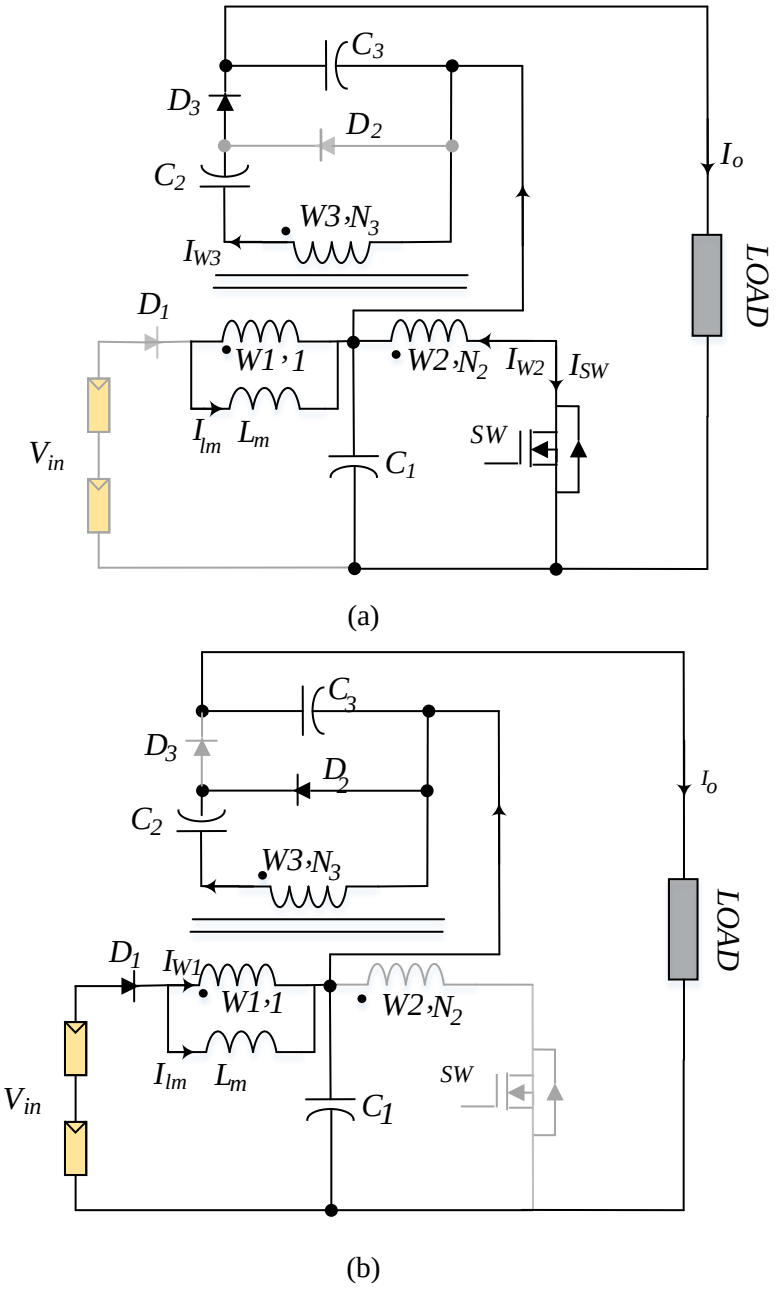


Figure 6. Current paths in different switching states for improved PPTSC. (**a**) ON state operation and (**b**) OFF state operation.

The capacitor voltage and I_{lM} ripples (ΔV_{Ci} and ΔI_{lM}) are calculated as:

$$\frac{2L_m\Delta I_{lm}}{DT_s} = \frac{V_{C_1}}{N_2} \Rightarrow \Delta I_{lm} = \frac{\Delta V_{C_1}}{2L_m N_2 f_{SW}}, \tag{20}$$

$$\frac{2C_1\Delta V_{C_1}}{DT_s} = I_{W2} - I_o \Rightarrow \Delta V_{C_1} = \frac{(I_{W2} - I_o)D}{2C_1 f_{SW}}, \tag{21}$$

$$\frac{2C_2\Delta V_{C_2}}{DT_s} = I_{W3} = \frac{I_o}{D} \Rightarrow \Delta V_{C_2} = \frac{I_o}{2C_2 f_{SW}}, \tag{22}$$

$$\frac{2C_3\Delta V_{C_3}}{DT_s} = I_o \Rightarrow \Delta V_{C_3} = \frac{(1-D)I_o}{2C_3 f_{SW}}. \tag{23}$$

All the relations for the steady-state analysis of the converters are derived, which can also be used for other analyses such as calculating the voltage and current stress on the elements and comparing the performance of the converters. In the next section, full-power TSC, conventional PPTSC, and improved PPTSC are compared in different terms.

3. Comparison of Full-Power TSC, Conventional PPTSC, and Improved PPTSC

To analyze the performance of the presented converters; full power TSC (FPTSC) (Figure 3b), conventional PPTSC (Figure 5a), and improved PPTSC (Figure 5b) are compared in terms of voltage gain, voltage and current stress on semiconductor devices, and converter efficiency. The fraction of power process (FPP) is shown in Figure 7. FPP is the proportion of total output power to the power processed by the converter and is one of the important values for comparison of PPCs [29]. Lower FPP is desirable as it is associated with less voltage and current stress on the elements and improves the converter performance. Figure 7 demonstrates that FPP is lower for the improved PPTSC.

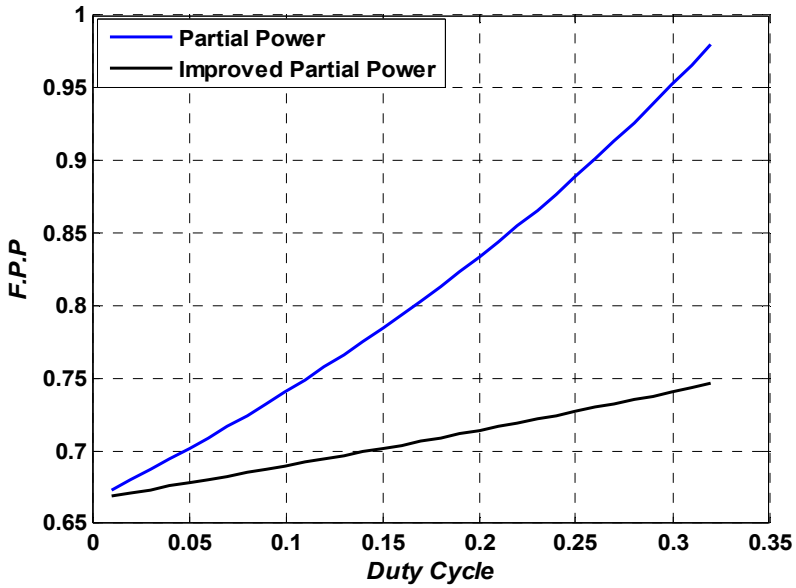


Figure 7. Fraction of power process (FPP) comparison of conventional and improved PPTSC.

In Figure 8, output voltage gain versus D is plotted and compared for three discussed converters in non-ideal conditions. The input voltage is 30 V. The value of non-idealities and converter parameters considered here are the same as the values mentioned for the prototype in Section 4. As shown in Figure 8, improved PPTSC shows a greater voltage gain for $D < 0.3$. Although the maximum achievable gain is achieved for the conventional PPTSC, the improved PPSC shows higher voltage gain for a wide range of duty cycle. In high values of D, the voltage drop of W1 is increased for improved PPTSC as a higher current passes through it. This limits the voltage gain of the improved PPTSC at high values of D.

The relationships for voltage and current stresses of the switches and diodes are shown in Table 1. The equations for voltage stress of any elements in all three converters are the same, but in similar operation conditions, i.e., the same input and output voltage, the required D for the improved PPTSC is lower and $(1 - D)N_2 - D$ (denominator of the voltage stress equation) is a decreasing function. Therefore, the voltage stress of the switch and diodes in the improved PPTSC is lower than the other two converters. Comparing the relations for current stress in Table 1 demonstrates that:

- The relations for the current stresses of the switch for all structures are the same. Although the relations are the same, lower D leads to lower current stress in PPTSC structures.

- The current stress of D_2 and D_3 are lower for improved PPTSC. The reason is the same as the above description. Although the relations are the same, a lower D leads to lower current stress in PPTSC structures.

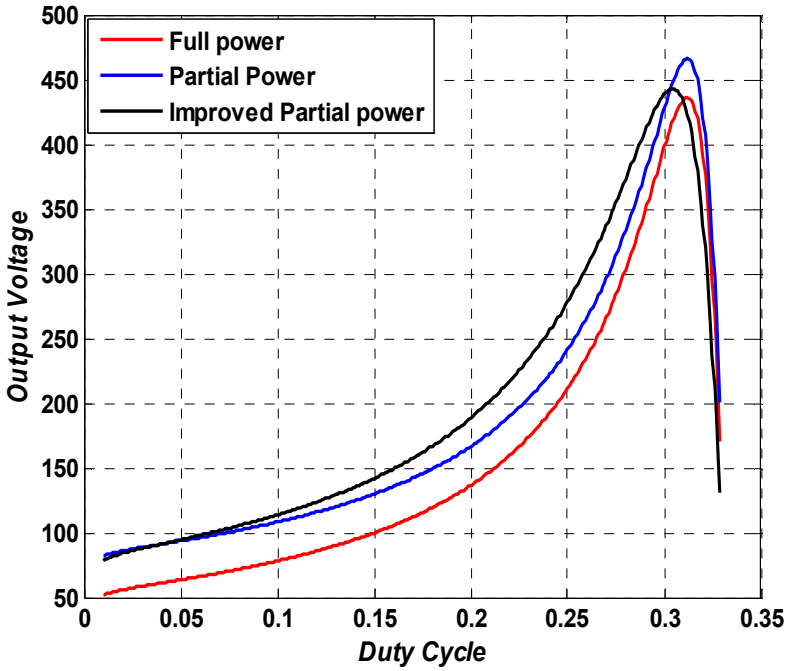


Figure 8. Output voltage gain versus duty cycle for FPTSC, conventional PPTSC, and improved PPTSC.

Table 1. Voltage and current stress of the switches and diodes for FPTSC, conventional PPTSC, and improved PPTSC.

	FPTSC	Conventional PPTSC	Improved PPTSC
Gain	$\frac{N_3}{(1-D)N_2-D}$	$\frac{N_3+(1-D)N_2-D}{(1-D)N_2-D}$	$\frac{N_3-N_2(1-D)}{(1-D)N_2-D}$
V_{SW}	$\frac{N_2V_{in}}{(1-D)N_2-D}$	$\frac{N_2V_{in}}{(1-D)N_2-D}$	$\frac{N_2V_{in}}{(1-D)N_2-D}$
V_{D_1}	$\frac{V_{in}}{(1-D)N_2-D}$	$\frac{V_{in}}{(1-D)N_2-D}$	$\frac{V_{in}}{(1-D)N_2-D}$
V_{D_2}	$\frac{N_3V_{in}}{(1-D)N_2-D}$	$\frac{N_3V_{in}}{(1-D)N_2-D}$	$\frac{N_3V_{in}}{(1-D)N_2-D}$
V_{D_3}	$\frac{N_3V_{in}}{(1-D)N_2-D}$	$\frac{N_3V_{in}}{(1-D)N_2-D}$	$\frac{N_3V_{in}}{(1-D)N_2-D}$
I_{SW}	$\frac{D+N_2}{D(1-D)N_1-D^2}I_o$	$\frac{D+N_2}{D(1-D)N_1-D^2}I_o$	$\frac{D+N_2}{D(1-D)N_1-D^2}I_o$
I_{D_1}	$\frac{N_3}{((1-D)N_2-D)(1-D)}I_o$	$\frac{N_3+(1-D)N_2-D}{((1-D)N_2-D)(1-D)}I_O$	$\frac{(N_3+(1-D)N_2)I_o}{((1-D)N_2-D)(1-D)}$
I_{D_2}	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$	$\frac{I_o}{1-D}$
I_{D_3}	$\frac{I_o}{D}$	$\frac{I_o}{D}$	$\frac{I_o}{D}$

The efficiency comparison of the converters shown in Figure 9 was obtained according to the relations described [30] for conduction and switching losses of the converters.

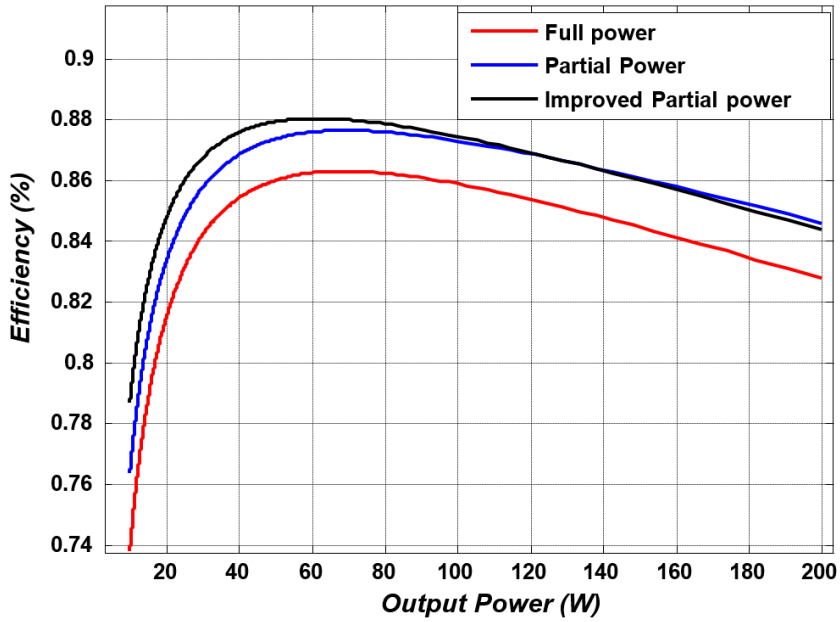


Figure 9. Converter efficiency versus output power for conventional PPTSC, improved PPTSC, and FPTSC.

The main non-idealities considered for the converters are metal oxide semiconductor field effect transistor (MOSFET) conduction resistance (R_{on}), transformer winding resistances (R_{W1}, R_{W2}, and R_{W3}), and forward voltage of the diodes (V_f). Regarding these parasitic elements, the main power losses are as follows:

- Conduction losses of switches, transformer windings, and diodes.
- Turn-ON and turn-OFF switching losses of the switches.

The conduction loss of windings ($P_{COND(W)}$) can be calculated:

$$P_{COND(W)} = \sum R_{Wi} I_{Wi}^2 \quad i = 1,\ 2,\ 3. \tag{24}$$

The expressions for the winding currents are extracted in Section 2 of the paper.

Using the root-mean-square (RMS) value of switch current and diode average current, the conduction losses of the switch and diodes ($P_{COND(S)}$ and $P_{COND(D)}$) are given by (25) and (26), respectively.

$$P_{COND(S)} = \sqrt{D} R_{on} I_{W2}^2 \tag{25}$$

$$P_{COND(S)} = \sqrt{D} R_{on} I_{W2}^2 \tag{26}$$

MOSFET switching loss P_{SW} is estimated based on the amount of dissipated energy E_{SW} in the switches during turn-ON and turn-OFF transitions [31], and given by (27).

$$E_{SW} = (\alpha_{ON} + \alpha_{OFF})(V_{SW} I_{SW}) \tag{27}$$

where,

$$\alpha_{ON} = \frac{3t_{fv} - 3t_{fv}t_{ri} + t_{ri}^2}{6}, \tag{28}$$

$$\alpha_{OFF} = 0.5\left(t_{rv} + t_{fi}\right), \tag{29}$$

$$I_{SW} = I_{W2}, \tag{30}$$

$$V_{SW} = V_{C1} + N_1(V_{in} - V_{c1}). \tag{31}$$

The above equations are the same for all structures. The difference in the value of D for a given output (PP converters require a lower duty cycle) results in efficiency improvement using the PP structure.

The converter parameters used to plot the efficiency diagram are the same as the parameters used for simulation, which is discussed in the next section. Figure 9 demonstrates a higher efficiency of PPCs compared to the full power converter. Comparison of efficiency diagrams for improved and conventional PPTSCs shows that, for lower loads, improved PPTSC efficiency is better, while at high loads, conventional PPTSC improves. The main reason for this is related to the conduction loss of W1 winding and D1. Whereas W1 and D1 process full power in improved PPTSC, their currents are higher than conventional PPTSC; therefore, efficiency is limited in this case while the current that goes through them increases (higher loads). The region in which improved PPTSC has higher efficiency is related to the converter parameters, while winding resistance of W1 and forward voltage of D1 play an important role in this.

The same parasitic elements are considered for calculating the non-ideal voltage conversion ratio (VCR). Modifying the relationships in two switching states can provide the relationship. As the voltage drop on windings and switches depends on the winding and switch currents, respectively, it is almost impossible to derive a unique relation for VCR in non-ideal conditions. For obtained non-ideal VCR, Equations (2) and (6) can be modified as follows:

$$V_L = \frac{V_{C_1} - R_1 I_{W1} - (R_2 + R_{on}) I_{W2}}{N_2} = \frac{V_{C_2} + V_{C_3} - 2V_f - R_3 I_{W3}}{N_3}, \tag{32}$$

$$V_L = V_{in} - V_{C_1} - R_1 I_{W1} = \frac{V_{C_2} - V_f}{N_3}. \tag{33}$$

The current of W1 is the same for all structures; therefore, the current of other windings and the switch (which is equal to I_{W2}) are lower for the improved PPTSC, which result in a lower voltage drop. The lower voltage drop on elements improves the non-ideal VCR of the improved PPTSC compared to the other structures.

4. Simulation and Experimental Result

To verify the performance of the presented converters, several simulations were performed and a prototype converter was built (Figure 10). Several experimental tests are carried out and compared with simulations and theoretical analysis. The parameters are listed in Table 2.

Table 2. Simulation and experimental parameters.

Parameter	Symbol	Value
Input voltage	V_{in}	30 V
Output voltage	V_{out}	150 V
Load	R	400 Ω
Switching frequency	f	30 kHz
Turns ratio of three winding transformer	$1{:}N_2{:}N_3$	00:06.6
Magnetizing inductance	L_{lm}	330 µH
Capacitance	C_1, C_2, C_3	470 µF
Diode forward voltage	V_f	1.2 V
Conduction resistance of switch	R_{on}	0.09 Ω
First winding resistance	R_1	0.2 Ω
Second winding resistance	R_2	0.1 Ω
Third winding resistance	R_3	0.3 Ω

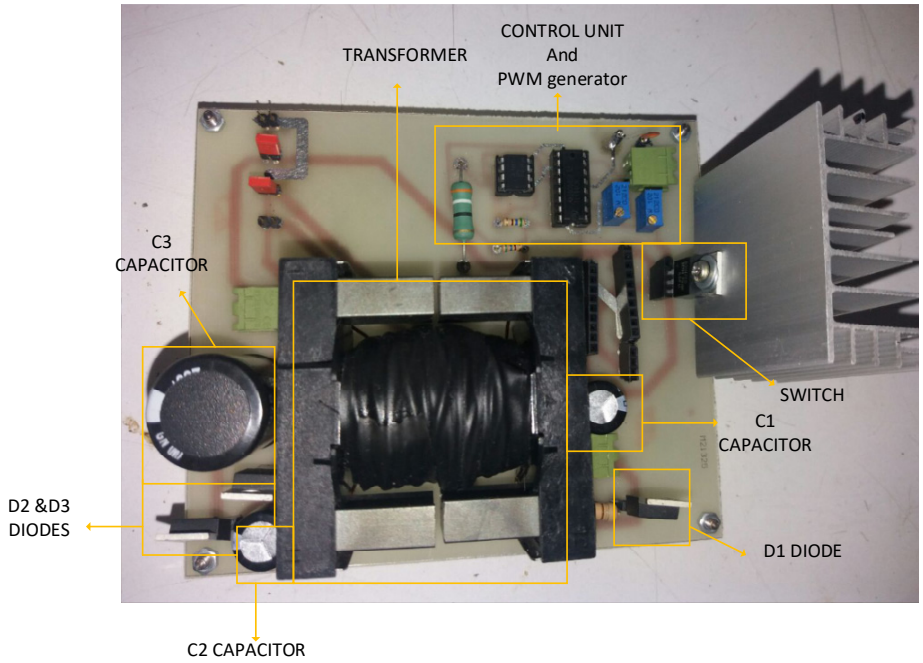
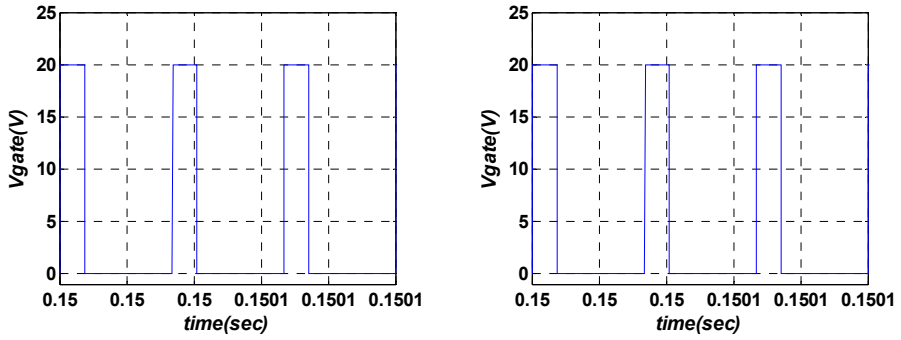


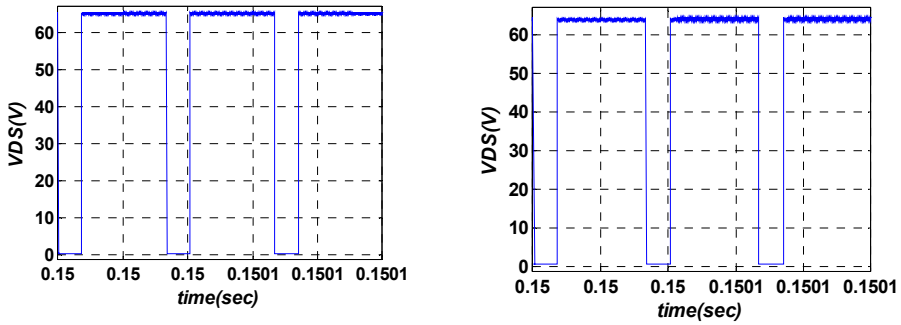
Figure 10. Laboratory prototype.

A total of two structures (conventional PPTSC and improved PPTSC) with the same duty cycles (Figure 11a) were simulated and the results are shown in Figure 11. Drain-source voltage, voltage across the transformer windings, magnetizing current, and capacitor voltage are shown in Figure 11b–i, respectively, for two converters. As expected by theoretical analysis, during the first subinterval (the switch is turned on) magnetizing inductance, C_3 charged while C_1 and C_2 discharged. Figure 11f shows that the peak value of magnetizing currents for both converters were maintained around constant values; therefore, an appropriate design of the transformer can guarantee it will work in the linear core region and prevent saturation. A disadvantage of the improved PPTSC compared to conventional PPTSC is related to the magnetizing current of the transformer. Figure 11f shows that the transformer magnetizing current for the improved PPTSC is higher than that of the conventional PPTSC. This is mainly because the first winding processes all the power and this part of the converter needs to be considered full power. This increases the peak value of the magnetizing current and affects the transformer design. The voltages of capacitors are regulated with a ripple of less than 0.1 V (0.5%). The ripple of the output voltage for both converters is less than 0.06%, and the proposed improved PPTSC has a higher voltage gain than the conventional PPTSC according to Figure 11j. Using the steady-state relations derived in the previous section and the simulation parameters listed in Table 2, the steady-state values for the capacitor voltages and magnetizing inductor currents were calculated as V_{C1} = 53 V, V_{C2} = 22 V, and V_{C3} = 105 V for both structures and I_{lM} = 2.05 A and I_{lM} = 3.25 A for conventional and improved PPTSC, respectively. The capacitor voltage is the same if similar duty cycles are applied to both structures. The obtained simulation results match the theoretical outcomes.

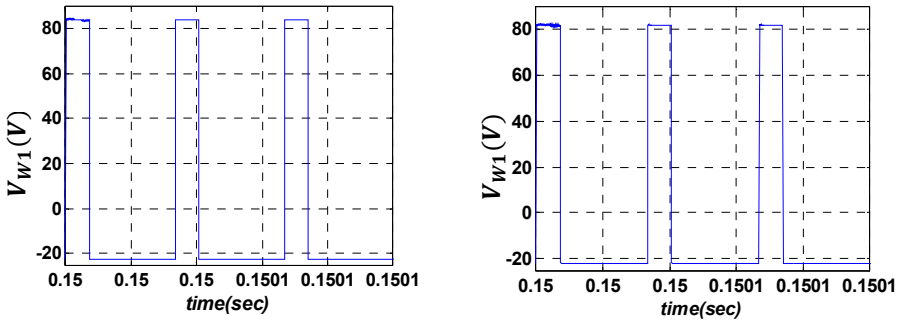
The experimental results of both presented converters are shown in Figures 12 and 13. The experiments were performed similarly to simulations for better comparison. The obtained results match the theoretical analysis and simulation results. Figure 14 shows the converter efficiency for three structures based on experiments and simulations for different output powers. The difference between input and output power is considered the converter loss. This efficiency curve verifies the theoretical analysis that improved PPTSC has higher efficiency compared to a conventional PPTSC and a full-power converter.



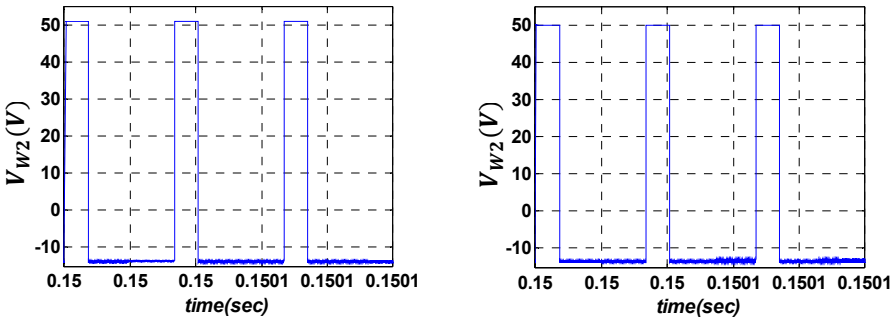
(**a**) Command signal



(**b**) Switch drain-source voltage

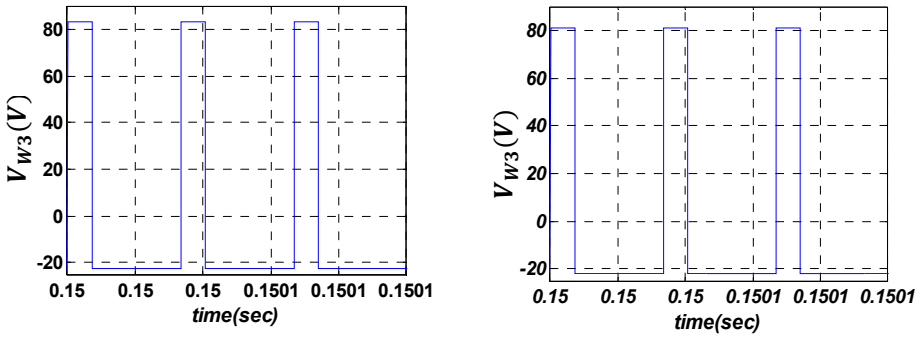


(**c**) First winding voltage

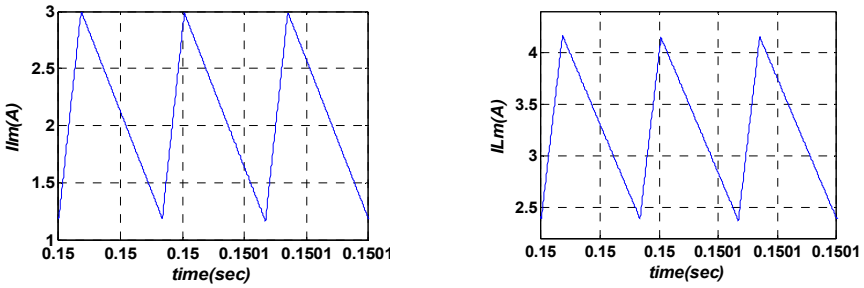


(**d**) Second winding voltage

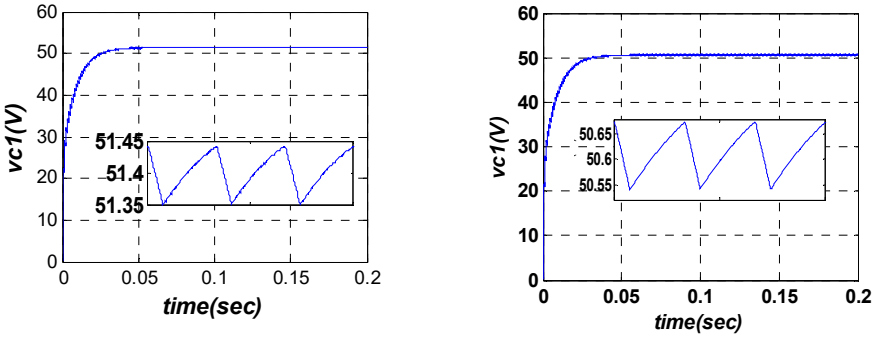
Figure 11. *Cont.*



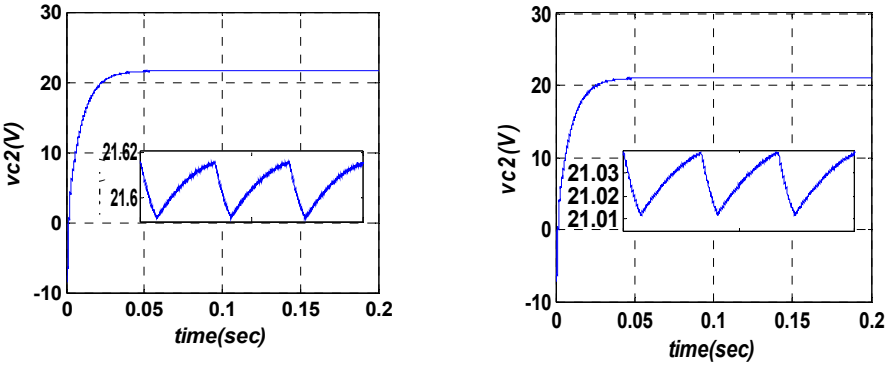
(**e**) Third winding voltage



(**f**) Magnetizing current

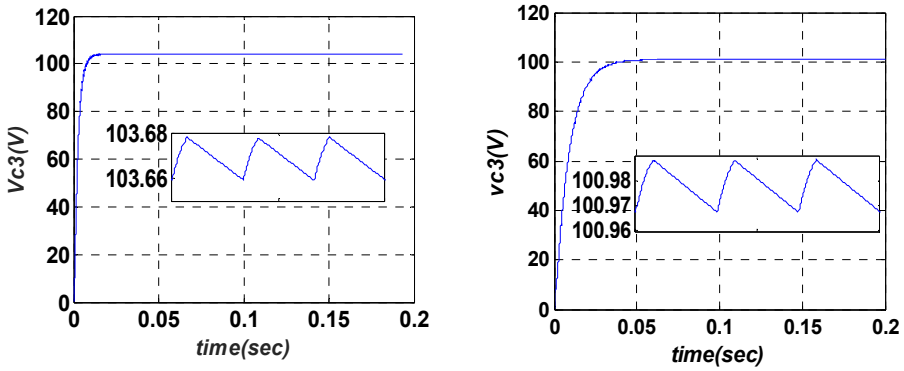


(**g**) V_{C1}

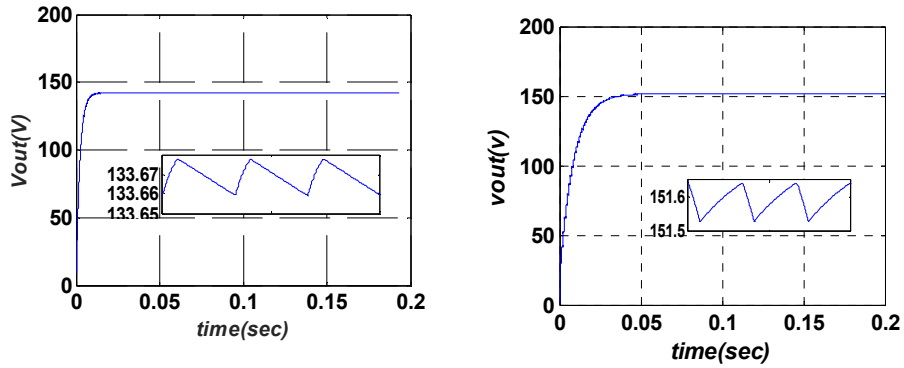


(**h**) V_{C2}

Figure 11. *Cont.*

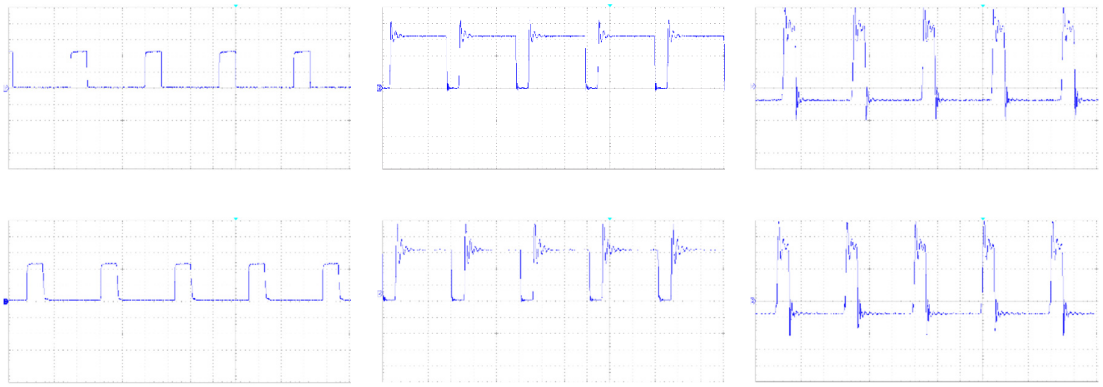


(**i**) V_{C3}



(**j**) Output voltage

Figure 11. Simulation results for the proposed converters, left: conventional PPTSC, right: improved PPTSC. (**a**) Command signal, (**b**) switch drain-source voltage, (**c**) first winding voltage, (**d**) second winding voltage, (**e**) third winding voltage, (**f**) magnetizing current, (**g**)V_{C1}, (**h**)V_{C2}, (**i**)V_{C3}, and (**j**) output voltage.

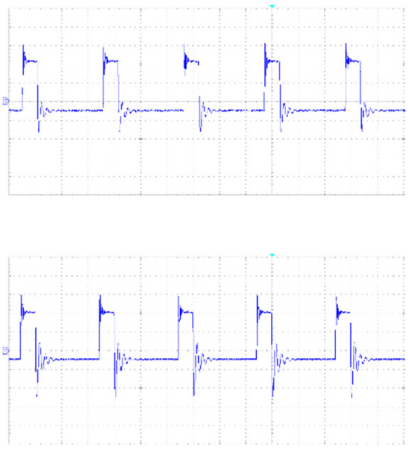


(**a**) Gate voltage (5 V/div, 10 μs/div)

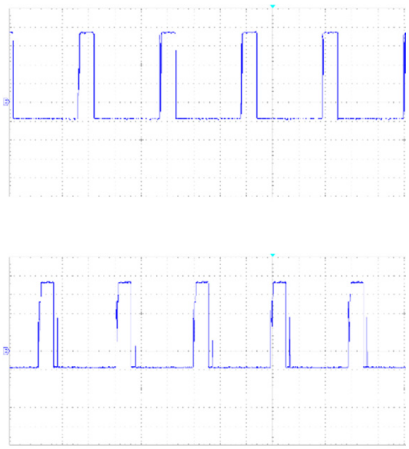
(**b**) Switch drain-source voltage (20 V/div, 10 μs/div)

(**c**) W_1 voltage (20 V/div, 10 μs/div)

Figure 12. *Cont.*

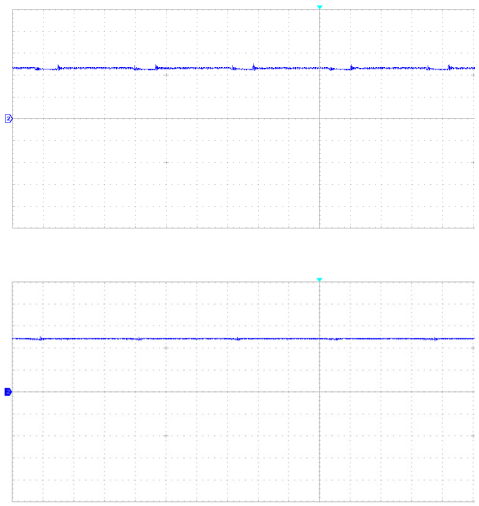


(**d**) W_2 voltage
(20 V/div, 10 μs/div)

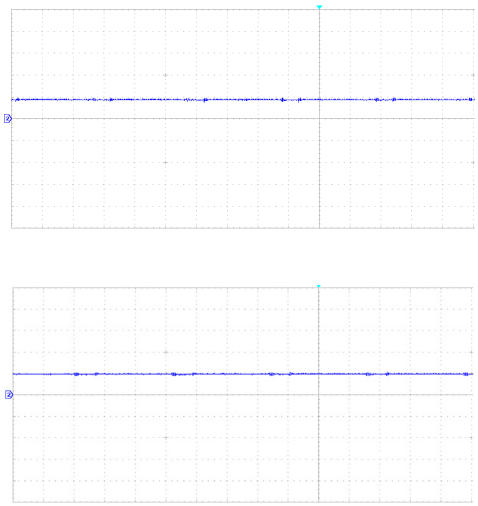


(**e**) W_3 voltage
(20 V/div, 10 μs/div)

Figure 12. Experimental results for the proposed converters, left: conventional PPTSC, right: improved PPTSC: (**a**) ate voltage, (**b**) switch drain-source voltage, (**c**) first winding voltage, (**d**) second winding voltage, and (**e**) third winding voltage.

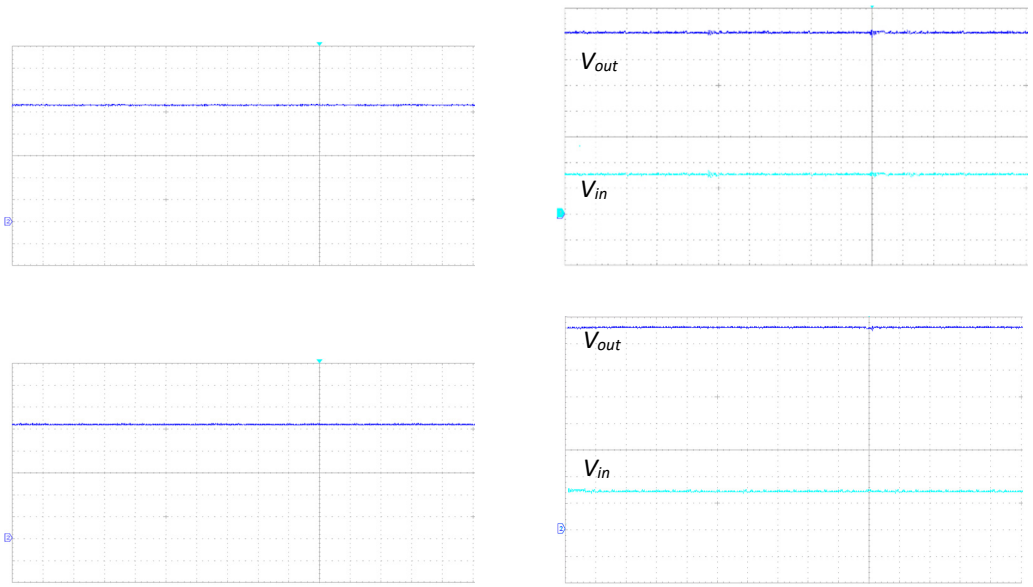


(**a**) V_{C1} (20 V/div, 10 μs/div)



(**b**) V_{C2} (20 V/div, 10 μs/div)

Figure 13. *Cont*.



(**c**) V_{C3} (20 V/div, 10 µs/div) (**d**) Output and input voltage (20 V/div, 10 µs/div)

Figure 13. Experimental results for the capacitor voltage and output voltage of the proposed converters, left: conventional PPTSC, right: improved PPTSC. (**a**) V_{C1}, (**b**)V_{C2}, (**c**)V_{C3}, and (**d**) output and input voltage.

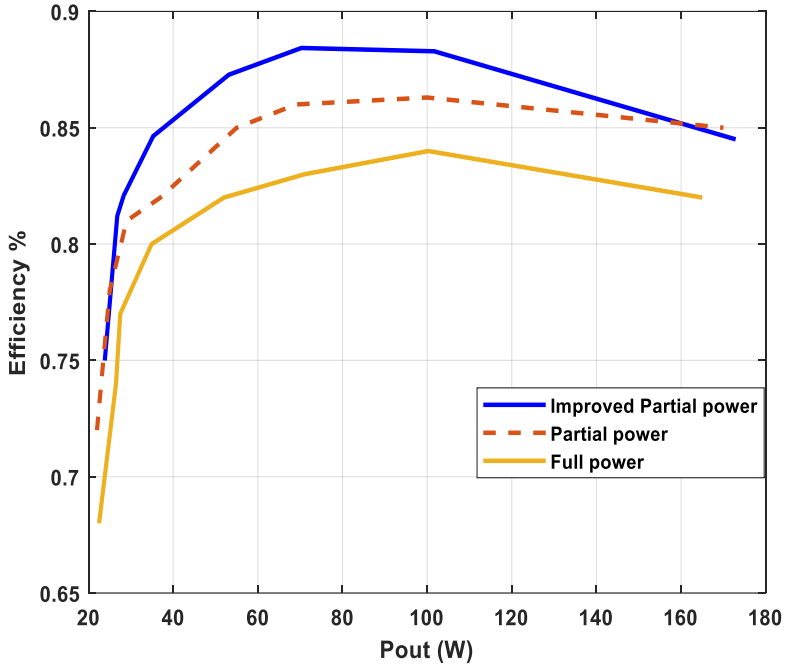


Figure 14. Converter efficiency versus output power for conventional PPTSC, improved PPTSC, and FPTSC.

5. Conclusions

In this paper, a new DC/DC converter was proposed for renewable energy integration in UPS systems by adapting a T-source converter in a partial power processing structure. This converter, compared to other impedance source converters, requires fewer components, and we showed that its efficiency is higher. The operation principle of this converter was presented, and governing relations were obtained. The presented comparisons proved that it has higher voltage gain, lower voltage,

and current stresses on the semiconductors. Finally, the simulation and experimental results were presented to verify the performance of the converter.

Author Contributions: A.R. is the main researcher who initiated and organized research reported in the paper. He contributed to the sections on converter design, modeling, controlling, and writing the main parts of the paper. A.N. developed the prototype and performed the converter validation. M.S. (Mahdi Shahparasti) and M.S. (Mehdi Savaghebi) contributed to analysis, writing, and editing of the manuscript. All authors have read and agreed to the published version of the manuscript.

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Conflicts of Interest: The authors declare no conflict of interest.

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