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Fault Ride through Capability Augmentation of a DFIG-Based Wind Integrated VSC-HVDC System with Non-Superconducting Fault Current Limiter

Md Shafiul Alam ^{1,2} , Mohammad Ali Yousef Abido ^{1,*} , Alaa El-Din Hussein ¹ and Ibrahim El-Amin ¹

¹ Department of Electrical Engineering, King Fahd University of Petroleum & Minerals, Dhahran 31261, Saudi Arabia; shafiul@kfupm.edu.sa (M.S.A.); husseina@kfupm.edu.sa (A.E.-D.H.); imelamin@kfupm.edu.sa (I.E.-A.)

² Department of Electrical & Electronic Engineering, International Islamic University Chittagong, Chittagong 4318, Bangladesh

* Correspondence: mabido@kfupm.edu.sa; Tel.: +966508757838

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Abstract: This paper proposes a non-superconducting bridge-type fault current limiter (BFCL) as a potential solution to the fault problems of doubly fed induction generator (DFIG) integrated voltage source converter high-voltage DC (VSC-HVDC) transmission systems. As the VSC-HVDC and DFIG systems are vulnerable to AC/DC faults, a BFCL controller is developed to insert sizeable impedance during the inception of system disturbances. In the proposed control scheme, constant capacitor voltage is maintained by the stator VSC (SVSC) controller, while current extraction or injection is achieved by rotor VSC (RVSC) controller. Current control mode-based active and reactive power controllers for an HVDC system are developed. Balanced and different unbalanced faults are applied in the system to show the effectiveness of the proposed BFCL solution. A DFIG wind-based VSC-HVDC system, BFCL, and their controllers are implemented in a real time digital simulator (RTDS). The performance of the proposed BFCL control strategy in DFIG-based VSC-HVDC system is compared with a series dynamic braking resistor (SDBR). Comparative RTDS implementation results show that the proposed BFCL control strategy is very efficient in improving system fault ride through (FRT) capability and outperforms SDBR in all cases considered.

Keywords: doubly fed induction generator (DFIG); voltage source converter (VSC); bridge-type fault current limiter (BFCL); series dynamic braking resistor (SDBR); fault ride through (FRT) capability

1. Introduction

Due to the continuous depletion of fossil fuels as well as the perpetual escalation of energy demands, research on renewable energy resources has been a hot topic in recent years. The integration and planning of renewable energy has a great impact on the operation of the electric market [1–3]. Among several renewable energy resources, wind energy has drawn substantial attention from researchers due to its maximum power point tracking capability, high efficiency, self-regulating control of active and reactive power, and improved power quality [4,5]. Renewable energy resources, especially large-scale wind power based on doubly fed induction generator (DFIG) integration with the existing power grid is a challenging task for power engineers. Compared to other integration techniques, voltage source converter high-voltage DC (VSC-HVDC) has greater flexibility [6,7]. Additionally, since the VSC-HVDC system adopts an insulated-gate bipolar transistor (IGBT) switch instead of thyristor, it could prevent commutation failure due to grid fault. Hence, VSC-HVDC offers a better solution to the commutation problem in HVDC systems [8].

Although the HVDC system has several advantages; it is vulnerable to AC/DC faults in the system [9]. Due to disturbances, bulk power transmission is highly interrupted, causing power imbalance and instability in the system. Therefore, HVDC systems must be kept energized during faults. Various control techniques have been applied for VSCs to improve fault ride through (FRT) capability as well as transient stability [7,10]. In an HVDC system, for proper operation and control of the converters, DC link voltage must be regulated within permissible limits. Various DC link power dissipation techniques are presented in the literature [11] to keep the DC link voltage within expected limits during faults. These techniques involve a reduction in active power and the adjustment of wind turbine power, which depend on a fast communication route among the converter stations. DC link ripple reduction and a power oscillation damping method is presented with a negative sequence current controller [12]. Nevertheless, this method results in stresses on the mechanical system because of reduction of active power to zero from the sending terminal.

Electric power system reliability can be enhanced through the integration of several renewable energy resources [13–16]. However, disturbances in the grid may cause instability in such integrated systems. The integration of offshore wind turbines to grids through a medium-voltage DC transmission system is presented with a new magnetic linked converter [17]. The presented magnetic linked converter can eliminate the need for low frequency heavy transformers as well as solve isolation problems naturally. Among different wind energy integration techniques, DFIG is considered to be superior as its efficiency is high and the control of active and reactive powers can be decoupled [18–20].

The generated active and reactive powers are controlled by rotor-side converter (RSC), while DC link voltage and reactive power exchange with the grid are controlled by the grid-side converter (GSC) [21–23]. DFIG systems are vulnerable to grid faults due to the direct connection of the stator winding to the grid [24–26]. A new control technique for DFIG wind integration was presented whereby the continuation of the DFIG connection during a fault can be secured and the system stability can be improved under fault conditions [23].

Nowadays, it is imperative to maintain the security and stability of the power system, due to its complex structure. Fault current limiters (FCLs) are considered as an important candidate to be placed in power systems to augment stability and security. Generally, superconducting fault current limiter placement is dominant in AC power system [27–30]. A saturated iron-core superconducting fault current limiter (SISFCL) to improve distance protection of a 500 kV AC transmission line is presented [31]. Since SISFCL adds inductance to the transmission line, re-adjustment of distance relay settings was presented to achieve better coordination. In addition, a resistive-type superconducting FCL was presented [32]. However, it suffers from high current and high cost related to installation, operation, and maintenance. To overcome this problem, Nam et. al. [33] presented a hybrid resistive-type superconducting fault current limiter (SFCL) with thyristors where phase angle control of the thyristors is coordinated with SFCL to limit the fault current. However, this hybrid fault current limiting technique has been developed for small-scale system application. Further study and research on capability extension are needed for application in large-scale systems. Superconducting fault current limiting cables have been presented for protection purposes [34,35]. A systematic method for impedance selection of high-temperature superconducting cables under different fault conditions was developed [35]. Depending on fault current levels and relay operating times, the optimal impedance value is determined from the system protection perspective. Fault current limiting techniques with a series dynamic braking resistor (SDBR) are presented [36,37]. A controllable switch is connected in parallel with a resistive branch in SDBR. The switch can be turned off or on in a dynamic fashion to insert the resistance as a main current-limiting part in SDBR operation. However, the SDBR is sensitive to switching delay and has inadequate performance in restricting fault current and augmenting dynamic performance [38]. Furthermore, most of the FCLs have been examined and installed in AC power systems; however, their feasibility and placements have not been fully investigated in VSC-HVDC systems [39].

The non-superconducting bridge-type fault current limiter (BFCL) is a novel technology having promising competency to improve the dynamic stability of wind farms and power grids by inserting sizeable impedance during the inception of disturbances in the system [40–45]. However, determining the size of impedance of BFCL to restrict the fault current of DFIG wind-based HVDC systems is a challenging task. Also, the insertion of this determined impedance during fault conditions in the system needs proper fault detection and a BFCL operation strategy. Mainly, BFCL consists of some diodes, an IGBT switch, resistor, and inductor. Thanks to the non-superconducting nature of these elements [46], BFCL can easily be implemented in power system with less cost compared to other current-limiting devices. To sum up, there is gap in current studies examining and implementing low-cost BFCLs that needs to be filled by designing proper impedance as a prospective solution for fault impact mitigation of DFIG wind integrated HVDC systems.

This study proposes BFCL-based control for reducing the fault current, improving the fault ride through capability, and enhancing the transient stability of DFIG wind integrated VSC-HVDC systems. To the best of our knowledge, this non-superconducting BFCL has not been designed and examined for FRT capability enhancement of DFIG-based HVDC systems. In this work, the proper size of impedance of BFCL is designed and inserted under different fault conditions in HVDC systems. The proposed BFCL is also equated with SDBR to demonstrate its efficacy for reducing the fault current and improving the stability of VSC-HVDC systems with DFIG wind integration. Unlike other methods presented in the literature, the proposed BFCL-based protection scheme is superior for augmenting the FRT capability of DFIG wind farms integrated with VSC-HVDC systems. The following shortcomings in current studies are to be addressed as the main contributions of this research:

- (a) Excessive DC link voltage fluctuation
- (b) High fault current and oscillation in DFIG speed and active power
- (c) Improper size of BFCL impedance for DFIG-based HVDC systems

2. Bridge-Type Fault Current Limiter

Non-superconducting bridge-type fault current limiter (BFCL) is proposed to augment fault ride through capability of DFIG wind farm integration with VSC-HVDC. The construction, working principle, and proposed control strategy of BFCL are documented below.

2.1. BFCL Structure, Operation, and Design

As shown in Figure 1, BFCLs have two main parts [41,47]: shunt branch with resistor and inductor, and diode bridge with diodes, resistor, inductor, and IGBT switch. The shunt resistor, R_{sh} , and the inductor, L_{sh} , are the main current-limiting parts, the sizes of which need to be designed for the improvement of the dynamic performance of the system, while the DC resistor, R_{DC} , and inductor, L_{DC} , are chosen to have small values in order to have a very negligible impact on the system during normal operation. The main role of the BFCL is to inset the shunt branch impedance in series with the line under faulty conditions in order to limit the fault current.

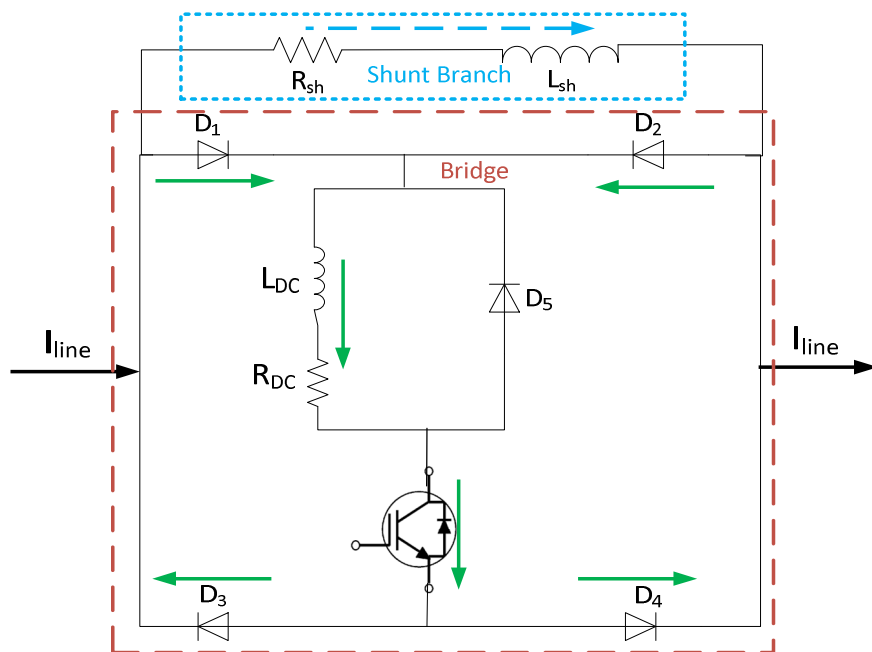


Figure 1. Configuration of a non-superconducting bridge-type fault current limiter (solid arrow is for normal current flow and dashed arrow is for fault current flow path).

The operation mode of BFCLs is controlled by proper control signal to the gate of the IGBT. For the system without fault mode, the objective is to bypass the shunt branch by short-circuiting the bridge part. Therefore, during normal conditions, the current passes through the D_1 - L_{DC} - R_{DC} -IGBT- D_4 path for the positive half cycle of the line current, while the current passes through the D_2 - L_{DC} - R_{DC} -IGBT- D_3 path for the negative half cycle of the line current. As a result, L_{DC} and R_{DC} carry the current, which is of a unified direction, and the L_{DC} charges to the peak value of the line current. It is worth mentioning that L_{DC} and R_{DC} have small values and the voltage drops across them are inconsequential. In conclusion, the bridge acts as a short circuit and it bypasses the shunt branch of the BFCL under normal conditions. In the disturbance mode operation of the BFCL, the IGBT switch is turned off, and thus, the bridge part acts as an open circuit. Consequently, the line current is now forced to flow through the shunt branch, which restricts the current in fault mode operation.

In this work, sizeable impedance of the shunt branch is determined on the basis of the pre-fault active power flow through the line cable. The same amount of power flows through each line during normal operation. Each of the BFCLs placed in each line should absorb the same or a greater amount of power, which flows through the line in pre-fault conditions. Now, the power flow of each BFCL in post-fault conditions is presented by the following Equations [48]:

$$P_{BFCL} \geq \frac{P_G}{3} \quad (1)$$

$$P_{BFCL} = \frac{V_{PCC}^2 R_{sh}}{R_{sh}^2 + X_{sh}^2} \quad (2)$$

where V_{PCC} is the voltage at point of common coupling (PCC) and P_G is the active power delivered to the grid. The simplification of Equations (1) and (2) gives the following equation:

$$R_{sh} \leq \frac{3V_{PCC}^2 + \sqrt{9V_{PCC}^4 - 4P_G^2 X_{sh}^2}}{2P_G} \quad (3)$$

R_{sh} must be a positive value. Thus, the term inside the root must be positive. This obligatory condition gives the following equation for determining the size of shunt branch reactance:

$$X_{sh} < 1.5 \frac{V_{PCC}^2}{P_G} \quad (4)$$

A similar systematic method is adopted to determine the size of R_{sh} . Since the BFCL bridge part needs to be short-circuited during normal operation, with negligible impact, lower values of L_{DC} and R_{DC} are chosen on a trial-and-error basis so that the DC current flowing through them is smooth.

2.2. BFCL Control Strategy

The BFCL control signal is generated based on the detection of a fault in the system. Fault detection in AC/DC systems could be achieved by the amount of voltage dip or over-current at the point of common coupling (PCC) [49]. This work uses the amount of voltage dip to sense the fault, as shown in Figure 2.

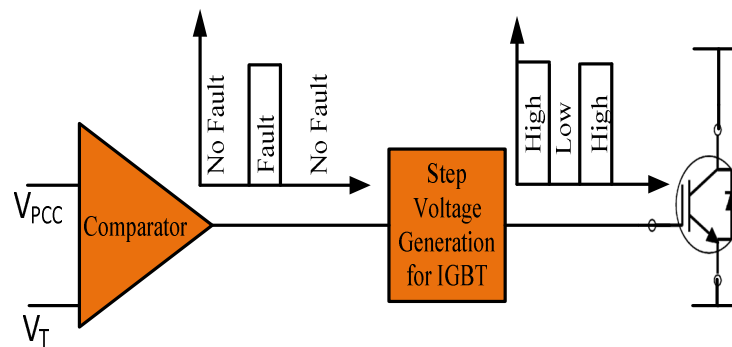


Figure 2. Control strategy of bridge-type fault current limiter.

A comparator circuit evaluates the voltage at PCC (V_{PCC}) with a pre-defined threshold voltage (V_T), which is arbitrarily chosen as 95% of the nominal V_{PCC} . V_T is chosen as 95% since the voltage below 0.95 p.u. is considered a worst-case scenario [50]. In normal conditions, V_{PCC} is greater than V_T . Therefore, the comparator provides a low signal output. The step voltage generation then provides a high-voltage signal to the gate of the IGBT and subsequently turns it on. Thus, the bridge part of the BFCL is short-circuited in this control mode. However, in faulty conditions, V_{PCC} has a voltage dip and while it is below 95% of its nominal value, V_T becomes higher than V_{PCC} . A fault appearance signal is generated in the output of the comparator and based on this signal, low step voltage is produced, which turns off the IGBT. Accordingly, the bridge part of the BFCL is open-circuited and line current is forced to flow through the shunt branch. Now, insertion of the sizeable shunt branch impedance in the line restricts fault current and hence improves the dynamic performance of DFIG wind integrated VSC-HVDC systems. The current through L_{DC} has a tendency to rise drastically during fault initiation. However, L_{DC} limits this current and the IGBT switch is protected against high di/dt .

3. DFIG Wind System Modeling

In this study, a doubly fed induction generator (DFIG) is used for generating wind energy as it has better performance in variable speed wind systems [51]. Another benefit of DFIG is that only small amounts of power, usually 25 to 30% of the machine-rated power, is controlled by converters. Thus, the power loss is reasonably low in the converters compared to cases where converters have to exchange the entire amount of power. The DFIG wind integrated VSC-HVDC system shown in Figure 3 is modeled and implemented in a real time digital simulator (RTDS) to show the efficacy of the proposed non-superconducting BFCL control strategy. The HVDC system allows power flow from the wind farm to the utility grid. HVDC link voltage must be controlled to a specified value for

the proper flow of the active power from the DFIG wind farm to the grid through the DC link. The proposed controller of the grid voltage source converter (GVSC) regulates the voltage of the DC link capacitor by controlling charging and discharging. The system components are modeled as follows.

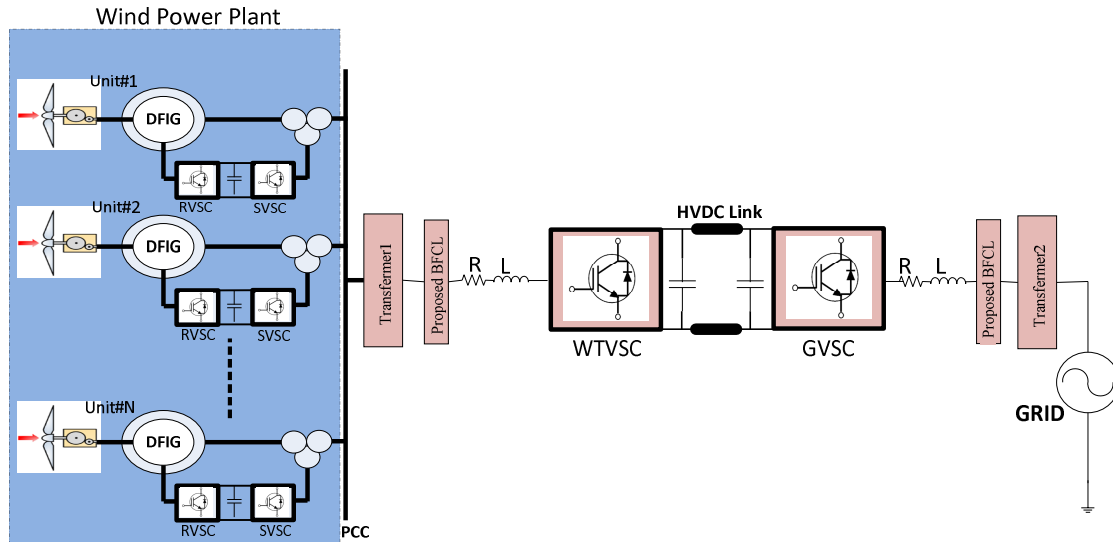


Figure 3. Schematic diagram of a doubly fed induction generator (DFIG) wind integrated voltage source converter-high-voltage DC (VSC-HVDC) system.

3.1. Wind Turbine Modeling

Generally, the operating principle of a wind turbine is described by its mechanical power, given as [52]:

$$P_{tur} = 0.5\rho AV_w^3 C_p(\lambda, \beta) \quad (5)$$

where ρ is air mass density in kg/m^3 , A is turbine swept area $= \pi r^2$, r is turbine radius, V_w is turbine speed in m/s, C_p is the performance coefficient, β is the blade pitch angle, and λ is the tip speed ratio.

The tip speed ratio is given by the following equation.

$$\lambda = \frac{r\omega_{tur}}{V_w} \quad (6)$$

where ω_{tur} is the turbine angular speed in rad/s. Power delivered by the wind turbine (P_{tur}) can be controlled by varying the performance coefficient. Variation of C_p is achieved by varying ω_{tur} and β since wind speed V_w cannot be controlled. C_p is a highly nonlinear function of β and λ given by the equation below [53].

$$C_p(\lambda, \beta) = \frac{1}{2}(\lambda - 0.022\beta^2 - 5.6)e^{-0.17\lambda} \quad (7)$$

3.2. Doubly Fed Induction Generator (DFIG) Modeling

Wind energy is extracted and integrated to the grid with a doubly fed induction generator, which is basically a three phase wound-rotor induction machine. A mechanically coupled gear box is used to connect the wind turbine with the DFIG system. The stator side of the DFIG is directly connected to the PCC, as shown in Figure 3, while the DFIG rotor is connected to the PCC with an AC/DC/AC conversion system with voltage source converters (VSCs). A common DC bus of the VSCs contains a capacitor. Rotor voltage in d - q frame is given as [54]:

$$V_{dr} = R_r i_{dr} + \sigma L_r \frac{di_{dr}}{dt} - \omega_{slip}(\sigma L_r i_{qr}) \quad (8)$$

$$V_{qr} = R_r i_{qr} + \sigma L_r \frac{di_{qr}}{dt} + \omega_{slip} (\sigma L_r i_{dr} + L_m i_{ms}) \quad (9)$$

where mutual inductance, $L_m = \frac{(L_o)^2}{L_s}$; leakage factor, $\sigma = 1 - \frac{(L_o)^2}{L_r L_s}$; R_r is the rotor resistance; L_r is the rotor inductance; L_s is the stator inductance; L_o is the magnetizing inductance; and ω_{slip} is the slip frequency, which is the difference between stator and rotor frequency.

4. Controller Design

The following subsections describe the design of the stator voltage source converter (SVSC), rotor voltage source converter (RVSC), wind turbine voltage source converter (WTVSC), and grid voltage source converter (GVSC) controllers in detail.

4.1. Control of Stator Voltage Source Converter (SVSC)

The stator-side converter consists of a two-level, six-pulse AC/DC VSC, the AC side of which is connected to the PCC and the DC side of which is connected to the capacitor. In the SVSC controller, the outer loop regulates DC bus voltage, while the inner loop controls current, as shown in Figure 4 [55].

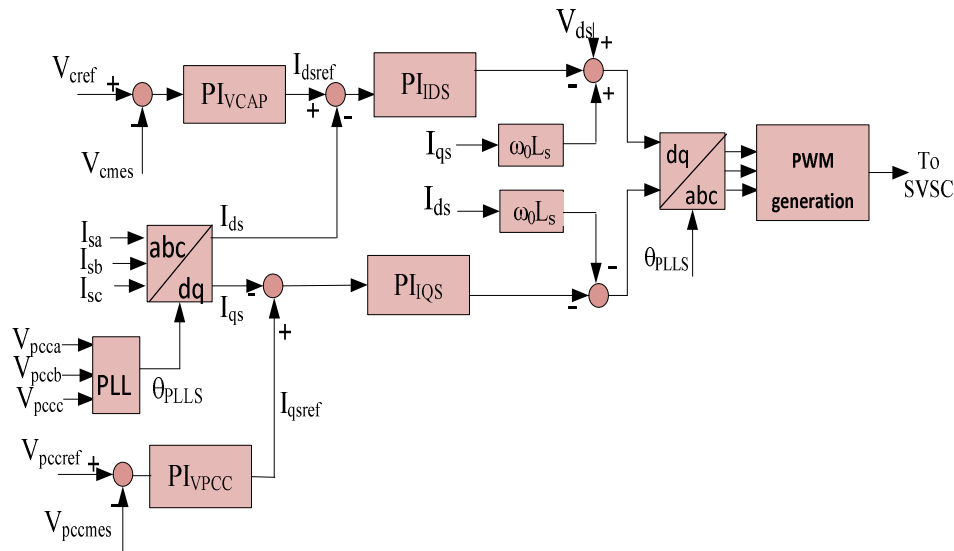


Figure 4. Schematic diagram of the stator voltage source converter (SVSC) controller.

The error between the measured DC capacitor voltage (V_{cmes}) and the reference voltage (V_{cref}) is processed by a proportional integral (PI) regulator. The output of the PI regulator provides the reference direct axis current (I_{dsref}) to an inner current controller. The measured three-phase stator current is converted to d - q components using Park's transformation and compared with corresponding reference currents then processed by inner PI current regulators. Output of the inner PI controllers is added with decoupling terms ($I_{qs}\omega_0 L_{sp}$ and $I_{ds}\omega_0 L_{sp}$) in which L_{sp} is the reactance between the SVSC terminal and the PCC. The stator-side converter consists of a two-level six-pulse AC/DC VSC, the AC side of which is connected to the PCC and the DC side of which is connected to a capacitor. In the SVSC controller, the outer loop regulates the DC bus voltage while the inner loop controls the current, as shown in Figure 4. The following subsections describe the design of the stator voltage source converter (SVSC), rotor voltage source converter (RVSC), wind turbine voltage source converter (WTVSC), and grid voltage source converter (GVSC) controllers in detail.

4.2. Control of Rotor Voltage Source Converter (RVSC)

The RVSC controller is developed in d - q frame to regulate powers, as in Figure 5. The base equations and symbol descriptions for the following controller are given in Section 3.2.

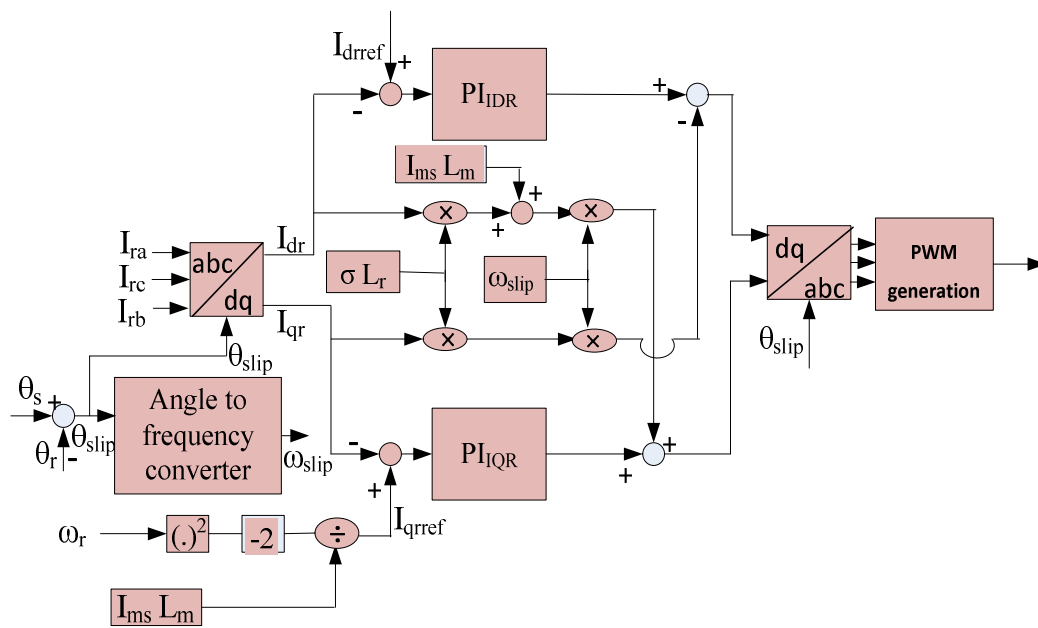


Figure 5. Schematic diagram of the rotor voltage source converter (RVSC) controller.

Figure 5 shows that the measured three-phase rotor current is converted to d - q components with a rotating reference frame (θ_{slip}), which is computed from the difference between the position of the stator flux (θ_s) and rotor flux (θ_r) vector [55]. Reactive reference rotor current (I_{qrref}) is provided by the optimal power point tracker, as shown in the above schematic diagram.

4.3. Control of Wind Turbine Voltage Source Converter (WTVSC)

The active power exchange between the wind farm and the grid is regulated by the WTVSC. Additionally, the reactive power interchange between the wind farm and the PCC can be controlled by the WTVSC in order to control AC voltage at the PCC. d - q components-based active and reactive powers are given as follows, as per instantaneous power theory [56].

$$P_s = \frac{3}{2} [V_d I_d + V_q I_q] \quad (10)$$

$$Q_s = \frac{3}{2} [-V_d I_q + V_q I_d] \quad (11)$$

Phase-locked loop (PLL) is employed to measure grid angle and synchronize VSC with the grid in such a way that the quadrature axis voltage (V_q) is zero. Thus, we get the following equations from the above two equations:

$$P_s = \frac{3}{2} V_d I_d \quad (12)$$

$$Q_s = -\frac{3}{2} V_d I_q \quad (13)$$

Therefore, control of active and reactive power is achieved by simply controlling the direct axis and quadrature axis current, respectively, as below.

$$I_{dref} = \frac{2}{3V_d} P_{ref} \quad (14)$$

$$I_{qref} = -\frac{2}{3V_d} Q_{ref} \quad (15)$$

By means of an a - b - c to d - q conversion technique, the following first-order differential equations and converter equations are obtained.

$$L \frac{dI_d}{dt} = L\omega_0 I_q - RI_d + V_{td} - V_d \quad (16)$$

$$L \frac{dI_q}{dt} = -L\omega_0 I_d - RI_q + V_{tq} - V_q \quad (17)$$

$$V_{td} = \frac{V_{DC}}{2} m_d \quad (18)$$

$$V_{tq} = \frac{V_{DC}}{2} m_q \quad (19)$$

where m_d and m_q are d -axis and q -axis modulating signals, respectively. Based on the above equations, the following controller has been developed for the WTVSC to control active and reactive powers.

As shown in Figure 6, inner current controllers control the active and reactive power with corresponding d -axis and q -axis currents, respectively. Both d -axis and q -axis currents are controlled by proportional integral (PI) controllers. Controller parameters for inner PIs are tuned by using the pole-zero cancellation technique. Implementation of a feed-forward filter (FFF) scheme removes undesirable start-up transient in VSC. The third harmonic injected pulse width modulation (PWM) method is adopted in this study as the required minimum DC bus voltage level is lower than classical PWM generation, which, in turn, increases system stability in the worst-case scenario [56]. In the third harmonic injected PWM technique, the squares of d -axis and q -axis signals are added together to generate the modulating signal (m). BFCL impedance is inserted by the control action during disturbances to keep the fault current within the limit, which eventually enhances transient stability of the DFIG-based HVDC system. Furthermore, the impact of fault current on wind turbine VSC is minimized by the proposed controller.

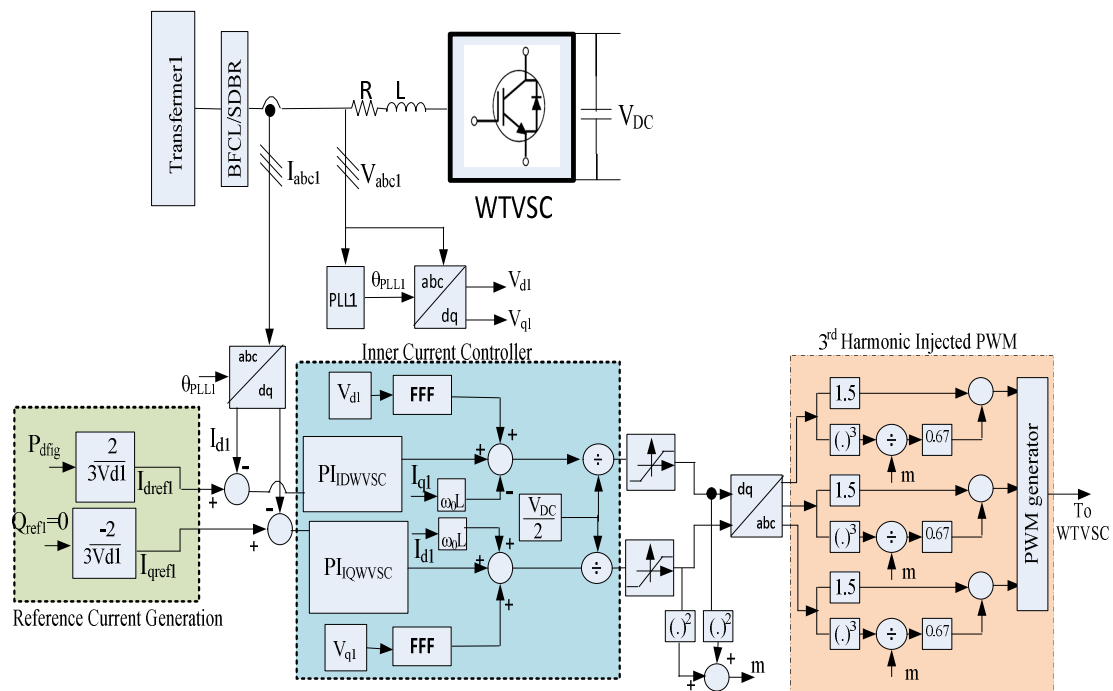


Figure 6. Schematic diagram of the wind turbine voltage source converter (WTVSC) controller.

4.4. Control of Grid Voltage Source Converter (GVSC)

Control performance of the outer DC link voltage controller directly affects the system's stability [57]. The GVSC controller employs a double control loop: an outer loop to control DC link voltage and an inner loop to control active and reactive power. The inner control loop for the GVSC is similar to the current control loop of the WTVSC and is presented in Figure 7. The main difference is that the reference active power (P_{ref2}) for the GVSC is delivered by the outer DC voltage regulator, as shown in Figure 7.

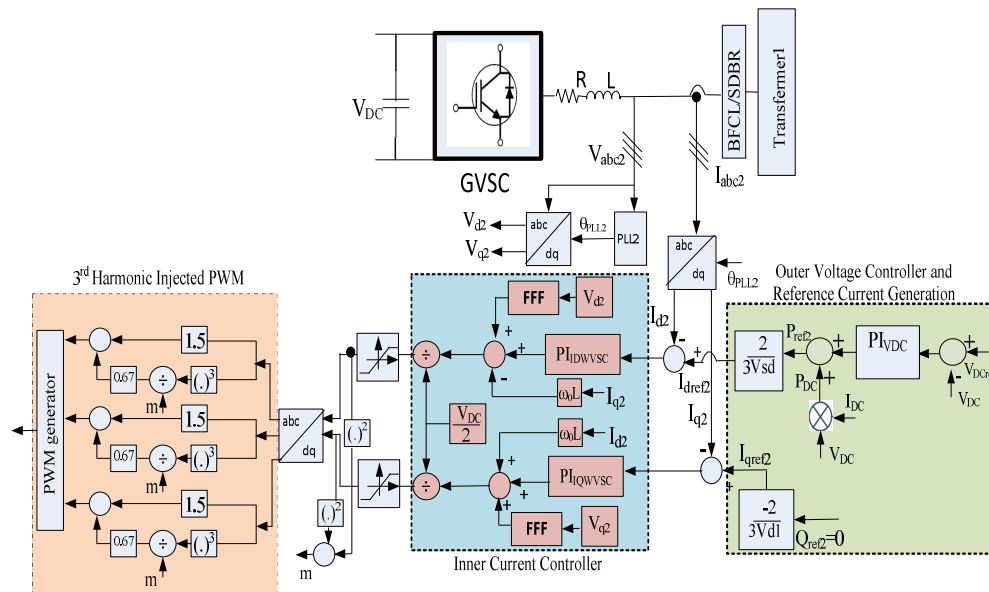


Figure 7. Schematic diagram of the grid voltage source converter (GVSC) controller.

In the outer voltage controller, the error between the measured DC voltage (V_{DCmes}) and the reference DC voltage (V_{DCref}) is processed by proportional integral (PI) controller. The outer PI parameters are obtained by employing the symmetrical optimum method [58]. The output of the outer PI is added to the amount of active power transferred from the wind farm to the grid for the active reference power generation of GVSC. Then, the d -axis reference current is generated and processed by the inner current control loop.

5. Results and Discussions

5.1. System Data

DFIG wind integrated VSC-HVDC with a BFCL system, as shown in Figure 3, is considered in this work to validate the proposed control strategies. The proposed fault current limiting device, the BFCL, is connected to both the wind power plant and the grid side of the system considered. The parameters of the HVDC system and the DFIG are listed in Tables 1 and 2, respectively.

Table 1. HVDC system parameters.

Parameter	Value
HVDC system power rating	30 MVA
Grid voltage	140 kV (L-L rms)
System frequency	60 Hz
Transformer rating	30 MVA
Transformer ratio	140/18 kV (Delta/Y)
Transformer equivalent delta side leakage inductance	110 mH
Resistor (R)	88 mΩ
Inductor (L)	8.5 mH
DC capacitor	500 μF
DC bus voltage	35 kV
BFCL shunt resistor	10 mΩ
BFCL shunt inductor	2 mH
SDBR resistor	10 mΩ
Feed forward function (FFF)	$1/(1 + 7 \times 10^{-6} \text{ s})$

Table 2. DFIG system parameters.

Parameter	Value
Power rating	2 MW
Stator voltage	0.69 kV
Stator resistance	0.001 Ω
Rotor resistance	0.0013 Ω
Stator reactance	0.0022 Ω
Magnetizing reactance	0.941 Ω
Rotor reactance	0.024 Ω
Rotor/stator turn ratio	2.6377

5.2. Controller Parameter Design

The pole-zero elimination method [59] is used to determine the parameters of the inner current controllers. In addition, the symmetrical optimum method [58] is used for parameter tuning of outer voltage controllers. Controller parameters obtained by these methods are listed in Table 3 for all proportional integral (PI) controllers.

Table 3. Controller Parameters.

Name	K _p	K _i
PI _{IDS}	0.300	10
PI _{IQS}	0.300	10
PI _{IDR}	1.387	35.6
PI _{IQR}	1.387	35.6
PI _{IDWVSC}	8.500	88
PI _{IQWVSC}	8.500	88
PI _{VDC}	0.1036	17.77

5.3. RTDS Implementation

The test system of Figure 3 is implemented in a real time digital simulator (RTDS) to confirm the efficacy of the proposed BFCL in enhancing the system's stability and improving the fault ride through capability. The proposed BFCL is also equated with the SDBR to demonstrate the augmentation of system performance to limit current during faults.

RTDS is a completely digital power system simulator working in real time. It comes with custom hardware with high-speed processor and software named RSCAD. The RTDS platform has been widely

recognized by most of the electrical utilities, research institutes, protection equipment manufacturers, and educational institutions for the development and testing of power system equipment [60].

The RTDS rack is connected to the workspace computer with a network hub, as shown in Figure 8. The DFIG system and associated controllers are built in RSCAD software and compiled in the workspace computer. After successful compilation, codes are downloaded to the RTDS hardware to run the system in real time and observe the system's behavior. Detailed RTDS implementation results are presented and discussed below.

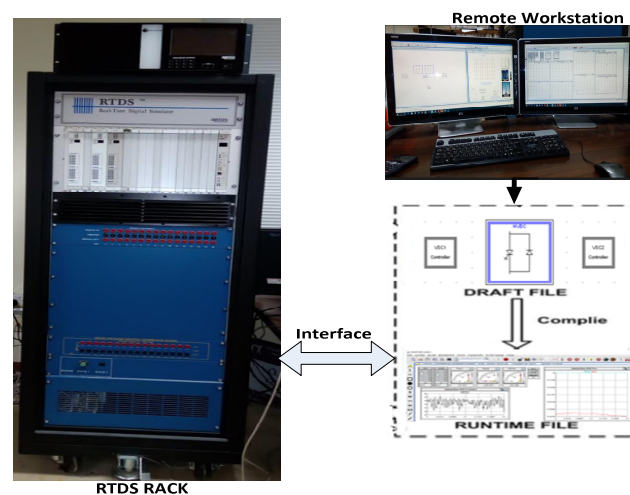


Figure 8. Laboratory setup of the real time digital simulator.

5.4. Simulation Results

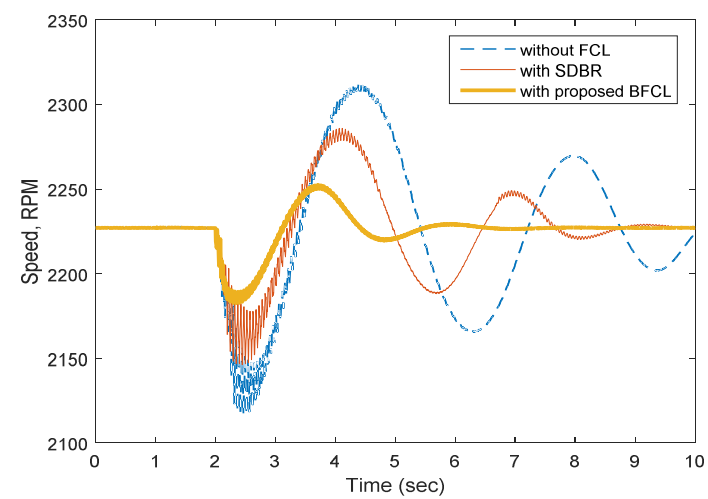
Initially, the system operates in its normal condition. Balanced 3LG and unbalanced 1LG disturbances are then applied separately at the point of common coupling. The duration of these faults is six cycles. Under each fault, three different simulation conditions are tested to show the effectiveness of the proposed BFCL control technique. These conditions are:

- (i) without FCL;
- (ii) with SDBR;
- (iii) with proposed BFCL.

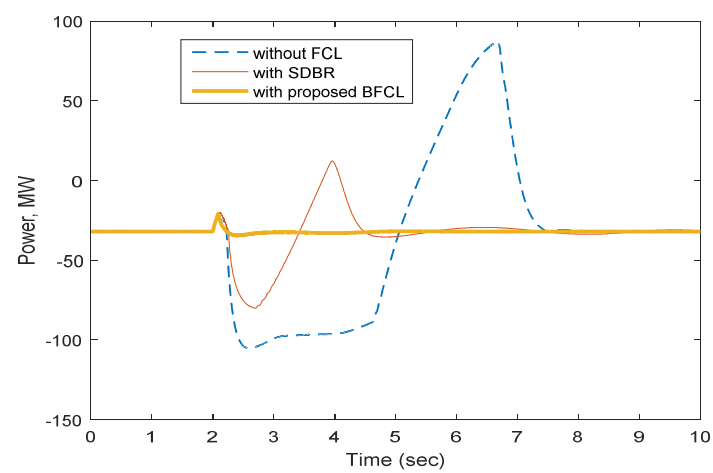
5.4.1. Balanced Fault Applications

At the start, the VSCs are disconnected from the system and the DC link capacitors are discharged. When the capacitors are fully discharged, VSCs are connected to the system through an interface reactor and resistors. As a result, the capacitors are now gradually charged and reach a steady state value. The reference voltage is then step-changed to 35 kV and all the controllers are unblocked. Thus, the outer DC link voltage controllers of the GVSC regulate the DC link voltage to the reference value. At this level, the system is ready to apply different faults and observe the improvement of the system's transient response with the proposed BFCL-based control technique.

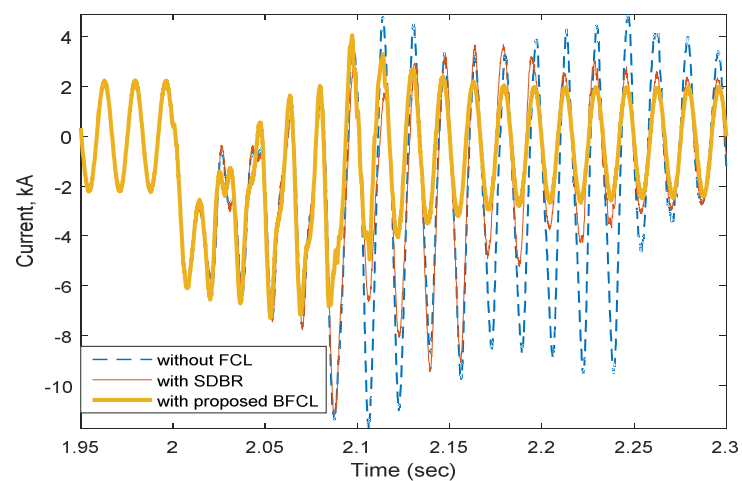
Figure 9a shows that the speed of the DFIG fluctuates over a wide range without any auxiliary controller for a balanced 3LG fault. The implementation of SDBR reduces speed fluctuation by only 40%, as observed below. On the other hand, the proposed non-superconducting BFCL-control-based approach provides a greater speed oscillation damping performance, which is around 65%. Moreover, the settling time for speed oscillation is 9.5 seconds with the SDBR, which is significantly reduced to 5.8 seconds with the proposed technique. The DFIG speed oscillates during the entire simulation period without any auxiliary control techniques. In addition, the effectiveness of the proposed BFCL solution is clearly visualized in Figure 9b–d for a 3LG fault at the PCC, as the DFIG power oscillations, stator fault current, and DC link voltage fluctuations have been greatly reduced.



(a)



(b)



(c)

Figure 9. Cont.

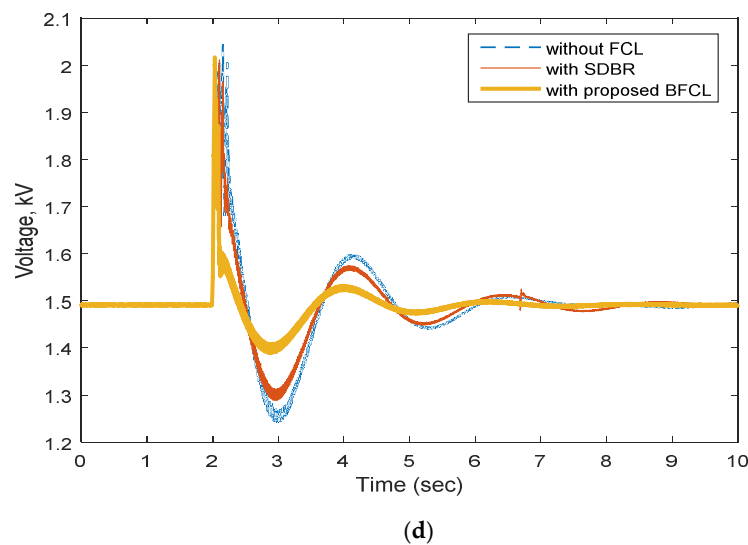


Figure 9. Comparison of transient response of DFIG system balanced 3LG fault at the point of common coupling (PCC). (a) DFIG speed; (b) DFIG active power; (c) DFIG stator current; (d) DC link capacitor voltage of wind power plant. FCL: fault current limiter; BFCL: bridge-type fault current limiter.

Improvement in HVDC system response with the proposed BFCL has also been observed. The DC capacitor voltage, grid active power, and grid current under the fault condition are shown in Figure 10. Figure 10a shows that the DC link voltage of HVDC is oscillating over the entire simulation period. The SDBR reduces voltage fluctuation by 26.6%, while the fluctuation is significantly suppressed, by 41.6%, with the proposed BFCL, as observed in Figure 10a. Reduction in grid power oscillation and fault current is shown in Figure 10b–c, where the superiority of the proposed BFCL is evident.

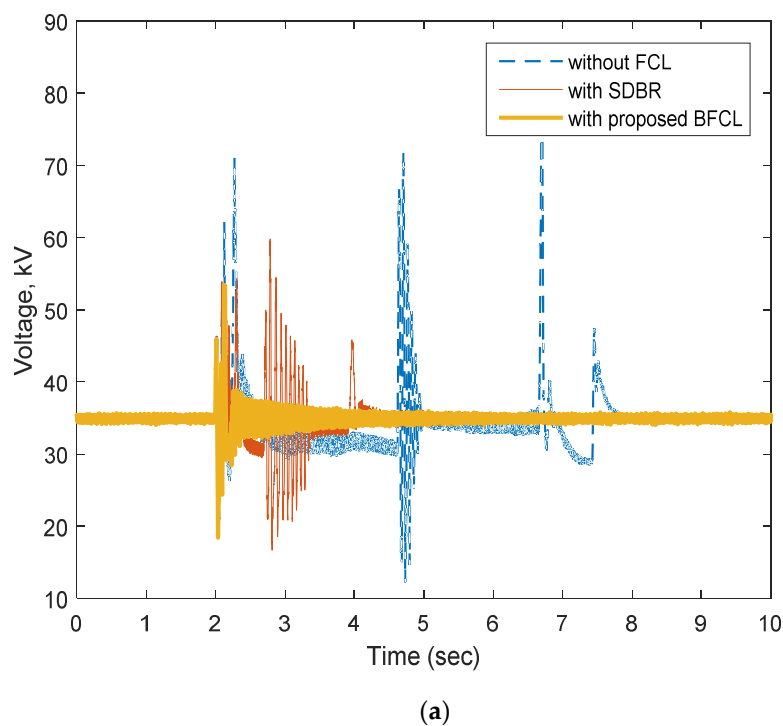


Figure 10. Cont.

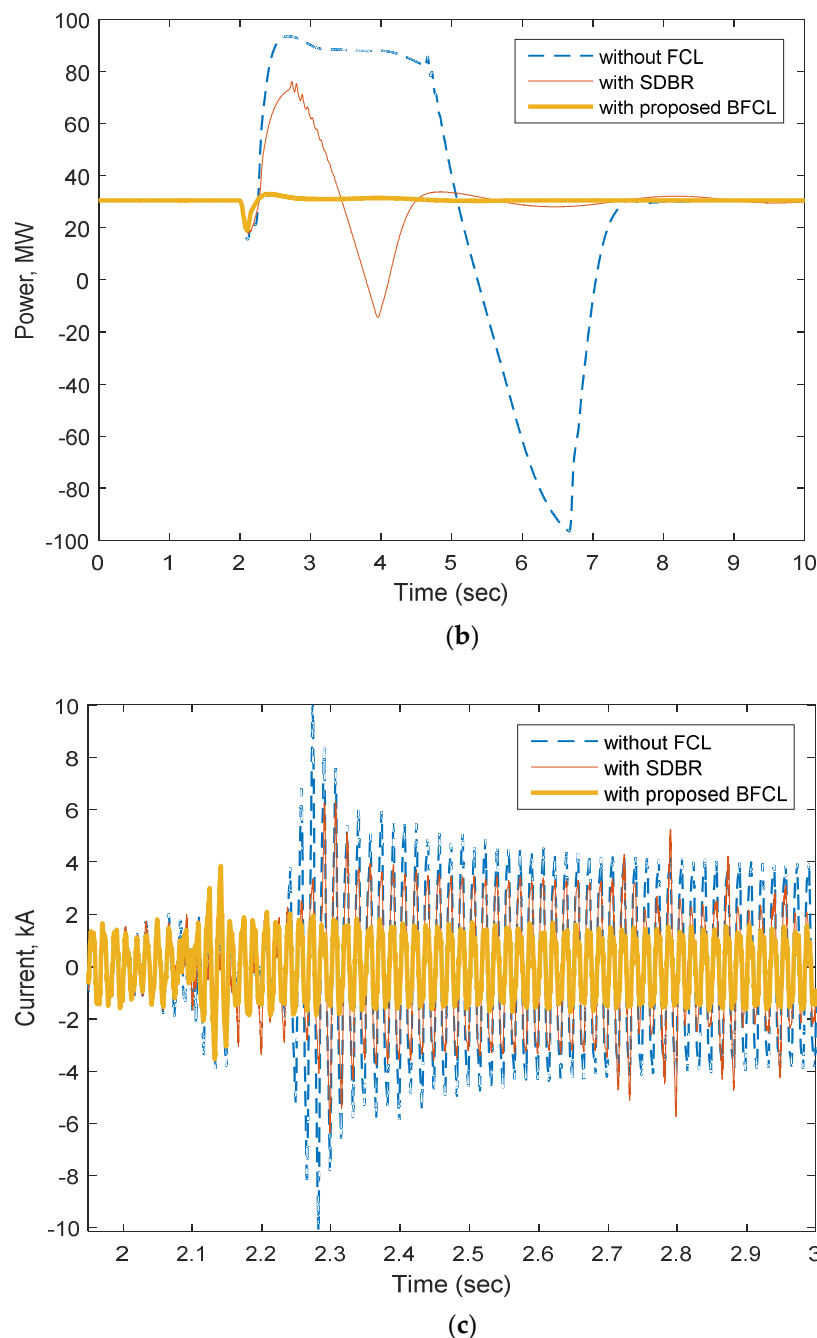
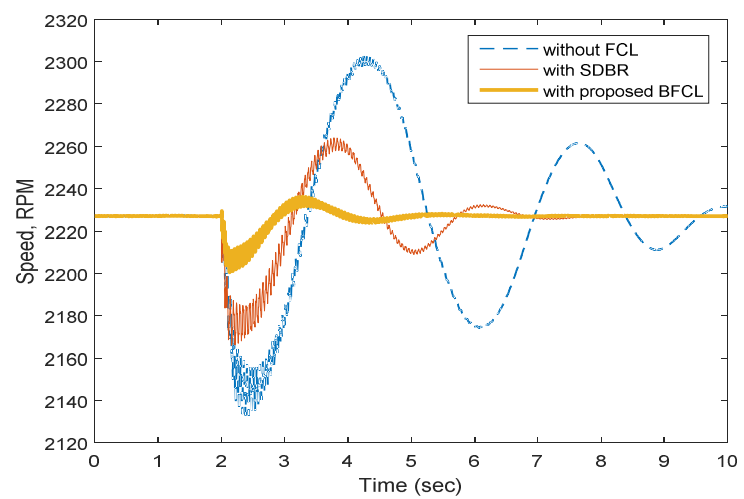


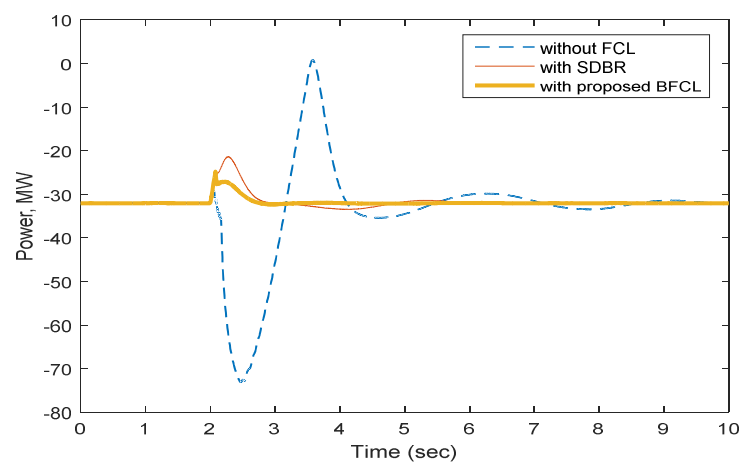
Figure 10. Comparative transient response of HVDC subject to a balanced 3LG fault at the PCC. (a) HVDC DC link voltage; (b) grid active power; (c) grid current.

5.4.2. Unbalanced Fault Applications

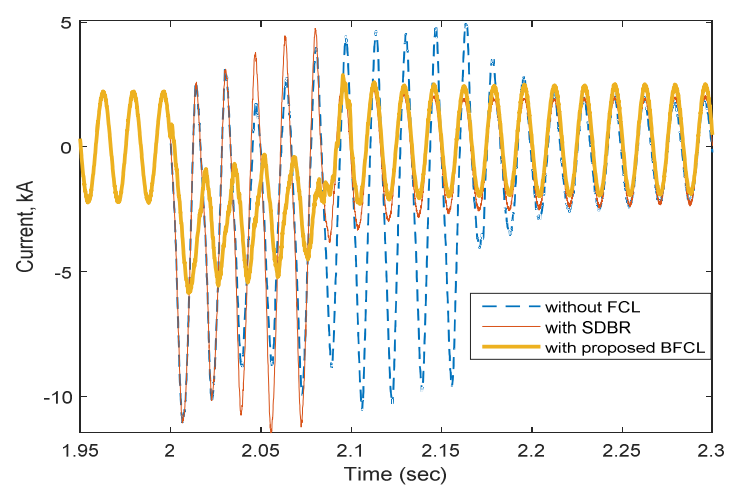
An unbalanced single-line-to-ground (1LG) fault was applied at the PCC. Real time simulation in Figure 11 clearly shows the positive effect of the proposed BFCL in reducing system oscillation. Figure 11a shows the DFIG speed response of the system with a 1LG fault applied at the PCC. Without FCL, DFIG oscillates over a wide range and does not reach the steady state value within the entire simulation period. System performance is slightly improved with the SDBR. However, the proposed BFCL-based strategy keeps the DFIG speed oscillation within a narrow range during the fault. Time taken for DFIG speed to reach its reference value is also small for the proposed BFCL compared to without FCL and under SDBR conditions. A noteworthy reduction in fault current, power oscillation, and capacitor voltage fluctuation is observed and shown in Figure 11b–d.



(a)



(b)



(c)

Figure 11. Cont.

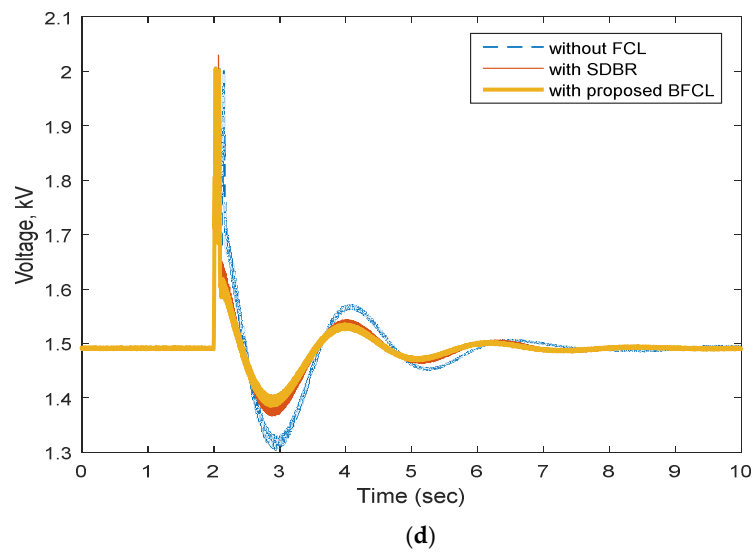


Figure 11. Comparison of the transient response of the DFIG system for an unbalanced 1LG at the PCC. (a) DFIG speed; (b) DFIG active power; (c) DFIG stator current; (d) DC link capacitor voltage of wind power plant.

Fault ride through capability of HVDC with the proposed BFCL is shown in Figure 12a–c. Without any fault current limiter, the DC link voltage of HVDC fluctuates exceedingly. With the application of the SDBR, fluctuation is reduced by 17.5%. Throughout the entire simulation period, the proposed BFCL keeps the DC link voltage within the permissible limit compared to the SDBR and without auxiliary controller. Line current and power profile improvement with the proposed control approach is shown in Figure 12b–c.

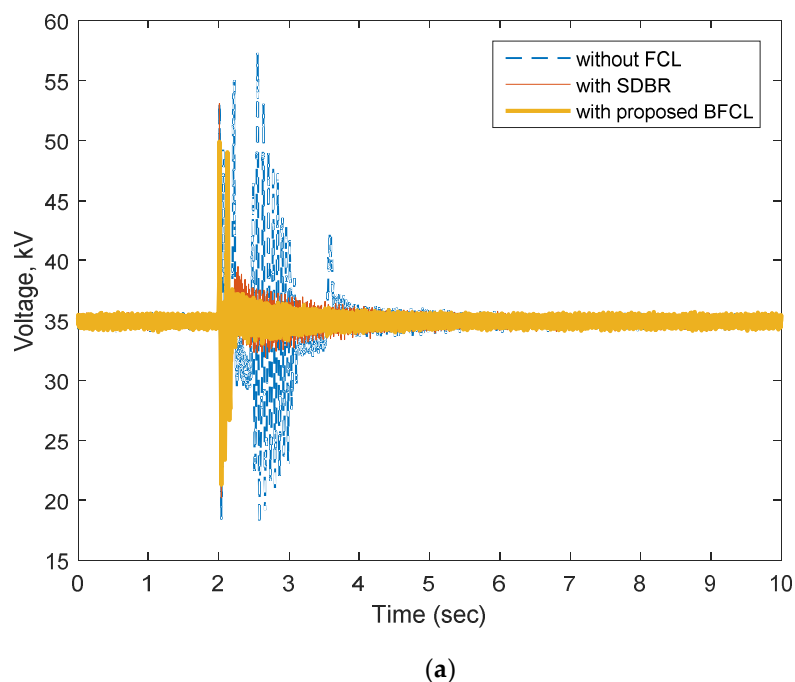
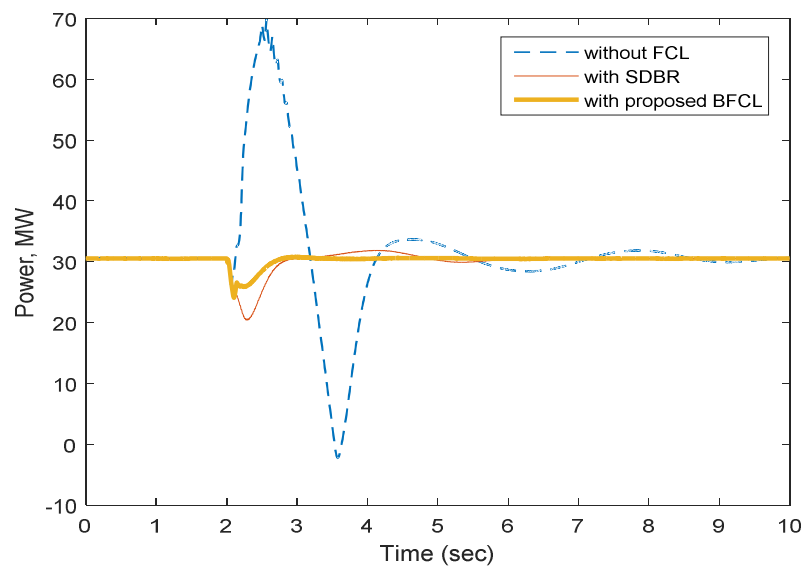
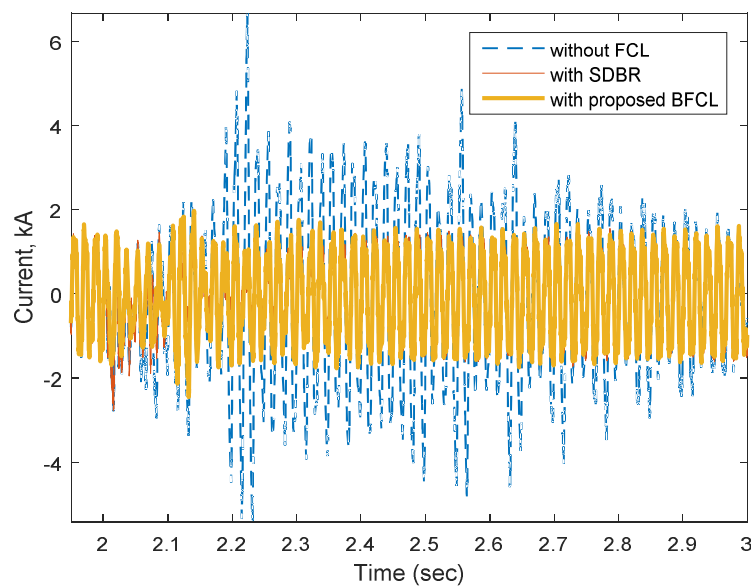


Figure 12. Cont.



(b)



(c)

Figure 12. Comparative transient response of HVDC subject to symmetrical fault at PCC. (a) HVDC DC link voltage; (b) grid active power; (c) grid current.

5.4.3. Index-Based Comparison

For a clearer perception of DFIG wind integrated VSC-HVDC system fault ride through capability enhancement with the proposed control-based BFCL, several performance indices are evaluated. These are based on the deviations in DC voltage, AC power, line current, and DFIG speed. The mathematical expressions for the above-mentioned indices are given as

$$DC_{volt} = \int_0^T |\Delta V_{DC}| dt \quad (20)$$

$$AC_{pow} = \int_0^T |\Delta P| dt \quad (21)$$

$$line_{curr} = \int_0^T |\Delta i| dt \quad (22)$$

$$DFIG_{speed} = \int_0^T |\Delta N| dt \quad (23)$$

where ΔV_{DC} , ΔP , Δi , and ΔN represent deviations of DC link voltage, active power flow, line current, and DFIG speed, respectively.

Performance indices for balanced and unbalanced disturbances are listed in Tables 4 and 5, respectively.

Table 4. DFIG wind-based HVDC system performance index improvement with the proposed method for balanced 3LG fault.

Index %	Without FCL	SDBR	Proposed BFCL
DFIG _{speed}	80.8175	42.3763	14.2806
DC _{volt} [DFIG]	0.068902	0.05728	0.026487
DC _{volt} [HVDC]	3.586	1.7927	0.68626
AC _{pow} [DFIG]	52.1791	11.119	0.6223
AC _{pow} [GRID]	49.975	10.4877	1.0446
line _{curr} [Stator]	0.73031	0.68826	0.63546
line _{curr} [Grid]	1.3788	0.55428	0.38678

Table 5. DFIG wind-based HVDC system performance index improvement with the proposed method for unbalanced 1LG fault.

Index Parameters, %	Without FCL	SDBR	Proposed BFCL
DFIG _{speed}	66.561	21.6401	4.9367
DC _{volt} [DFIG]	0.052067	0.035011	0.02854
DC _{volt} [HVDC]	1.5677	0.56259	0.46095
AC _{pow} [DFIG]	8.0379	1.1163	0.43776
AC _{pow} [GRID]	7.6162	1.2649	0.76578
line _{curr} [Stator]	0.73031	0.68826	0.63546
line _{curr} [Grid]	1.3788	0.55428	0.38678

The results in Tables 4 and 5 show that the deviations in all indices considered are much smaller with the proposed BFCL control strategy. It can be concluded that the performance of the DFIG wind integrated VSC-HVDC system is substantially improved with the proposed BFCL.

5.4.4. BFCL Implementation Feasibility

Bridge-type fault current limiter (BFCL) implementation requires diodes, an IGBT, inductors, and resistors. Nowadays, due to the advancement of power electronic applications, IGBTs and diodes with high ratings are available on the market. Therefore, the assembling cost of BFCL can be calculated for implementation in real DFIG-based VSC-HVDC systems. Even though the actual cost of the practical implementation of BFCL is not yet known; it can be inferred from the components needed for implementing BFCL.

6. Conclusions

In this study, a non-superconducting BFCL-based control approach was demonstrated for augmenting the FRT capability of DFIG wind integrated VSC-HVDC systems. Depending on fault detection based on PCC voltage, the BFCL controller was designed to insert resistance and inductance during system faults. Stator VSC and rotor VSC controllers were proposed to control DC link capacitor voltage and power, respectively. Current control approaches based in VSC-HVDC transmission system controllers were developed to deliver DFIG power to the grid. The systems, including wind turbine, DFIG, converters, HVDC cable, and associated controllers, were implemented in RTDS. Symmetrical as well as unsymmetrical faults were applied at the PCC to demonstrate the augmentation of system performance with the proposed method. The main outcomes of this study can be highlighted as follows:

- The proposed BFCL is a potential solution for restricting the fault current of DFIG wind-based VSC-HVDC during severe faults.
- DFIG speed, DC link voltage, and power oscillations were reduced significantly with the proposed BFCL control scheme.
- The superiority of the proposed BFCL-based control is demonstrated by comparing with the reported literature.

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Nomenclature

Abbreviations

BFCL	Bridge-type fault current limiter
DFIG	Doubly fed induction generator
FFF	Feed-forward function
FRT	Fault ride through
GSC	Grid-side converter
HVDC	High-voltage DC
IGBT	Insulated-gate bipolar transistor
PCC	Point of common coupling
PI	Proportional integral
PLL	Phase-locked loop
RSC	Rotor-side converter
RTDS	Real time digital simulator
SDBR	Series dynamic braking resistor
VSC	Voltage source converter
WT	Wind turbine

Subscripts

d	Direct axis
G	Grid
m	Mutual
mes	Measured
q	Quadrature axis
r	Rotor
ref	Reference
s	Stator
sh	Shunt

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