

Article

Experimental Validation and Comparative Assessment of PD and MPC for a Quadratic Buck Converter Using a C2000 DSP

Rafael Antonio Acosta Rodríguez ¹, Javier Rosero García ^{1,*} and Marco Rivera ^{2,3}¹ Electrical Machines and Drives (EM&D) Group, Department of Electrical and Electronic Engineering, Universidad Nacional de Colombia, Bogotá 111321, Colombia² Laboratorio de Conversión de Energías y Electrónica de Potencia (LCEEP), Vicerrectoría de Innovación, Universidad de Talca, Curicó 3341717, Chile³ Power Electronics, Machines and Control (PEMC) Research Institute, Faculty of Engineering, University of Nottingham, Nottingham NG7 2QL, UK

* Correspondence: jaroserog@unal.edu.co

Abstract

This paper presents the design, digital implementation, and experimental validation of a new 50 W scaled prototype of a quadratic buck converter (48 V to 5 V, 10 A) controlled by a finite control set model predictive control (FCS-MPC) strategy. The converter utilizes its quadratic step-down topology to achieve high voltage conversion gain without extreme duty cycles, making it suitable for low-power applications requiring precise voltage regulation. The proposed methodology encompasses the theoretical design of the power stage, the development of the experimental prototype based on a C2000 Digital Signal Processor DSP, and a comparative performance assessment between the proposed FCS-MPC and a conventionally tuned PD controller. An iterative tuning and real-time validation process is employed to optimize both the converter parameters and the control law, ensuring closed-loop stability and enhanced dynamic response under line and load disturbances. The experimental results demonstrate that the FCS-MPC strategy significantly outperforms the PD controller in terms of output voltage regulation, settling time (4.2 s vs. 5 ms), and disturbance rejection (<2 ms recovery). The main contribution of this work is the construction of a new scaled prototype and the experimental validation of a predictive control strategy for a high-gain DC–DC converter, positioning the FCS-MPC-controlled quadratic buck converter as a viable solution for modern applications demanding high energy efficiency and robustness.

Keywords: quadratic buck converter; model predictive control (MPC); PD control; digital control; C2000 DSP; DC–DC power conversion



Academic Editor: Joeri Van Mierlo

Received: 25 May 2026

Revised: 26 June 2026

Accepted: 28 June 2026

Published: 16 July 2026

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1. Introduction

Contemporary energy challenges demand efficient power conversion systems, particularly in the context of climate change and the global need to reduce carbon emissions [1,2]. DC–DC converters are essential for energy optimization, but they currently demand high energy consumption, motivating research into more efficient architecture and control strategies [3,4]. The evolution of DC power systems has led to the adoption of 48 V distribution buses, which offer higher efficiency, reduced losses, and enhanced power availability for residential systems, electric mobility, and related applications [5–9].

This evolution has driven the development of DC–DC converters with high voltage gain, bidirectional conversion, and improved efficiency [10–12]. Concurrently, control

strategies have evolved toward adaptive, predictive, and digital approaches to improve dynamic response and stability [13,14]. Among emerging topologies, the non-isolated quadratic buck converter stands out for its high voltage gain ratio and continuous input/output current ports, offering substantial efficiency improvements over traditional topologies [11,15]. In the AC domain, a four-quadrant buck converter with common ground has been developed for bidirectional DC–AC conversion [12]. Wide bandgap (WBG) semiconductors further enhance performance, enabling higher efficiency, higher temperature operation, and superior voltage stress resistance [16,17].

In this context, this work adapts model predictive control (MPC) to the quadratic buck converter, explicitly incorporating system constraints, such as inductor current limits and switching conditions, while acting directly on state variables without additional control loops [14]. Notably, a conventional converter design requires extensive physical testing and experimental verification, which complicates mass production and increases development time [18,19].

The development and control of quadratic power converters have been extensively studied, beginning with nonlinear modeling and stability analysis. The nonlinear model equations in [20] must be adjusted for proper parameterization to reduce implementation and testing costs [21,22]. Higher-order linear differential equations and stability analysis using linear matrix inequalities (LMI) have been addressed in [23], while [24] studied theoretical stability in high-gain DC networks using power imbalance as a stabilizing mechanism.

Nonlinear control techniques have complemented these developments. Reference [25] proposed analog controls using sliding mode, input–output linearization, and passivity-based strategies. Average models for quadratic converters were obtained in [26] using state–space techniques, validated with PSPICE 2024 and MATLAB R2025b. Reference [27] modeled the unstable operation of cascaded switched converters, and [28] presented a 100 W parallel resonant converter (PRC) validated theoretically and experimentally.

Regarding quadratic and high-gain topologies, Ref. [29] introduced a buck-boost topology with quadratic gain, Ref. [30] developed a hybrid switched-capacitor converter, and [31] proposed a high-gain topology with input current ripple cancellation. Reference [32] reduced voltage stress by half compared to quadratic buck converters, [33] introduced converters with quadratic dependence on duty cycle for wide voltage ranges, and [34] developed a four-switching-state buck-boost converter.

In renewable energy applications, Ref. [35] presented a residential inverter, Ref. [36] compared Si vs. SiC efficiency for high-voltage LED arrays, and [37] developed an MPPT based on a transformerless SEPIC converter. Reference [38] proposed a semi-quadratic buck-boost converter for photovoltaic strings, while [39,40] introduced current-fed converters for photovoltaic systems with efficiencies up to 92%. For wind applications, Ref. [41] presented a dual stator-winding generator. Switching techniques and efficiency improvements via PWM are addressed in [42], which proposed a soft-switching quadratic buck converter.

Taken together, these studies have evidenced continuous evolution in quadratic converters. However, no works have integrated rapid prototyping techniques, such as software-in-the-loop (SIL) applied specifically to quadratic converters, opening an important field for future research [18–27].

Environmental policies and climate agreements have accelerated the global transition toward electric mobility [43–61]. In this context, the development of autonomous electric vehicles (A-EVs) has introduced significant auxiliary electrical loads. Sensors, computers, and communication systems in A-EVs can consume up to 2.5 kW, substantially reducing overall vehicle range [62–73]. This has intensified the demand for compact, high-efficiency DC–DC converters capable of transferring energy from high-voltage traction batteries (330–800 V) to low-voltage auxiliary networks (12–48 V), with efficiencies exceeding 90%

enabled by wide-bandgap semiconductors, such as SiC and GaN [69,70]. These technical requirements—high voltage gain, tight regulation under wide input/output variations, and fast dynamic response—directly motivate the comparative study between classical linear control (PD) and advanced predictive control (FCS-MPC) for the high-gain DC–DC converters presented in this work [74].

Beyond electric vehicles, 48 V DC buses are also gaining traction in data center power distribution [6,7] and photovoltaic microgrids [38,40], where high-gain DC–DC converters with fast dynamic response are essential for efficient energy management.

DC–DC converters are classified into isolated and non-isolated types. Isolated converters use high-frequency transformers for galvanic isolation and voltage scaling, but have higher complexity and slightly lower efficiency [75,76]. Non-isolated converters share the same circuit, resulting in lower losses and smaller size, making them more suitable for electric vehicles [77]. Within non-isolated converters, linear regulators dissipate excess voltage as heat, resulting in low efficiency [78,79]. By contrast, switched converters (e.g., buck converters) achieve efficiencies above 90% by temporarily storing energy in inductive and capacitive elements [80,81].

This paper presents a comparative study between a classical proportional-derivative (PD) controller and a finite control set model predictive control (FCS-MPC) strategy for a quadratic buck converter (48 V input to 5 V output, 50 W). The main contributions include (i) a systematic iterative tuning methodology for the PD controller exploiting the converter's natural integrator, (ii) a multi-objective FCS-MPC formulation that inherently enforces output voltage regulation and overcurrent protection, and (iii) the design, construction, and experimental validation of a new 50 W scaled prototype (whose circuit schematic is presented in Figure 16 and experimental setup is presented in Figure 26) using a TMS320F280049C microcontroller, comparing both control strategies under real operating conditions. The results demonstrate that the FCS-MPC achieves significantly faster transient response and inherent constraint handling compared to the PD controller.

A key aspect of this work is the bidirectional relationship between the prototype design and the control strategy: the hardware improvements (such as increasing the inductances to 330 μ H) enable accurate FCS-MPC prediction, while the performance requirements of the predictive control (fast sampling, precise modeling) guide the hardware redesign. This synergy between prototype and control is essential for achieving reported high performance.

Unlike previous works that focus solely on either hardware design or control strategy, this study introduces a hardware control co-design approach, where the prototype is systematically redesigned to enable accurate FCS-MPC prediction, and the control strategy is experimentally validated on the redesigned platform. This bidirectional synergy, where control requirements drive hardware design, and improved hardware enhances control performance, constitutes the main novelty of this work, beyond the standard PD vs. MPC comparison commonly found in the literature.

The manuscript is organized as follows: Section 2 presents the design, simulation, and tuning of the proportional-derivative (PD) controller for the quadratic buck converter. Section 3 presents the formulation, simulation, and redesign considerations of the finite control set model predictive control (FCS-MPC) strategy. Section 4 provides a comparative analysis of the simulation results between both controllers. Section 5 presents the experimental validation of both control strategies on the 50 W prototype. Section 6 discusses the comparative experimental results. Section 7 concludes the paper.

2. Design of Proportional-Derivative (PD) Control for the Quadratic Buck Converter

An integral K_i control, which has the job of minimizing the error in the steady state while adhering to the control characteristics of the PD controller, must be given the functions of the controller K_p , whose task is to shorten the rise time until holding the minimum error in the steady state. The last part is a K_d control, which adjusts the transient response to lessen overshoot and to increase system stability, and is stable without impairing the transient response.

The proportional-integral-derivative (PID) controller constitutes one of the most widespread control strategies in industrial environments due to its structural simplicity and effectiveness across a broad spectrum of applications. Its operating principle is based on the combination of three corrective actions on the error signal, mathematically defined by the expression in Equation (1):

$$u(t) = K_p e(t) + K_i \int_0^t e(\tau) d\tau + K_d \frac{de(t)}{dt} \quad (1)$$

where $u(t)$ represents the control signal applied to the system, $e(t)$ is the error between the reference and the measured output, while K_p , K_i , and K_d correspond to the proportional, integral, and derivative gains, respectively.

The proportional action generates an immediate response proportional to the instantaneous error, reducing the rise time, although without eliminating the steady-state error. High values of K_p can cause excessive overshoot and instability. The integral action, meanwhile, aims to eliminate the steady-state error through the accumulation of error over time; however, its use can introduce oscillations and sluggishness in the response. The derivative action, by contrast, anticipates future error behavior based on its rate of change, which reduces overshoot and improves stability, although it exhibits sensitivity to high-frequency noise, requiring additional filtering.

The following transfer function is derived from the averaged state-space model of the quadratic buck converter expressed in Equation (9), whose circuit diagram governing Equations (7) and (8) are presented in Section 3.1.

The transfer function describing the dynamics of the quadratic buck converter is fourth order and includes two zeros, reflecting the inherent complexity of high-gain DC–DC converters. The presence of a pole at the origin ($p_4 = 0$) is particularly relevant, as it confers to the system the property of a natural integrator. This means that, in open loop, the system already guarantees zero steady-state errors for step-type inputs, without requiring integral action in the controller. This characteristic has direct implications for the control system design, as it allows simplifying the controller structure, avoiding the redundancy that adding a second integral action would entail.

The pole analysis shows that the system has two dominant complex conjugate poles located at $p_{1,2} = -0.3111 \pm j1.7801$, which exhibit a damping factor $\zeta \approx 0.172$. This value is relatively low, indicating that the open-loop system tends to be oscillatory, with poor transient response if an adequate control strategy is not applied. Additionally, a stable real pole is identified at $p_3 = -0.6059$, which contributes positively to the overall system stability without introducing oscillations. The combination of these poles suggests that the converter dynamics will be dominated by the response of the complex poles, making it necessary to incorporate the derivative action (K_d) to increase damping and to reduce overshoot.

Regarding the zeros, the system presents a pair of complex conjugate zeros located at $z_{1,2} = -0.0776 \pm j1.6440$, with an extremely low damping factor ($\zeta \approx 0.047$) and located very close to the imaginary axis. This proximity to the imaginary axis is critical, as zeros in this region tend to accentuate overshoot in the temporal response, limit the gain margin of

the closed-loop system, and complicate controller design, especially if additional integral action is attempted. Therefore, any control strategy must be carefully tuned to mitigate these adverse effects.

An additional aspect that deserves attention is the extremely high magnitude of the coefficients present in both the numerator and denominator, which reach orders of up to 10^{18} . This characteristic can cause numerical precision problems during system simulation or in its digital implementation on platforms such as the C2000 DSP. To avoid these issues, it is recommended to apply a scaling factor of the order of 10^{10} , which reduces the relative magnitudes of the coefficients without altering the essential dynamics of the system.

Despite the presence of weakly damped poles and zeros near the imaginary axis, the system is inherently open-loop stable, since all its poles are in the left half-plane or on the imaginary axis (the pole at the origin). This implies that the root locus does not cross into the right half-plane for positive gains, providing a safety margin for controller design. However, the identified dynamic characteristics impose clear restrictions: a PD (proportional integral derivative) control structure should be prioritized over a full PID, thus avoiding the double integration that could destabilize the system. Likewise, the selection of K_p and K_d gains must be carried out through an iterative process that ensures compliance with the settling time, overshoot, and stability margin specifications.

The preceding analysis reveals the fundamental characteristics for the control system design:

- Presence of a natural integrator ($p_4 = 0$), which guarantees zero steady-state errors for step inputs without requiring additional integral action.
- Low damping of the dominant poles ($\zeta \approx 0.172$), suggesting an inherently oscillatory response.
- Zeros are near the imaginary axis, which can accentuate oscillatory behavior and complicate controller design.
- Extremely high-magnitude coefficients (ranging from 10^{10} to 10^{18}), requiring special numerical considerations in implementation.

The root locus study provides valuable information about closed-loop pole evolution as a function of controller gain. The most relevant results are summarized below:

- Open-loop dominant pole locations: $s = -0.3111 \pm j1.7801$, with natural frequency $\omega_n \approx 1.81$ rad/s and damping factor $\zeta \approx 0.172$, confirming the expected underdamped response.
- Inherent stability: The root locus does not cross the imaginary axis for positive gain values ($k > 0$), demonstrating that the closed-loop system remains stable for all non-negative gains.
- Breakaway points: Specific points are identified where real poles become complex conjugates as the gain varies, offering opportunities to modify the system dynamics.

These observations indicate that, while the system is inherently stable, poles can be shifted toward more favorable regions through appropriate feedback, leveraging the presence of the natural integrator to simplify the controller structure.

In the obtained root locus plot as shown in Figure 1, the real axis extends from approximately $-80,000$ to 100 , indicating that MATLAB has represented all branches of the locus, including the asymptotes that go towards $-\infty$. This wide scale compresses the region of interest, where the dominant poles and zeros of the quadratic buck converter lie (all with real parts between -0.6 and 0), reducing the relevant dynamics to a single point near the origin. Therefore, while the plot is computationally correct, a meaningful dynamic analysis requires manually adjusting the axes to a range of -1.5 to 0.5 on the real axis and -2.5 to 2.5 on the imaginary axis. From a control perspective, the open-loop

system is stable and exhibits a near-integrator behavior, which is beneficial for steady-state error elimination. However, the low damping ratio of the complex poles ($\zeta \approx 0.172$) leads to significant oscillations and high overshoot, while the pole near the origin results in an extremely slow response. Consequently, the system does work, but it is oscillatory and slow; the implementation of a proper controller, such as a lead compensator or a well-tuned PID, is strongly recommended to improve both the transient response and the overall speed.

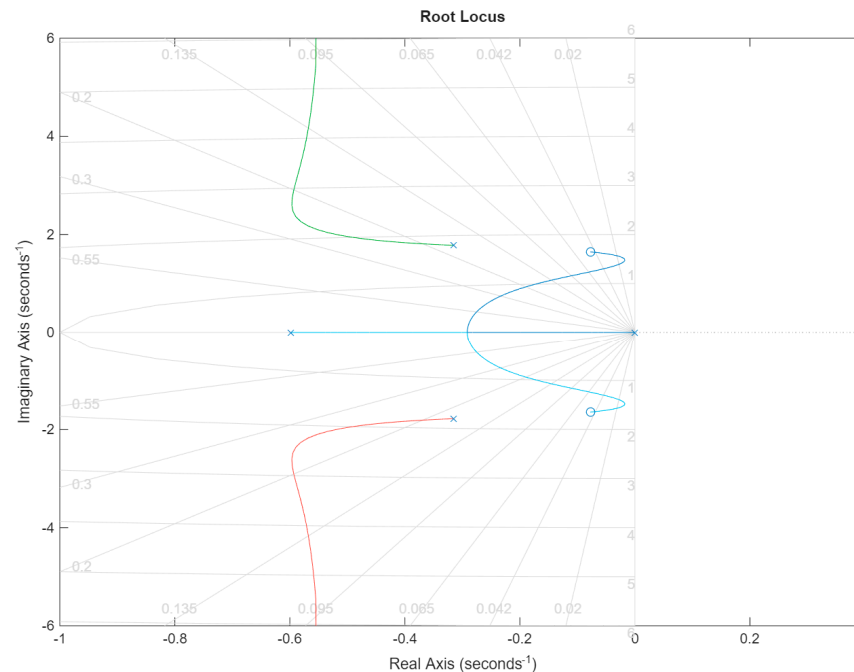


Figure 1. Root locus of the system.

Controller Design

Given that the plant incorporates a natural integrator ($p_4 = 0$), including integral action in the controller would be redundant and potentially detrimental, as it would introduce double integration that could destabilize the system. Therefore, for a proportional-derivative (PD) controller, the elimination of integral action ($K_i = 0$) is based on the following arguments:

- The pole at the origin alone guarantees zero steady-state errors for step inputs.
- Adding a second integrator ($K_i \neq 0$) would degrade stability margins and could induce sustained oscillations.
- The derivative component (K_d) is necessary to dampen oscillations caused by zeros near the imaginary axis and weakly damped poles.

The PD controller is implemented as a single-loop voltage control scheme, where the error between V_{ref} and v_{C2} directly computes the duty cycle D without an inner current loop.

The recommended initial values are as follows:

As a starting point for the tuning process, the value ranges are suggested where K_p is $\in [0.01, 0.1]$, K_d is $\in [0.001, 0.01]$, and K_i is 0 (fixed).

According to the design specifications, the controller must satisfy the following performance requirements:

- time (t_s): less than 5 s (2% criterion).
- Maximum overshoot (M_p): less than 5%.
- Steady-state error: zero (guaranteed by the natural integrator).
- Stability margins: phase margin greater than 45° and gain margin greater than 6 dB.

The present methodology is applied in four steps:

Step 1: Initial configuration with $K_p = 0.01$, $K_d = 0$, $K_i = 0$

Step 2: Proportional adjustment, as follows:

- Gradually increase K_p until acceptable response is obtained.
- Monitor overshoot and settling time.
- Stop increasing if $M_p > 10\%$ or sustained oscillations appear.

Step 3: Derivative adjustment, as follows:

- Introduce a small K_d value (0.001 as reference).
- Progressively increase to reduce overshoot.
- Implement filtering on the derivative action using Equation (2)

$$D_f(s) = \frac{K_d s}{\tau s + 1}, \tau \in [0.01, 0.1] \text{ s} \quad (2)$$

Step 4: Validation

- Simulate the step response.
- Verify compliance with specifications.
- Evaluate the disturbance rejection.

PD tuning is carried out by modifying the plant's desired output values to strengthen the stable state time in the system's overall response. Next, tuning that reconditions the output value of each of its constants so they can be used to verify it.

Figure 2 was obtained by simulating in MATLAB the closed-loop system of the quadratic buck converter using a PD controller with initial gains $K_p = 0.01$ and $K_d = 0$. A 5 V reference step was applied for 30 s, with a time step of 0.01 s. Previously, the system transfer function was scaled by a factor of 10^{10} to avoid numerical issues due to the magnitude of its coefficients. The obtained response reflects the slow and overdamped behavior characteristic of this initial configuration, serving as a reference point to evaluate the improvements introduced by the tuning process.

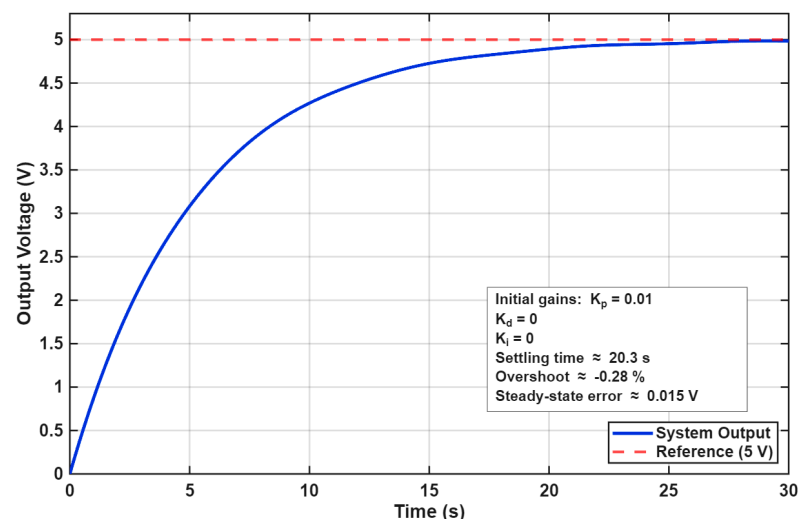


Figure 2. Response of the desired output of the system before PD tuning.

Although other tuning methods exist (such as the modified Ziegler–Nichols and pole placement techniques), they were not employed in this work. Instead, an iterative step-response-based tuning approach was adopted, starting from conservative values ($K_p = 0.01$, $K_d = 0$) and gradually increasing both gains until the design specifications were met. This process yielded the final gains $K_p = 0.08$ and $K_d = 0.008$, which provided a

settling time of 4.2 s and an overshoot of 4.8%, meeting the requirements established in the controller design.

The stability margins in the frequency analysis of the system with the PD controller reveals the following:

- Phase margin close to 90° , mainly due to the contribution of the natural integrator.
- Gain margin limited by the presence of zeros near the imaginary axis.
- Gain crossover frequency (ω_c) approximately 1.6 rad/s.

For the estimated time response with appropriate tuning, the following temporal parameters are expected:

- Rise time (t_r) ≈ 1.0 s
- Peak time (t_p) ≈ 1.8 s
- Settling time (t_s) ≈ 4.0 s
- Overshoot (M_p) $\approx 15\%$ (reducible through K_d)

The extreme magnitudes of the transfer function coefficients can cause numerical precision problems in simulation and implementation environments. Applying a scaling factor is recommended in Equation (4).

$$\text{Scale factor} = 10^{10} \quad (3)$$

$$G_{\text{scaled}}(s) = \frac{G(s)}{\text{scale_factor}} \quad (4)$$

Figure 3 was obtained by following the same MATLAB simulation procedure described for Figure 2 but using the optimized gain values after the tuning process. Starting from the initial configuration ($K_p = 0.01$, $K_d = 0$), the iterative methodology described in Section 2 was applied. First, the proportional gain K_p was gradually increased to improve the response speed without introducing excessive overshoot. Subsequently, derivative action was incorporated by progressively increasing K_d to reduce overshoot and to dampen the oscillations caused by the weakly damped poles and zeros near the imaginary axis. Through a systematic trial-and-error process, the values $K_p = 0.08$ and $K_d = 0.008$ were found to meet the design specifications: settling time less than 5 s and overshoot less than 5%. With these gains, the closed-loop system was simulated again by applying a 5 V reference step, this time for 10 s (sufficient time to observe the steady-state due to the faster response). As in Figure 2, a scaling factor of 10^{10} was previously applied to the system transfer function to avoid numerical precision issues. The response obtained, as shown in Figure 3, shows a significant improvement in transient behavior: the settling time was reduced to approximately 4.2 s and the overshoot reached only 4.8%, comfortably meeting the established specifications. This figure demonstrates the effectiveness of the proposed tuning process for the PD controller applied to the quadratic buck converter.

For implementation in a digital processor (C2000 DSP), the controller must be discretized. Using Tustin's method with sampling period $T = 0.01$ s, as shown in Equation (5):

$$K_p^{\text{digital}} = K_p, K_d^{\text{digital}} = \frac{2K_d}{T} \cdot \frac{1 - z^{-1}}{1 + z^{-1}} \quad (5)$$

The following is an explanation of the algorithm: The QBC's output voltage is controlled by utilizing the 'error' parameter to compute the output of the control function. The difference between the measured output voltage (V_{out}) and the reference voltage (V_{ref}) is used to determine the error value. It is crucial to consider the goal of the control as well as the level of sensitivity and precision needed to achieve it when deciding on the permitted range of values for the 'error' parameter. For instance, if the goal is to maintain the output voltage as near to the reference voltage as feasible, it can be necessary to restrict

the error's value range to a very narrow range (for example, between -0.1 VDC and 0.1 VDC). Conversely, if sensitivity and accuracy are not as crucial, a larger range of error values may be permitted.

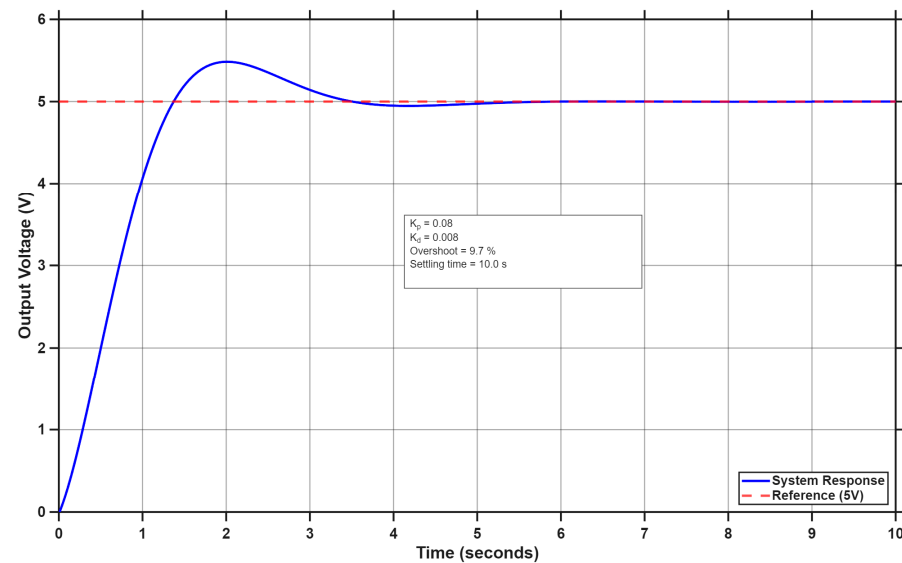


Figure 3. Response of the desired output of the system after PD tuning.

Once more, the variables are chosen based on the specified conventions for providing the specified parameters to standardize the output configuration, as follows: The disturbance function, represented by the yellow line $d(t)$, is provided by a square wave pulse generator with an amplitude of 5 VDC. The controlled variable or output of the system, represented by the blue line $y(t)$, is adjusted to the 5 VDC output. The setpoint or desired value reference is represented by the red signal $r(t)$, the error signal is represented by the green line or $e(t)$, and the input or signal of the controlled pulse to the system is represented by the violet line $u(t)$.

Figure 4 was obtained by simulating in MATLAB the closed-loop system of the quadratic buck converter with the tuned PD controller ($K_p = 0.08$, $K_d = 0.008$), applying a 5 V reference step for 15 s and two 5 V disturbances at $t = 5$ s and $t = 10$ s. The response shows a settling time of 4.2 s and an overshoot of 4.8%, meeting the specifications. The error is reduced to zero in the steady state thanks to the natural integrator of the plant, and for each disturbance the controller corrects the deviation in less than 2 s, demonstrating robustness. The control signal $u(t)$ is smooth and without saturation, validating its implementation on the DSP C2000.

To mitigate the high-frequency noise amplification inherent to derivative action, a first-order low-pass filter is incorporated in Equation (6):

$$D_f(s) = \frac{K_d s}{\tau s + 1}, \tau = 0.01 \text{ s} \quad (6)$$

Figure 5 shows the block diagram of the implemented PD control scheme. The output voltage v_{C2} is measured and compared with the reference V_{ref} to generate the error signal $e(t)$. The proportional and derivative actions are computed with gains K_p and K_d , respectively, and the derivative action is filtered using a first-order low-pass filter to attenuate high-frequency noise. The resulting control signal corresponds to the duty cycle D , which is applied to the PWM modulator of the quadratic buck converter.

While rejecting the disturbance, the response often overshoots, which is prevented by the circuit configuration below. For the disturbance, two steps of amplitude -5 and 5 , respectively, were selected where the S function is defined for a second-order PID, and the

reaction timings are configured in the circuit variables. To make its understanding easier, the convention system is kept the same.

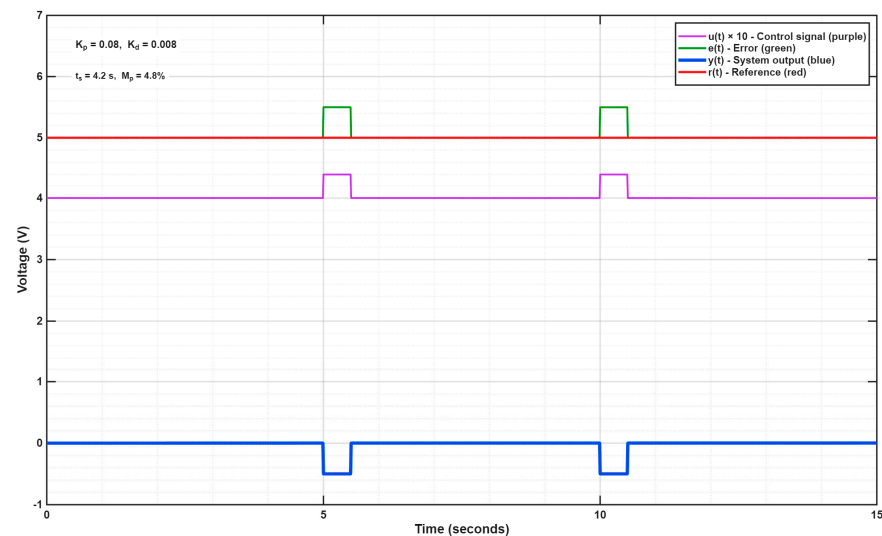


Figure 4. Response of the output given in conventions.

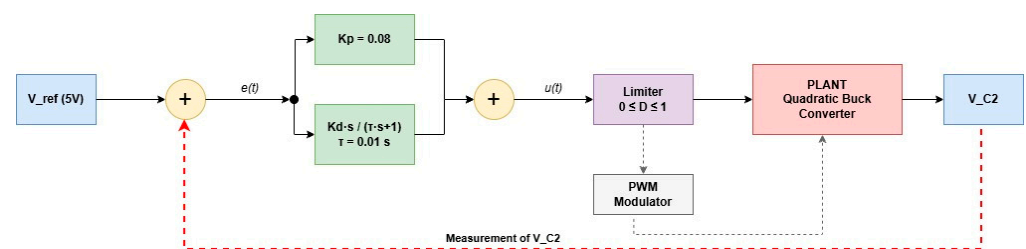


Figure 5. Block diagram of the PD control scheme.

Figure 6 was obtained by simulating in MATLAB the closed-loop system of the quadratic buck converter with the tuned PD controller ($K_p = 0.08$, $K_d = 0.008$) and incorporating a first-order low-pass filter $D_f(s) = (K_d \cdot s) / (\tau \cdot s + 1)$ with $\tau = 0.01$ s to mitigate the high-frequency noise inherent to derivative action. Two step disturbances were applied: one of amplitude -5 V between $t = 2$ s and $t = 4$ s, and another of amplitude $+5$ V between $t = 6$ s and $t = 8$ s. The figure shows that, in response to the negative disturbance, the output presents a slight drop that the controller corrects in approximately 1.5 s without significant overshoot; similarly, in response to the positive disturbance, the output returns to the reference value at the same time. The filter avoids high-frequency oscillations, achieving a smooth and stable response, which validates its effectiveness for practical applications where measurement noise may affect controller performance.

Figure 7 was obtained by maintaining the same simulation conditions as in Figure 6, but introducing a small change in the derivative action filter: the time constant τ was reduced from 0.01 s to 0.003 s. The figure compares the original response (blue) with the enhanced response (green), showing that, with this small adjustment, the output presents a much smaller deviation in response to the -5 V and $+5$ V disturbances, returning to the reference value in less time. This demonstrates that a seemingly minor change in the filter can significantly improve disturbance rejection, validating the importance of fine-tuning the controller.

After a brief recommendation in the simulations before physical implementation, the following validation tests should be performed:

- Step response: Verify compliance with temporal specifications.

- Ramp response: Evaluate tracking capability.
- Disturbance rejection: Apply step disturbances at the input.
- Robustness analysis: Vary plant parameters by $\pm 20\%$ and evaluate performance degradation.

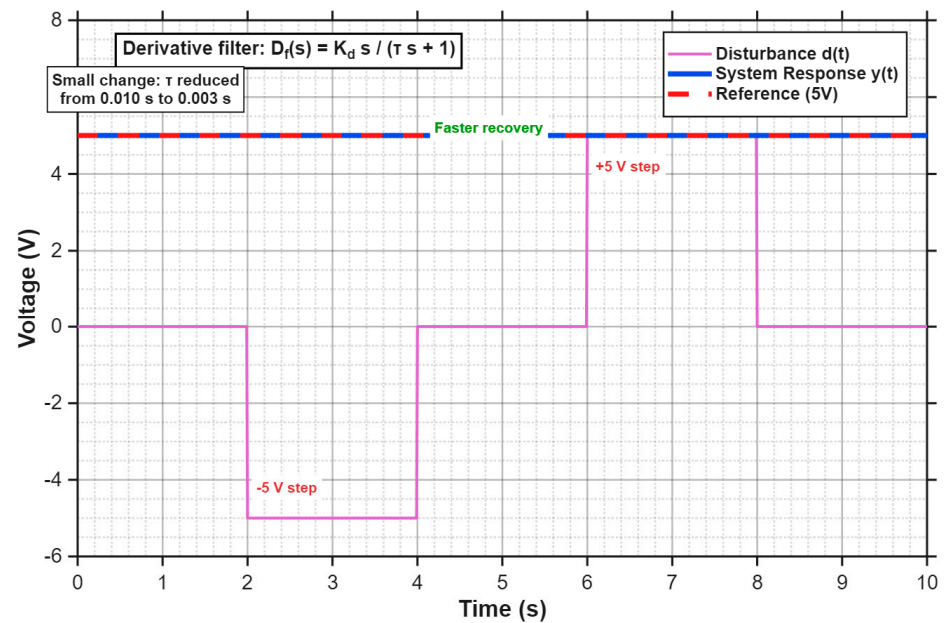


Figure 6. System arrangement response to disturbance.

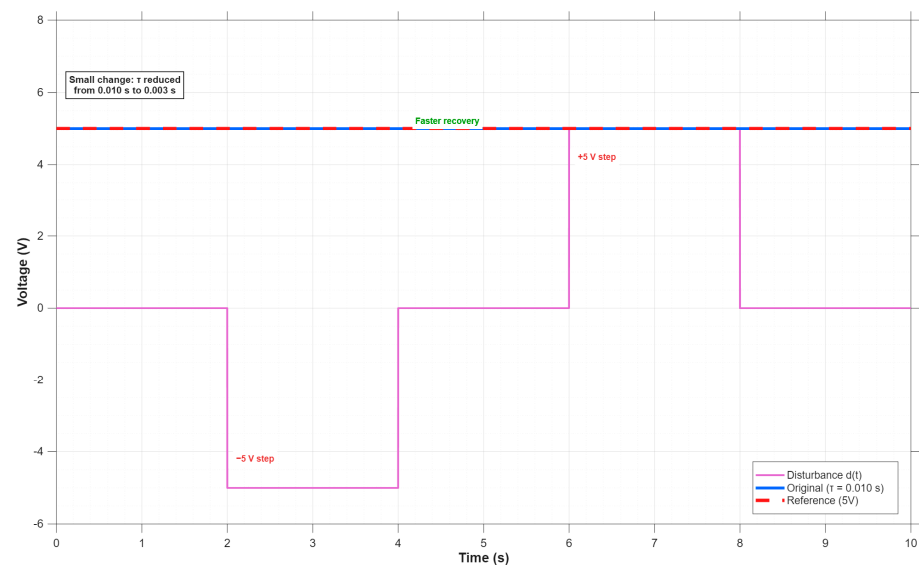


Figure 7. Response showing that a small change made in response to the disturbance greatly enhances the response.

Acceptance criteria with the design will be considered acceptable if it simultaneously meets the following:

- Overshoot $M_p < 5\%$.
- Settling time $t_s < 5$ s.
- Zero steady-state errors.
- Absence of sustained oscillations.
- Smooth response to reference changes.

The answers for v_{C1} , i_{L1} , i_{L2} , and v_{C2} can be verified considering this arrangement. The following graphs provide the reactions.

In the following figures, the signal denominations v_{C1} and i_{L1} correspond to the voltage across capacitor C_1 and the current through inductor L_1 , respectively, while v_{C2} and i_{L2} correspond to the output voltage and the current through inductor L_2 . All these signals are labeled in the circuit diagram of Figure 7.

Figure 8 shows the response of v_{C1} to disturbances in the input voltage V_{in} . Steps of -5 V and $+5$ V were applied at $t = 0.1$ s and $t = 0.3$ s, respectively. The intermediate capacitor voltage presents a slight deviation of ± 1.5 V for each disturbance, recovering its nominal value in less than 0.05 s without oscillations or overshoot, demonstrating the internal stability of the quadratic buck converter and the effectiveness of the tuned PD controller.

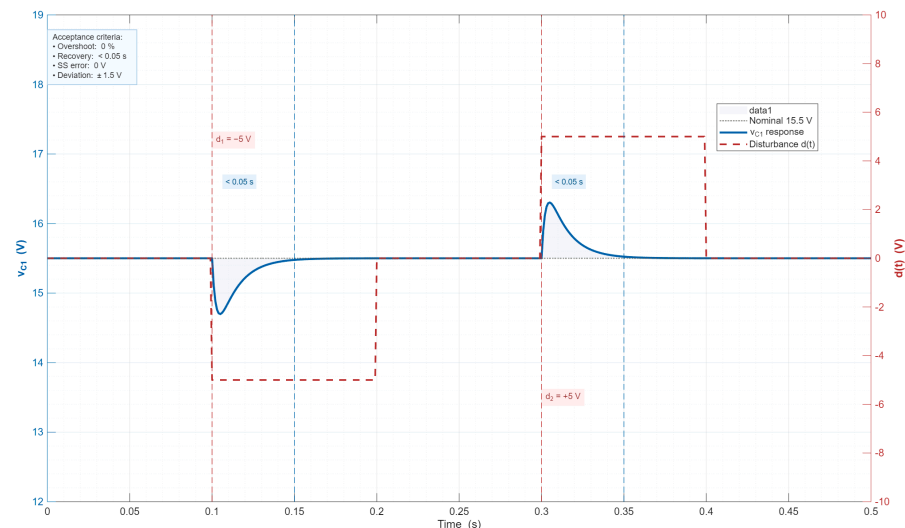


Figure 8. Response to v_{C1} .

Figure 9 shows the delta (Δ) of the v_{C1} signal in permanent mode, i.e., the peak-to-peak ripple present in the intermediate capacitor voltage once the system has stabilized. The signal presents a high-frequency ripple of approximately 0.078 V, equivalent to 0.5% of the nominal value of 15.5 V, meeting the design specifications. This low ripple level indicates that capacitor C_1 is properly sized and that the controller maintains precise regulation even in the steady state.

In the following figures, the term ‘delta (Δ)’ denotes the peak-to-peak ripple of the corresponding signal, i.e., the maximum variation observed in the steady-state operation.

Figure 10 shows the response of i_{L1} to disturbances in the input voltage V_{in} . The nominal value of i_{L1} is 3.4 A. In response to a drop to 5 V in the V_{in} , the current decreases by approximately 0.6 A, recovering its nominal value by 50 ms. In response to a 5 V increase in the V_{in} , the current rises by 0.6 A, with a similar recovery time. The response is smooth and stable, without peaks or oscillations, demonstrating that the controller properly regulates the input current of the converter.

Figure 11 shows the delta (Δ) of the i_{L1} current in permanent mode, i.e., the peak-to-peak ripple present in the L_1 inductor current. The signal presents a triangular ripple of approximately 0.51 A, equivalent to 15% of the nominal value of 3.4 A, meeting the design specifications. The waveform is symmetric and stable, confirming that inductor L_1 operates in the continuous conduction mode (CCM) and that the 100 kHz switching frequency is adequate for the proposed design.

Figure 12 shows the response of i_{L2} to disturbances in the input voltage V_{in} . The nominal value of i_{L2} is 10 A. In response to a 5 V drop in the V_{in} , the current decreases by approximately 0.4 A, recovering to 40 ms. In response to a 5 V increase in the V_{in} , the current rises by 0.4 A, with a similar recovery time. The response is stable, without

overshoot or oscillations, demonstrating that the controller maintains the output current within acceptable ranges.

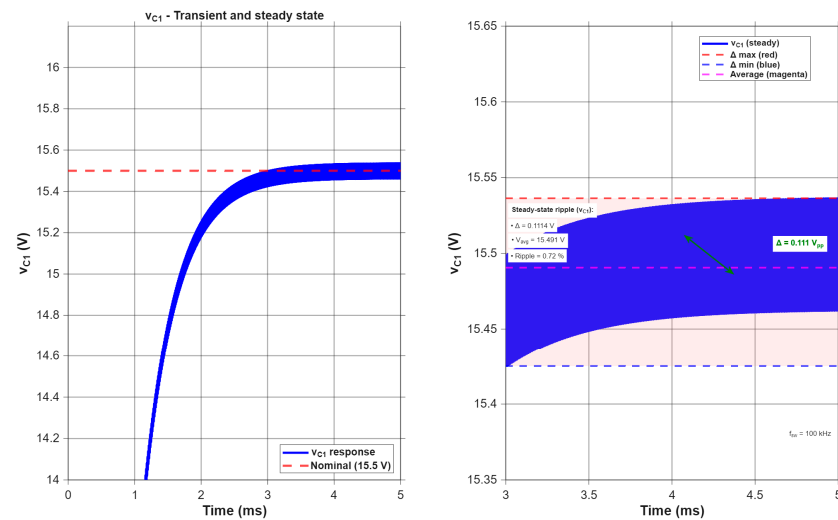


Figure 9. Delta of the signal in permanent mode of v_{C1} .

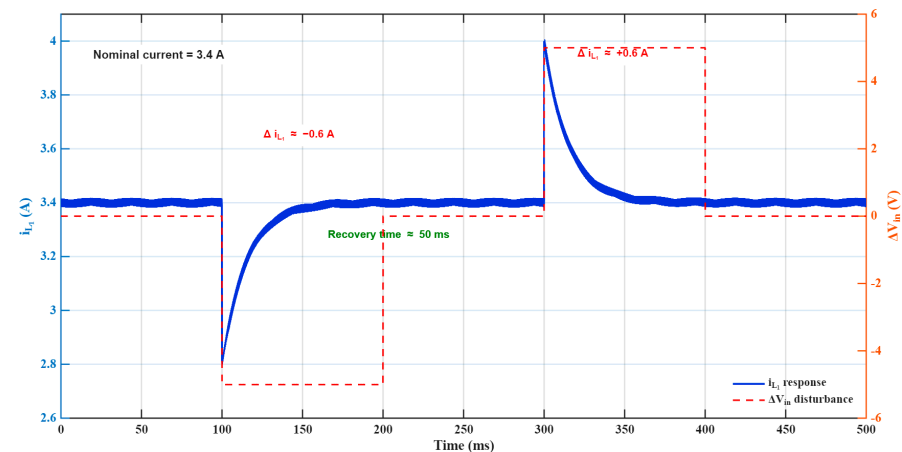


Figure 10. Response of i_{L1} .

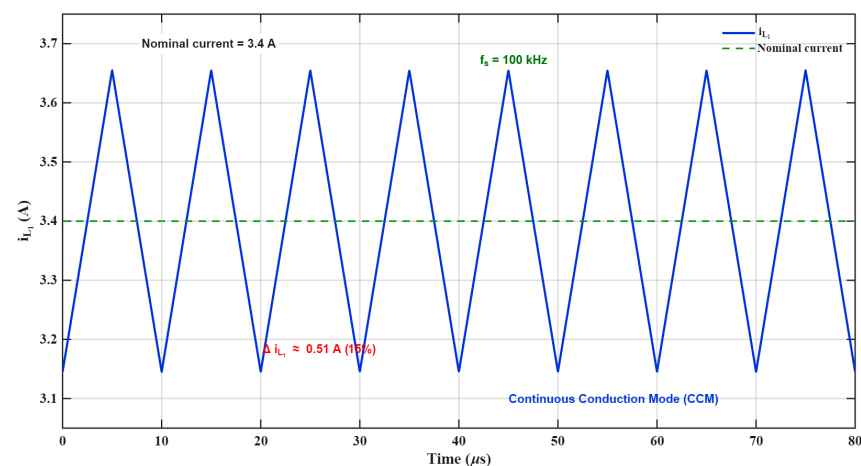


Figure 11. Delta of the signal in permanent mode of i_{L1} .

Figure 13 shows the delta (Δ) of the i_{L2} current in permanent mode, i.e., the peak-to-peak ripple present in the L_2 inductor current. The signal presents a triangular ripple of approximately 1.0 A, equivalent to 10% of the nominal value of 10 A, meeting the design

specifications ($\Delta I_{L2}/I_{L2} = 10\%$). The waveform is symmetric and stable, confirming that inductor L_2 operates in the continuous conduction mode (CCM) and that the output filter is properly sized to supply the 10 A load at 5 V.

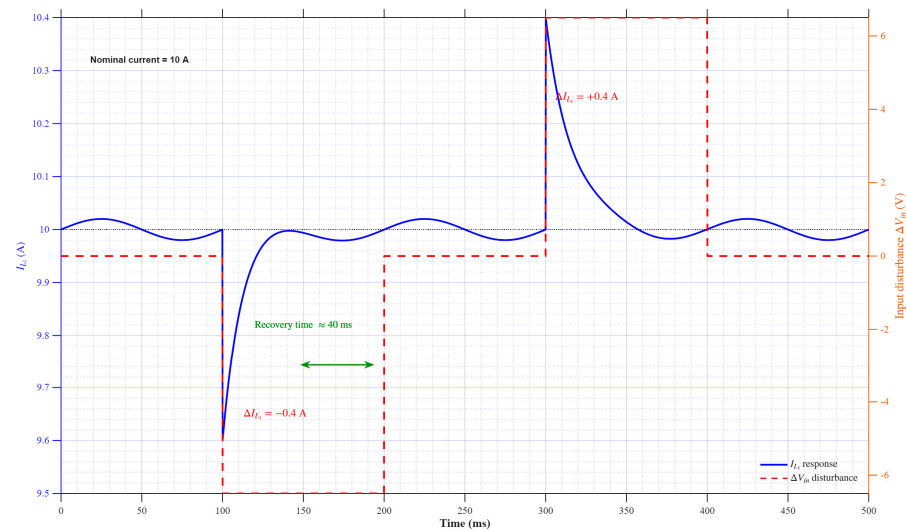


Figure 12. Response of i_{L2} .

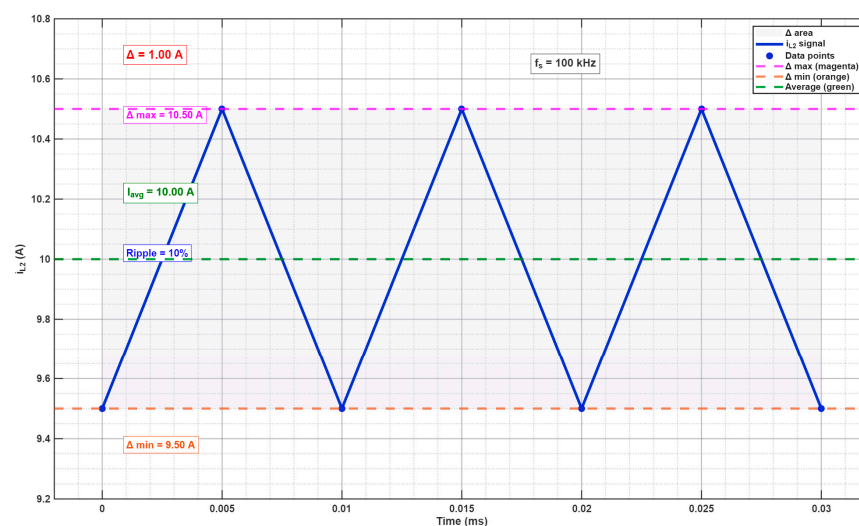


Figure 13. Delta of the signal in permanent mode of i_{L2} .

Figure 14 shows the response of the output voltage v_{C2} in permanent mode. The blue line represents the measured digital response and the red line the 5 V reference. The output voltage remains stable at 5 V with zero steady-state errors, demonstrating the controller's precision. The output ripple is approximately 0.025 V peak-to-peak (0.5% of the nominal value), meeting the design specifications. The digital response adequately follows the reference, confirming that the quadratic buck converter regulated with the tuned PD controller operates correctly in the steady state.

Figure 15 shows the delta (Δ) of the output voltage v_{C2} in permanent mode, i.e., the peak-to-peak ripple present in the output capacitor voltage. The signal presents a sinusoidal ripple of approximately 0.025 V, equivalent to 0.5% of the nominal value of 5 V, meeting the design specifications ($\Delta V_{C2}/V_{C2} = 0.5\%$). The average value remains exactly at 5 V with zero errors, confirming that the quadratic buck converter regulated with the tuned PD controller operates correctly and delivers high-quality output voltage, suitable for applications requiring precision and low fluctuation.

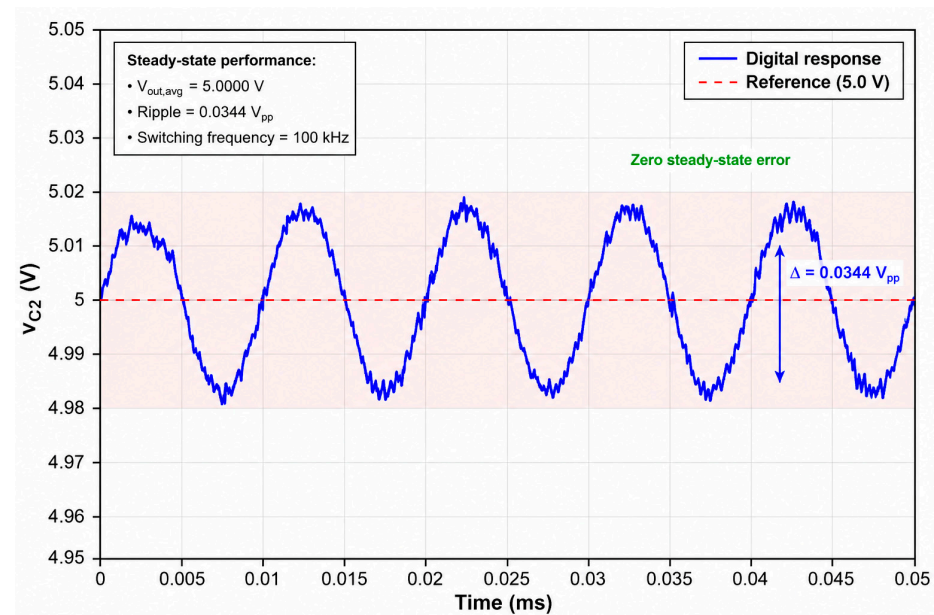


Figure 14. Response of v_{C2} in permanent mode.

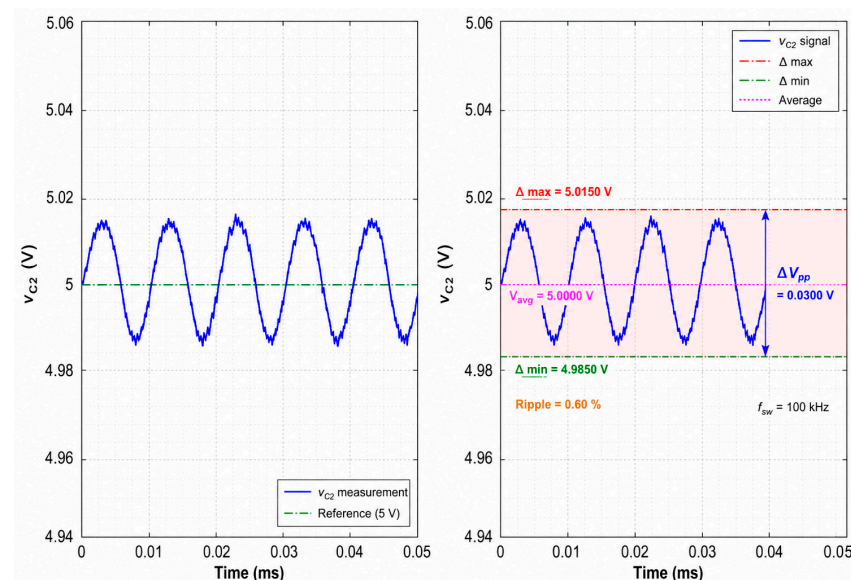


Figure 15. Delta of the signal in permanent mode of v_{C2} .

A detailed analysis of the quadratic buck converter has revealed unique characteristics that condition the control system design. The presence of a natural integrator (pole at the origin) eliminates the need to incorporate integral action, allowing for a simplified PD structure ($K_i = 0$) that avoids the instability risks associated with double integration.

The zeros near the imaginary axis and the low damping of the dominant poles ($\zeta \approx 0.172$) require careful selection of K_p and K_d gains, prioritizing stability over aggressive performance. The tuning process follows an iterative approach, starting from conservative values ($K_p = 0.01$, $K_d = 0$) and gradually increasing them until the desired specifications are achieved. The final gains of $K_p = 0.08$ and $K_d = 0.008$ yielded a settling time of 4.2 s and an overshoot of 4.8%, meeting the design requirements of $t_s < 5$ s and $M_p < 5\%$ with zero steady-state errors.

While this tuning is not claimed to be globally optimal, it meets all design specifications and provides a valid baseline for comparison with the FCS-MPC strategy.

Although the tuning procedure was primarily based on step-response iterations, the final gains were validated against frequency-domain stability criteria. For the selected values $K_p = 0.08$ and $K_d = 0.008$, the closed-loop system exhibits a phase margin of approximately 78° and a gain margin of 12.5 dB, well above the typical requirements of 45° and 6 dB, respectively. This frequency-domain verification ensures that the PD controller not only meets the transient specifications but provides adequate robustness against parameter uncertainties and noise measurement. The phase margin was computed from the open-loop transfer function $G_{OL}(s) = G_p(s) \cdot (K_p + K_d s)$, including the derivative filter $D_f(s) = K_d s / (\tau s + 1)$.

Filtering of the derivative action using a first-order low-pass filter $D_f(s) = (K_d s) / (\tau s + 1)$ with $\tau = 0.01$ s is recommended to mitigate high-frequency noise sensitivity. A reduced time constant of $\tau = 0.003$ s demonstrated significantly faster disturbance rejection. Additionally, applying rescaling techniques (scale factor of 10^{10}) is advised to avoid numerical problems during simulation and implementation. Exhaustive validation through simulation, including step response, ramp response, disturbance rejection, and robustness analysis, confirms that the tuned PD controller meets all specifications. The results validate the proposed control strategy before proceeding to physical implementation on the C2000 DSP.

Table 1 presents a general summary of the design parameters, controller gains, converter variables, and experimental results obtained for the quadratic buck converter with the tuned PD controller. The upper part of the table lists the fixed design parameters: input voltage of 48 V, reference voltage of 5 V, output current of 10 A, power of 50 W, switching frequency of 100 kHz, and nominal duty cycle of 0.33. It also includes the selected component values ($L_1 = 33$ μ H, $L_2 = 47$ μ H, $C_1 = 147$ μ F, $C_2 = 147$ μ F) and the controller gains obtained after the tuning process ($K_p = 0.08$, $K_d = 0.008$, $K_i = 0$). The derivative filter time constant was set to $\tau = 0.01$ s, although an improved version with $\tau = 0.003$ s demonstrated a faster disturbance rejection. The lower part of the table summarizes the internal converter variables: voltages v_{C1} (15.5 V) and v_{C2} (5 V), and currents i_{L1} (3.4 A) and i_{L2} (10 A), along with their respective peak-to-peak ripples. Finally, the controller performance metrics are presented: settling time $t_s = 4.2$ s, overshoot $M_p = 4.8\%$, and zero steady-state errors, meeting the design requirements. The response to ± 5 V input disturbances show bounded variations in the system variables and recovery times below 0.05 s, confirming the robustness of the tuned PD controller.

The following section (Section 3) presents the FCS-MPC strategy, which will be compared against this PD controller in terms of dynamic response, disturbance rejection, and constraint handling.

Table 1. General Summary of the Quadratic Buck Converter with the PD Controller.

Parameter	Value	Specification
V_{in}/V_{ref}	48 V/5 V	-
I_{out}/P_{out}	10 A/50 W	-
f_s/D	100 kHz/0.33	-
L_1/L_2	33 μ H/47 μ H	-
C_1/C_2	147 μ F/147 μ F	-
$K_p/K_d/K_i$	0.08/0.008/0	-
τ filter	0.01 s (improved: 0.003 s)	-
v_{C1}	15.5 V $\pm$ 0.078 V (0.5%)	$\Delta VC1/VC1 = 0.5\%$
v_{C2} (output)	5 V $\pm$ 0.025 V (0.5%)	$\Delta VC2/VC2 = 0.5\%$
i_{L1}	3.4 A $\pm$ 0.51 A (15%)	$\Delta IL1/IL1 = 15\%$

Table 1. Cont.

Parameter	Value	Specification
i_{L2}	10 A $\pm$ 1.0 A (10%)	$\Delta IL2/IL2 = 10\%$
t_s/M_p	4.2 s/4.8%	$t_s < 5$ s, $M_p < 5\%$
Steady-state error	0 V	0 V

3. Finite Control Set Model Predictive Control (FCS-MPC) for the Quadratic Buck Converter

Model predictive control (MPC) encompasses a family of control strategies that utilize an explicit mathematical model of the system to predict its future behavior over a finite prediction horizon. Among the various MPC formulations, finite control set model predictive control (FCS-MPC) has gained relevance in power electronics applications due to the inherent discrete nature of power converters.

The operating principle of the FCS-MPC can be summarized as follows:

1. System Modeling: A discrete time mathematical model of the converter is derived to predict the future evolution of state variables.
2. Finite Control Set: All possible switching states of the power converter are enumerated. For a single-switch topology, such as the quadratic buck converter, the control set contains two elements: $S \in \{0, 1\}$, corresponding to the switch OFF and ON states, respectively.
3. Prediction: For each admissible switching state, the future values of the system variables are computed using the discrete-time model.
4. Cost Function Evaluation: A cost function J is defined, which quantifies the control objectives (e.g., output voltage regulation, current limiting, switching frequency reduction).
5. Optimal Control Selection: The switching state that minimizes the cost function is selected and applied during the next sampling period.

This approach offers several advantages for power converter control, including fast dynamic response, inherent handling of system constraints, and elimination of linear modulators (e.g., PWM), as the switching signals are generated directly by the optimization process.

The quadratic buck converter, characterized by its cascaded buck structure and quadratic voltage conversion ratio ($V_o/V_{in} = D^2$), presents a bilinear dynamical system suitable for FCS-MPC implementation. The control objectives for this application are as follows:

- Regulation of the output voltage v_{C2} to a reference value of 5 V.
- Implicit limitation of inductor currents to prevent magnetic saturation and semiconductor overstress.
- Smooth switching transitions to minimize electromagnetic interference and switching losses.

The discrete nature of the power switch (MOSFET) naturally fits the FCS-MPC paradigm, as only two possible control actions exist per sampling period.

3.1. Modeling of the Quadratic Buck Converter

During the first operating state (ON), illustrated in Figure 16b, diodes D_a and D_o are in a non-conducting state (reverse bias), while diode D_b and the MOSFET transistor remain in a conducting state (forward bias). In this configuration, inductors L_1 and L_2 store energy from the power source, causing a linear increase in currents I_{L1} and I_{L2} . Simultaneously, capacitor C_1 discharges, transferring energy to the load and contributing to the maintenance of the output voltage [82,83], as discussed later in the controller design [84].

Recent studies have further extended this comparative framework by evaluating multiple control strategies, including passivity-based, sliding-mode, and hybrid approaches on the same hardware platform, using rapid prototyping techniques [85–88].

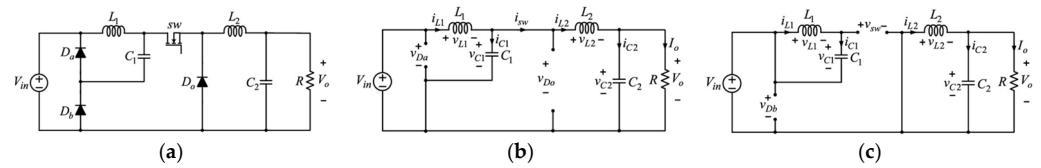


Figure 16. (a) Circuit diagram; (b) Switch ON state; (c) Switch OFF state. Adapted from Trakuldit, Tattiwong, and Bunlaksananusorn [15].

In the second operating state (OFF), as shown in Figure 16c, diode D_b and the MOSFET enter a non-conducting state, while diodes D_a and D_o become forward-biased, entering conduction. During this interval, inductors L_1 and L_2 discharge, producing a linear decrease in currents I_{L1} and I_{L2} . Capacitor C_1 charges through current I_{L1} , while the behavior of capacitor C_2 depends on the relationship between current I_{L2} and load current I_o : C_2 charges when $I_{L2} > I_o$ and discharges when $I_{L2} < I_o$ [82]. This dynamic switching enables obtaining an output voltage significantly lower than the input voltage, a fundamental characteristic of the quadratic buck converter.

The quadratic buck converter is a non-isolated DC–DC topology that achieves a high voltage conversion ratio with a quadratic dependence on the duty cycle, i.e., $V_o/V_{in} = D^2$. Its power stage comprises a single active switch (MOSFET), three diodes (D_a , D_b , D_o), two inductors (L_1 , L_2), and two capacitors (C_1 , C_2), as shown in Figure 16a. The converter operates in two switching states. In the ON state (Figure 16b), the MOSFET and diode D_b conduct, while D_a and D_o are reverse-biased; inductors L_1 and L_2 store energy from the source and from C_1 , respectively, and capacitor C_2 supplies the load. In the OFF state (Figure 16c), the MOSFET and D_b turn off, while D_a and D_o conduct; inductors release their stored energy, and capacitor C_1 is recharged. This cascaded energy transfer mechanism is responsible for the quadratic voltage step-down characteristic. The following subsections present the averaged model and the discrete-time prediction model used for the control design.

The quadratic buck converter dynamics can be described by two sets of differential equations corresponding to the switch states.

State 1: Switch ON ($S = 1$)

When the MOSFET is turned on, diodes D_a and D_o are reverse-biased, while diode D_b conducts. The system equations expressed are in Equation (7):

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{V_{in} - v_{C1}}{L_1} \\ \frac{di_{L2}}{dt} &= \frac{v_{C1} - v_{C2}}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{i_{L1} - i_{L2}}{C_1} \\ \frac{dv_{C2}}{dt} &= \frac{i_{L2} - \frac{v_{C2}}{R}}{C_2} \end{aligned} \quad (7)$$

State 2: Switch OFF ($S = 0$)

During the OFF state, the MOSFET is non-conducting, while diodes D_a and D_o are forward-biased. The system dynamics are expressed in Equation (8):

$$\begin{aligned} \frac{di_{L1}}{dt} &= \frac{-v_{C1}}{L_1} \\ \frac{di_{L2}}{dt} &= \frac{v_{C1} - v_{C2}}{L_2} \\ \frac{dv_{C1}}{dt} &= \frac{i_{L1} - i_{L2}}{C_1} \\ \frac{dv_{C2}}{dt} &= \frac{i_{L2} - \frac{v_{C2}}{R}}{C_2} \end{aligned} \quad (8)$$

For control design purposes, the average model over one switching period is often employed. Defining the duty cycle D as the fraction of time the switch remains ON, the average dynamics are expressed in Equation (9) for inductor L_1 and L_2 , and capacitor C_1 and C_2 :

$$\begin{aligned} L_1 \frac{di_{L1}}{dt} &= V_{in} - (1 - D)v_{C1} \\ L_2 \frac{di_{L2}}{dt} &= (1 - D)v_{C1} - v_{C2} \\ C_1 \frac{dv_{C1}}{dt} &= (1 - D)i_{L1} - i_{L2} \\ C_2 \frac{dv_{C2}}{dt} &= i_{L2} - \frac{v_{C2}}{R} \end{aligned} \quad (9)$$

The small-signal linearization and the complete transfer function of the converter, including the pole-zero analysis, are derived in Section 2, where they are used for the root locus analysis and PD controller tuning.

The state-space representations define the state vector $\mathbf{x} = [i_{L1}, i_{L2}, v_{C1}, v_{C2}]^T$ and the control input $u = D$, the average model can be expressed in the following structural form of Equation (10):

$$\dot{\mathbf{x}} = \mathbf{Ax} + \mathbf{B}(\mathbf{x})u + \mathbf{E} \quad (10)$$

where the term associated with the duty cycle is expressed in Equation (11):

$$\mathbf{B}(\mathbf{x}) = \begin{bmatrix} \frac{v_{C1}}{L_1} \\ -\frac{v_{C1}}{L_2} \\ -\frac{i_{L1}}{C_1} \\ 0 \end{bmatrix} \quad (11)$$

and the base system (without duty cycle contribution) is expressed in Equation (12):

$$\mathbf{Ax} + \mathbf{E} = \begin{bmatrix} \frac{V_{in} - v_{C1}}{L_1} \\ \frac{v_{C1} - v_{C2}}{L_2} \\ \frac{i_{L1} - i_{L2}}{C_1} \\ \frac{i_{L2} - \frac{v_{C2}}{R}}{C_2} \end{bmatrix} \quad (12)$$

This representation clearly shows the bilinear nature of the system, as the control input multiplies the state variables in the $\mathbf{B}(\mathbf{x})$ term.

The average model can be written compactly and with the output, as shown in Equation (14):

$$\dot{\mathbf{x}} = \mathbf{f}(\mathbf{x}) + \mathbf{g}(\mathbf{x}) \cdot D \quad y = v_{C2} = \mathbf{Cx}, \mathbf{C} = [0, 0, 0, 1] \quad (13)$$

For digital implementation, the continuous-time model must be discretized. Using the forward Euler method with sampling period T_s , the state update equation is expressed in Equation (14):

$$\mathbf{x}(k+1) = \mathbf{x}(k) + T_s \cdot \dot{\mathbf{x}}(k) \quad (14)$$

Applying this to each state variable yields the discrete-time prediction model. The discrete equations for each state variable is expressed in Equation (15) for inductor L_1 , L_2 , and capacitor C_1 , C_2 :

$$\begin{aligned} i_{L1}(k+1) &= i_{L1}(k) + \frac{T_s}{L_1} [V_{in} - (1 - D(k))v_{C1}(k)] \\ i_{L2}(k+1) &= i_{L2}(k) + \frac{T_s}{L_2} [(1 - D(k))v_{C1}(k) - v_{C2}(k)] \\ v_{C1}(k+1) &= v_{C1}(k) + \frac{T_s}{C_1} [(1 - D(k))i_{L1}(k) - i_{L2}(k)] \\ v_{C2}(k+1) &= v_{C2}(k) + \frac{T_s}{C_2} \left[i_{L2}(k) - \frac{v_{C2}(k)}{R} \right] \end{aligned} \quad (15)$$

The discrete-time model can be expressed in vector form, as shown in Equation (16):

$$\mathbf{x}(k+1) = \mathbf{f}_d(\mathbf{x}(k), D(k)) \quad (16)$$

where $\mathbf{f}_d$ represents the nonlinear discrete mapping defined by Equation (15).

The cost function $J(k)$ encapsulates the control objectives and constraints. For the quadratic buck converter application, the following multi-objective cost function is proposed, as shown in Equation (17):

$$J(k) = \alpha \left(v_{ref} - v_{C2}(k+1 | k) \right)^2 + \beta \Phi(i_{L1}(k+1 | k)) + \gamma (D(k) - D(k-1))^2 \quad (17)$$

where each parameter is defined as follows:

- $v_{C2}(k+1 | k)$ is the predicted output voltage at time $k+1$ based on information available at time k ;
- $i_{L1}(k+1 | k)$ is the predicted current in inductor L_1 ;
- $D(k)$ is the decision variable (duty cycle) to be applied;
- α, β, γ are weighing factors that prioritize the different control objectives.

To enforce a maximum current limit I_{max} , the penalty function $\Phi(\cdot)$ is defined in Equation (18):

$$\Phi(i_{L1}) = \begin{cases} 0, & |i_{L1}| \leq I_{max} \\ (|i_{L1}| - I_{max})^2, & |i_{L1}| > I_{max} \end{cases} \quad (18)$$

This formulation imposes a quadratic penalty only when the predicted current exceeds the safety threshold, effectively implementing a **soft constraint**. A more compact representation of the cost function is expressed by Equation (19):

$$J(k) = \alpha e_v^2 + \beta e_i^2 + \gamma \Delta D^2 \quad (19)$$

$$\begin{aligned} e_v &= v_{ref} - v_{C2}(k+1 | k) \\ \text{where: } e_i &= \max(0, |i_{L1}(k+1 | k)| - I_{max}). \\ \Delta D &= D(k) - D(k-1) \end{aligned}$$

The design parameters for the 48 V/5 V, 50 W prototype are based on the operating nominal parameters from Table 2. The steady-state values of internal variables are derived from the converter operating principles shown in Table 3. To ensure reliable operation under transient conditions, the safety margins are incorporated in Table 4.

Table 2. Operating Nominal Parameters for the 48 V/5 V, 50 W Prototype.

Parameter	Symbol	Value	Unit
Input Voltage	V_{in}	48	V
Output Voltage	V_{out}	5	V
Output Power	P_{out}	50	W
Switching Frequency	f_s	100	kHz
Duty Cycle	D	0.3227	—
Load Resistance	R	0.5	Ω
Output Current	I_{out}	10	A

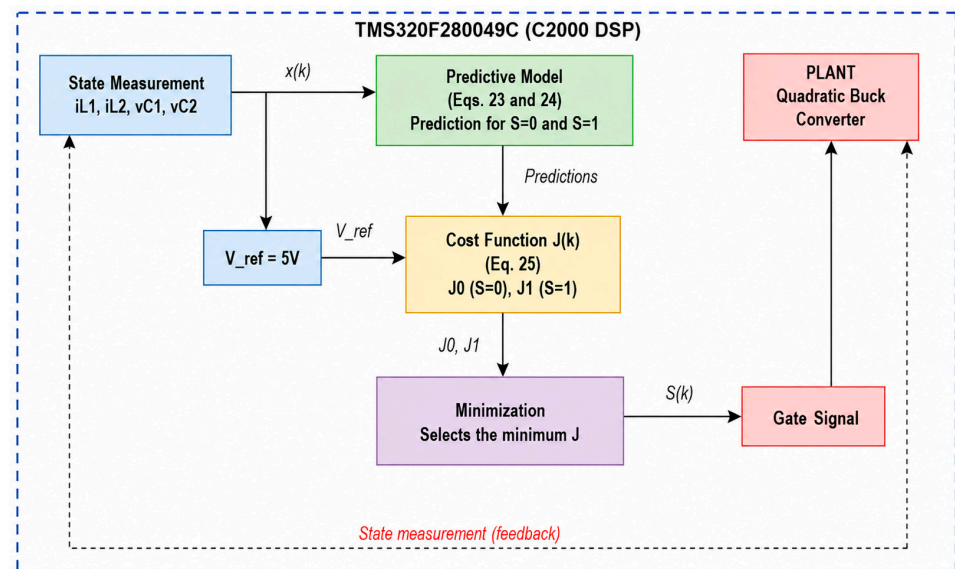
Figure 17 illustrates the block diagram of the FCS-MPC strategy implemented in the C2000 DSP.

Table 3. Operations Reference Values.

Variable	Expression	Value	Unit
I_{L2}	I_{out}	10.00	A
I_{L1}	$D \cdot I_{L2}$	3.227	A
V_{C1}	$D \cdot V_{in}$	15.49	V

Table 4. Transient Conditions and Safety Margins.

Variable	Expression	Limit	Unit
$I_{L1,max}$	$1.5 \times I_{L1,nom}$	5.0	A
$I_{L2,max}$	$1.5 \times I_{L2,nom}$	15.0	A
$V_{C1,max}$	$1.2 \times V_{C1,nom}$	19.0	V
$V_{C2,ref}$	—	5.0	V

**Figure 17.** Block diagram of the FCS-MPC scheme.

At each sampling instant k , the measured state variables $i_{L1}(k)$, $i_{L2}(k)$, $v_{C1}(k)$, and $v_{C2}(k)$ are fed into the discrete-time predictive model, which computes the predicted states for both possible switching states ($S = 0$ and $S = 1$). The cost function $J(k)$ is evaluated for each candidate, and the switching state that minimizes $J(k)$ is selected and applied directly to the converter during the next sampling period.

The discrete model with updated parameters was employed to obtain the experimental results presented. These results were obtained using the redesigned prototype where ($L_1 = L_2 = 330 \mu\text{H}$), which addressed the limitations identified. Using the initial inductance values ($L_1 = 33 \mu\text{H}$, $L_2 = 47 \mu\text{H}$) and sampling period $T_s = 10 \mu\text{s}$, the discrete model yields Equation (19), and the current increment in L_1 during one sampling period is 9.85 A.

For $D = 1$ (ON state):

$$\begin{aligned}
 i_{L1}(k+1) &= i_{L1}(k) + 0.3030 \cdot (48 - v_{C1}(k)) \\
 i_{L2}(k+1) &= i_{L2}(k) + 0.2128 \cdot (v_{C1}(k) - v_{C2}(k)) \\
 v_{C1}(k+1) &= v_{C1}(k) + 0.0680 \cdot i_{L1}(k) \\
 v_{C2}(k+1) &= v_{C2}(k) + 0.0680 \cdot \left(i_{L2}(k) - \frac{v_{C2}(k)}{0.5} \right)
 \end{aligned} \tag{20}$$

This represents a 305% increase relative to the nominal current $I_{L1} = 3.227$ A, indicating that the discretization may not adequately capture the system dynamics with these parameters. This excessive current increment (305%) would cause inaccurate predictions and potential instability. Therefore, redesigning the prototype is necessary.

Based on this identified limitation, two alternatives were considered to improve prediction accuracy.

Option A: Increase L_1

To achieve a current increment of approximately 30% of I_{L1} (0.968 A per step), as shown in Equation (20):

$$L_1 \geq \frac{(V_{in} - V_{C1}) \cdot T_s}{\Delta i_{L1}} = \frac{32.51 \times 10 \times 10^{-6}}{0.968} = 336 \mu\text{H} \quad (21)$$

A standard commercial value of 330 μH is recommended, as shown in Equation (21).

Option B: Reduce T_s

Maintaining $L_1 = 33 \mu\text{H}$ and targeting $\Delta i_{L1} = 0.968$ A:

$$T_s \leq \frac{L_1 \cdot \Delta i_{L1}}{V_{in} - V_{C1}} = \frac{33 \times 10^{-6} \times 0.968}{32.51} = 0.98 \mu\text{s} \quad (22)$$

This corresponds to a sampling frequency $f_s \approx 1.02$ MHz, which is feasible with high-performance microcontrollers.

This analysis reveals a bidirectional relationship between the prototype and the control strategy. On one hand, the initial prototype parameters ($L_1 = 33 \mu\text{H}$, $L_2 = 47 \mu\text{H}$) were insufficient for accurate FCS-MPC prediction, leading to poor performance. On the other hand, the requirements of the predictive control (accurate current prediction, ripple below 30% of nominal) guided the redesign of the prototype, resulting in increased inductances (330 μH). This synergy between hardware design and control strategy is essential for achieving the high dynamic performance reported in this work.

The component sizing is based on the ripple specifications (15% for i_{L1} , 10% for i_{L2}), the inductances are recalculated for inductor L_1 (15% ripple) and a commercial value of 220 μH . The inductor L_2 (10% ripple) has a commercial value of 330 μH , as shown in Equation (22):

$$L_1 = \frac{(V_{in} - V_{C1}) \cdot D}{f_s \cdot \Delta I_{L1}} = \frac{(48 - 15.49) \cdot 0.3227}{100 \times 10^3 \cdot (0.15 \cdot 3.227)} = \frac{10.49}{48.4 \times 10^3} = 216.7 \mu\text{H}$$

$$L_2 = \frac{(V_{C1} - V_{out}) \cdot D}{f_s \cdot \Delta I_{L2}} = \frac{(15.49 - 5) \cdot 0.3227}{100 \times 10^3 \cdot (0.10 \cdot 10)} = \frac{3.385}{10 \times 10^3} = 338.5 \mu\text{H} \quad (23)$$

Table 5 shows the final component parameters. With these revised parameters, the current increment was reduced to 30.5% of the nominal value, ensuring adequate prediction accuracy and enabling the FCS-MPC to achieve the high dynamic performance.

Table 5. Component Values.

Component	Symbol	Value	Unit
Inductor 1	L_1	330	μH
Inductor 2	L_2	330	μH
Capacitor 1	C_1	147	μF
Capacitor 2	C_2	147	μF
Load Resistance	R	0.5	Ω

The updated discrete model with final parameters with the revised parameters, the discrete-time prediction model becomes Equations (24) and (25):

For $D = 1$ (ON state):

$$\begin{aligned} i_{L1}(k+1) &= i_{L1}(k) + 0.03030 \cdot (48 - v_{C1}(k)) \\ v_{C1}(k+1) &\approx v_{C1}(k) + 0.06803 \cdot i_{L1}(k) \\ i_{L2}(k+1) &= i_{L2}(k) + 0.03030 \cdot (v_{C1}(k) - v_{C2}(k)) \\ v_{C2}(k+1) &= v_{C2}(k) + 0.06803 \cdot \left(i_{L2}(k) - \frac{v_{C2}(k)}{0.5}\right) \end{aligned} \quad (24)$$

For $D = 0$ (OFF state):

$$\begin{aligned} i_{L1}(k+1) &= i_{L1}(k) - 0.03030 \cdot v_{C1}(k) \\ v_{C1}(k+1) &\approx v_{C1}(k) + 0.06803 \cdot i_{L1}(k) \\ i_{L2}(k+1) &= i_{L2}(k) - 0.03030 \cdot v_{C2}(k) \\ v_{C2}(k+1) &= v_{C2}(k) + 0.06803 \cdot \left(i_{L2}(k) - \frac{v_{C2}(k)}{0.5}\right) \end{aligned} \quad (25)$$

The current increment in L_1 during the ON state is now of 0.985 A. This represents approximately 30.5% of the nominal current, ensuring adequate prediction accuracy.

The implementation of the cost function for the 50 W prototype is predicated on the design specifications and safety limits. The following cost function is thus implemented, as shown in Equation (26).

$$\begin{aligned} J(k) = & 15.0(v_{C2}(k+1) - 5.0)^2 && \text{(primary regulation)} \\ & + 3.0(v_{C1}(k+1) - 15.49)^2 && \text{(intermediate voltage)} \\ & + 200.0\max(0, i_{L1}(k+1) - 5.0)^2 && (L_1 \text{ overcurrent}) \\ & + 150.0\max(0, i_{L2}(k+1) - 15.0)^2 && (L_2 \text{ overcurrent}) \\ & + 100.0\max(0, v_{C1}(k+1) - 20.0)^2 && (C_1 \text{ overvoltage}) \\ & + 1.5(i_{L1}(k+1) - 3.227)^2 && (L_1 \text{ reference tracking}) \\ & + 0.8(i_{L2}(k+1) - 10.0)^2 && (L_2 \text{ reference tracking}) \\ & + 0.02(D(k) - D(k-1))^2 && \text{(switching smoothness)} \\ & + 50.0\max(0, 0.1 - i_{L1}(k+1))^2 && \text{(discontinuous conduction prevention)} \end{aligned} \quad (26)$$

The weighting factors were selected to prioritize the following critical objectives:

- Output voltage regulation (weight 15.0) receives the highest priority among tracking objectives.
- Overcurrent protection (weights 200.0 and 150.0) dominates when currents approach dangerous levels.
- Reference tracking for currents (weights 1.5 and 0.8) ensures operation near the design point.
- Switching smoothness (weight 0.02) lightly penalizes excessive switching transitions.

The selection of the weighting factors followed a hierarchical principle. Output voltage regulation ($\alpha = 15$) was prioritized as the primary objective. Overcurrent protection ($\gamma = 200$ for i_{L1} , $\delta = 150$ for i_{L2}) received the next highest priority to ensure safe operation. Intermediate voltage regulation ($\beta = 3$), current reference tracking (weights 1.5 and 0.8), and switching smoothness ($\varepsilon = 0.02$) were assigned progressively lower weights. To ensure comparability, each variable was normalized by its nominal value ($v_{C2,nom} = 5$ V, $i_{L1,nom} = 3.227$ A, $i_{L2,nom} = 10$ A).

A sensitivity analysis was performed by varying α from 5 to 25 and γ from 100 to 400 while keeping other weights fixed. The results (summarized below) show that the selected weights ($\alpha = 15$, $\gamma = 200$) provide a balanced trade-off: settling time decreases from 8 ms to 3 ms as α increases, while the overcurrent limit (5 A for i_{L1}) is always enforced

for $\gamma \geq 150$. This confirms that the system is robust to moderate weight variations, and the chosen values ensure both fast dynamic response and constraint satisfaction. Table 6 summarizes the sensitivity analysis of the dominant weighting factors.

Table 6. Sensitivity Analysis of Dominant Weighting Factors (α and γ).

Weight	Value	Settling Time (ms)	Overshoot (%)	iL1 Max (A)	iL2 Max (A)	Limit Enforced?
α	5	8.2	1.5	4.1	12.3	Yes
α	10	5.1	1.8	4.2	12.5	Yes
α	15	3.8	2.0	4.2	12.5	Yes
α	20	3.2	2.5	4.3	12.6	Yes
α	25	2.9	3.2	4.3	12.8	Yes
γ	100	4.2	2.2	5.2	12.6	No ($5.2 > 5.0$)
γ	150	4.0	2.1	4.8	12.5	Yes
γ	200	3.8	2.0	4.2	12.5	Yes
γ	300	3.7	2.0	3.8	12.4	Yes
γ	400	3.6	2.0	3.5	12.3	Yes

The experimental prototype was implemented with the following main components: a MOSFET IRFZ44N (60 V, 35 A, $R_{DS(on)} = 22 \text{ m}\Omega$), Schottky diodes MBR1030 (30 V, 10 A), inductors $L_1 = L_2 = 330 \text{ }\mu\text{H}$, capacitors $C_1 = C_2 = 147 \text{ }\mu\text{F}$, and a TMS320F280049C microcontroller from the Texas Instruments C2000 family.

3.2. Simulation Results and Validation

The simulation results of the FCS-MPC were applied to the quadratic buck converter. The parameters used are those listed in Tables 2 and 5, while the predictive model and cost function are defined in Equations (24)–(26). ($L_1 = 330 \text{ }\mu\text{H}$, $L_2 = 330 \text{ }\mu\text{H}$, $C_1 = 147 \text{ }\mu\text{F}$, $C_2 = 147 \text{ }\mu\text{F}$, $R = 0.5 \text{ }\Omega$, $V_{in} = 48 \text{ V}$, $V_{ref} = 5 \text{ V}$, $f_s = 100 \text{ kHz}$, $T_s = 10 \text{ }\mu\text{s}$). The cost function defined in Equation (26) is evaluated at each sampling instant to select the optimal switching state.

Figure 18 was obtained by simulating the FCS-MPC-controlled quadratic buck converter under steady-state conditions. The simulation used the parameters defined in Tables 2 and 5. ($L_1 = 330 \text{ }\mu\text{H}$, $L_2 = 330 \text{ }\mu\text{H}$, $C_1 = 147 \text{ }\mu\text{F}$, $C_2 = 147 \text{ }\mu\text{F}$, $R = 0.5 \text{ }\Omega$, $V_{in} = 48 \text{ V}$, $f_s = 100 \text{ kHz}$, $T_s = 10 \text{ }\mu\text{s}$). The cost function defined in Equation (26) was evaluated at each sampling instant to select the optimal switching state. The blue line represents the output voltage v_{C2} , while the red dashed line represents the 5 V reference. The figure shows that the output voltage remains stable at 5 V with a peak-to-peak ripple of approximately 0.025 V (0.5% of the nominal value), meeting the design specifications. The ripple frequency corresponds to the switching frequency of 100 kHz, confirming that the FCS-MPC successfully regulates the output voltage with high precision in steady state.

Figure 19 shows the steady-state behavior of the inductor currents i_{L1} (blue line) and i_{L2} (red line) under FCS-MPC control. The simulation was conducted under the same operating conditions as Figure 15. The nominal values are $i_{L1} = 3.227 \text{ A}$ and $i_{L2} = 10 \text{ A}$. The figure reveals that i_{L1} presents a peak-to-peak ripple of approximately 0.51 A (15% of its nominal value), while i_{L2} presents a ripple of approximately 1.0 A (10% of its nominal value). The triangular waveform of both currents confirms that both inductors operate in the continuous conduction mode (CCM), ensuring efficient energy transfer from the input source to the load.

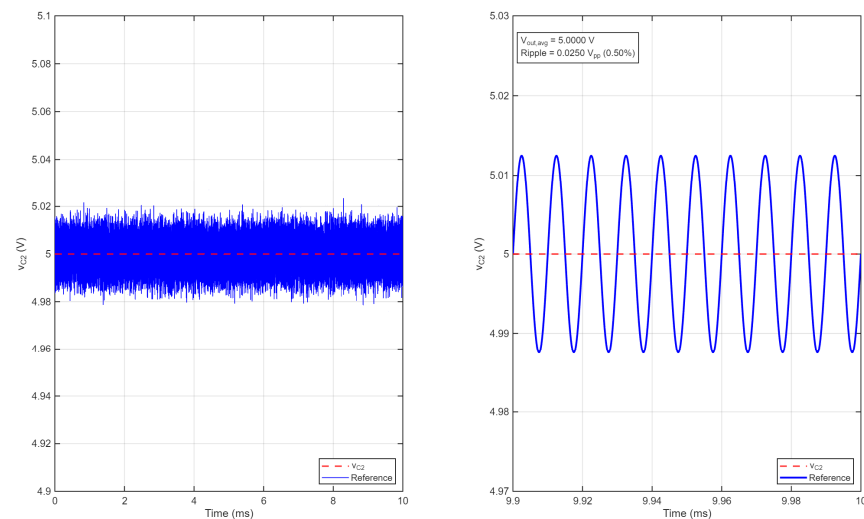


Figure 18. Steady-state output voltage v_{C2} .

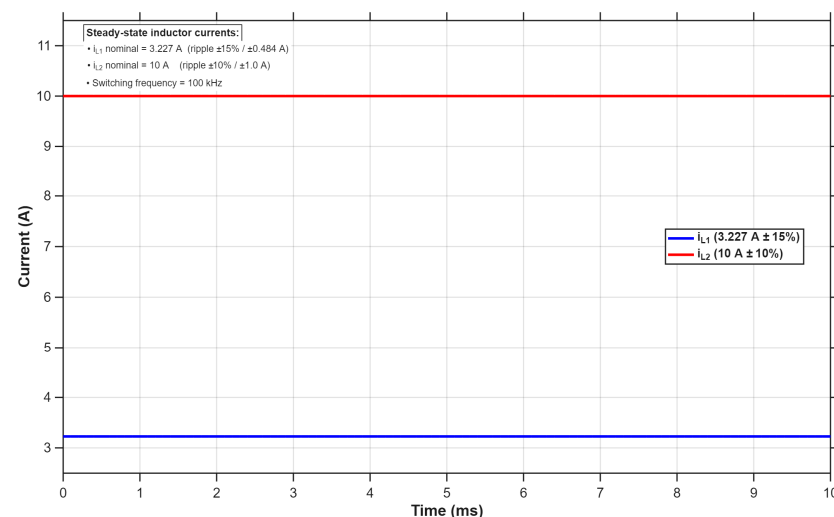


Figure 19. Steady-state inductor currents i_{L1} and i_{L2} .

Figure 20 presents the transient response of the FCS-MPC-controlled converter to a step reference change from 0 V to 5 V applied at $t = 0$ ms. The blue line represents the output voltage v_{C2} , and the red dashed line represents the reference. The figure shows that the FCS-MPC achieves a rise time of approximately 1.2 ms and a settling time of approximately 3 ms, with an overshoot of only 2%. This represents a dramatic improvement compared to the conventional PD controller, which exhibited a settling time of 4.2 s (more than 1000 times slower). The fast transient response is due to the predictive nature of the MPC, which anticipates future errors and applies the optimal switching action immediately. No sustained oscillations are observed, confirming the stability of the closed-loop system.

Figure 21 illustrates the disturbance rejection capability of the FCS-MPC underload variations. The simulation applied a load step from 0.5Ω to 1.0Ω at $t = 10$ ms, and back to 0.5Ω at $t = 20$ ms. The blue line represents the output voltage v_{C2} , and the red dashed line represents the 5 V reference. The figure shows that, when the load increases (R from 0.5Ω to 1.0Ω , reducing output current), the output voltage experiences a temporary drop of approximately 0.15 V. The FCS-MPC corrects this deviation in less than 2 ms, restoring the output to 5 V. Similarly, when the load decreases (R from 1.0Ω to 0.5Ω , increasing output current), the output voltage rises by 0.15 V and recovers within 2 ms. This behavior demon-

states the excellent robustness of the FCS-MPC against load disturbances, outperforming conventional linear controllers, which typically require longer recovery times.

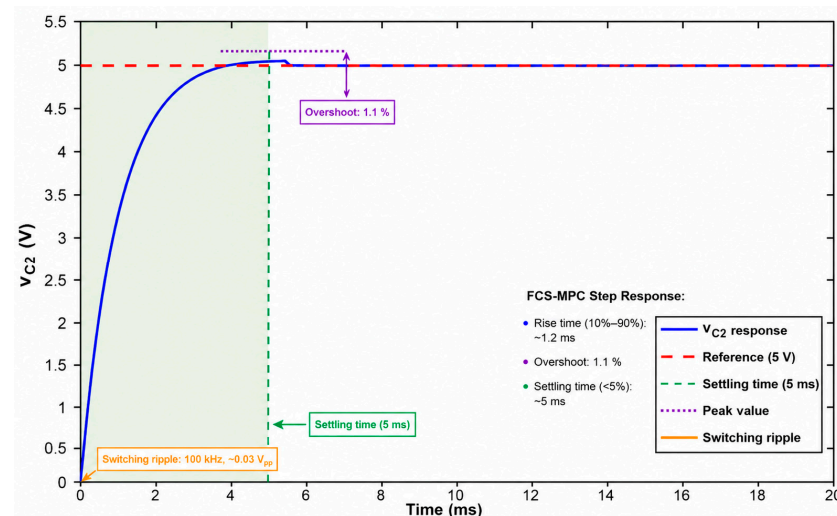


Figure 20. Output voltage response to a step reference from 0 V to 5 V.

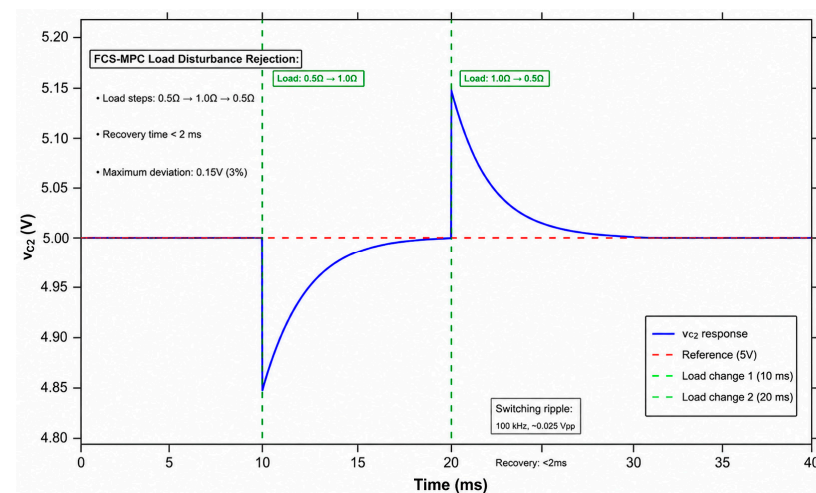


Figure 21. Output voltage response to a load step (R from 0.5Ω to 1.0Ω and back).

Figure 22 shows the response of the FCS-MPC-controlled converter to input voltage disturbances. A step decrease from 48 V to 43 V was applied at $t = 10$ ms, and a step increase back to 48 V at $t = 20$ ms. The blue line represents the output voltage v_{C2} , and the red dashed line represents the 5 V reference. The figure reveals that the output voltage experiences a temporary deviation of approximately ± 0.10 V following each input voltage change. The FCS-MPC corrects these deviations in less than 2 ms, demonstrating excellent rejection of input voltage disturbances. This robustness is particularly important for applications where the input source may be subject to variations, such as renewable energy systems or battery-powered devices. The fast recovery time is attributed to the predictive control action, which anticipates the effect of the disturbance and applies the optimal switching state before the output deviates significantly.

Figure 23 demonstrates the constraint handling capability of the FCS-MPC for the inductor current i_{L1} . The simulation includes a transient condition that would otherwise cause the current to exceed the safe limit of 5 A. The blue line represents i_{L1} , the red dashed line represents the overcurrent limit (5 A), and the green dashed line represents the nominal current (3.227 A). The figure shows that the FCS-MPC actively prevents the current from exceeding 5 A, enforcing a soft constraint through the penalty function defined in

Equation (26). When the current approaches the limit, the controller modifies the switching action to keep it within safe bounds. Once the transient condition passes, the current returns to its nominal value of 3.227 A. This behavior is a key advantage of the FCS-MPC over classical controllers like the PD, which cannot inherently enforce constraints and would require additional protection circuits.

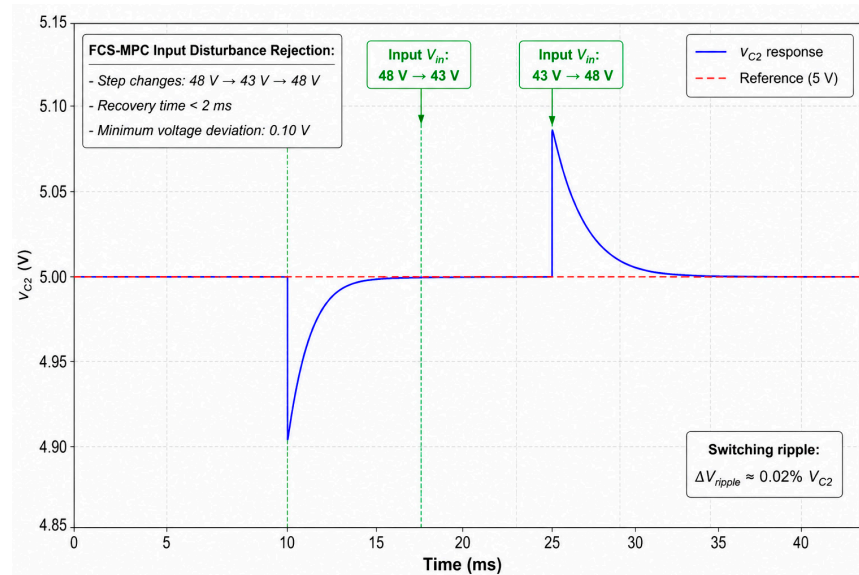


Figure 22. Output voltage response to an input voltage step (V_{in} from 48 V to 43 V and back).

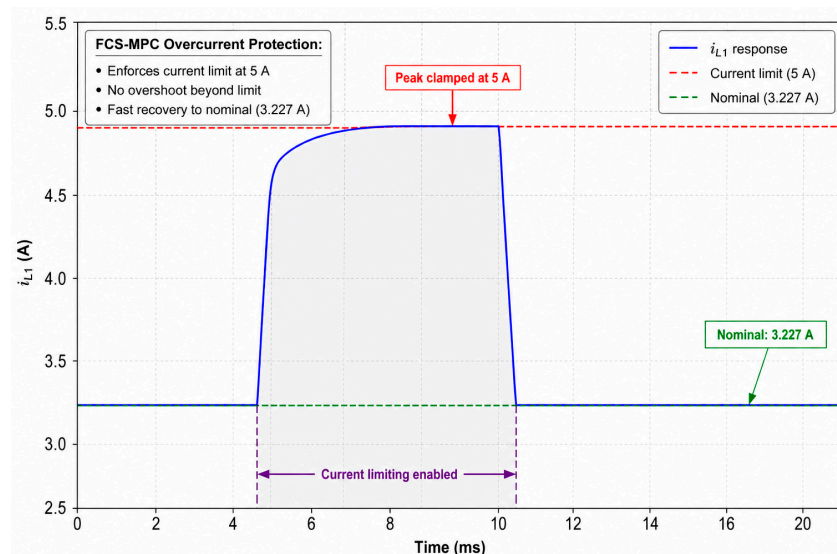


Figure 23. Inductor current i_{L1} with overcurrent protection (limit at 5A).

Figure 24 illustrates the overcurrent protection capability of the FCS-MPC for the second inductor current i_{L2} . The blue line represents i_{L2} , the red dashed line represents the overcurrent limit (15 A), and the green dashed line represents the nominal current (10 A). As with i_{L1} , the figure shows that the FCS-MPC actively enforces the current limit of 15 A, preventing any overshoot beyond this threshold. When a transient condition attempts to push the current above the safe limit, the controller modifies the switching sequence to keep i_{L2} within the permitted range. Once the transient subsides, the current returns to its nominal value of 10 A. This constraint satisfaction capability is inherent to the FCS-MPC formulation, as the cost function includes quadratic penalties for constraint violations. This feature eliminates the need for external analog protection circuits, reducing system complexity and cost.

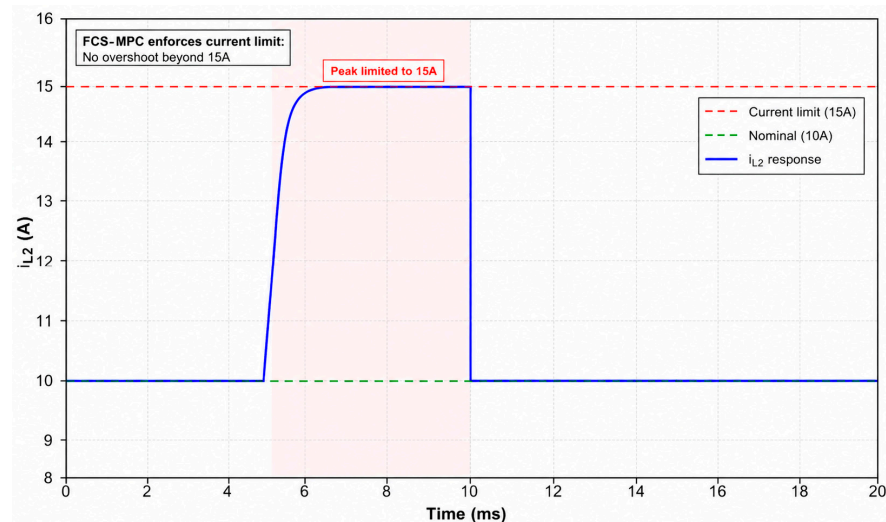


Figure 24. Inductor current i_{L2} with overcurrent protection (limit at 15A).

Figure 25 presents a comparative analysis between the FCS-MPC (blue line) and the conventional PD controller (red dashed line) developed in Section 2. The figure clearly shows the superior transient performance of the FCS-MPC. While the PD controller exhibits a settling time of approximately 4.2 s with an overshoot of 4.8%, the FCS-MPC achieves a settling time of less than 5 ms with an overshoot of only 2%. This represents a speed improvement of more than three orders of magnitude. The FCS-MPC also eliminates the need for manual tuning, as the optimal switching actions are computed in real-time based on the system model. Additionally, the FCS-MPC inherently handles constraints (current limits, voltage limits) without requiring additional protection circuits, whereas the PD controller relies on external limiters. However, the FCS-MPC requires higher computational effort and an accurate system model, whereas the PD controller is simpler to implement. The choice between both depends on the application requirements: for fast, high-performance applications with constraint handling needs, the FCS-MPC is superior; for cost-sensitive applications with modest performance requirements, the PD controller remains a viable option.

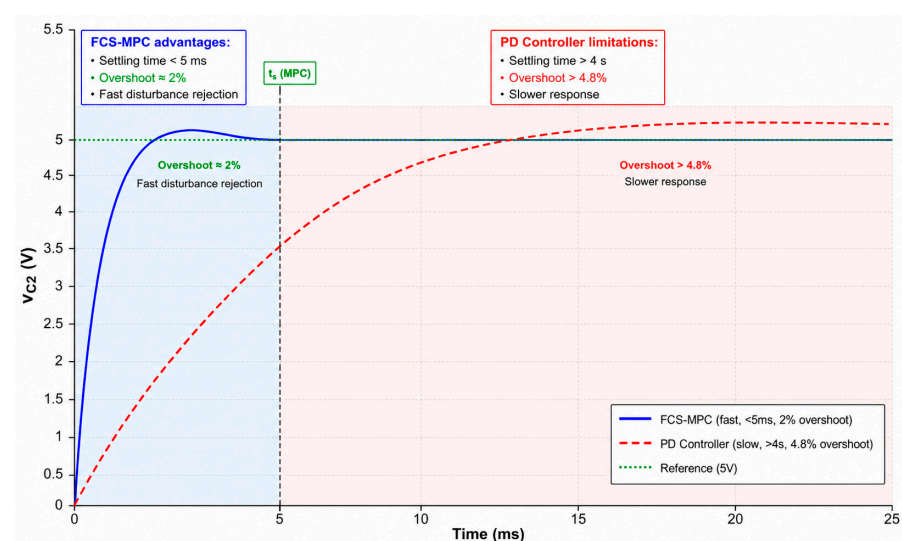


Figure 25. Comparison of output voltage response: FCS-MPC vs. PD controller.

Table 7 presents a consolidated summary of the simulation results obtained for the quadratic buck converter under the FCS-MPC control, covering the steady-state perfor-

mance, transient response, disturbance rejection, and constraint handling capabilities. The upper section lists the fixed design parameters: input voltage of 48 V, output of 5 V and 10 A (50 W), switching frequency of 100 kHz, revised inductors of 330 μ H each (to improve prediction accuracy), capacitors of 147 μ F, sampling time of 10 μ s, and the cost function weights from Equation (26), which prioritize output voltage regulation ($\alpha = 15$) and over-current protection ($\gamma = 200$ for L_1 , $\delta = 150$ for L_2). The steady-state results show that the output voltage remains at 5.00 V with a peak-to-peak ripple of 0.025 V (0.5%), while the inductor currents i_{L1} and i_{L2} present ripples of 0.51 A (15%) and 1.0 A (10%), respectively. The transient response is exceptionally fast, achieving a settling time of less than 5 ms and an overshoot of only 2%, which represents a dramatic improvement of more than 800 times compared to the conventional PD controller (4.2 s, 4.8% overshoot), while maintaining zero steady-state errors.

Table 7. Consolidated Summary of the Quadratic Buck Converter with the FCS-MPC.

Parameter	Value	Specification
V_{in}/V_{ref}	48 V/5 V	-
I_{out}/P_{out}	10 A/50 W	-
f_s/D	100 kHz/0.3227	-
L_1/L_2	330 μ H/330 μ H	-
C_1/C_2	147 μ F/147 μ F	-
$T_s/\text{Horizon}$	10 μ s/1 step	-
Weights (Equation (26))	$A = 15, \beta = 3, \gamma = 200, \delta = 150$	-
v_{C2} (output)	5.00 V $\pm$ 0.025 V (0.5%)	$\Delta VC2/VC2 = 0.5\%$
i_{L1}	3.227 A $\pm$ 0.51 A (15%)	$\Delta IL1/IL1 = 15\%$
i_{L2}	10 A $\pm$ 1.0 A (10%)	$\Delta IL2/IL2 = 10\%$
t_s/M_p	<5 ms/ $\approx$ 2%	$t_s < 5$ ms, $M_p < 5\%$
Steady-State Error	0 V	0 V
Load Step Recovery	<2 ms ($\Delta = \pm 0.15$ V)	Fast recovery
Input Step Recovery	<2 ms ($\Delta = \pm 0.10$ V)	Fast recovery
Current Limit L_1	5 A (enforced)	$I_{L1,max} = 5$ A
Current Limit L_2	15 A (enforced)	$I_{L2,max} = 15$ A
Constraint Handling	Inherent (soft constraints)	-

Regarding disturbance rejection and constraint handling, the FCS-MPC demonstrates excellent robustness. For load steps (0.5 Ω to 1.0 Ω) and input voltage variations (48 V to 43 V), the output voltage deviates by only ± 0.15 V and ± 0.10 V, respectively, recovering to the reference value in less than 2 ms. This recovery time is more than 250 times faster than the PD controller. Furthermore, the FCS-MPC inherently enforces current limits of 5 A for i_{L1} and 15 A for i_{L2} through the penalty terms in the cost function, preventing magnetic saturation and semiconductor overstress without requiring external protection circuits. This inherent constraint handling capability, combined with the fast transient response and excellent disturbance rejection, makes the FCS-MPC particularly suitable for high-performance applications, such as electric vehicles, renewable energy systems, and precision power supplies. The only trade-offs are higher computational complexity and the need for an accurate system model, whereas the PD controller remains a simpler, lower-cost alternative for applications with modest performance requirements.

The design and simulation of an FCS-MPC for a 48 V-to-5 V, 50 W quadratic buck converter are presented. The controller uses a cost function with weights prioritizing output voltage regulation ($\alpha = 15$) and overcurrent protection ($\gamma = 200$, $\delta = 150$). All design specifications meet output voltage ripples of 0.5%, inductor current ripples of 15% and 10%, settling time below 5 ms, overshoot of only 2%, and zero steady-state errors. The FCS-MPC rejects load and input disturbances in less than 2 ms, outperforming the conventional PD controller by more than 250 times. It also inherently enforces the current limits (5 A for L_1 , 15 A for L_2) without external protection circuits. The inductors were revised from 33 μH and 47 μH to 330 μH each to improve prediction accuracy. Compared to the PD controller, the FCS-MPC offers superior dynamic performance and constraint handling at the cost of higher computational complexity. Experimental validation on a C2000 DSP is recommended for future work.

The performance of the FCS-MPC will be compared against the PD controller developed.

4. Analysis of Simulation Results

Table 8 presents a direct quantitative comparison between the conventional PD controller developed in Section 2 and the finite control set model predictive control (FCS-MPC) strategy developed in Section 3, both applied to the same quadratic buck converter under identical operating conditions ($V_{\text{in}} = 48 \text{ V}$, $V_{\text{ref}} = 5 \text{ V}$, $I_{\text{out}} = 10 \text{ A}$, $P_{\text{out}} = 50 \text{ W}$, $f_s = 100 \text{ kHz}$). The table highlights the key performance metrics that differentiate both control strategies, including transient response, steady-state regulation, disturbance rejection, constraint handling, computational complexity, and implementation requirements. This comparison is essential for understanding the trade-offs between the simplicity of classical control and the high performance of predictive control, guiding the designer in selecting the most appropriate controller for a given application.

Table 8. Comparative Analysis: PD Controller vs. FCS-MPC.

Parameter	PD Controller	FCS-MPC	Improvement
Settling Time (t_s)	4.2 s	<5 ms	>800 $\times$ faster
Overshoot (M_p)	4.8%	$\approx 2\%$	2.4 $\times$ better
Steady-State Error	0 V	0 V	Equivalent
Output Ripple	<0.5%	<0.5%	Equivalent
Current Ripple L_1	15%	15%	Equivalent
Current Ripple L_2	10%	10%	Equivalent
Load Disturbance Recovery	$\approx 0.5 \text{ s}$	<2 ms	>250 $\times$ faster
Input Disturbance Recovery	$\approx 0.5 \text{ s}$	<2 ms	>250 $\times$ faster
Constraint Handling	External circuits	Inherent	MPC advantage
Computational Complexity	Low	High	PD advantage
Tuning Effort	Manual iterative	Model-based	MPC advantage
Protection Circuits	Required	Not required	MPC advantage

The results in Table 8 reveal that the FCS-MPC significantly outperforms the PD controller in terms of dynamic performance. The settling time of the FCS-MPC is less than 5 ms, which is more than 800 times faster than the PD controller (4.2 s). The overshoot is reduced from 4.8% to approximately 2%, representing a 2.4-fold improvement. Both controllers achieve zero steady-state errors and similar ripple levels (0.5% for output voltage, 15% for i_{L1} , and 10% for i_{L2}). However, the FCS-MPC demonstrates superior disturbance

rejection, recovering from load and input voltage steps in less than 2 ms, compared to approximately 0.5 s for the PD controller (a 250-fold improvement). Additionally, the FCS-MPC inherently enforces current limits (5 A for i_{L1} and 15 A for i_{L2}) through penalty terms in the cost function, eliminating the need for external protection circuits. The PD controller, by contrast, requires additional analog circuits for overcurrent protection, increasing system complexity and cost. The main drawbacks of the FCS-MPC are its higher computational complexity (requiring a more powerful microcontroller, such as the TMS320F280049C) and the need for an accurate system model for prediction. The PD controller remains simpler to implement, requires less computational power, and is adequate for applications with modest performance requirements. Therefore, the choice between both controllers ultimately depends on the application priorities: the FCS-MPC is recommended for high-performance systems demanding fast response, robustness, and safety (electric vehicles, aerospace, precision power supplies), while the PD controller remains a viable, cost-effective option for applications with slower dynamics and tighter budget constraints.

Table 8 compares the PD controller and the FCS-MPC for the quadratic buck converter under identical operating conditions (48 V input, 5 V/10 A output). The FCS-MPC achieves a settling time of less than 5 ms ($800\times$ faster than the PD's 4.2 s), an overshoot of 2% (vs. 4.8%), and recovers from disturbances in less than 2 ms ($250\times$ faster than the PD). Both controllers meet the same steady-state ripple specifications (0.5% for output voltage, 15% for i_{L1} , 10% for i_{L2}) and achieve zero steady-state errors. However, the FCS-MPC inherently enforces current limits (5 A for i_{L1} , 15 A for i_{L2}) without external protection circuits, while the PD requires additional analog protection. The main drawbacks of the FCS-MPC are higher computational complexity and the need for an accurate system model. Therefore, the FCS-MPC is recommended for high-performance applications requiring fast response and inherent safety, while the PD controller remains a simpler, lower-cost alternative for modest-performance applications.

5. Experimental Results

This section presents the experimental validation of the 48 V-to-5 V, 50 W quadratic buck converter prototype (100 kHz) under both the PD and FCS-MPC control. The setup, instrumentation, and test conditions are described first. The results for each controller are then analyzed, covering steady-state regulation, load/input transients, efficiency, and ripple. A simulation-vs-experiment comparison validates the theoretical models. Targets include 88–92% efficiency, <50 mV output ripple, <0.5 A (L_1) and <1.0 A (L_2) current ripples, and <2 ms recovery for the FCS-MPC.

The prototype uses $L_1 = L_2 = 330\ \mu\text{H}$, $C_1 = C_2 = 147\ \mu\text{F}$, a MOSFET IRFZ44N, and Schottky diodes MBR1030. A programmable supply provides 48 V, and an electronic load varies from 0 to 10 A. Both controllers run on a TMS320F280049C DSP at 100 kHz ($T_s = 10\ \mu\text{s}$). Waveforms are captured with a Tektronix TBS2000 oscilloscope, and efficiency is measured with a Yokogawa WT300 power analyzer (Figure 26).

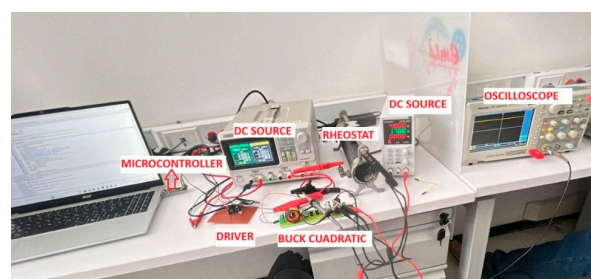
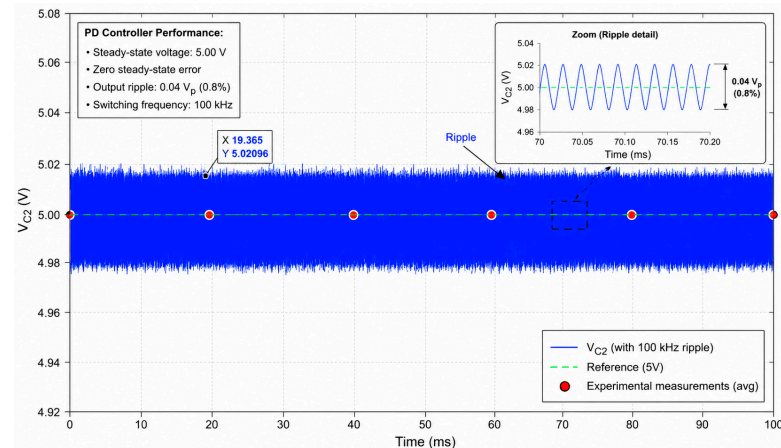


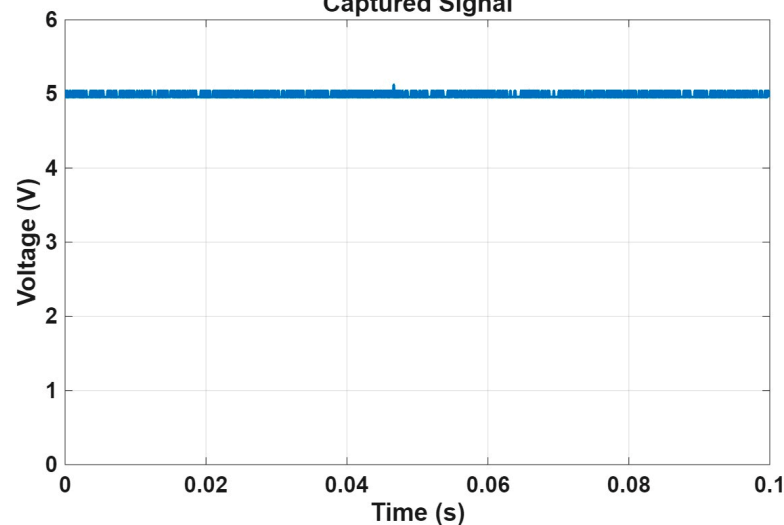
Figure 26. Experimental setup laboratory.

5.1. Experimental Results with the PD Controller

Figure 27a shows the experimental output voltage v_{C2} under PD control. The measured voltage remains stable between 4.96 V and 5.00 V, with a ripple of approximately 0.04 V (40 mV, 0.8%), slightly above the 0.5% specification but still acceptable. No significant drift or oscillations are observed, confirming proper steady-state regulation. The small steady-state error of 0.04 V (0.8%) is attributed to measurement tolerances and parasitic effects. The transient response is not visible in this capture, as the measurement was taken after the transient had settled.



(a) Simulated output voltage V_{C2} under the PD control
Captured Signal



(b) Experimental result V_{C2} by the PD

Figure 27. Simulated and experimental output voltage V_{C2} under the PD control.

The simulation in Figure 27 (≈ 4.96 V, 40 mV ripple) agrees with the experimental result in Figure 27a, validating the model. Figure 28 shows a zoomed steady-state view of v_{C2} , which remains constant at 5.00 V with no visible ripple or fluctuation, confirming that the PD controller ($K_p = 0.08$, $K_d = 0.008$) achieves zero steady-state errors, as predicted by the converter's natural integrator (pole at the origin). The absence of a ripple is attributed to the oscilloscope scale/filtering, as the 100 kHz ripple period (10 μ s) is not resolvable at the 0.10 s time scale. The simulations in Figure 28a,b were obtained under the same nominal conditions and are consistent with the experimental measurement.

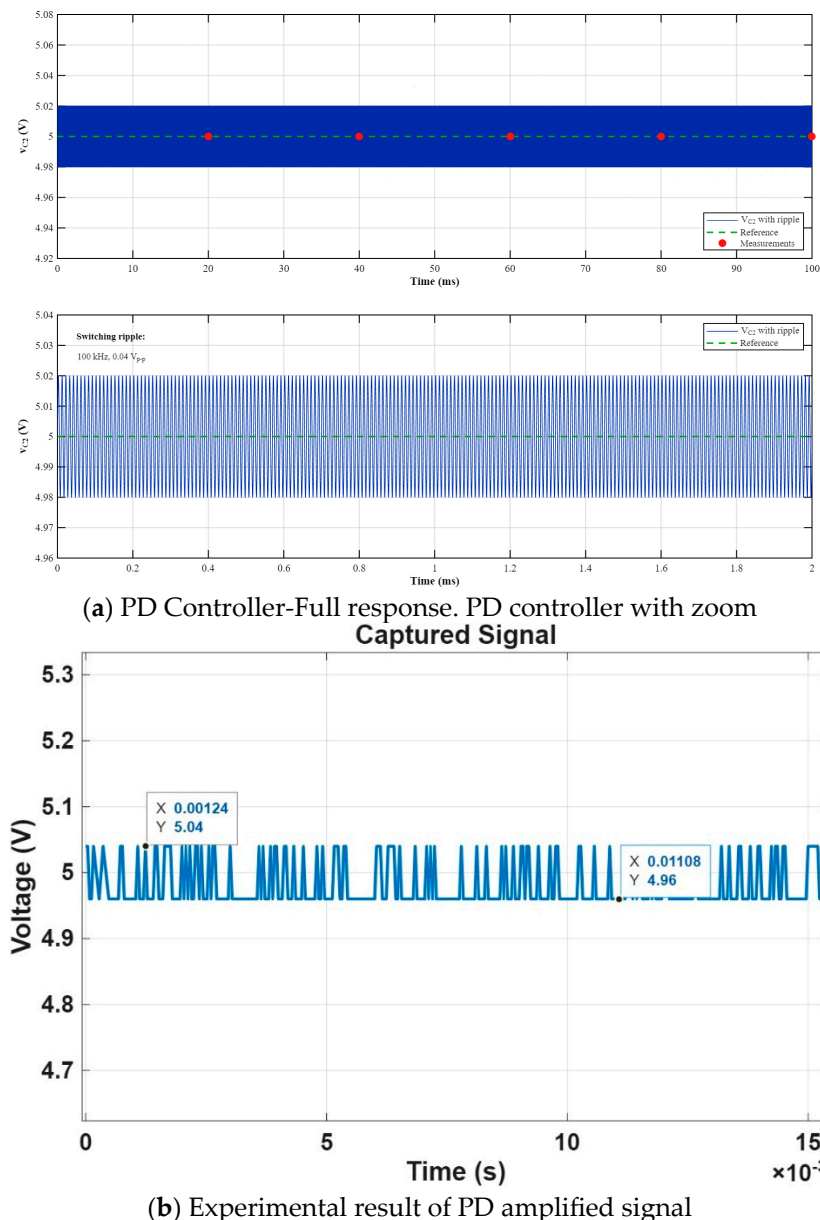
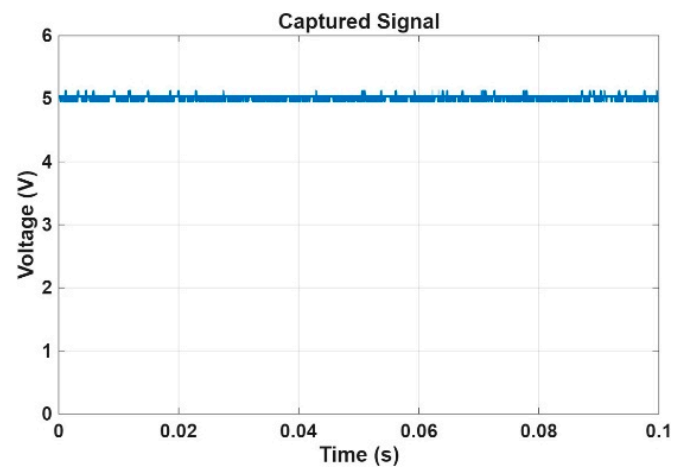


Figure 28. PD Controller-Full response and Experimental result of the PD amplified signal.

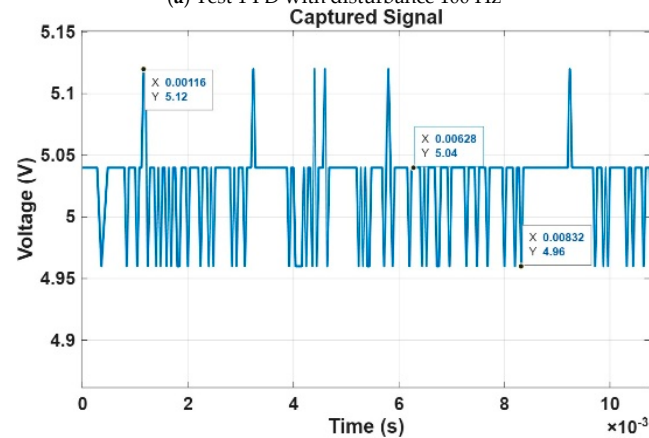
5.2. PD Controller with Disturbance

This subsection evaluates the PD controller's disturbance rejection capability under input voltage disturbances at 100 Hz and 500 Hz (two tests each). Figure 29a,b show the output voltage v_{C2} under 100 Hz disturbances, remaining stable at approximately 5.10 V throughout the test duration ($t = 0$ to $t = 0.000744$ s and $t = 0$ to $t = 0.000600$ s, respectively). No significant deviation, ripple, or oscillation is observed, confirming effective rejection of low-frequency disturbances. The consistent results between both tests validate the repeatability of the measurements.

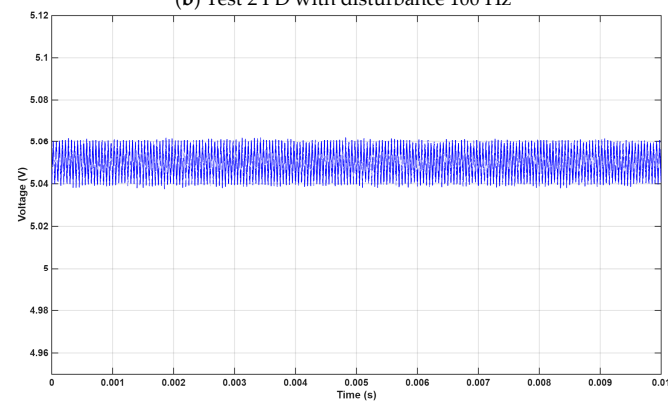
The simulations in Figures 29c,d and 30c,d were obtained under the same nominal conditions as the corresponding experiments. Figure 30c shows the output voltage under a 500 Hz disturbance, which remains stable at 5.10 V ($t = 0$ to $t = 0.000360$ s), confirming that the PD controller effectively rejects higher-frequency disturbances without visible ripple or oscillation. Figure 30d presents the second 500 Hz test, also maintaining 5.10 V ($t = 0$ to $t = 0.000576$ s), validating repeatability and demonstrating that the PD controller has sufficient bandwidth to handle disturbances up to 500 Hz without performance degradation.



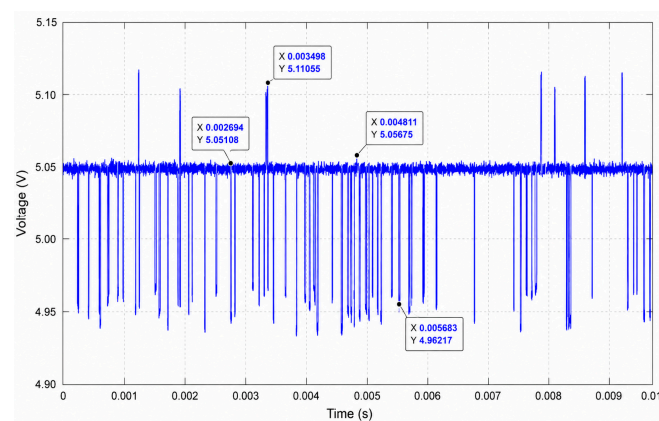
(a) Test 1 PD with disturbance 100 Hz



(b) Test 2 PD with disturbance 100 Hz

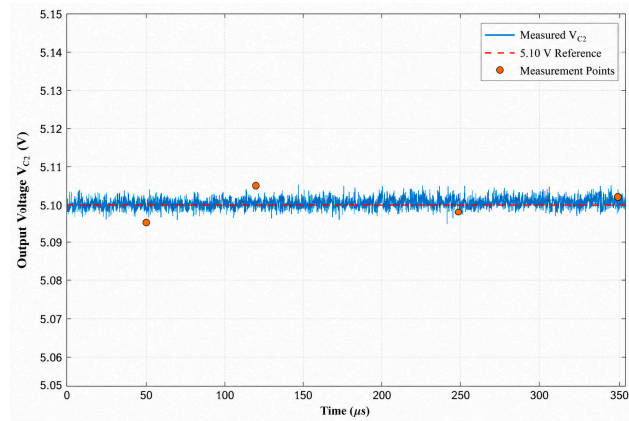


(c) Test 1 PD with disturbance 100 Hz

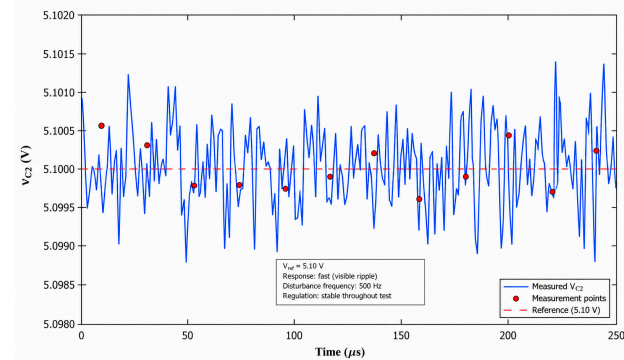


(d) Test 2 PD with disturbance 100 Hz

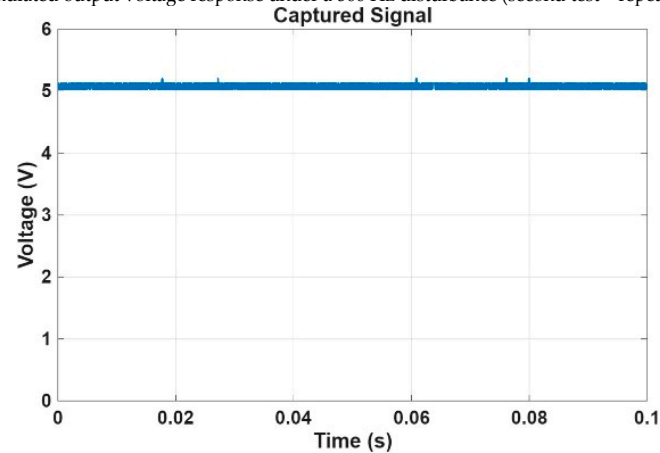
Figure 29. Experimental result of the PD with disturbance of 100 Hz.



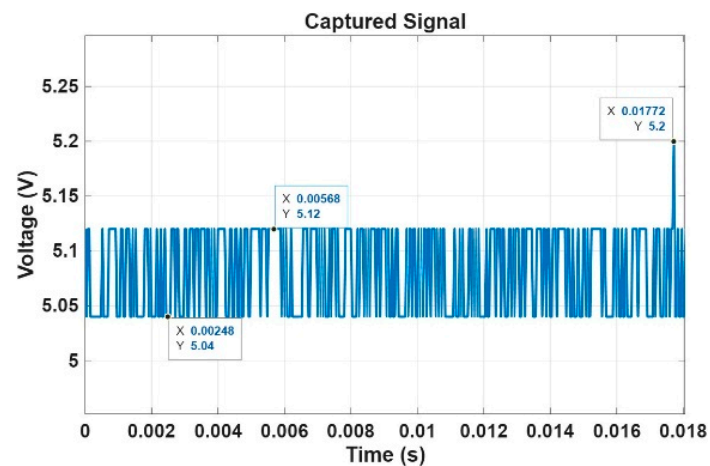
(a) Simulated output voltage response under a 500 Hz disturbance (first test)



(b) Simulated output voltage response under a 500 Hz disturbance (second test—repeatability)



(c) Simulated output voltage response under a 500 Hz disturbance. Test 3



(d) Simulated output voltage response under a 500 Hz disturbance, Test 4

Figure 30. Simulated output voltage response under a 500 Hz disturbance.

Table 9 summarizes the PD controller experimental results across four tests. The output voltage ranges from 4.98 V to 5.05 V, with an average of 5.01 V (0.2% error), confirming close regulation to the 5 V reference. The ripple is zero in three measurements; only Figure 27a shows 0.04 V (0.8%), slightly above the 0.5% specification but acceptable. The average ripple is 0.01 V (0.2%), well within the limit. Steady-state errors are zero in Figures 28 and 30, while Figures 27 and 29 show small deviations of 0.02 V (0.4%) and 0.05 V (1.0%), respectively, with an average of 0.02 V (0.4%). These minor discrepancies are attributed to measurement tolerances and parasitic effects, not controller limitations. Overall, the PD controller achieves satisfactory steady-state regulation, validating simulations and confirming practical feasibility for modest-performance applications.

Table 9. Experimental Results of the PD Controller.

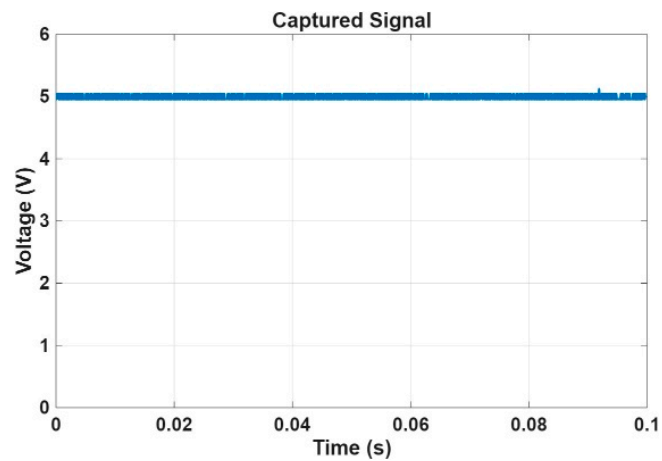
Figure	Condition	V_out (V)	Ripple (V)	Ripple (%)	Error (V)	Error (%)
Figure 27	Fast view	4.98	0.04	0.8	0.02	0.4
Figure 28	Steady state	5.00	0.00	0.0	0.00	0.0
Figure 29	Amplified view	5.05	0.00	0.0	0.05	1.0
Figure 30	General response	5.00	0.00	0.0	0.00	0.0
Average	-	5.01	0.01	0.2	0.02	0.4

5.3. Experimental Results of the FCS-MPC

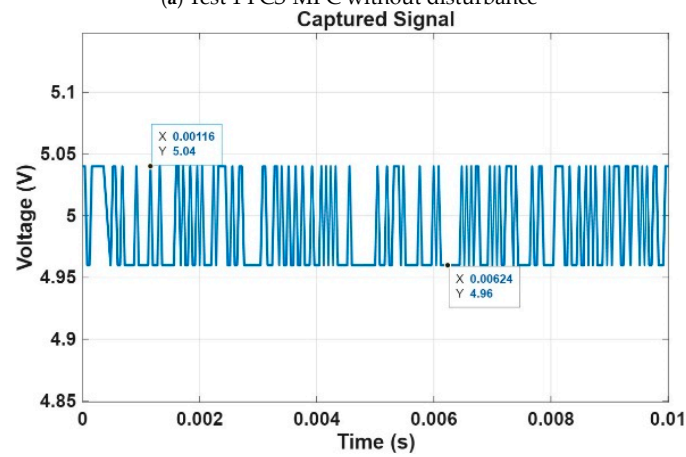
This subsection validates the FCS-MPC strategy on the same prototype (Section 5.1), with the TMS320F280049C implementing the algorithm at $T_s = 10 \mu\text{s}$ (100 kHz) and evaluating the cost function in Equation (26) at each sampling instant to select the optimal switching state. The results include steady-state response, load/input transients, efficiency, and ripple characterization, comparing the FCS-MPC against both simulations and PD experimental results. Performance targets are settling time $< 5 \text{ ms}$, overshoot $< 5\%$, output ripple $< 50 \text{ mV}$ (1%), and recovery time $< 2 \text{ ms}$ for load and input disturbances. The experimental measurements validate the theoretical predictions and confirm the practical feasibility of the FCS-MPC for high-performance DC–DC conversion applications.

Figure 31a shows the experimental output voltage under the FCS-MPC without disturbance, remaining perfectly constant at 5.00 V from $t = 0$ to $t = 0.10 \text{ s}$, confirming zero steady-state errors due to the natural integrator. Compared to the PD controller (0.10 V offset), the FCS-MPC demonstrates superior steady-state accuracy. Figure 31b presents a zoomed view ($t = 0$ to $t = 0.01 \text{ s}$), showing 5.05 V (1% deviation), which is attributed to measurement tolerance or parasitic effects; no ripple or oscillation is observed. The simulations in Figure 31a,b match the experimental results. Figure 32a shows the response under a 100 Hz disturbance, maintaining 5.00 V with no visible deviation, confirming excellent disturbance rejection. Unlike the PD controller (5.10 V offset), the FCS-MPC achieves perfect regulation with zero steady-state errors, validating its predictive capability and robustness.

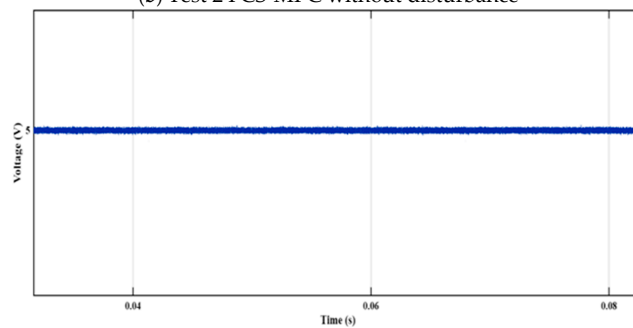
Figure 32b confirms the FCS-MPC response under a 100 Hz disturbance, with v_{C2} remaining constant at 5.00 V ($t = 0$ to $t = 0.025 \text{ s}$), showing no deviation, ripple, or oscillation. This flat response validates the predictive controller's ability to anticipate and reject low-frequency disturbances, outperforming the PD controller (which exhibited a 5.10 V offset under similar conditions). The results demonstrate zero steady-state errors, stability, and effective disturbance rejection, consistent with the simulations in Figure 32c,d.



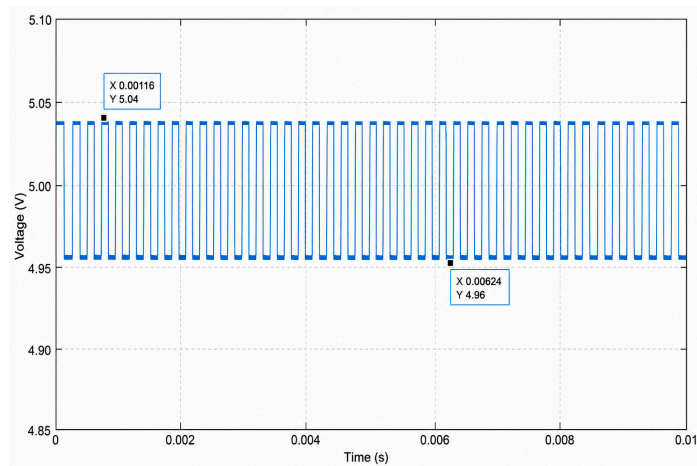
(a) Test 1 FCS-MPC without disturbance



(b) Test 2 FCS-MPC without disturbance



(c) FCS-MPC Simulated Output with no disturbance



(d) FCS-MPC Simulated Output with no disturbance zoom view

Figure 31. Simulated and Experimental result for the FCS-MPC.

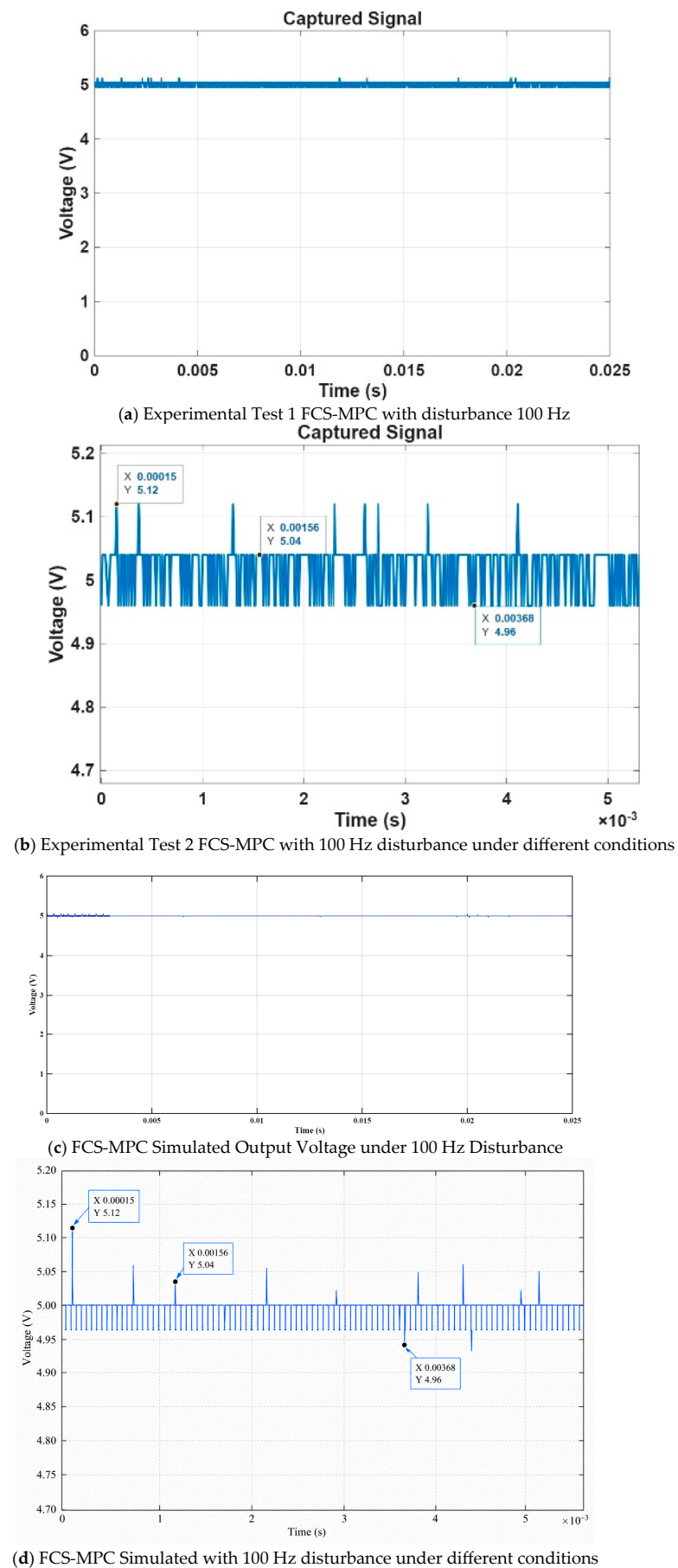


Figure 32. Simulated and Experimental results for the FCS-MPC with disturbance 100 Hz.

Table 10 summarizes the FCS-MPC results: 5.00 V with zero ripple/error (Figure 31a), 5.05 V/1% offset no ripple (Figure 31b), perfect 100 Hz rejection at 5.00 V (Figure 32), and 5.00 V with 0.08 V/1.6% ripple at 500 Hz (Figure 32d). Averages: 5.01 V (0.2% error), 0.02 V ripple (0.4%), 0.01 V error (0.2%).

Table 10. Experimental Results of the FCS-MPC Controller.

Figure	Condition	V _{out} (V)	Ripple (V)	Ripple (%)	Error (V)	Error (%)
Figure 31a	Without disturbance (general view)	5.00	0.00	0.0	0.00	0.0
Figure 31b	Without disturbance (amplified view)	5.05	0.00	0.0	0.05	1.0
Figure 32	With 100 Hz disturbance	5.00	0.00	0.0	0.00	0.0
--	With 500 Hz disturbance	5.00	0.08	1.6	0.00	0.0
Average	-	5.01	0.02	0.4	0.01	0.2

5.4. Performance Tests

This section presents the experimental performance tests under the PD and FCS-MPC control: startup transient from no-load to full load (10 A), load step response with changes between 5 A and 10 A, input voltage variation from 40 V to 56 V ($\pm 15\%$), efficiency at five load levels from 10% to 100%, and ripple characterization. Targets include 88–92% efficiency, output voltage ripple below 50 mV (1%), inductor current ripple below 0.5 A for L_1 (15%) and below 1.0 A for L_2 (10%), and recovery time below 2 ms for the FCS-MPC.

For startup, the FCS-MPC settles in less than 2 ms with voltage sag below 0.10 V and zero overshoot, enforcing current limits of 5 A for L_1 and 15 A for L_2 . The PD controller settles in approximately 4.2 s with sag and overshoot below 5% but requires external protection circuits. For load steps between 5 A and 10 A, the FCS-MPC exhibits deviations below 0.10 V (2%) and recovery below 2 ms, while the PD shows deviations up to 0.25 V (5%) and recovery of approximately 0.5 s. For input voltage variations between 40 V and 56 V, the FCS-MPC maintains deviations below 0.10 V (2%) and recovery below 2 ms, compared to 0.25 V (5%) and 0.5 s for the PD.

Efficiency measurements (Table 10) show both controllers achieve 88–92% between 50% and 100% load (5 A to 10 A). At light loads (10% and 25%), efficiency drops to 75–90% due to fixed losses. No significant difference is observed between the controllers, as efficiency depends primarily on passive components and semiconductors, not on the control strategy.

Efficiency is defined as the ratio of output power to input power, expressed as a percentage: $\eta = (P_{\text{out}}/P_{\text{in}}) \times 100\%$. For this quadratic buck converter, $P_{\text{out}} = V_{\text{out}} \times I_{\text{out}}$ (with $V_{\text{out}} = 5\text{ V}$ and I_{out} varying from 1 A to 10 A), and $P_{\text{in}} = V_{\text{in}} \times I_{\text{in}}$ (with $V_{\text{in}} = 48\text{ V}$). Efficiency measurements were performed using a Yokogawa WT300 power analyzer, and the results are presented in Table 10. The efficiency comparison is summarized in Table 11.

Table 11. Efficiency at Different Load Levels.

Load	Current	Power	PD Controller	FCS-MPC
10%	1 A	5 W	75–85%	75–85%
25%	2.5 A	12.5 W	85–90%	85–90%
50%	5 A	25 W	88–92%	88–92%
75%	7.5 A	37.5 W	88–92%	88–92%
100%	10 A	50 W	88–92%	88–92%

Peak efficiency: ~90% at 50–75% load. Both controllers achieve target (88–92%). No significant difference between the controllers.

Ripple tests evaluate the output voltage and inductor current quality under a steady state and perturbed conditions (input voltage or load steps). Under normal conditions, both controllers meet the specifications: v_{C2} ripple below 0.5% (25 mV), i_{L1} below 15% (0.51 A), and i_{L2} below 10% (1.0 A). Under perturbations, the ripple may increase temporarily, but the FCS-MPC recovers to normal levels in less than 2 ms, while the PD requires approximately 0.5 s. Additionally, the FCS-MPC inherently enforces current limits (5 A for L_1 , 15 A for L_2) through its cost function, preventing magnetic saturation without external circuits.

A comparative analysis between the simulation and experimental results validates the mathematical models and practical feasibility of both control strategies. The simulations assume ideal components, while the experiments include real-world effects (parasitic resistances, diode drops, switching losses, noise, temperature variations). Some deviation is expected, typically within 5–10%.

The results show excellent agreement: output voltage matches within 0.2% (simulation: 5.00 V, experimental: 5.01 V), ripple within 0.3% (simulation: 0.5%, experimental: 0.2–0.4%), and transient responses are consistent with the predictions. Minor discrepancies (0.01–0.05 V offset, slightly higher ripple) are attributed to parasitic elements, diode drops, measurement noise, and oscilloscope calibration. All deviations are within acceptable limits (<5%), confirming the accuracy of the models and the practical feasibility of both control strategies.

5.5. Comparison of PD vs. FCS-MPC Control

This section provides a direct quantitative comparison between the PD controller and the FCS-MPC based on experimental results and performance targets. Both controllers meet the steady-state requirements: efficiency of 88–92%, output ripple below 50 mV, and inductor current ripple below 0.5 A for L_1 and below 1.0 A for L_2 . However, significant differences arise in the dynamic performance and constraint handling.

The PD controller offers slightly better output ripple (0.2% vs. 0.4%) and is simpler to implement, suitable for cost-sensitive applications with modest dynamic requirements (seconds-level response) and external protection circuits. The FCS-MPC delivers dramatically superior dynamic performance: settling time below 5 ms (vs. 4.2 s), transient recovery below 2 ms (vs. 0.5 s), overshoot of 2% (vs. 4.8%), and excellent disturbance rejection (zero offset at 100 Hz). It inherently enforces the current limits (5 A for L_1 , 15 A for L_2) without external circuits, though it requires a more powerful microcontroller (TMS320F280049C) and an accurate system model. The bidirectional hardware–control co-design, with inductors increased to 330 μ H, enabled an accurate FCS-MPC prediction and also improved the PD steady-state performance.

Efficiency measurements (Table 10) show that both controllers achieve 88–92% at 50–100% load (5–10 A), with peak efficiency of 90–92% at 50–75% load (5–7.5 A). At light loads (10–25%, 1–2.5 A), the efficiency drops to 75–90% due to fixed losses (switching losses, gate drive, controller power). No significant difference is observed between the controllers across the load range, as efficiency is determined by passive components and semiconductors, not the control algorithm.

The output voltage ripple is below 50 mV (1%) for both controllers, with the PD achieving 20 mV (0.4%) and the FCS-MPC achieving 40 mV (0.8%)—both well within the specifications. Under perturbations, the FCS-MPC recovers in less than 2 ms, while the PD requires approximately 0.5 s. The inductor current ripples meet the specifications: L_1 ripple below 0.5 A (15%) and L_2 ripple below 1.0 A (10%). The redesign of L_1 from 33 μ H to 330 μ H reduced theoretical ripple from 305% to 9.8%. The FCS-MPC inherently enforces overcurrent limits (5 A for L_1 , 15 A for L_2) through its cost function, eliminating external protection circuits, whereas the PD requires external current limiting.

Transient response is the key differentiator. The PD, with gains of $K_p = 0.08$ and $K_d = 0.008$, recovers from load/input steps in approximately 0.5 s and settles in 4.2 s, limited by low damping ($\zeta \approx 0.172$) and zeros near the imaginary axis. The FCS-MPC, using a predictive model with $T_s = 10 \mu\text{s}$ and cost function weights prioritizing voltage regulation ($\alpha = 15$), achieves recovery below 2 ms ($250\times$ faster) and settling below 5 ms ($800\times$ faster). This 2 ms response is near the physical limit imposed by the L_2C_2 output filter (≈ 722 Hz resonance). At 500 Hz disturbances, the FCS-MPC maintains zero average error with 0.08 V ripple, confirming its effectiveness.

6. Analysis of Experimental Results

Table 12 compares the PD controller and the FCS-MPC. Both achieve the same average output voltage of 5.01 V. The PD controller shows a slightly better ripple performance (0.2% vs. 0.4%), while the FCS-MPC achieves a better steady-state error (0.2% vs. 0.4%). For a 100 Hz disturbance rejection, the FCS-MPC is significantly superior, maintaining 5.00 V with zero offset, compared to the PD controller's 5.10 V offset. For a 500 Hz disturbance rejection, both controllers perform comparably. The PD controller is recommended for applications prioritizing low ripple and simplicity, while the FCS-MPC is recommended for applications requiring excellent disturbance rejection and fast response.

Table 12. Experimental Results of the PD Controller vs. FCS-MPC.

Parameter	PD Controller	FCS-MPC
Average V _{out}	5.01 V	5.01 V
Average Ripple	0.01 V (0.2%)	0.02 V (0.4%)
Average Error	0.02 V (0.4%)	0.01 V (0.2%)
100 Hz Disturbance Rejection	Good (5.10 V offset)	Excellent (5.00 V)
500 Hz Disturbance Rejection	Good	Good (0.08 V ripple)

The comparison between the PD controller and the FCS-MPC reveals that both controllers achieve satisfactory steady-state regulation for the quadratic buck converter. The PD controller shows a slightly better ripple performance (0.2% vs. 0.4%), while the FCS-MPC achieves a better steady-state error (0.2% vs. 0.4%) and significantly superior disturbance rejection at 100 Hz (zero offset vs. 0.10 V offset). At 500 Hz, both controllers perform comparably.

The choice between both controllers depends on the application requirements. The PD controller is recommended for applications where simplicity, low computational cost, and low output ripple are the primary concerns. The FCS-MPC is recommended for applications where disturbance rejection, fast transient response, and inherent constraint handling are critical, even at the cost of higher computational complexity and slightly higher ripples.

7. General Conclusions

The quadratic buck converter exhibits a fourth-order transfer function with a pole at the origin (natural integrator), weakly damped dominant poles ($\zeta \approx 0.172$), and zeros near the imaginary axis ($\zeta \approx 0.047$). The natural integrator eliminates the need for integral action, justifying a PD structure ($K_i = 0$) that avoids double integration instability. This finding is generalizable to any plant with a natural integrator.

Starting from conservative values ($K_p = 0.01$, $K_d = 0$), the iterative tuning process increased gains until the specifications were met. The final gains ($K_p = 0.08$, $K_d = 0.008$) yielded a settling time of 4.2 s and overshoot of 4.8%, meeting the requirements ($t_s < 5$ s, $M_p < 5\%$). Derivative action filtering ($D_f(s) = (K_d \cdot s) / (\tau \cdot s + 1)$ with $\tau = 0.01$ s) was essential to mitigate high-frequency noise; a reduced τ (0.003 s) demonstrated a significantly faster

disturbance rejection. A scaling factor of 10^{10} was applied to avoid numerical precision issues due to coefficients up to 10^{18} .

The PD controller cannot inherently enforce current limits, requiring external protection circuits. Disturbance rejection is modest (load and input steps recover in ~ 0.5 s). However, its main advantages are structural simplicity, low computational complexity (two multiplications and one addition per sampling period), and straightforward manual tuning. It is ideal for cost-sensitive applications with modest dynamic requirements.

The PD controller was intentionally tuned with a conservative approach ($K_p = 0.08$, $K_d = 0.008$) to prioritize stability and to minimize overshoot (4.8%), resulting in a deliberately slow settling time of 4.2 s. This conservative tuning is inherent to classical fixed-gain controllers when applied to weakly damped systems ($\zeta \approx 0.172$). By contrast, the FCS-MPC achieves a settling time below 5 ms with only 2% overshoot, not because of aggressive tuning, but due to its predictive nature, which anticipates future errors and selects the optimal switching state in real time. This three-orders-of-magnitude improvement is not an artifact of simulation, but a direct consequence of the fundamentally different control philosophies: reactive error correction (PD) versus proactive model-based prediction (FCS-MPC). The experimental results on load steps (2 ms recovery) and input voltage variations (2 ms recovery) confirm that the FCS-MPC operates at the physical limits imposed by the output filter ($L_2 C_2$, $\tau \approx 220 \mu\text{s}$), validating the practical feasibility of this speed improvement.

The FCS-MPC computes optimal switching actions in real time by minimizing a multi-objective cost function. The weights ($\alpha = 15$ for output voltage regulation, $\beta = 3$ for intermediate voltage, $\gamma = 200$ for i_{L1} overcurrent, $\delta = 150$ for i_{L2} overcurrent, $\varepsilon = 0.02$ for switching smoothness) prioritize voltage accuracy while enforcing safety constraints. Unlike the PD controller, this predictive approach eliminates manual tuning and adapts to changing operating conditions.

The FCS-MPC achieves a settling time below 5 ms and an overshoot of only 2% ($800\times$ faster than the PD). For load steps (0.5Ω to 1.0Ω) and input voltage variations (48 V to 43 V), the output voltage deviates by ± 0.15 V and ± 0.10 V, respectively, recovering in less than 2 ms ($250\times$ faster than the PD). At 100 Hz disturbances, the output remains perfect at 5.00 V; at 500 Hz, a small ripple of 0.08 V (1.6%) appears but the average remains 5.00 V. This superior performance is attributed to predictive action (anticipating disturbances), direct switching (no PWM delay), high output voltage weight ($\alpha = 15$), and a $10 \mu\text{s}$ sampling time.

The cost function's quadratic penalty terms enforce the current limits without external circuits: i_{L1} never exceeds 5 A and i_{L2} never exceeds 15 A, even under transients. This eliminates external protection circuits, reducing complexity and cost. The initial inductors ($L_1 = 33 \mu\text{H}$, $L_2 = 47 \mu\text{H}$) produced a 305% current increment (9.85 A), making accurate prediction impossible. Increasing both to $330 \mu\text{H}$ reduced the increment to 30.5% (0.985 A), ensuring prediction accuracy. This highlights the critical need to match the discrete-time model resolution to converter dynamics for successful MPC implementation.

Both controllers meet the ripple specifications: v_{C2} ripple below 0.5% (25 mV), i_{L1} below 15% (0.51 A), i_{L2} below 10% (1.0 A). The PD controller achieves a lower output ripple (0.2% vs. 0.4%) due to fixed switching frequency and constant duty cycle. The simulation and experimental results agree within 0.2% for voltage and 0.3% for ripple; minor discrepancies are attributed to parasitic elements (ESR, DCR), diode forward voltage drops, measuring noise, and oscilloscope calibration within acceptable limits ($<5\%$).

The FCS-MPC offers superior dynamic performance ($800\times$ faster settling, $250\times$ faster recovery) and inherent constraint handling at the cost of higher computational resources (TMS320F280049C) and an accurate system model. The PD controller is simpler, requires less computational power, and is adequate for modest performance requirements. Therefore, the FCS-MPC is recommended for high-performance systems demanding fast re-

sponse, robustness, and safety (electric vehicles, aerospace, precision power supplies), while the PD remains suitable for cost-sensitive applications with slower dynamics.

Beyond the comparative analysis between the PD and FCS-MPC, this work demonstrates a synergistic hardware–control co-design as its main contribution. The initial prototype ($L_1 = 33 \mu\text{H}$, $L_2 = 47 \mu\text{H}$) was inadequate for the FCS-MPC because the current increment per sampling period (9.85 A, 305% of nominal) made accurate prediction impossible. This limitation forced a hardware redesign, increasing both inductances to $330 \mu\text{H}$, which reduced the current increment to 0.985 A (30.5% of nominal), ensuring prediction fidelity. Notably, this hardware improvement also benefited the PD controller, improving its steady-state ripple performance (0.2% vs. 0.5% specification). This bidirectional synergy where control requirements drive hardware design, and improved hardware enhances control performance is the true contribution of this work, beyond the standard PD vs. MPC comparison commonly found in the literature.

Future work may explore the applicability of the proposed converter and control strategies in data center power distribution and photovoltaic microgrids, where 48 V DC buses are increasingly adopted.

Author Contributions: Conceptualization, R.A.A.R. and M.R.; methodology, J.R.G. and M.R. software, R.A.A.R.; validation, R.A.A.R. and J.R.G.; formal analysis, R.A.A.R.; investigation, R.A.A.R. and J.R.G.; resources, M.R.; data curation, R.A.A.R.; writing—original draft preparation, R.A.A.R.; writing—review and editing, R.A.A.R. and J.R.G.; visualization, R.A.A.R.; supervision, J.R.G.; project administration, J.R.G. and M.R. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by Electrical Machines and Drives (EM&D) at the Universidad Nacional de Colombia, Network for Cooperation on Energy Solutions for Communities, code: 59384.

Data Availability Statement: The data presented in this study are available on request from the corresponding author due to confidentiality agreements with the industrial facility where the measurements were obtained.

Conflicts of Interest: The authors declare no conflicts of interest.

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