

Article

AI-Assisted Multi-Physics Evaluation of Mission Profile-Based Traction Inverter Design for Sustainability

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Abstract

As the global transition toward carbon neutrality accelerates, the sustainability of power electronics has received growing attention from both academia and industry. Nevertheless, standardized methodologies for evaluating the sustainability of power electronic systems—particularly traction inverters—remain limited, largely due to the absence of comprehensive databases and unified assessment frameworks. Leveraging industrial extensive design experience, this paper presents an enhanced methodology for sustainability evaluation of traction inverters. The proposed framework combines advanced component-level modelling with multi-physics-based analysis to more accurately quantify the environmental impacts associated with different power semiconductor technologies. A Random Forest (RF)-based algorithm is employed for junction temperature (T_j) estimation, offering reliable thermal data crucial for sustainability assessment. Experimental validation on a prototype automotive inverter confirms the accuracy and robustness of the RF-based T_j estimation approach, ensuring realistic thermal–environmental coupling within the evaluation workflow. From a thermal perspective, the sizing of power electronics key components (PEKCs) is performed with high precision, enabling a more accurate estimation of power electronics-related material (PERM) usage. Combined with a preliminary CO₂-equivalent (CO₂e) emissions database, this allows sustainability assessment to be integrated directly into the design stage of the traction inverter. The effectiveness of the proposed approach is demonstrated through a comparative evaluation of three representative inverter topologies.

Keywords: traction inverter; multiphysics design; sustainability; carbon footprint; mission profile; AI assisted; random forest



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1. Introduction

The global energy crisis is becoming increasingly severe, highlighting the urgent need for sustainable transportation solutions [1]. In this context, electric vehicles (EVs) offer significant advantages over conventional internal combustion engine vehicles, primarily by reducing dependence on fossil fuels and minimizing carbon dioxide (CO₂) emissions. As a critical component of EV powertrains, the traction inverter plays a fundamental role in converting direct current (DC) energy from the battery into alternating current (AC) energy required by the electric machine. The advancement of high-voltage power electronics technology, which is one of core technologies for EV traction inverters, has facilitated extensive research on various traction inverter topologies over the past decade, with a focus on improving efficiency, reliability, and performance [2–4].

However, the deployment of advanced power electronics technologies also raises sustainability concerns [5–7], largely attributable to the materials used in their manufacture,

referring to PERM. A typical power electronics system incorporates multiple components, each contributing to its overall environmental footprint. The power semiconductor, as the primary functional unit, is composed of semiconductor materials, copper, aluminum, and ceramics [8,9]. The DC-link capacitor stabilizes the voltage and reduces current ripple to ensure reliable inverter operation [10]. In addition, copper busbars—particularly laminated DC busbars—provide the critical electrical interface between the DC-link capacitor and the power semiconductor [11–13]. The production of these components inevitably results in greenhouse gas (GHG) emissions, including CO₂, highlighting the importance of systematic sustainability assessment. Moreover, end-of-life treatment and the growing volume of E-waste [14] introduce further environmental challenges that must be addressed.

Recent research on power electronics sustainability has primarily focused on two areas: improving converter performance [15,16], and promoting the recycling or reuse of PERM [6,7,17]. Current optimization efforts mainly aim to enhance specific converter attributes—such as efficiency and reliability—to achieve higher performance without increasing the consumption of PERM. In addition, [17] integrates “R-design strategies” and circular economy principles into the development of power semiconductor devices in pursuit of net-zero carbon goals, while Refs. [6,7] investigate recycling pathways for PERM. However, strategies for reducing PERM consumption at the design stage, particularly through the appropriate sizing of PEKCs, have received limited attention in existing literature.

Based on a thermal perspective, this paper presents a systematic traction-inverter design methodology that integrates a multi-physics power electronics framework with artificial intelligence (AI) for sizing PEKCs. Instead of estimating only the mean T_J using AI [18–20], the proposed RF-based approach computes T_J while capturing thermal transients induced by both switching-frequency events and the AC fundamental frequency. This method replaces the computationally intensive portions of full finite-element simulations, requiring only thermal-network extraction, thereby reducing computational effort and dependency on hardware resources. On the other hand, the proposed approach integrates the concept of carbon footprint—grounded in the ecological footprint framework established by Rees and Wackernagel at the University of British Columbia in 1990—to quantify the CO₂e associated with PEKC selection during inverter design. The mission profile of the traction inverter determines the thermal loading of each PEKC, which directly influences material usage and thus the resulting CO₂e. As summarized in [21], power semiconductors and their cooling systems, DC-link capacitors, and busbars constitute the major PEKCs that dominate traction-inverter cost and volume, and therefore account for the largest share of PERM consumption. For this reason, these three components are the primary focus of the present study.

Using this methodology, different traction inverter architectures—including multi-phase topologies [22–24] and flying-capacitor-based configurations [25–27]—are evaluated. By quantifying and comparing their respective carbon footprints, this study offers insights into the environmental implications of various power electronics technologies and supports the development of more sustainable traction inverter solutions. These findings contribute to a deeper understanding of sustainability within power electronics and support future innovation toward environmentally responsible EV powertrain design.

The remainder of this paper is organized as follows. Section 2 presents the proposed PEKC design methodology, including analysis examples and experimental validation illustrating the mission-profile impact on CO₂e. Section 3 reports CO₂e assessment results for three representative inverter topologies, highlighting their influence on traction inverter sustainability. Section 4 concludes the paper and discusses potential directions for future research.

2. Proposed Design Methodology

Figure 1 presents the proposed methodology for traction inverter CO₂e ($CO_2e_{inverter}$) evaluation including copper busbar CO₂e (CO_2e_{Busbar}), power semiconductor CO₂e (CO_2e_{PS}) and Capacitor CO₂e (CO_2e_{Cap}). For a given inverter topology and mission profile, the required electrical and thermal specifications of the individual PEKC are generated as shown in Figure 1.

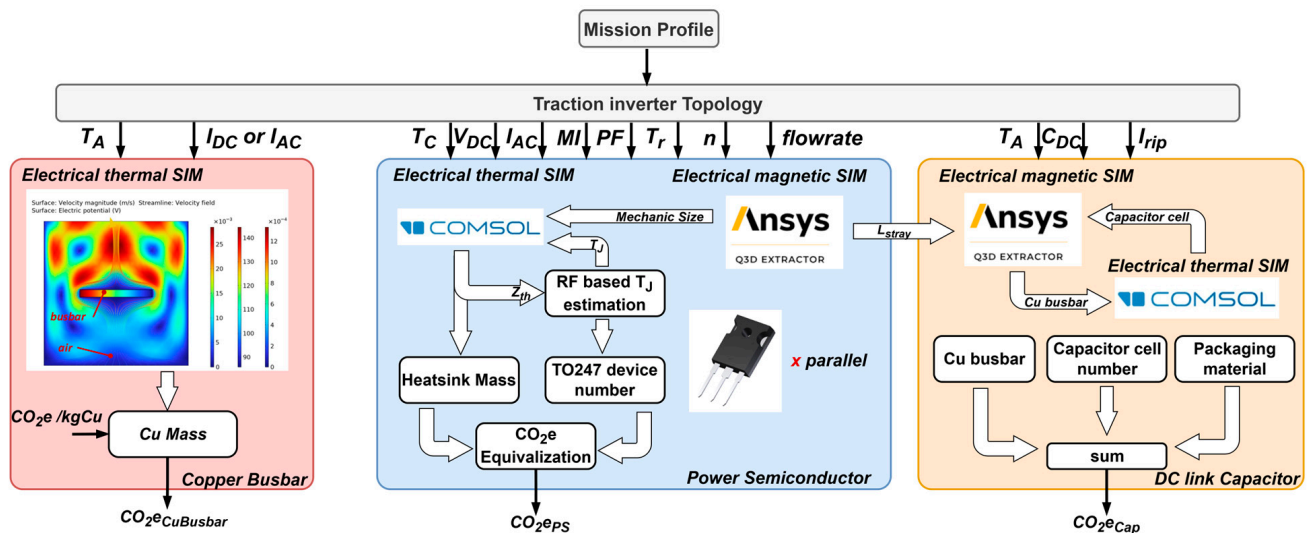


Figure 1. Proposed design methodology: traction inverter considering busbar, power semiconductor and DC-link Capacitor.

For copper busbars, the ambient temperature T_A extracted from the mission profile, together with the RMS value of traction inverter AC output current (I_{AC}) and the DC-link current (I_{DC}), serves as a key design input for both AC and DC busbar analysis. Electrical–thermal–fluid simulation in COMSOL 6.2 is performed to determine the minimum busbar volume that satisfies the thermal limits listed in Table 1. By multiplying the resulting copper volume by the material density and its CO₂e-per-kg value, the CO_2e_{Busbar} is obtained.

Table 1. Thermal limitations for Busbar, Power Semiconductor and DC-link Capacitor.

Component	Maximum Allowed Temperature (degC)
Busbar	100
Power Semiconductor T_J	150
DC-link capacitor temperature	100

A similar workflow is applied to power semiconductor and the DC-link capacitor. In this case, the evaluation processes of these two components are interdependent due to the influence of stray inductance (L_{stray}). Iterative simulations between Ansys Q3D and COMSOL 6.2 (similar electrical thermal simulation as busbar) are performed to determine the required capacitor cell number, internal busbar layout, and packaging material volume in accordance with the thermal constraints listed in Table 1 and key parameters that are derived based on mission profile and topology include T_A , capacitance C_{DC} -based DC-link voltage ripple V_{DCrip} , and equivalent series resistance (ESR) based on DC-link ripple current I_{rip} . Using the CO₂e-per-kg data of the relevant materials, the CO_2e_{Cap} is then calculated.

Unlike busbars [28] and DC-link capacitors [29–31], whose electrical characteristics exhibit a relatively linear dependence on temperature, the T_J of power semiconductor devices shows pronounced nonlinear behaviour. T_J is strongly influenced by six inverter-operating

parameters—including machine speed (n), torque (T_r), power factor (PF), modulation index (MI), DC-link voltage (V_{DC}), and switching frequency (f_{sw})—as well as the thermal impedance network of the power module [32–34]. To address this nonlinearity and reduce the computational effort required by physics-based thermal models, an RF-based approach is employed [35,36]—RF-based T_j estimation (Figure 1). A TO-247 discrete package is adopted in this study to avoid bias toward any proprietary module design and to demonstrate the generality of the methodology. Multiple TO-247 devices may be paralleled to emulate high-power module operation. Apart from V_{DC} , n , T_r , MI , PF , I_{AC} , coolant temperature T_C and flowrate are also critical information that can be extracted from mission profile. L_{stray} analysis with Ansys Q3D launch a limitation mechanic size for COMSOL 6.2 simulation. Using the proposed multi-physics simulation framework combined with the AI-based T_j estimation, the heatsink size, which is dominated by thermal impedance from junction to coolant (Z_{th}), and the required number of TO-247 devices are determined, enabling computation of CO_2e_{PS} . More details will be presented in Section 2.3.

The following subsections provide mission profile-dependent CO_2e evaluation results for copper busbars, power semiconductor, and DC-link capacitors, illustrating the critical role of the mission profile in sustainability assessment considering three-phase two-level traction inverter topology.

2.1. Copper Busbars

As shown in Figure 1, an electro–thermal–fluid simulation is carried out in COMSOL 6.2 by incorporating natural convection heat transfer in air, including the effect of gravity. The thermal boundary condition is set to an ambient temperature of $T_A = 85$ degC, and laminar flow is selected for the fluid model. Figure 2a illustrates the copper busbar thermal performance under two different I_{AC} s—550 A_{rms} and 200 A_{rms} at T_A of 85 degC. Under identical thermal constraints, increasing I_{AC} to 550 A_{rms} causes the busbar temperature to reach 100 degC within only 16 s. For a mission profile requiring 550 A_{rms} over 16 s, the copper busbar volume must be increased (assuming an unchanged cooling condition) to maintain the temperature within allowable limits, highlighting the strong impact of the mission profile on busbar sizing. Figure 2b presents the corresponding CO_2e_{Busbar} under two mission profiles: 16 s/400 A_{rms} and 180 s/400 A_{rms} . Sustaining 400 A_{rms} for 180 s results in a CO_2e_{Busbar} of 100 g by using a preliminary CO_2e -per-kg value of 1.6 kg-per-kg copper. In contrast, when the duration is reduced to 16 s, CO_2e_{Busbar} drops to 45 g. These results underscore that the mission profile is a critical design input and must be considered when assessing the sustainability of traction inverter components.

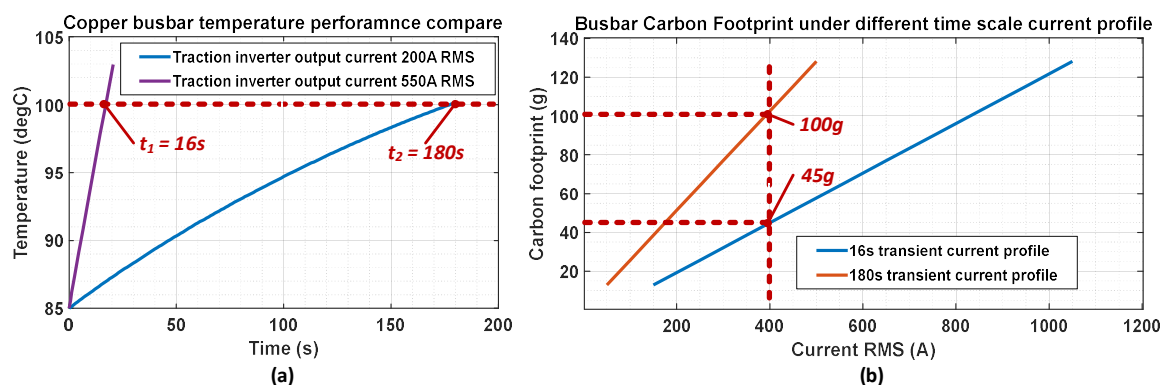


Figure 2. (a) Busbar temperature rises, with two I_{AC} s: 550 A_{rms} and 200 A_{rms} . (b) CO_2e_{Busbar} with 16 s and 180 s with 400 A_{rms} I_{AC} .

2.2. DC-Link Capacitor

Two ripple-current conditions are considered in this evaluation: $I_{rip} = 300 A_{rms}$ and $I_{rip} = 232 A_{rms}$, both at an T_A of 85 degC. Simulation in COMSOL 6.2 adopts the same setting as copper busbar. During the analysis, the internal busbar configuration, the number of DC-link capacitor cells, and the overall capacitor module size are adjusted to satisfy the thermal limits specified in Table 1. In addition, the total stray inductance contributed by the DC-link capacitor is constrained to remain below a certain limitation, for instance 15 nH, in accordance with the reverse-bias safe operating area (RBSOA) requirements of the selected power semiconductor devices. The thermal simulation results for the two ripple-current levels are shown in Figure 3. To ensure that the maximum internal temperature of the DC-link capacitor remains below 100 degC, a higher I_{rip} necessitates the use of additional capacitor cells, thereby increasing the total capacitor volume. Considering the three primary material contributors—copper busbar, film-based capacitor cells, and packaging material (e.g., resin)—the corresponding CO₂e results are summarized in Figure 4, using preliminary CO₂e-per-kg values for each component. It can be observed that a higher I_{rip} leads to an increased CO_2e_{Cap} , with the packaging materials contributing the largest share of the total emissions.

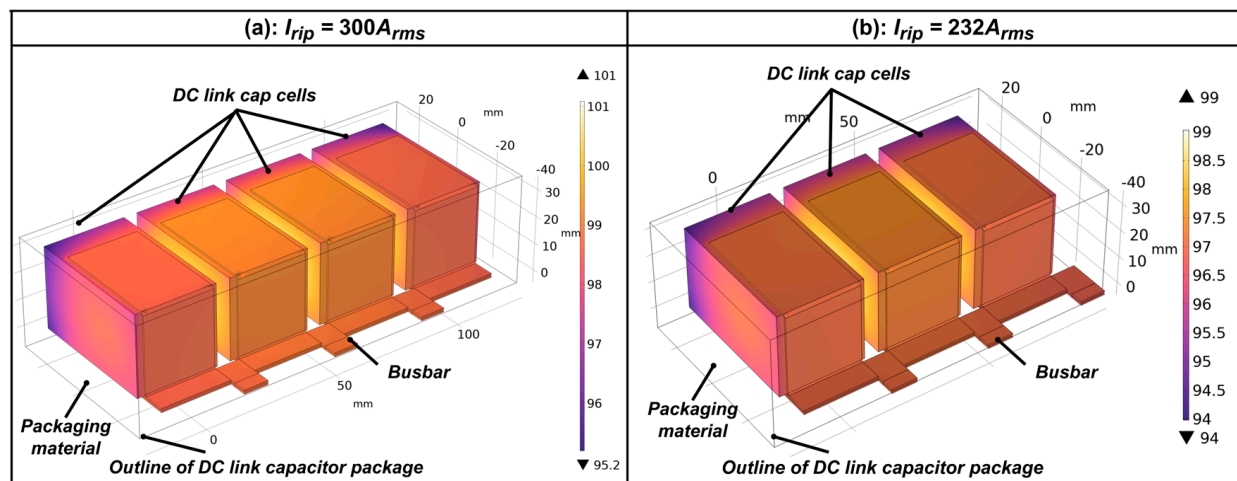


Figure 3. Thermal simulation under different I_{rip} s. (a) $I_{rip} = 300 A_{rms}$. (b) $I_{rip} = 232 A_{rms}$.

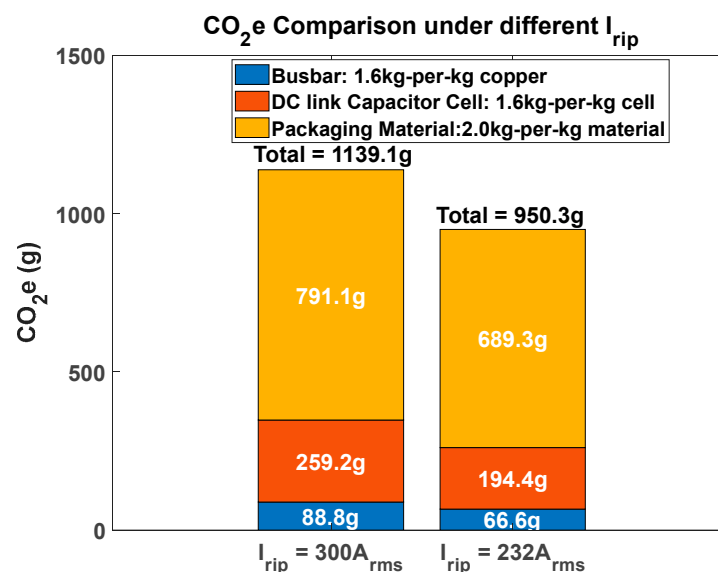


Figure 4. CO_2e_{Cap} under different I_{rip} s: $I_{rip} = 300 A_{rms}$ and $I_{rip} = 232 A_{rms}$.

2.3. Power Semiconductor

A power semiconductor package typically includes multiple materials such as copper, ceramic substrates, solder or sintered layers, and silicone gel [17]. As no public CO₂e database exists for these materials, this study simplifies the assessment by estimating only the number of TO-247 devices, using it as a representative indicator of the total CO₂e contribution from all internal packaging materials. Figure 5 illustrates the proposed method for incorporating TO-247 devices into the sustainability evaluation framework. L_{stray} extracted from Ansys Q3D imposes design constraints on d_{HL} , d_{HW} , d_1 , and d_2 . Iterative analysis is then performed between COMSOL 6.2 (thermal-fluid transient simulation for Z_{th} extraction) and the RF-based T_j estimation to determine both the required heatsink mass by obtaining proper d_{HL} , d_{HW} , d_1 , and d_2 [37] and the number of TO-247 devices.

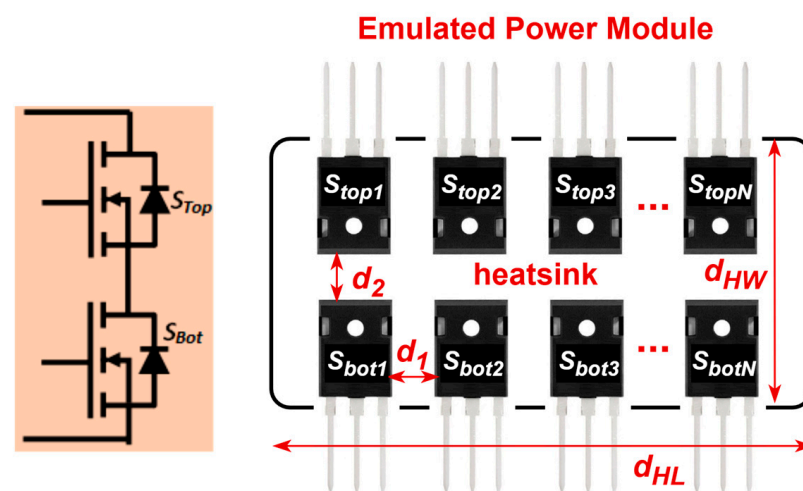
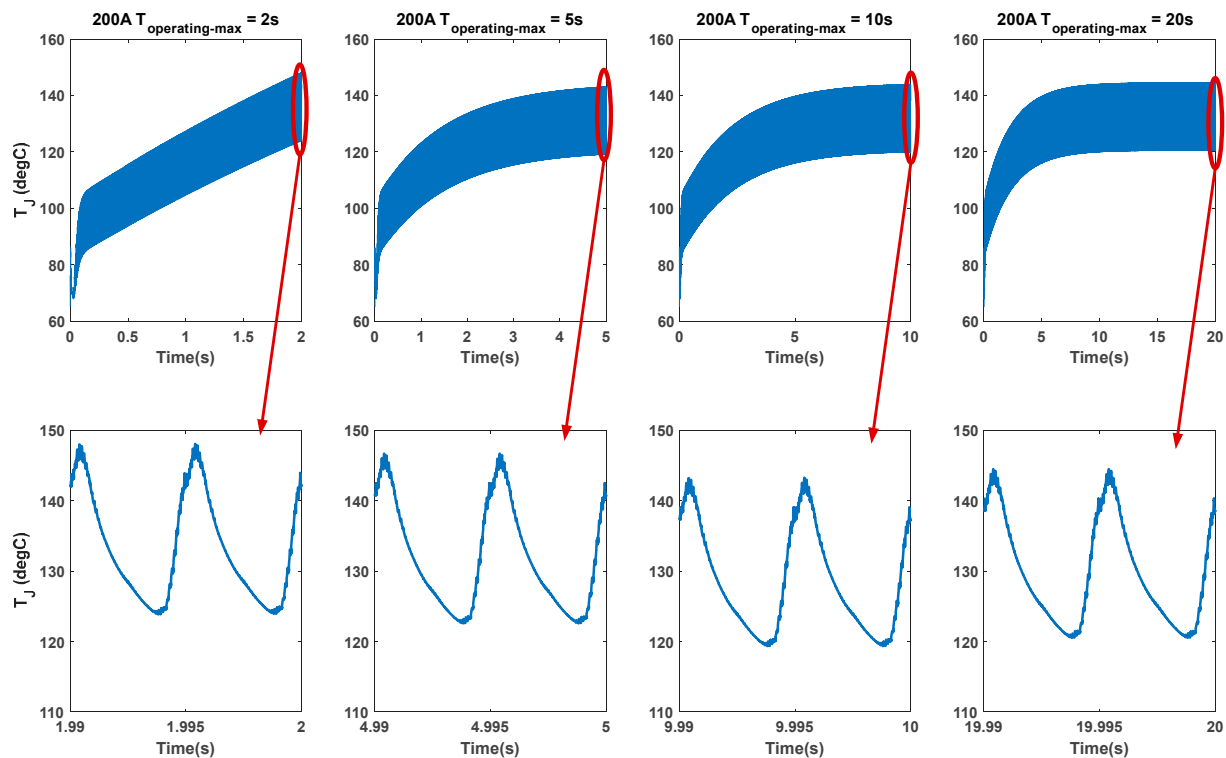


Figure 5. Analysis approach by using parallel TO247 to emulate high current power module.

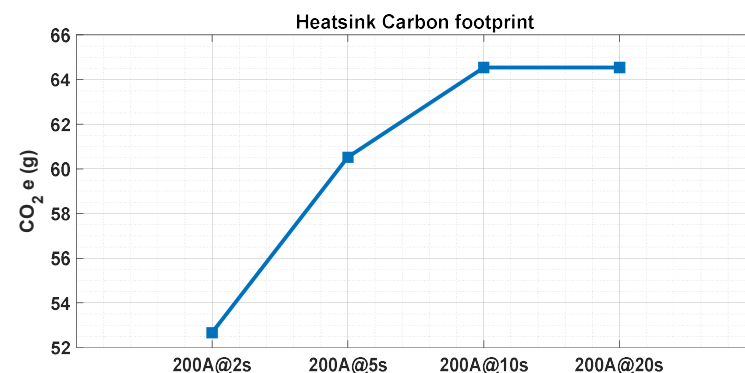
Based on the mission profiles in Table 2, the heatsink size is adjusted according to the maximum operating duration ($T_{operating_max}$, 2–20 s) to balance thermal resistance, thermal capacitance, and L_{stray} . Two SiC MOSFETs (E3M0016120K) are connected in parallel, with T_j limits specified in Table 1. Smaller heatsinks exhibit lower thermal capacitance, causing a faster rise in T_j and making them unsuitable for longer $T_{operating_max}$. For example, at $I_{AC} = 200 A_{rms}$ and $T_{operating_max} = 2$ s in Figure 6, a compact heatsink with smaller spacing d_1 is used, reducing thermal capacitance but increasing thermal coupling among parallel devices, which accelerates T_j rise. For $T_{operating_max} = 5$ s, the original thermal management is insufficient to maintain $T_j < 150$ degC. Increasing the spacing to $d_1 = 15$ mm enhances thermal capacitance, slows the T_j rise, mitigates thermal coupling, and reduces the effective thermal resistance. For $T_{operating_max} = 2$ s and 5 s, T_j remains in the transient regime and does not reach steady state. When $T_{operating_max}$ is extended to 10 s and 20 s, T_j begins to approach steady state as indicated by Figure 6, as the operating duration exceeds the system's thermal time constant, determined by the interaction of thermal capacitance and resistance. Remaining in the transient regime necessitates a larger heatsink to manage the thermal load, which adversely affects cost efficiency and power density.

Table 2. Evaluation details for four mission profiles— $V_{DC} = 800$ V.

Operating Points	Parallel	d_1 (mm)	d_2 (mm)	Heatsink W $\times$ L (mm)
$I_{AC} = 200$ A _{rms} $T_{operating_max} = 2$ s	2	5	20	67 $\times$ 92
$I_{AC} = 200$ A _{rms} $T_{operating_max} = 5$ s	2	15	20	77 $\times$ 92
$I_{AC} = 200$ A _{rms} $T_{operating_max} = 10$ s	2	20	20	82 $\times$ 92
$I_{AC} = 200$ A _{rms} $T_{operating_max} = 20$ s	2	20	20	82 $\times$ 92

**Figure 6.** T_{Js} of SiC (T_{JSiC}) with four mission profiles in Table 2 with 10 L/min and 65 degC coolant.

Since the number of parallel-connected devices is constant across the mission profiles in Table 2, the CO₂e contribution from the power semiconductors remains unchanged. However, the heatsink's CO₂e varies, as shown in Figure 7. As $T_{operating_max}$ increases, CO₂e of heatsink rises. At $T_{operating_max} = 20$ s, heatsink CO₂e saturates, which means that a trade-off between cost, power density, and thermal design is required. Increasing the spacing d_1 between parallel devices reduces thermal coupling but also increases CO₂e due to the additional copper material needed.

**Figure 7.** Power module Heatsink CO₂e under four different mission profiles listed in Table 2.

2.4. AI-Assisted Power Semiconductor T_J Calculation

In practical engineering design, mission profiles are usually far more complex than the simplified cases in Table 2. Table 3 provides a representative example that includes acceleration and regenerative braking with varying speed n and torque T_r . Running such detailed profiles entirely in software environments (e.g., PLECS or Simulink) is computationally demanding and becomes increasingly time-consuming for long-duration or multi-scenario studies.

Table 3. One typical mission profile of traction inverter design.

Time (s)	Torque (p.u.)	Speed (RPM)	Time (s)	Torque (p.u.)	Speed (RPM)
0.05	0.36	69	6.91	0.54	7353
0.08	0.65	88	6.93	0.43	7322
0.09	0.67	13	6.99	0.26	7226
0.10	0.67	0	7.12	0.06	7191
0.12	0.67	75	7.19	0.00	7170
0.17	0.67	103	7.24	−0.04	7148
4.58	0.67	5044	7.31	−0.11	7107
5.41	0.67	5961	7.44	−0.19	7031
5.82	0.63	6376	7.49	−0.19	7012
6.28	0.58	6808	7.86	−0.33	6727
6.8	0.55	7261	10	−0.33	4773

Based on the discrete power semiconductor devices illustrated in Figure 5, an RF-based T_J estimation methodology is proposed, as shown in Figure 8a, to accelerate the T_J calculation process. $[n, T_r, V_{DC}, f_{sw}, PF, MI]$ is generated considering mission profile and inverter topologies are provided as inputs for the RF model to estimate the real-time power losses of power semiconductors, together with Z_{th} for both the top and bottom switches (S_{Top} and S_{Bot}), as illustrated in Figure 5. Depending on the coolant flowrate, coolant temperature T_C , and the selected discrete device, the Z_{th} —including $(R_{T1}–R_{TN}, C_{T1}–C_{TN})$ for S_{Top} and $(R_{B1}–R_{BN}, C_{B1}–C_{BN})$ for S_{Bot} —are adjusted accordingly to represent different thermal boundary conditions. By using estimated $[P_{top}, P_{bot}]$, $[T_{Jtop}, T_{Jbot}]$ is generated with Z_{th} .

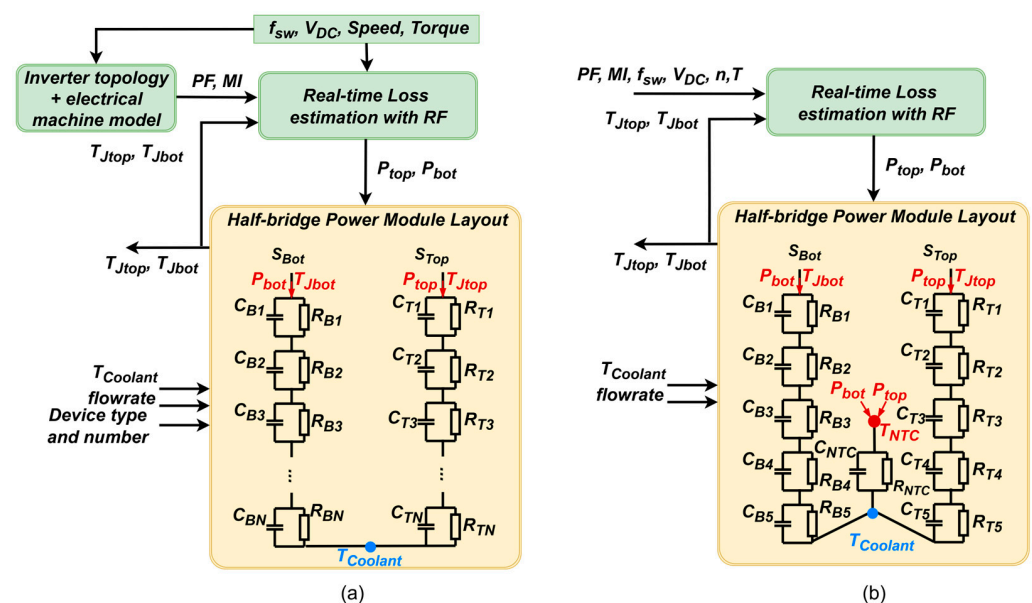


Figure 8. (a) Proposed RF-based T_J estimation method architecture. (b) Experimental validation diagram based on proposed method shown in (a).

For a selected discrete power semiconductor, the switching loss data (E_{on} and E_{off}) and conduction loss data ($R_{DS(on)}$) can be obtained either from the datasheet or through double-pulse testing. Following the procedure illustrated in Figure 9, RF can then be trained. For a given mission profile and selected semiconductor device, both f_{sw} and Z_{th} can be decided for the first step. The parameters n , T_r , V_{DC} , PF , and MI can be varied within the rated design range to generate multiple datasets— $[n, T_r, V_{DC}, f_{sw}, PF, MI, T_J]$ vs. $[P_{top}, P_{bot}]$ —without going through the entire mission profile. These datasets can be automatically produced using PLECS simulations or mathematical models of different inverter topologies implemented in Python (version 3.14.2). By fixing f_{sw} at 10 kHz and Z_{th} of the selected power semiconductor, other parameters are sampled based on the following discrete points: V_{DC} varies from 50 V to 1000 V with a step size of 50 V; n ranges from 0 to 10,000 rpm with a step size of 100 rpm; T_r varies from 0 p.u. to 1 p.u. with an increment of 0.1 p.u. PF and MI are generated from n , T_r , and V_{DC} using mission profile and topology. The T_J varies from 0 degC to 200 degC with a step size of 25 degC. This parameter discretization strategy effectively reduces the training workload for the RF model, while maintaining sufficient data diversity to ensure robust T_J calculation across varying operating conditions.

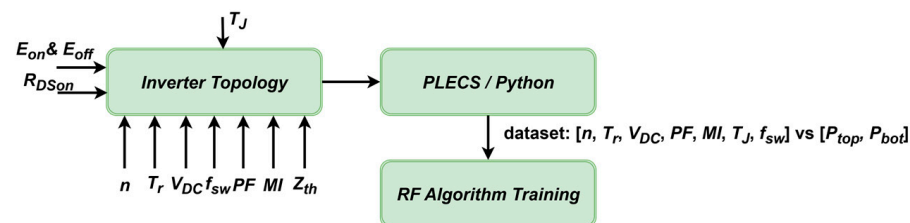


Figure 9. Training data generation process for the selected RF algorithm.

2.5. Experimental Validation

The accuracy of the proposed RF-based T_J calculation approach was experimentally validated under the mission profile specified in Tables 3 and 4—**Test Profile**. The experimental setup and measurement platform are depicted in Figure 10, including a three-phase two-level SiC-based inverter, electrical machine emulator and environmental chamber, with corresponding system capability detailed in Table 4—**Test Platform**. To enable real-time T_J estimation, the RF is deployed to predict the output vector $y_o = [P_{top}, P_{bot}]^T$ using the input vector $u_{in} = [n, T, V_{DC}, f_{sw}, PF, MI, T_J]$ as shown in Figure 8b. The RF model selected here consists of 20 decision trees ($T = 20$), each with a maximum depth of $D = 5$. The input dimension D_{in} and outputs dimension D_{out} is 7 and 2, respectively, considering u_{in} and y_o . Each decision tree recursively partitions the input space based on learned thresholds of selected features. A non-leaf node stores a feature index, a threshold value, and two child pointers, while each leaf node stores the output vector corresponding to D_{out} .

Table 4. Hardware test platform and test condition.

Test Platform		Test Profile	
Parameter	Value	Parameter	Value
V_{DC}	0.5–1 kV	V_{DC}	690 V
f_{sw}	2–15 kHz	f_{sw}	10 kHz
T_C	25–85 degC	T_C	40 degC
flowrate	1–15 L/min	flowrate	6 L/min
Torque	–500–500 NM	T_A	35 degC
Speed	0–20 k RPM		
Power	500 kW max		

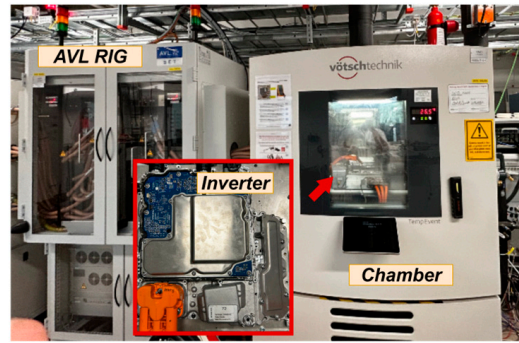


Figure 10. Experimental validation hardware platform for proposed AI-assisted T_j estimation.

Total nodes of RF can be derived as follows:

$$N_{total} = T(2^{D+1} - 1) = 1260 \quad (1)$$

Leaves per tree can be calculated as follows:

$$N_{leaves} = T2^D = 640 \quad (2)$$

Total parameter number is derived as follows:

$$N_{paraRF} = N_{total} + D_{out}N_{leaves} = 2540 \quad (3)$$

The total memory footprint is 9.92 kB in float32 format, which is non-trivial to manage in resource-constrained embedded controllers. Considering a typical traction inverter micro controller unit, such as the Infineon AURIX™ TC3xx series operating at a clock frequency of 300 MHz, which results in floating-point multiply–accumulate (MAC) computational time $T_{MAC} = 5/300$ MHz, the estimated computation time for one time inference is as follows:

$$T_{RF} \approx (TD + T)T_{MAC} = 2\mu s \quad (4)$$

The RF model achieves a single-inference latency of 2 μs , meeting the real-time requirements of power electronic controllers, which typically operate with millisecond-level control cycles (e.g., $f_{sw} = 10$ kHz). **Real-time Loss estimation with RF** (Figure 8b) outputs, $[P_{top}, P_{bot}]$, serve as inputs for the subsequent real-time T_j calculation for one half bridge using the proposed structure depicted in Figure 8b. The T_j of the SiC devices ($[T_{jtop}, T_{jbot}]$) are derived based on $[P_{top}, P_{bot}]$. The top-switch Foster thermal network, consisting of $R_{T1}–R_{T5}$ and $C_{T1}–C_{T5}$, is extracted through testing using a T3ster system or via simulation [38], while the bottom-switch network ($R_{B1}–R_{B5}$ and $C_{B1}–C_{B5}$) is obtained via a similar method. The NTC temperature (T_{NTC}) inside the power module is also estimated to provide a reference for validating the proposed method, since direct measurement of the SiC T_j is not feasible after inverter assembly. Furthermore, the foster network parameters are affected by coolant flowrate and T_c , as discussed in [39]. A virtual thermal network is constructed to estimate T_{NTC} as shown in Figure 8b. Based on transient FEM simulations, the thermal impedance from the NTC to coolant is defined as $Z_{NTC}(t) = (T_{NTC}(t) - T_c(t))/(P_{top} + P_{bot})$, assuming simultaneous heating from both top and bottom switches. This assumption is justified by the sensor's location near the lateral midpoint between the two switches. By fitting the impedance response [40], the corresponding thermal resistance R_{NTC} and capacitance C_{NTC} are extracted.

The validation results are presented in Figure 11, together with the corresponding residuals and R^2 values. Since direct measurement of SiC T_j is not feasible once the

power module is integrated into the inverter, only T_{NTC} can be experimentally measured. Therefore, the first step is to compare the measured T_{NTC} with the T_{NTC} obtained from the PLECS simulation. The strong agreement between $T_{NTCTest}$ and $T_{NTCPLECS}$ reflected by an R^2 of 0.9454, confirms that the simulated T_J (T_{JPLECS}) accurately represents the actual thermal behaviour during testing. The T_{NTC} estimated by the proposed RF-based method (" T_{NTCRF} ") also aligns closely with both $T_{NTCTest}$ and $T_{NTCPLECS}$, achieving R^2 values of 0.8591 and 0.9477, respectively. In addition, T_J estimated by the RF (T_{JRf}) demonstrates excellent accuracy, with less than 5 degC deviation from T_{JPLECS} and an R^2 of 0.9977, indicating an equivalent error level relative to the tested T_J . These results collectively verify the feasibility and reliability of the proposed method for accurate T_J estimation under real operating conditions.

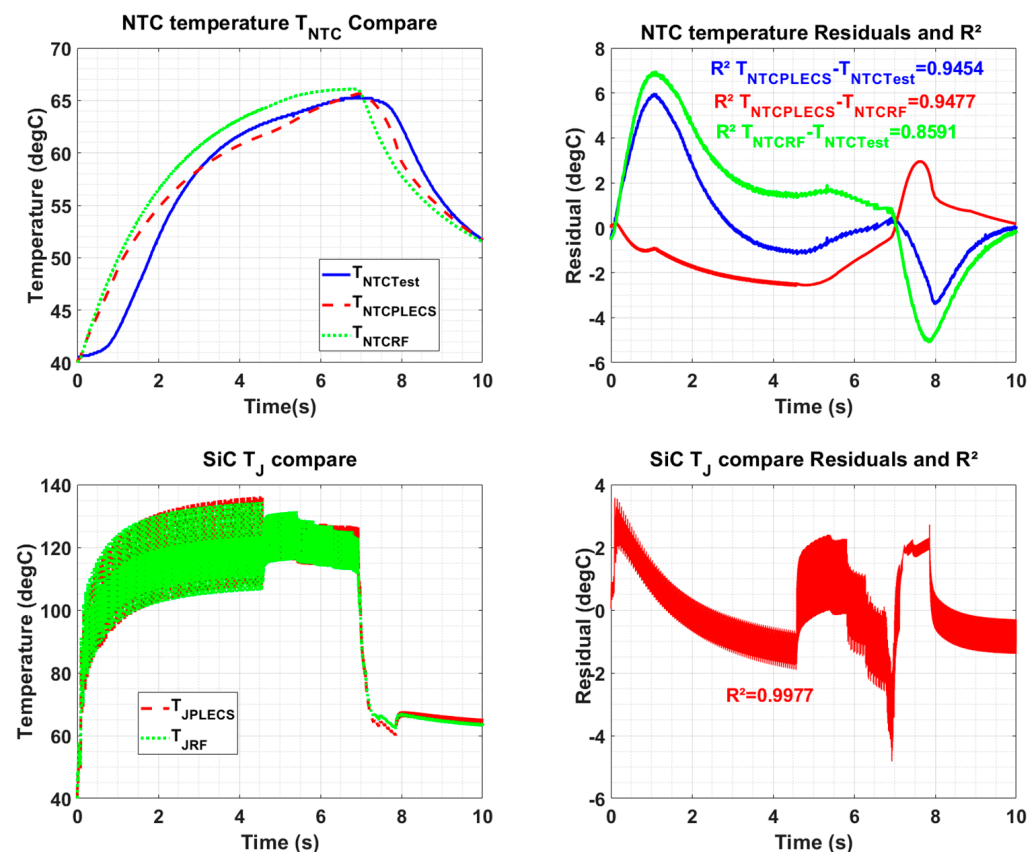


Figure 11. Experimental validation results for RF-based T_J estimation by using Table 3 test profile.

3. Analysis Examples

The design methodology described in Section 2 is applied to assess the CO₂e impact of three traction inverter topologies, as shown in Figure 12: the conventional three-phase two-level inverter, the flying-capacitor inverter, and the six-phase two-level inverter. In the schematic, red traces indicate internal busbar connections, green traces represent DC-link capacitor components, and black blocks denote power semiconductor. The mission profile used for the sizing and CO₂e evaluation is provided in Tables 3 and 4 (Test Profile). Power semiconductor CO₂e estimation follows the procedure outlined in Figure 8a.

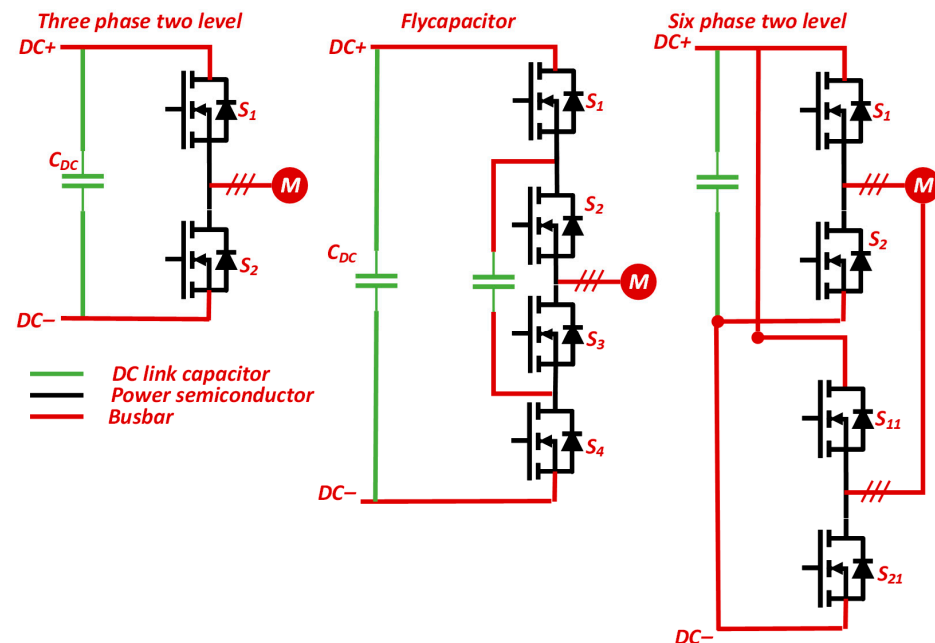


Figure 12. Three traction inverter topologies—three-phase two-level, fly capacitor, and multiphase—6 phase.

Following the procedure in Figure 1, the CO_2e of busbars for the three inverter topologies was estimated. The flying-capacitor and six-phase two-level topologies were normalized against the conventional three-phase two-level inverter, which is set as the 100% reference, by using $CO_2e_{Busbar} \text{—flying capacitor} / CO_2e_{Busbar} \text{—three-phase two-level}$, $CO_2e_{Busbar} \text{—six-phase two-level} / CO_2e_{Busbar} \text{—three-phase two-level}$, respectively. DC-link capacitor follows the same approach. Figure 13a shows that the flying-capacitor inverter shows the highest CO_2e for both components due to the additional flying capacitors required. The six-phase topology exhibits a slightly higher busbar CO_2e but achieves the lowest DC-link capacitor CO_2e among the three configurations.

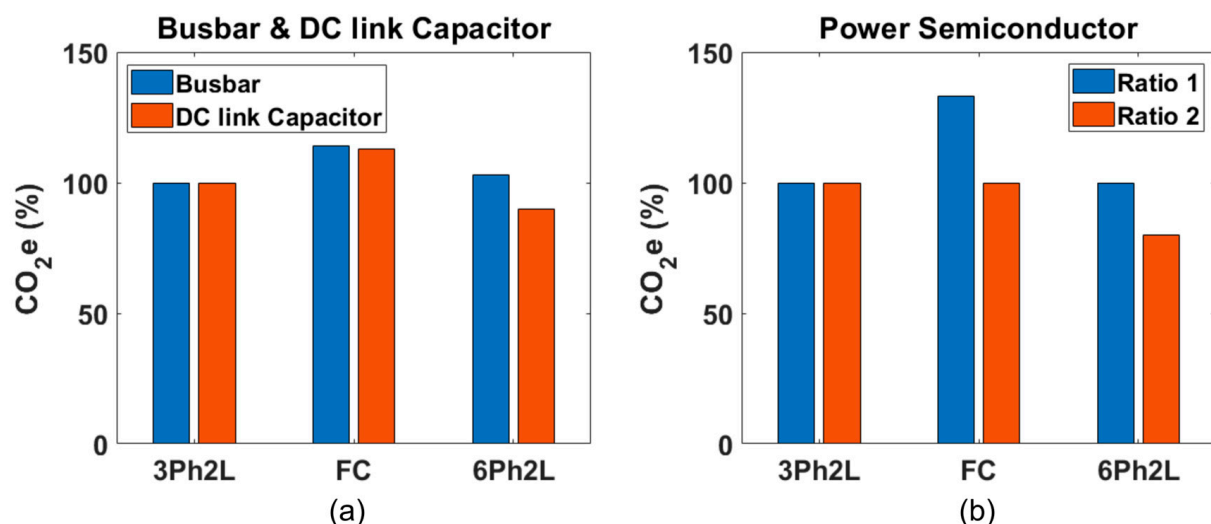


Figure 13. CO_2e comparison regarding (a) Busbar and DC-link capacitor (b) power semiconductor considering three-phase two-level (3Ph2L), fly capacitor (FC), and six-phase two-level (6Ph2L).

Figure 13b presents the CO_2e associated with power semiconductor under two estimation scenarios, due to the lack of publicly available CO_2e data for power module manufacturing. The assessment is based on the energy consumption of SiC die fabrication,

with the device types summarized in Table 5. Manufacturing a 1.2 kV die typically requires $\sim 1.5\text{--}2\times$ the energy of a 650 V die, while a 125 A die requires $\sim 1.6\text{--}2.5\times$ the energy of a 67 A die. Accordingly, Ratio 1 assumes scaling factors of 1.5 (voltage) and 1.6 (current), whereas Ratio 2 assumes 2.0 and 2.5.

Table 5. Power semiconductor voltage and current rating for three topologies.

	Three-Phase Two-Level	Flying Capacitor	Six-Phase Two-Level
Device Part Number	E3M0016120K	C3M0015065K	E3M0032120K
Device Voltage	1.2 kV	650 V	1.2 kV
Device Current (25 degC)	125 A	120 A	67 A

Taking Ratio 1 as an example, since the current ratings of the SiC devices are nearly identical, the voltage rating dominates the energy consumption for die fabrication. The energy for the flying-capacitor topology is estimated as $1.5 \times (\text{number of SiC devices in flying-capacitor topology}) \div (\text{number of SiC devices in three-phase two-level})$. A similar approach is applied to the six-phase two-level topology, focusing on the impact of current rating. based on Figure 13b, under Ratio 1, the flying-capacitor inverter exhibits the highest semiconductor-related CO₂e, while the three-phase and six-phase inverters show similar levels. Under Ratio 2, the six-phase topology achieves the lowest CO₂e, whereas the three-phase and flying-capacitor inverters yield comparable, higher CO₂e values.

4. Conclusions

This paper presents an AI-assisted, multi-physics-based methodology for evaluating the sustainability of traction inverters by focusing on PEKCs, including power semiconductor, busbars, and DC-link capacitors. The mission profile is incorporated as a critical design input—together with the selected inverter topology—due to its strong impact on PEKC thermal loading and, consequently, on CO₂e performance. To enhance computational efficiency, an RF-based T_J estimator is introduced to accurately predict T_J under a wide range of operating conditions. The RF model effectively captures the nonlinear interactions between electrical variables, thermal dynamics, and mission-profile variations, enabling substantial acceleration of the thermal evaluation process. Experimental validation shows that the proposed RF-based estimator achieves an accuracy within ± 5 degC compared to reference measurements, confirming its suitability for sustainability-oriented power electronics design workflows.

A key challenge identified during the analysis is the absence of a unified CO₂e database for power electronics materials, particularly for power semiconductors, which combine copper, ceramics, solders, encapsulants, and semiconductor materials. Establishing such a database will require coordinated efforts between industry and academia to ensure transparency and consistency in sustainability assessments. The thermal-driven design methodology proposed in this work also lays the foundation for integrating additional perspectives into future multi-objective sustainability evaluations, including thermo-mechanical fatigue, reliability, lifetime, and manufacture, as well as cost, and can also be extended to other traction inverter topologies, such as T type neutral clamp and I type neutral clamp. These extensions will further enhance the comprehensiveness and practical relevance of sustainability assessment frameworks for next-generation traction inverters.

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