

Article

Active Neutral-Point Voltage Balancing Strategy for Single-Phase Three-Level Converters in On-Board V2G Chargers

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Abstract

Driven by the rapid advancement of Vehicle-to-Grid (V2G) and Grid-to-Vehicle (G2V) technologies, improving power quality and system stability during charging and discharging has become a research focus. To address this, this paper proposes a Model Predictive Control (MPC) strategy for Active Neutral-Point Voltage Balancing (ANPVB) in a single-phase three-level converter used in on-board V2G chargers. Traditional converters rely on passive balancing using redundant vectors, which cannot ensure neutral-point (NP) voltage stability under sudden load changes or frequent power fluctuations. To solve this issue, an auxiliary leg is introduced into the converter topology to actively regulate the NP voltage. The proposed method avoids complex algorithm design and weighting factor tuning, simplifying control implementation while improving voltage balancing and dynamic response. The results show that the proposed Model Predictive Current Control-based ANPVB (MPCC-ANPVB) and Model Predictive Direct Power Control-based ANPVB (MPDPC-ANPVB) strategies maintain the NP voltage within ± 0.7 V, achieve accurate power tracking within 50 ms, and reduce the total harmonic distortion of current (THDi) to below 1.89%. The proposed strategies are tested in both V2G and G2V modes, confirming improved power quality, better voltage balance, and enhanced dynamic response.

Keywords: electric vehicles; vehicle-to-grid; grid-to-vehicle; neutral-point voltage balance; single-phase three-level converters; model predictive control



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1. Introduction

With the global transition of energy structures and growing awareness of environmental protection, electric vehicles (EVs) have become an innovative alternative to traditional fuel vehicles. According to the Global EV Outlook 2025 released by the International Energy Agency (IEA) [1], global electric car sales exceeded 17 million in 2024, accounting for more than 20% of new vehicle sales. China remains the largest market, contributing over 60% of global EV sales and hosting around 65% of public charging points. In contrast, growth in Europe and the United States has slowed due to reduced subsidies and unchanged emissions targets. These trends highlight the increasing importance of EV infrastructure. As the interface between EVs and the grid, the on-board charger (OBC) plays a critical role in determining charging efficiency and system reliability. It is responsible for converting grid-side alternating current (AC) into direct current (DC) suitable for charging the traction battery, and has thus become a major focus of ongoing research.

The OBC mainly consists of a front-stage AC/DC conversion and a rear-stage DC/DC conversion [2]. The front-stage AC/DC circuit performs power factor correction (PFC) and voltage conversion. It ensures that the input current remains synchronized with the grid voltage and reduces harmonic pollution to the grid. The rear-stage DC/DC circuit adjusts the DC voltage from the front stage to match the needs of the battery. It also provides electrical isolation and charging control. With the deep integration of smart grids and electric vehicles, OBCs are shifting from unidirectional charging to bidirectional energy exchange. V2G refers to discharging energy from the EV battery back to the grid to support peak shaving and frequency regulation. G2V represents the conventional charging process from the grid to the vehicle. These bidirectional energy flow modes place stricter requirements on the front-end converter of the OBC. First, the bidirectional flow of energy requires the converter to support power transfer in both directions. Second, grid connection standards require high-quality current waveforms and good PFC performance from the converter [3].

Compared with traditional two-level topologies, multilevel topologies, especially three-level topologies, have clear advantages. The total DC bus voltage is divided among multiple switching devices. This division reduces the voltage stress and the voltage change rate on each device. As a result, harmonic generation decreases, and the cost of passive filters is lowered [4,5]. At the same time, the three-level structure produces lower output voltage distortion. It also improves the THDi, enhancing overall power quality.

Although the three-level topology has many advantages, some problems still remain. First, it needs more power semiconductor devices, which increases the cost. Second, because the DC link is split, the NP voltage imbalance can degrade system performance. If a voltage imbalance occurs between the upper and lower DC-link capacitors, the output voltage waveform becomes distorted. Extra harmonic components may appear. Some devices may be exposed to excessive voltage stress. These problems reduce system efficiency and reliability [6].

The control strategy plays an important role in both V2G and G2V modes [7]. There are many control strategies for single-phase converters. Proportional-Integral (PI) control is a commonly used method. However, when the grid frequency drifts, tracking error increases, especially under dynamic scheduling in V2G applications [8]. Proportional-Resonant (PR) control may increase noise peaks in the system's output spectrum. This often makes it difficult to meet grid connection standards [9,10]. Repetitive control is a steady-state control method derived from the internal model principle, enabling the output waveform to accurately follow the periodic reference signal. However, its main drawback is slow dynamic response. These methods are often not suitable for complex power electronic systems with multiple variables and constraints [11]. Super-Twisting Sliding Mode Control offers fast response and strong disturbance rejection. However, it requires many parameters and repeated trial-and-error tuning [12,13]. In recent years, MPC has been widely studied in the field of power electronics. As a feedforward optimization control method, it can achieve multi-objective control while meeting system constraints [14]. To address the NP voltage balancing problem, an effective method is to embed proper weighting factors into the cost function [15].

Although MPC provides multi-objective optimization capability, the selection of multiple weighting factors and its stability analysis still involve many uncertainties. In most cases, weighting factors are selected based on experience [16,17], yet they play a critical role in shaping the performance of power electronic controllers. Therefore, eliminating weighting factors entirely is a better way to reduce their influence on the control system. Reference [18] determines the voltage imbalance by evaluating the output current tracking error, which avoids directly sampling the voltages of the two capacitors. This reduces sys-

tem cost and complexity. However, it may be difficult to detect faults in time if components fail. Reference [19] presents a sliding mode control approach that independently regulates the capacitor voltage and inductor current to their respective reference values, thus eliminating the need for weighting coefficients. However, this method is not suitable for single-phase three-level converters. Reference [20] avoids the use of weighting coefficients by forcing all control objectives to converge within a bounded invariant set. However, its strategy is too complex. These approaches focus solely on control methods and often involve complicated procedures.

To address this problem, a dedicated voltage balancing circuit can be added at the hardware level. Reference [21] proposed a voltage balancing circuit with flying capacitors for a diode-clamped five-level converter. This circuit achieved fast balancing of the DC-side capacitor voltages and stabilization of the NP voltage. However, its complex structure increases hardware cost, and the state machine control adds to the complexity of the control strategy. Some three-level inverter topologies inherently provide self-balancing of capacitor voltages. In the scheme of [22], a hybrid Cuk-Sepic DC-DC stage is used at the front end, which can automatically balance its two output voltages. As a result, the inverter's performance is not affected by NP voltage imbalance. The approach in [23] uses a switched capacitor module, which connects split capacitors in parallel when outputting the semi-DC loop voltage to achieve voltage balancing. However, this method is only applicable to specific circuit topologies and lacks general applicability.

Traditional three-level converters rely on passive balancing strategies, which adjust the NP current direction by using the redundancy of switching vectors. However, this strategy is limited in effectiveness under the frequently changing load conditions typical of OBCs. To address this problem, this study proposes an improved solution by adding a third leg to the single-phase three-level topology. By actively controlling the third leg, the NP current can be directly regulated, thereby dispensing with the need for complex control algorithms and the use of weighting factors. This significantly enhances the stability and response speed of NP voltage balancing.

The remainder of this paper is organized as follows. Section 2 provides a detailed introduction to the mathematical model of the single-phase three-level topology. Section 3 discusses the mathematical model of the third leg and the active NP voltage balancing method. Section 4 verifies the proposed strategy through results and analysis. Section 5 presents the conclusion of this paper.

2. Mathematical Model

The topology of a single-phase three-level converter with three legs is illustrated in Figure 1. The variable u_{dc} denotes the DC bus voltage on the EV side, which typically originates from the traction battery and the DC-DC converter. A current i_f is injected into the midpoint of the DC bus via two power switches, T_1 and T_2 , and an inductor L_f . This balancing leg is responsible for regulating or balancing the voltages U_{c1} and U_{c2} across the upper and lower DC bus capacitors, C_1 and C_2 , respectively. The central part of the circuit is a single-phase three-level converter composed of two bridge legs, A and B. The corresponding switching devices are $S_{a1} \sim S_{a4}$ and $S_{b1} \sim S_{b4}$. The midpoint of the DC capacitors, denoted as point O , serves as the DC-side NP and enables three-level voltage output. On the AC side, the output is connected through an LC filter consisting of an inductor L_s and capacitor C_s , along with an AC voltage source e . The variables i_L and i_s represent the current through the filter inductor and the current on the AC side, respectively.

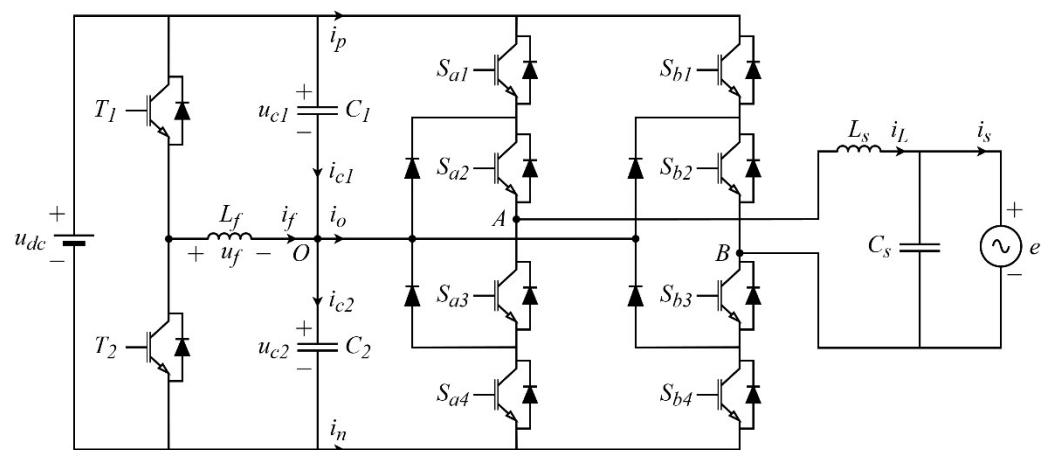


Figure 1. Topology of a single-phase three-level converter with three legs.

The single-phase three-level converter topology includes two main inverter legs. Each leg consists of four switching devices and two clamping diodes, and supports three distinct switching states, defined as $S_i \in \{1, 0, -1\}$, where $i \in \{A, B\}$. The detailed switching combinations for each state are presented in Table 1.

Table 1. Switch States of Each Leg.

S_i	S_{i1}	S_{i2}	S_{i3}	S_{i4}
1	on	on	off	off
0	off	on	on	off
-1	off	off	on	on

Based on the defined switching states, a total of nine distinct voltage vectors can be derived for the converter. The converter's operating characteristics corresponding to various switching states are summarized in Table 2.

Table 2. Operating States and Voltage Vectors of the Single-Phase Three-Level Converter.

State	S_a	S_b	i_o	u_{ab}	Vectors
0	1	1	0	0	u_0
1	1	0	$-i_L$	u_{c1}	u_1
2	1	-1	0	$u_{c1} + u_{c2}$	u_2
3	0	1	i_L	$-u_{c1}$	u_3
4	0	0	0	0	u_4
5	0	-1	i_L	u_{c2}	u_5
6	-1	1	0	$-(u_{c1} + u_{c2})$	u_6
7	-1	0	$-i_L$	$-u_{c2}$	u_7
8	-1	-1	0	0	u_8

Under ideal conditions, it is typically assumed that the voltages across the upper and lower DC-side capacitors, C_1 and C_2 , in a single-phase three-level converter, are balanced. However, in practical operation, these two voltages are often not exactly equal. As a result, based on the switching states shown in Table 2, the terminal voltages can be expressed as functions of the switching and the capacitor voltages, as given below

$$u_{ao} = \frac{S_a(S_a + 1)}{2}u_{c1} - \frac{S_a(S_a - 1)}{2}u_{c2} \quad (1)$$

$$u_{bo} = \frac{S_b(S_b + 1)}{2}u_{c1} - \frac{S_b(S_b - 1)}{2}u_{c2} \quad (2)$$

$$u_{ab} = u_{ao} - u_{bo} = \left[\frac{S_a(S_a + 1)}{2} - \frac{S_b(S_b + 1)}{2} \right] u_{c1} - \left[\frac{S_a(S_a - 1)}{2} - \frac{S_b(S_b - 1)}{2} \right] u_{c2} \quad (3)$$

The power switches are assumed to operate under ideal conditions. During the commutation process, all switching devices are considered free of switching losses and energy storage. Based on this assumption, the instantaneous power on the AC side and the DC side is considered balanced, leading to

$$u_{ab}i_L = i_p u_{c1} - i_n u_{c2} \quad (4)$$

i_p represents the current flowing out of node p on the DC side, and i_n denotes the current flowing out from node n on the DC side.

Substituting Equation (3) into Equation (4), the comparison yields

$$i_p = \frac{S_a(S_a + 1) - S_b(S_b + 1)}{2} i_L \quad (5)$$

$$i_n = \frac{S_a(S_a - 1) - S_b(S_b - 1)}{2} i_L \quad (6)$$

Applying Kirchhoff's Current Law to the capacitors and their DC side gives the following equations

$$i_o = -(i_p + i_n) = -(S_a^2 - S_b^2) i_L \quad (7)$$

MPCC and MPFC Algorithms

In recent years, extensive research has been conducted on methods for generating virtual orthogonal components from single-phase signals. Common techniques include 90-degree phase shifting, the Hilbert transform, all-pass filters, and the Second-Order Generalized Integrator (SOGI) [24]. Among these, SOGI has emerged as a widely adopted method due to its structural simplicity, favorable dynamic characteristics, and strong capability to suppress harmonics and mitigate the effects of frequency deviations. Building upon this, the integration of SOGI with a Phase-Locked Loop (PLL) yields the SOGI-PLL structure, which further improves the accuracy of amplitude, phase, and frequency tracking. This configuration provides the necessary phase reference for implementing rotating coordinate transformations in single-phase systems [25].

As shown in Figure 2, the Second-Order Generalized Integrator (SOGI) processes the input signal $x(s)$ through an internal structure of integrators and feedback, generating a quadrature signal $x_\beta(s)$ with a 90° phase shift and equal amplitude to the in-phase signal $x_\alpha(s)$. The corresponding transfer functions of the SOGI in the s -domain are given as follows

$$\begin{cases} x_\alpha(s) = \frac{k\omega_n s}{s^2 + k\omega_n s + \omega_n^2} x(s) \\ x_\beta(s) = \frac{k\omega_n^2}{s^2 + k\omega_n s + \omega_n^2} x(s) \end{cases} \quad (8)$$

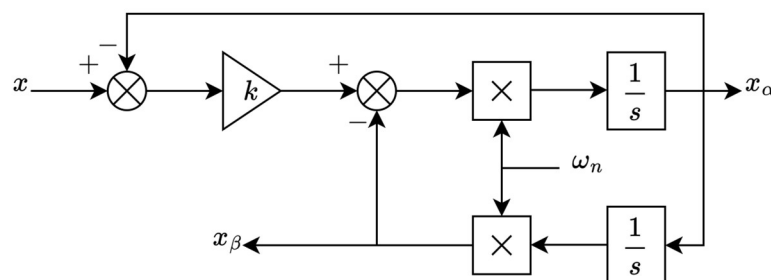


Figure 2. Block diagram of the SOGI controller.

Here, ω_n denotes the angular frequency of the fundamental grid voltage, and k is the gain coefficient used to adjust the filtering level and dynamic response characteristics of the system to the input signal.

As shown in Figure 1, applying Kirchhoff's voltage law to analyze the voltage across the LC filter results in

$$L_s \frac{di_L}{dt} = u_{ab} - e - Ri_L \quad (9)$$

By applying Equation (8) separately to the grid-side voltage e and the inductor current i_L , the expressions for their rotating vectors of voltage and current are obtained as follows

$$\begin{cases} e_\alpha = e = E \cos(\omega t) \\ e_\beta = E \sin(\omega t) \end{cases} \quad (10)$$

$$\begin{cases} i_{L\alpha} = I_L \cos(\omega t - \varphi) \\ i_{L\beta} = I_L \sin(\omega t - \varphi) \end{cases} \quad (11)$$

In the above expressions, E and I_L represent the peak values of the grid-side voltage and the inductor current of L_s , respectively.

Substituting Equations (10) and (11) into Equation (9) yields

$$\begin{cases} L_s \frac{di_{L\alpha}}{dt} = u_\alpha - Ri_{L\alpha} - e_\alpha \\ L_s \frac{di_{L\beta}}{dt} = u_\beta - Ri_{L\beta} - e_\beta \end{cases} \quad (12)$$

After applying the Park transformation to the d-q rotating reference frame, the following expression is obtained

$$\begin{cases} L_s \frac{di_{Ld}}{dt} = u_d - e_d - Ri_{Ld} + \omega L_s i_{Lq} \\ L_s \frac{di_{Lq}}{dt} = u_q - e_q - Ri_{Lq} - \omega L_s i_{Ld} \end{cases} \quad (13)$$

Let the sampling period be T_s . By applying the forward Euler method to discretize (13), the MPCC expression can be obtained as follows

$$\begin{cases} i_{Ld}(k+1) = \frac{T_s}{L_s} [u_d(k) - e_d(k) + \omega L_s i_{Lq}(k)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Ld}(k) \\ i_{Lq}(k+1) = \frac{T_s}{L_s} [u_q(k) - e_q(k) - \omega L_s i_{Ld}(k)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Lq}(k) \end{cases} \quad (14)$$

Taking the leg current as the control target, the current cost function is defined as follows

$$J_1 = [i_{Ldref}(k+1) - i_{Ld}(k+1)]^2 + [i_{Lqref}(k+1) - i_{Lq}(k+1)]^2 \quad (15)$$

Based on the instantaneous power theory, the instantaneous active power P and reactive power Q of the single-phase converter in the synchronous rotating d-q reference frame can be expressed as follows

$$\begin{cases} P = \frac{1}{2}(e_d i_{Ld} + e_q i_{Lq}) \\ Q = \frac{1}{2}(e_q i_{Ld} - e_d i_{Lq}) \end{cases} \quad (16)$$

When the d-axis of the synchronous rotating d-q reference frame is aligned with the grid voltage vector e , it follows that $e_d = E$ and $e_q = 0$. Under this condition, Equations (14) and (16) can be simplified as follows

$$\begin{cases} i_{Ld}(k+1) = \frac{T_s}{L_s} [u_d(k) - E(k) + \omega L_s i_{Lq}(k)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Ld}(k) \\ i_{Lq}(k+1) = \frac{T_s}{L_s} [u_q(k) - \omega L_s i_{Ld}(k)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Lq}(k) \end{cases} \quad (17)$$

$$\begin{cases} P = \frac{1}{2} E i_{Ld} \\ Q = -\frac{1}{2} E i_{Lq} \end{cases} \quad (18)$$

The differentials of P and Q are given by

$$\begin{cases} \frac{dP}{dt} = \frac{1}{2} E \frac{di_{Ld}}{dt} \\ \frac{dQ}{dt} = -\frac{1}{2} E \frac{di_{Lq}}{dt} \end{cases} \quad (19)$$

Through the joint application of Equations (13), (18) and (19), the following expression is obtained

$$\begin{cases} \frac{dP}{dt} = \frac{1}{2L_s} u_d E - \frac{1}{2L_s} E^2 - \frac{R}{L_s} P - \omega Q \\ \frac{dQ}{dt} = -\frac{1}{2L_s} E^2 - \frac{R}{L_s} Q + \omega P \end{cases} \quad (20)$$

Discretizing Equation (20) using the forward Euler approach yields the mathematical formulation of MPDPC as shown below

$$\begin{cases} P(k+1) = T_s \left[\frac{1}{2L_s} u_d(k) E - \frac{1}{2L_s} E^2(k) - \omega Q(k) \right] + \left(1 - \frac{T_s R}{L_s} \right) P(k) \\ Q(k+1) = T_s \left[-\frac{1}{2L_s} E^2(k) + \omega P(k) \right] + \left(1 - \frac{T_s R}{L_s} \right) Q(k) \end{cases} \quad (21)$$

Taking the grid-side power as the control objective, the power cost function is defined as follows

$$J_2 = \left[P_{ref}(k+1) - P(k+1) \right]^2 + \left[Q_{ref}(k+1) - Q(k+1) \right]^2 \quad (22)$$

3. Model Predictive Control of Active NP Voltage Using the Third Leg

3.1. Operating Modes of the Third Leg

By controlling the switching devices of the third leg to turn on and off, appropriate charging strategies are applied to the upper and lower DC bus capacitors, enabling the balancing of the NP voltage. When the voltage across C_1 is higher, energy is transferred from C_1 to C_2 through the third leg; conversely, when the voltage across C_2 is higher, energy is transferred from C_2 to C_1 via the third leg, causing the voltage of C_1 to increase. Based on the switching states and the direction of the inductor current, there are six operating modes, as illustrated in Figures 3 and 4.

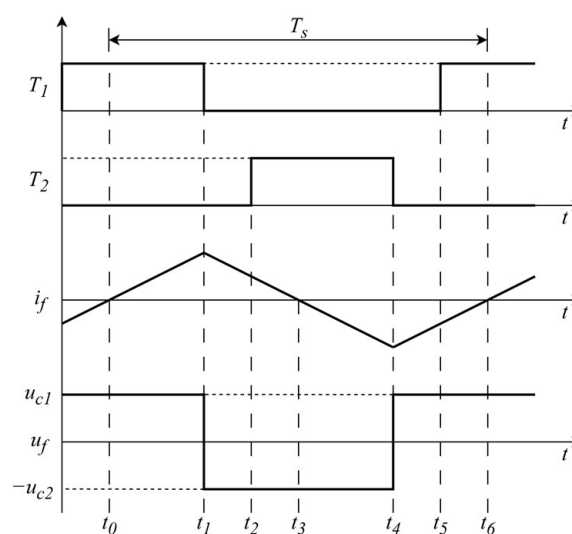


Figure 3. Voltage and current characteristics of the third leg during ANPVB.

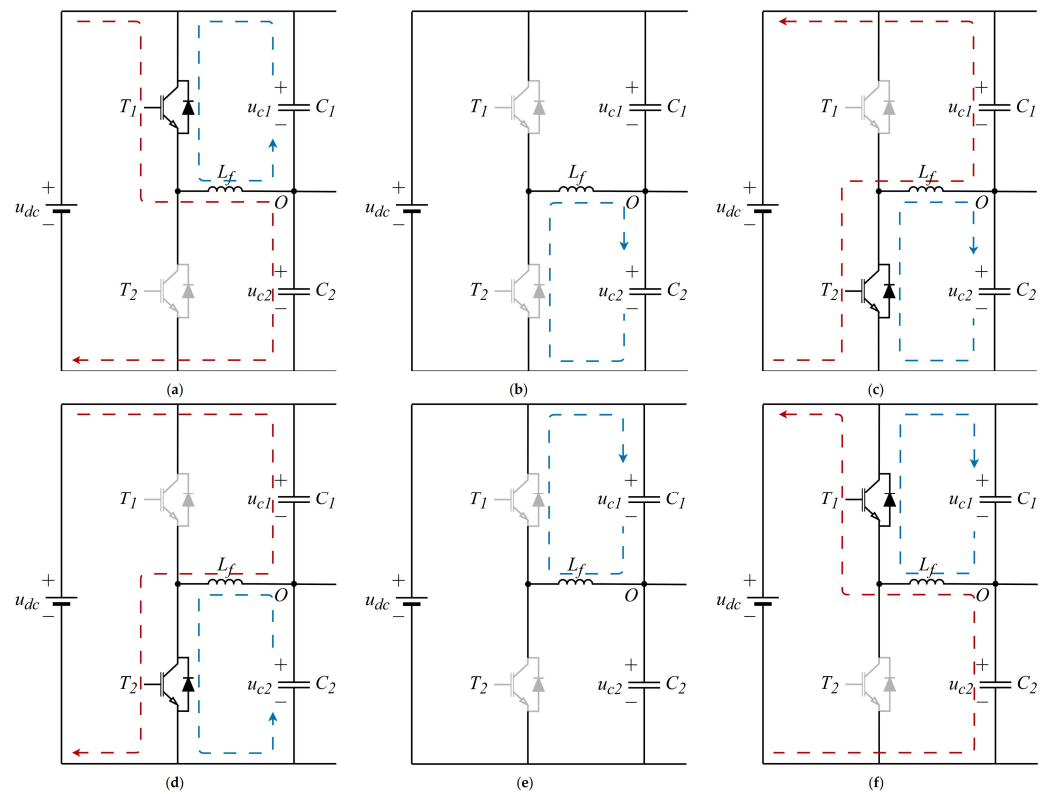


Figure 4. Switching States and Operating Modes of the Third Leg. (a) Mode 1. (b) Mode 2. (c) Mode 3. (d) Mode 4. (e) Mode 5. (f) Mode 6.

Mode 1: T_1 is turned ON while T_2 is turned OFF. This mode corresponds to the interval $t_0 - t_1$. The current i_f begins increasing from zero. A closed loop is formed by the DC bus voltage u_{dc} , T_1 , L_f , and C_2 , allowing the DC source to charge C_2 . Meanwhile, C_1 , T_1 , and L_f form another loop where C_1 charges L_f . The voltage across L_f equals u_{c1} , resulting in u_{c1} decreasing and u_{c2} increasing.

Mode 2: Both T_1 and T_2 are turned OFF during the interval $t_1 - t_2$. The current i_f remains positive and flows through a loop formed by C_2 , T_2 , and L_f . In this state, L_f charges C_2 , with the voltage across L_f being opposite to u_{c2} . Voltage u_{c2} increases.

Mode 3: T_1 is OFF and T_2 is ON in the interval $t_2 - t_3$. The current i_f remains positive. A loop is formed by u_{dc} , T_2 , L_f , and C_1 , where C_1 supplies energy to the DC bus. Simultaneously, C_2 , T_2 , and L_f form another loop that continues to charge C_2 . The voltage across L_f is opposite to u_{c2} , leading to a decrease in u_{c1} and an increase in u_{c2} .

Mode 4: During the interval $t_3 - t_4$, T_1 remains OFF and T_2 is ON. The current i_f becomes negative. The loop formed by u_{dc} , T_2 , L_f , and C_1 allows the DC source to charge C_1 . Meanwhile, C_2 , T_2 , and L_f form a loop where C_2 discharges into L_f . The voltage across L_f is opposite to u_{c2} . As a result, u_{c1} increases and u_{c2} decreases.

Mode 5: Both T_1 and T_2 are OFF during the interval $t_4 - t_5$, and i_f remains negative. A loop is formed by C_1 , T_1 , and L_f , where L_f charges C_1 . The voltage across L_f equals u_{c1} , resulting in an increase of u_{c1} .

Mode 6: T_1 is ON and T_2 is OFF during the interval $t_5 - t_6$. The current i_f remains negative. A loop formed by u_{dc} , T_1 , L_f , and C_2 allows C_2 to supply energy to the DC bus. At the same time, C_1 , T_1 , and L_f form a loop, where L_f continues to charge C_1 . The voltage across L_f equals u_{c1} , leading to an increase in u_{c1} and a decrease in u_{c2} .

3.2. Model Predictive Control of NP Voltage

Let the DC bus voltage be denoted as u_{dc} , and the NP voltage difference as u_o . Then, u_{dc} and u_o can be expressed as follows

$$\begin{cases} u_{dc} = u_{c1} + u_{c2} \\ u_o = u_{c2} - u_{c1} \end{cases} \quad (23)$$

The currents of the upper and lower capacitors on the DC bus can be expressed as

$$\begin{cases} i_{c1} = C_1 \frac{d[\frac{1}{2}(u_{dc}-u_o)]}{dt} \\ i_{c2} = C_2 \frac{d[\frac{1}{2}(u_{dc}+u_o)]}{dt} \end{cases} \quad (24)$$

The designed circuit employs $C_1 = C_2 = C$. Based on Kirchhoff's law, the circuit Equation for the third bridge arm is given by

$$i_f - i_o = i_{c2} - i_{c1} = C \frac{du_o}{dt} \quad (25)$$

$$u_f = L_f \frac{di_f}{dt} \quad (26)$$

By applying the forward Euler method to discretize Equations (25) and (26), the following expressions can be obtained

$$u_o(k+1) = \frac{T_s}{C} [i_f(k) - i_o(k)] + u_o(k) \quad (27)$$

$$i_f(k+1) = \frac{T_s}{L_f} u_f(k) + i_f(k) \quad (28)$$

Equation (28) provides the required expression for model predictive NP voltage control. From Figure 3, along with Equations (27) and (28), it can be seen that u_f is related to both the switching actions and i_f . The value of i_f at time step $k+1$ depends on u_f at time step k , while the predicted NP voltage difference u_o at $k+1$ depends on i_f at k , and is therefore independent of u_f at k . This indicates that Equation (27) alone cannot be used to control the NP voltage difference at $k+1$ through the switching action at k . To resolve this problem, a two-step prediction method is employed. Applying the two-step prediction to Equation (27) yields the following

$$u_o(k+2) = \frac{T_s}{C} [i_f(k+1) - i_o(k+1)] + u_o(k+1) \quad (29)$$

By substituting Equations (27) and (28) into Equation (29), the following expression is obtained

$$u_o(k+2) = \frac{T_s}{C} \left[\frac{T_s}{L_f} u_f(k) + i_f(k) - i_o(k+1) \right] + \frac{T_s}{C} [i_f(k) - i_o(k)] + u_o(k) \quad (30)$$

Taking the capacitor voltage difference as the control objective, the DC bus voltage balancing cost function is defined as follows

$$J_3 = [u_{oref}(k+2) - u_o(k+2)]^2 \quad (31)$$

The above method provides a theoretical basis for controlling a single-phase three-level three-leg converter. However, in practice, MPC algorithms inherently suffer from delay

issues. At the beginning of each sampling period, the processes of voltage and current sampling, reference acquisition, and the computational burden of the MPC algorithm consume significant processing time on the digital controller. This results in action delay, causing the predicted values to deviate from the reference values and degrading overall system performance. Therefore, delay compensation must be considered in the control algorithm. To mitigate this issue, this paper adopts a two-step prediction method to compensate for the delay-induced errors. The specific steps are as follows:

- (1) Sample the controlled variables at time step k .
- (2) Use the mathematical model to calculate the estimated values of i_{Ld} , i_{Lq} , e_d , e_q , i_f , u_o , P , and Q at time step $k + 1$.
- (3) Based on these estimates and the predictive model, calculate the predicted values of each voltage vector at time step $k + 2$, namely

$$\begin{cases} i_{Ld}(k+2) = \frac{T_s}{L_s} [u_d(k+1) - E(k+1) + \omega L_s i_{Lq}(k+1)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Ld}(k+1) \\ i_{Lq}(k+2) = \frac{T_s}{L_s} [u_q(k+1) - \omega L_s i_{Ld}(k+1)] + \left(1 - \frac{T_s R}{L_s}\right) i_{Lq}(k+1) \end{cases} \quad (32)$$

$$\begin{cases} P(k+2) = T_s \left[\frac{1}{2L_s} u_d(k+1) E(k+1) - \frac{1}{2L_s} E^2(k+1) - \omega Q(k+1) \right] + \left(1 - \frac{T_s R}{L_s}\right) P(k+1) \\ Q(k+2) = T_s \left[-\frac{1}{2L_s} E^2(k+1) + \omega P(k+1) \right] + \left(1 - \frac{T_s R}{L_s}\right) Q(k+1) \end{cases} \quad (33)$$

Since the NP voltage difference at time step $k + 2$ cannot be controlled directly by the switching actions at $k + 1$, it is necessary to predict the estimated value of u_o at $k + 2$

$$u_o(k+3) = \frac{T_s}{C} \left[\frac{T_s}{L_f} u_f(k+1) + i_f(k+1) - i_o(k+2) \right] + \frac{T_s}{C} [i_f(k+1) - i_o(k+1)] + u_o(k+1) \quad (34)$$

At this point, the expressions of the cost functions are given by

$$J_1 = [i_{Ldref}(k+2) - i_{Ld}(k+2)]^2 + [i_{Lqref}(k+2) - i_{Lq}(k+2)]^2 \quad (35)$$

$$J_2 = [P_{ref}(k+2) - P(k+2)]^2 + [Q_{ref}(k+2) - Q(k+2)]^2 \quad (36)$$

$$J_3 = [u_{oref}(k+3) - u_o(k+3)]^2 \quad (37)$$

- (4) Store the optimal predicted values, switching states, and i_o , which will serve as input data for the next sampling period.

The configuration of the proposed predictive control strategy is shown in Figure 5.

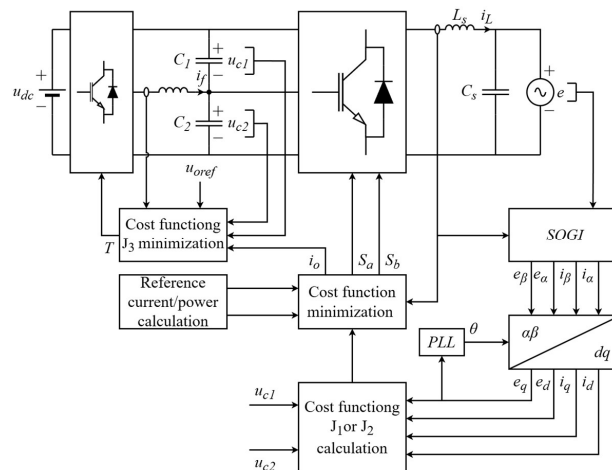


Figure 5. Block diagram of the proposed MPC-ANPVB strategy.

4. Results and Analysis

4.1. Parameter Selection

According to Kirchhoff's law, the current loop equation of the LC-type filter circuit can be expressed as

$$C_s \frac{de}{dt} = i_L - i_s \quad (38)$$

By combining Equations (9) and (38) and neglecting the grid-side load, the transfer function of the LC filter is obtained as

$$\frac{U_C(s)}{U_{ab}(s)} = \frac{1}{L_s C_s s^2 + R C_s s + 1} = \frac{\omega_L^2}{s^2 + 2\zeta \omega_L s + \omega_L^2} \quad (39)$$

The resonant angular frequency is given by $\omega_L = 1/\sqrt{L_s C_s}$, and the damping ratio is $\zeta = 1/2R\sqrt{C_s/L_s}$. It can be observed that the system is a second-order oscillatory system, and its cutoff frequency is

$$f_L = \frac{1}{2\pi\sqrt{L_s C_s}} \quad (40)$$

The current ripple of the output filter determines the minimum inductance value. Typically, the ripple current is selected as 20% of the peak output current under rated operating conditions.

$$\Delta I_{L\max} = \frac{\sqrt{2}P_{\max}}{E/\sqrt{2}} \times 20\% = \frac{2P_{\max}}{5E} \quad (41)$$

Let ΔI_L denote the inductor current ripple. According to Kirchhoff's law, the ripple current across the inductor is given by

$$\Delta I_L = \frac{u_{dc} - e}{L_s} \times \frac{D(t)}{f_s} \quad (42)$$

where $D(t)$ is the duty cycle and f_s is the switching frequency. Since the switching frequency is much higher than the grid frequency, it can be assumed that

$$e = D(t)u_{dc} \quad (43)$$

Substituting (43) into (42) yields

$$\Delta I_L = \frac{[D(t) - D^2(t)]u_{dc}}{f_s L_s} \quad (44)$$

The ripple current reaches its maximum when $D(t) = 0.5$, and can be expressed as

$$\Delta I_{L\max} = \frac{u_{dc}}{4f_s L_s} \quad (45)$$

By combining (41) and (45), the minimum filter inductance is given by

$$L_{s\min} = \frac{5u_{dc}E}{8f_s P_{\max}} \quad (46)$$

When the cutoff frequency is much lower than the switching frequency, harmonic suppression is most effective. Typically, the cutoff frequency f_L of the LC filter is selected

to be less than 1/10 of the switching frequency f_s . According to Equation (40), the filter capacitance should satisfy the following condition

$$C_s \geq \frac{1}{L_s \left(2\pi f_s \times \frac{1}{10} \right)^2} \quad (47)$$

According to the power conservation principle, the energy stored in the DC-link capacitor over one period is given by

$$W = \frac{P}{f} \quad (48)$$

Let f denote the grid frequency. The energy supplied by the filter capacitor in each cycle is given by

$$\frac{W}{2} = 2 \times \frac{C}{2} \left[u_{dc}^2 - (u_{dc} - \Delta u)^2 \right] \quad (49)$$

Here, Δu represents the ripple amplitude of the DC bus voltage, generally taken as 5% of the DC bus voltage. By combining Equations (48) and (49), we obtain

$$C = \frac{P}{2f(2u_{dc}\Delta u - \Delta u^2)} \quad (50)$$

The inductance of the third bridge leg can be designed with reference to the boost converter inductor. The inductance is calculated by the following formula

$$L_f > \frac{D(t)[1 - D(t)]^2 u_{dc}^2 T_s}{\eta P} \quad (51)$$

η is the current ripple coefficient, usually less than 1. When $D(t) = 1/3$, the right-hand side of the equation reaches its maximum value, that is

$$L_f > \frac{4u_{dc}^2 T_s}{27\eta P} \quad (52)$$

To verify the effectiveness and superiority of the proposed MPC-ANPVB strategy for the single-phase three-level converter, a detailed simulation study was conducted. The simulation parameters are summarized in Table 3. The proposed method was compared with the conventional MPCC, MPDPC, and PI-ANPVB strategies. The simulations were carried out using MATLAB/Simulink R2023b.

Table 3. Main parameters of the simulation.

Variable	Description	Value
L_s	Filter inductor	8 mH
C_s	Filter capacitor	6 μ F
C	DC-link capacitors	2100 μ F
R	Filter resistance	0.1 Ω
e	RMS of Grid voltage	220 V
u_{dc}	DC voltage	400 V
f	Grid frequency	50 Hz
f_s	Switching frequency	10 kHz

4.2. Comparative Analysis of Control Strategies

In the experimental setup, the active power reference was 5 kW from 0 to 0.3 s and -5 kW from 0.3 to 0.5 s, while the reactive power reference remained at 0 Var throughout.

NP voltage balancing was initiated at 0.1 s, and the system mode switched from V2G to G2V at 0.3 s. Performance comparisons of the five methods are presented in Figures 6–8.

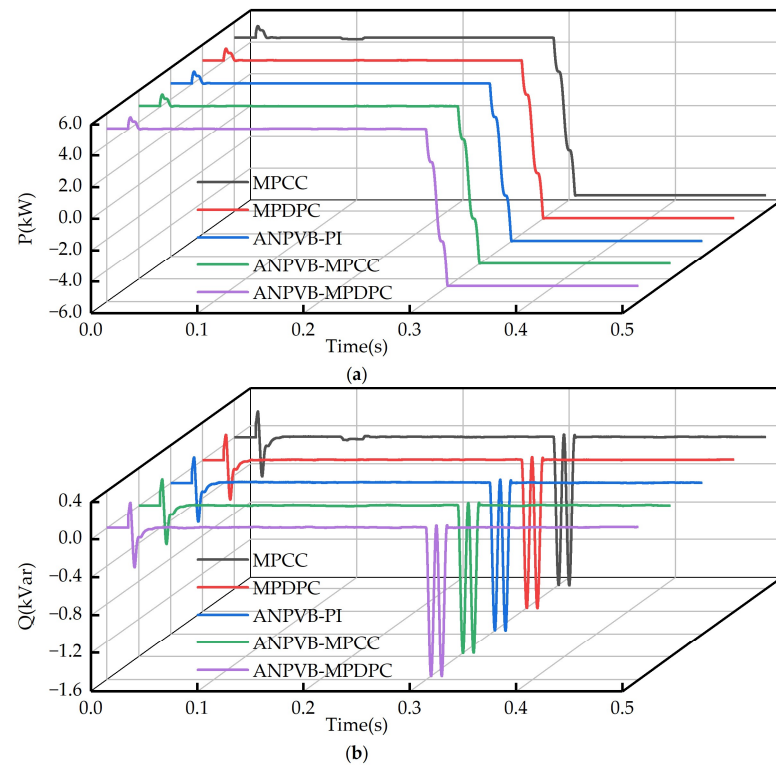


Figure 6. Power waveforms. (a) Active power. (b) Reactive power.

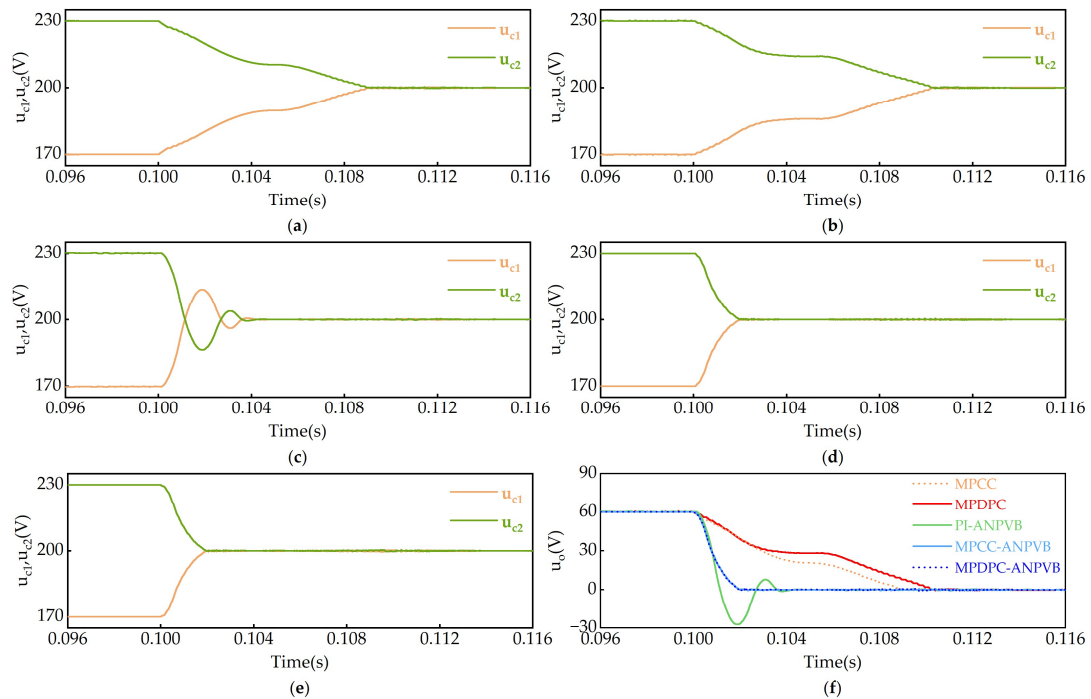


Figure 7. DC-link capacitor voltages and NP voltage difference under NP balancing at 0.1 s. (a) MPCC. (b) MPDPC. (c) PI-ANPVB. (d) MPCC-ANPVB. (e) MPDPC-ANPVB. (f) NP voltage difference comparison.

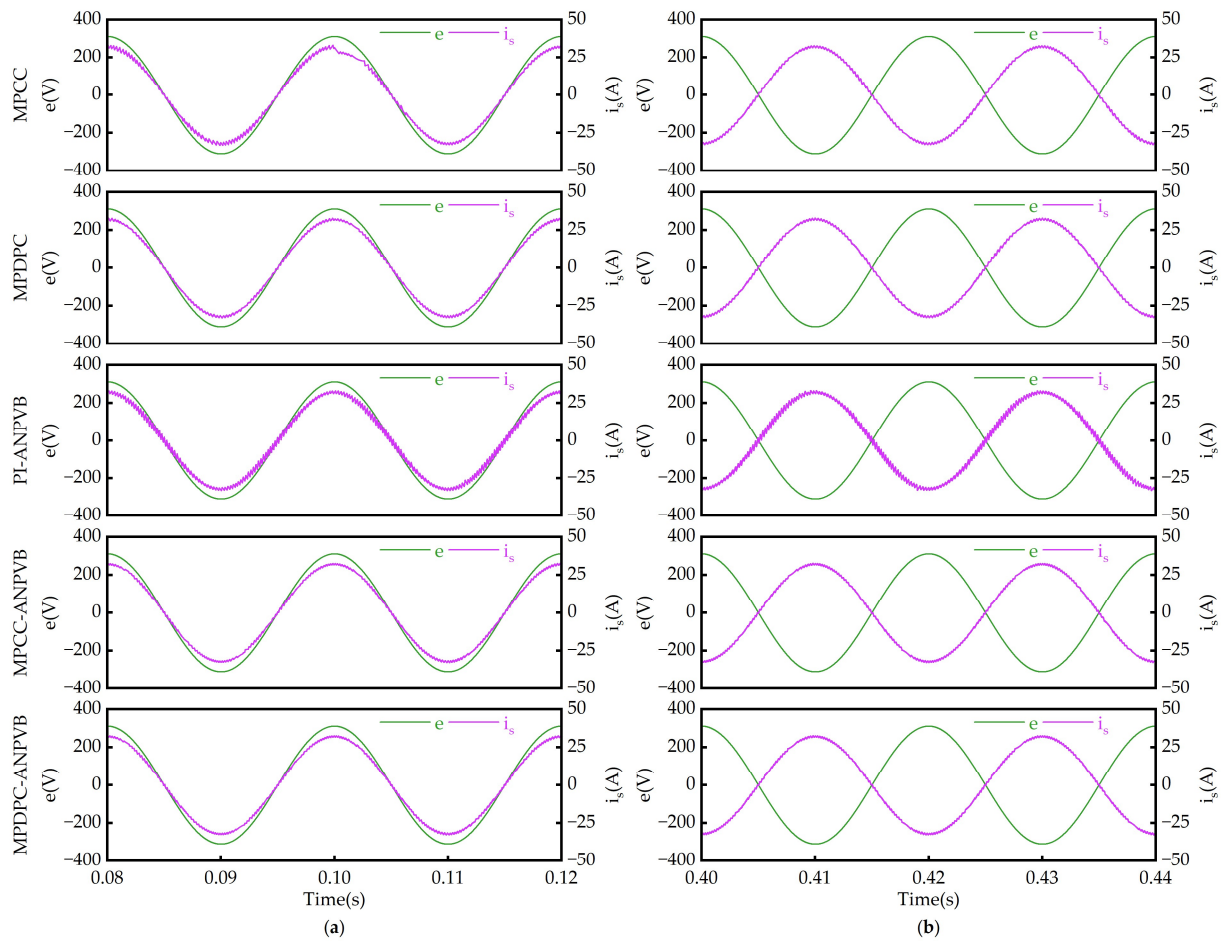


Figure 8. Grid voltage and current waveforms under five control strategies. (a) V2G mode. (b) G2V mode.

Figure 6 shows the active and reactive power response curves under the five control strategies. As shown in Figure 6a, after the NP voltage balancing was activated at 0.1 s, the conventional MPCC exhibited a transient deviation of approximately 100 W in active power, which quickly recovered within around 20 ms. In contrast, the other four strategies maintained smoother responses without significant fluctuation. For the reactive power in Figure 6b, a transient disturbance of about 33 Var was observed under conventional MPCC, while the other methods were nearly unaffected. During the mode transition at 0.3 s, all strategies exhibited some fluctuations in reactive power caused by the abrupt change in operating conditions, but the steady-state control performance remained unaffected.

Figure 7 illustrates the variations of the upper and lower DC-link capacitor voltages, u_{c1} and u_{c2} , under the five control strategies when NP balancing is activated at 0.1 s. As shown in Figure 7a,b, the conventional MPCC and MPDPC exhibit relatively slow recovery processes after NP balancing is triggered, and the voltage difference decreases at a slower rate. Figure 7c presents the results for the PI-ANPVB approach. Although it shows noticeable oscillations during the initial adjustment phase, the voltage difference between u_{c1} and u_{c2} decreases rapidly, and the total settling time is shorter than that of the traditional model predictive methods. In Figure 7d,e, corresponding to MPCC-ANPVB and MPDPC-ANPVB, respectively, the capacitor voltages converge rapidly within a short time frame, with no observable oscillation and a smooth dynamic response. As shown in Figure 7f, the PI-based strategy exhibits a transient fluctuation in NP voltage at 0.1 s but restores balance within 4 ms. In contrast, MPCC and MPDPC take nearly 10 ms to gradually converge. By comparison, the two improved strategies based on ANPVB, namely MPCC-ANPVB and MPDPC-ANPVB, achieve near-complete voltage balance in

approximately 2 ms without any significant oscillation, demonstrating faster regulation and superior voltage symmetry.

To further validate the performance of the proposed strategy, the grid currents under the five control methods are compared. The grid voltage and current waveforms are shown in Figure 8. In Figure 8a,b, corresponding to the V2G and G2V modes, respectively. In the V2G mode, the grid current remains in phase with the voltage waveform, while in the G2V mode, it is in antiphase, aligning with the power flow characteristics illustrated in Figure 6. Under the PI-ANPVB strategy, noticeable current ripples can be observed. At 0.1 s, NP voltage balancing is activated. As seen in Figure 8a, the current waveform under the conventional MPCC strategy exhibits significant distortion near 0.1 s.

To further evaluate waveform quality, the THDi was extracted and compared for the five control strategies. The results are summarized in Table 4. Under the V2G mode, the THDi values of the conventional MPCC and MPDPC strategies are 1.96%, and under the G2V mode, they are 2.08% and 2.05%, respectively, indicating relatively low current distortion. In contrast, the PI-ANPVB strategy exhibits increased THDi values of 4.76% and 4.78% in the two operating modes, significantly higher than those of the other methods. The two improved strategies, MPCC-ANPVB and MPDPC-ANPVB, demonstrate better current quality, with waveforms closer to the ideal sinusoid. Their THDi values remain below 1.89% in both operating modes.

Table 4. THD of grid-side current under different control strategies.

Methods	THDi	
	V2G	G2V
MPCC	1.96%	2.08%
MPDPC	1.96%	2.05%
PI-ANPVB	4.76%	4.78%
MPCC-ANPVB	1.89%	1.85%
MPDPC-ANPVB	1.89%	1.83%

4.3. Dynamic Performance Under Active Power Changes

The active power reference starts at 5000 W and decreases stepwise every 0.2 s to 3000 W, 0 W, −3000 W, and −5000 W, while the reactive power reference remains at 0 Var. The results of the improved strategy are shown in Figure 9. Current waveforms exhibit slight distortion at the initial stage and during active power step changes; however, these distortions are brief and rapidly recover, indicating good overall current quality. Regarding power response, active power closely follows the reference changes with smooth step transitions, minimal overshoot, and the steady-state control process completing within approximately 50 ms. Reactive power experiences transient fluctuations during power transitions, with fluctuation magnitude roughly proportional to the active power change; larger changes lead to more noticeable transient deviations, but most recover to near zero within 50 ms, meeting the system's reactive power requirements. The upper and lower capacitor voltages remain symmetric throughout the power variation process without significant deviation or oscillation, with the amplified voltage waveform maintained within ± 0.7 V.

To highlight the advantages of the proposed method, Table 5 compares it with several typical single-phase bidirectional AC/DC converters reported in the recent literature. The comparison covers control strategies, power ratings, charging levels, DC bus or battery voltages, circuit complexity, and performance indicators such as power factor (PF) and total harmonic distortion (THD).

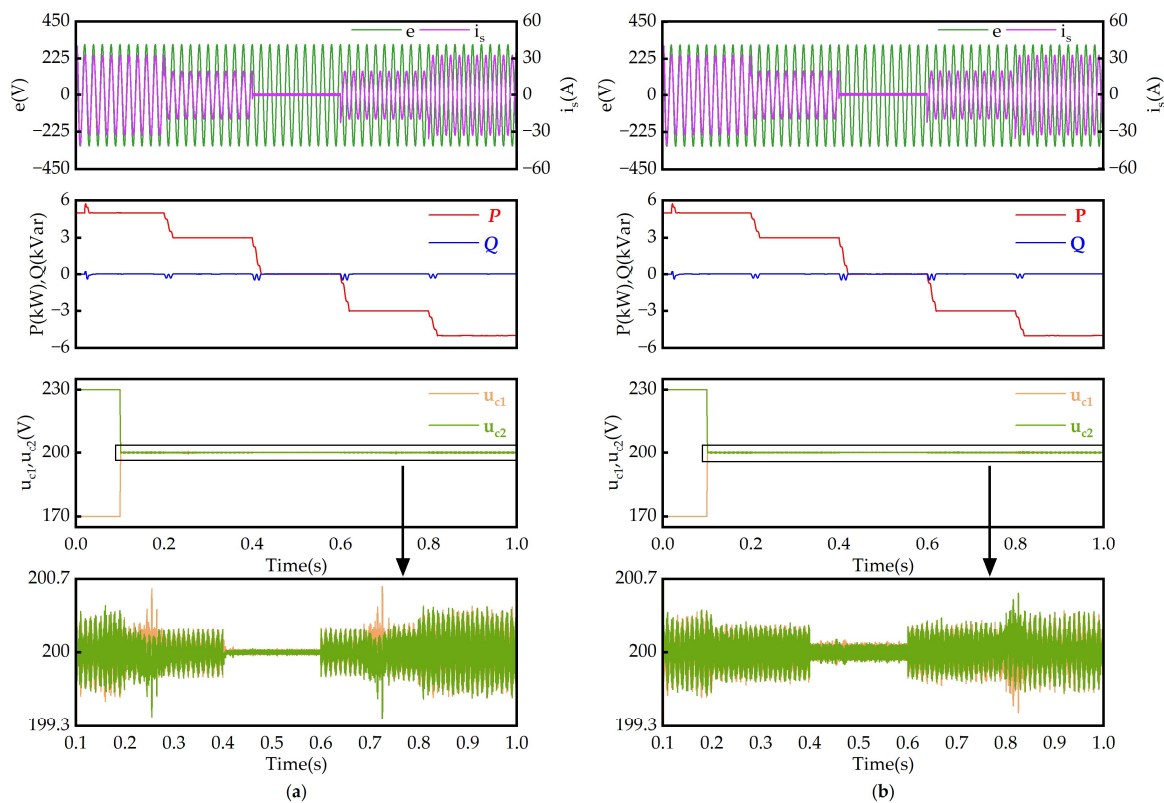


Figure 9. Waveforms under MPCC-ANPVB and MPDPC-ANPVB during active power step changes. (a) MPCC-ANPVB. (b) MPDPC-ANPVB.

Table 5. Comparison of bidirectional on-board chargers with the proposed method.

Ref.	Control	Power Rating (kW)	SAE Charging Level	DC Bus/Battery Voltage (V)	Switches	Filters	PF	THD
[26]	PR	1.5	AC L-1	300	8	L	0.99	2.67%
[27]	PR	1.5	AC L-1	300	12	L	0.99	2.55%
[28]	PI	8	AC L-1/2	700	6	L	0.99	3%
[29]	PI	2	AC L-1	400	8	L	NA	NA
[30]	PI	2.8	AC L-1	NA	6	L	NA	<6%
[31]	PI	0.4	AC L-1	120	4	LC	NA	6.15%
Proposed	MPC	5	AC L-1/2	400	10	LC	0.99	1.89%

4.4. Comparison

To further highlight the effectiveness of the proposed method, a comparison with several existing bidirectional converter solutions is provided. As shown in Table 5, most existing solutions adopt PI or PR control methods with relatively simple filter structures and low component counts. The proposed MPC-based strategy, despite a slightly more complex structure, achieves lower THD (1.89%) while maintaining a high PF of 0.99, demonstrating improved power quality. In addition, it supports SAE Level 1/2 charging with 5 kW output, making it suitable for mid-power V2G applications.

5. Conclusions

This paper proposed an improved model predictive control strategy integrating the hardware-based ANPVB for single-phase three-level converters in on-board V2G applications. Two approaches, MPCC-ANPVB and MPDPC-ANPVB, were developed and evaluated. The proposed methods effectively mitigate NP voltage imbalance without relying on weighting factor tuning. By directly adjusting the NP voltage via hardware,

the control system is simplified, enhancing robustness and feasibility. Compared with conventional MPC and other existing methods reported in the literature, the improved strategies demonstrate faster and more stable balancing performance, maintaining better voltage symmetry across the DC-link capacitors under dynamic operating conditions. Simulation results under two key scenarios, bidirectional mode switching and active power step changes, show that MPCC-ANPVB and MPDPC-ANPVB maintain smoother current waveforms, lower current harmonic distortion, and accurate power tracking. Even during continuous step changes in active power reference, the NP voltage remains well balanced without significant deviation. In conclusion, the proposed control schemes enhance NP voltage regulation while ensuring high power quality and dynamic performance. These features make them suitable for practical V2G converter control applications. While the proposed control strategies have been validated through detailed simulation studies, practical implementation may encounter additional challenges such as measurement noise, parameter variation, and digital control delay. Therefore, future work will focus on building a hardware prototype platform to experimentally verify their effectiveness and robustness under realistic operating conditions.

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