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A Discontinuous Modulation Method with Variable Clamping Interval Width of the Modular Multilevel Converter

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Abstract: The modular multilevel converter (MMC) has been widely used because of the advantages of easier expansion, lower harmonic distortion and higher output voltage level. If the MMC is adapted to high voltage application, more submodules need to be connected in series in each arm. Thus, the switching loss needs to be considered a key issue. A discontinuous modulation method with variable clamping interval width is proposed in this paper in order to reduce the switching loss under variable power factor conditions. Different widths of the clamping interval can be selected according to the requirements of the system. Meanwhile, the capacitor voltage ripple of the submodules can also be reduced. The feasibility and effectiveness of the proposed modulation method are verified under a RT-LAB rapid control prototype based MMC system.

Keywords: modular multilevel converter; discontinuous modulation; switching loss

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1. Introduction

The modular multilevel converter (MMC) is considered to be the most promising multilevel power converter in medium and high voltage applications. It has the advantages of modularity, low switching frequency, low harmonic distortion and expandability [1,2]. These excellent characteristics enable the MMC to be applied to high-voltage DC (HVDC) transmission, the static synchronous compensator (STATCOM), high-power motor drive and the unified power flow controller (UPFC) [3–6]. The research on the MMC mainly focus on the capacitor voltage balance strategy of submodules, the circulating current control algorithm and the modulation method [1].

The output waveform quality and the switching loss are directly affected by the modulation method. Thus, various modulation methods have been proposed for MMC, such as carrier-based pulse width modulation, space vector pulse width modulation (SVPWM), nearest level modulation (NLM) and selective harmonic elimination (SHE) [7–11]. More submodules need to be connected in series if the MMC is adapted to high voltage application. Thus, the switching loss needs to be considered a key issue.

Discontinuous pulse width modulation (DPWM) can clamp the output voltage of a certain phase to the DC bus in each fundamental period to reduce the switching loss. In [12], an improved DPWM method is proposed to modify the reference voltage of each submodule by splitting and rotating discontinuous modulated waves, which solves the problem of unbalanced power distribution among submodules. However, the output waveform quality is poor and the capacitor voltage ripple of submodules is large. Moreover, the control complexity increases with the increase in the number of submodules. In [13], a DPWM method with zero-sequence voltage injection is proposed, which reduced the capacitor voltage ripple and switching loss of the submodule. However, this scheme requires redundant submodules to prevent overmodulation. In [14], a DPWM method based on the space vector concept is proposed. The zero-sequence voltage can be determined based on the position of the two-level space vector. This method only uses the two-level space vector and the clamping interval width cannot be changed. In [15], a model predictive control

technology based on the DPWM scheme is proposed to reduce the switching loss of the submodules, but the algorithm is complex.

In this paper, a discontinuous modulation method with variable clamping interval width is proposed. The influence of power factor on output current phase is considered, and different clamping interval positions can be determined by the selection of different zero-sequence components. The width of the clamping interval can also be changed according to the requirement of the switching loss and the output waveform quality.

2. Principle of Modular Multilevel Converter

The topology of the three-phase MMC is shown in Figure 1. The upper and lower arms of each phase are composed of several half-bridge submodules and arm inductors in series. The switching state of power devices of each submodule and the corresponding output voltage of the submodule are shown in Table 1. If T_1 is ON and T_2 is OFF, the state of the submodule is defined as ON, and the output voltage of the submodule is u_c; on the contrary, if T_1 is OFF and T_2 is ON, the state of the submodule is defined as OFF, and the output voltage of the submodule is 0.

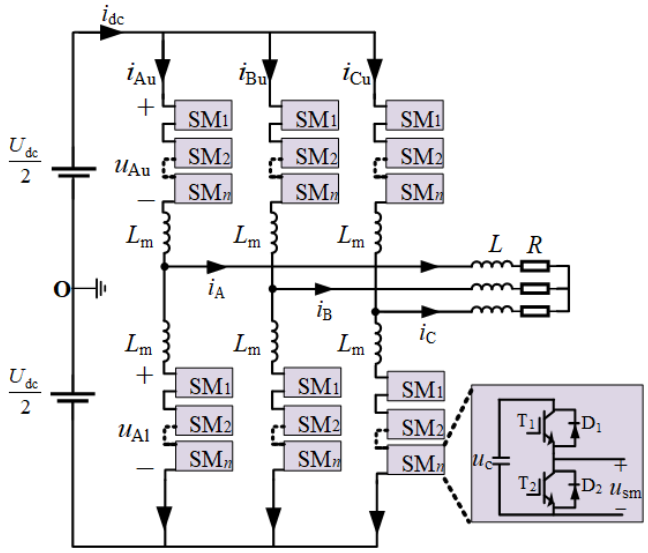

Figure 1. Topology of the three-phase modular multilevel converter (MMC).

Table 1. The operating state of modular multilevel converter (MMC).

State	T_1	T_2	u_{sm}
ON	ON	OFF	u_c
OFF	OFF	ON	0

The total output voltage of the submodules of the upper and lower arms of any phase in the MMC can be expressed as:

$$\begin{cases} u_{xu} = \sum_{h=1}^{n} S_{xu,h} \times u_{c,h} \\ u_{xl} = \sum_{h=1}^{n} S_{xl,h} \times u_{c,h} \end{cases} \quad (1)$$

where $x \in \{A, B, C\}$, u and l represent upper and lower arms, respectively, h represents the h-th submodule and $h \in \{1, 2,..., n\}$.

Taking Phase A as an example, ignoring the voltage drop of arm inductance, the following expression can be obtained from Kirchhoff's voltage law:

$$\begin{cases} u_{\mathrm{A}} - \frac{U_{\mathrm{dc}}}{2} + u_{\mathrm{Au}} + L\frac{di_{\mathrm{Au}}}{dt} = 0 \\ u_{\mathrm{A}} + \frac{U_{\mathrm{dc}}}{2} - u_{\mathrm{Al}} - L\frac{di_{\mathrm{Al}}}{dt} = 0 \end{cases}. \tag{2}$$

The output voltage of Phase A can be expressed as:

$$u_{\mathrm{A}} = \frac{1}{2}(u_{\mathrm{Al}} - u_{\mathrm{Au}}) + \frac{L}{2}\frac{d}{dt}(i_{\mathrm{Al}} - i_{\mathrm{Au}}). \tag{3}$$

Similarly, the arm current can be expressed as:

$$\begin{cases} i_{x\mathrm{u}} = +\frac{1}{2}i_x + i_{xz} \\ i_{x\mathrm{l}} = -\frac{1}{2}i_x + i_{xz} \end{cases} \tag{4}$$

where i_x and i_{xz} are the phase current and differential current flowing through the arm, which can be expressed as:

$$\begin{cases} i_x = i_{x\mathrm{u}} - i_{x\mathrm{l}} \\ i_{xz} = \frac{1}{2}(i_{x\mathrm{u}} + i_{x\mathrm{l}}) \end{cases}. \tag{5}$$

3. Conventional Discontinuous Modulation Method

Each phase of the MMC can be clamped to the DC bus by injecting discontinuous zero-sequence voltage into the three-phase reference voltage. If any phase is clamped to the DC bus, the switching state of the corresponding power device will remain unchanged, and the switching loss will be significantly reduced. For the MMC, when the upper and lower arm of any arbitrary phase are in the clamping state, the submodule of the arm is bypassed and the submodule has no switching action, which significantly reduces the switching loss. Due to the specific topology of the MMC, no current flows through the capacitors in the bypassed submodules. As a result, the voltage fluctuation of capacitors is reduced.

The three-phase reference voltage of the MMC can be expressed as:

$$\begin{cases} u_{\mathrm{A}}(t) = (mU_{\mathrm{dc}}/2)\cos\omega t \\ u_{\mathrm{B}}(t) = (mU_{\mathrm{dc}}/2)\cos(\omega t - 2\pi/3) \\ u_{\mathrm{C}}(t) = (mU_{\mathrm{dc}}/2)\cos(\omega t + 2\pi/3) \end{cases} \tag{6}$$

where ω is the frequency of the reference voltage and m is the modulation index, which is defined as:

$$m = \frac{U_{\mathrm{m}}}{U_{\mathrm{dc}}/2} \tag{7}$$

where U_{m} is the amplitude of the reference voltage.

The reference voltage after zero-sequence component injection can be expressed as:

$$u'_x = u_x + u_z. \tag{8}$$

Conventional discontinuous modulation methods can be classified into four types: DPWM0~DPWM3 (as shown in Figure 2). A, B and C represent the clamping phase, P represents the phase is clamped to the positive DC bus and N indicates that the phase is clamped to the negative DC bus.

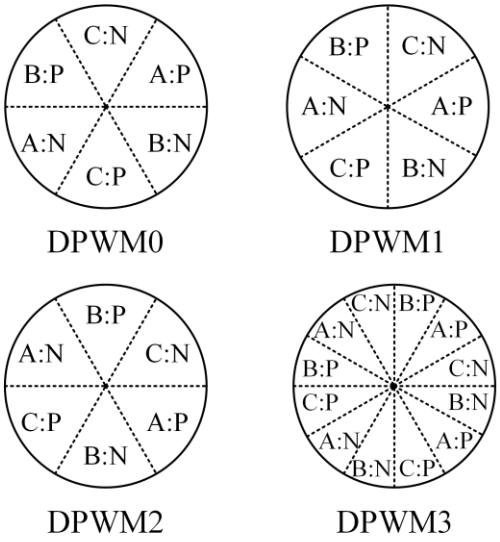

Figure 2. Four common clamp state area division.

According to the division of clamping interval in Figure 2, let us take Phase A as an example. λ is defined as the clamping factor. λ is equal to 1 when Phase A is in the clamping interval. While λ is equal to 0 when Phase A is in the non-clamping interval. The value of λ in each sector for DPWM0~DPWM3 is shown in Figure 3. Then the expression of zero-sequence voltage can be expressed as:

$$u_z = (2 \cdot \lambda - 1) - \lambda \cdot u_{\max} - (1 - \lambda) \cdot u_{\min} \tag{9}$$

where $u_{\max} = \max\{u_A, u_B, u_C\}$ and $u_{\min} = \min\{u_A, u_B, u_C\}$. Thus, the expression of zero-sequence voltage can be further expressed as:

$$u_z = \begin{cases} 1 - u_{\max}, \lambda = 1 \\ -1 - u_{\min}, \lambda = 0 \end{cases}. \tag{10}$$

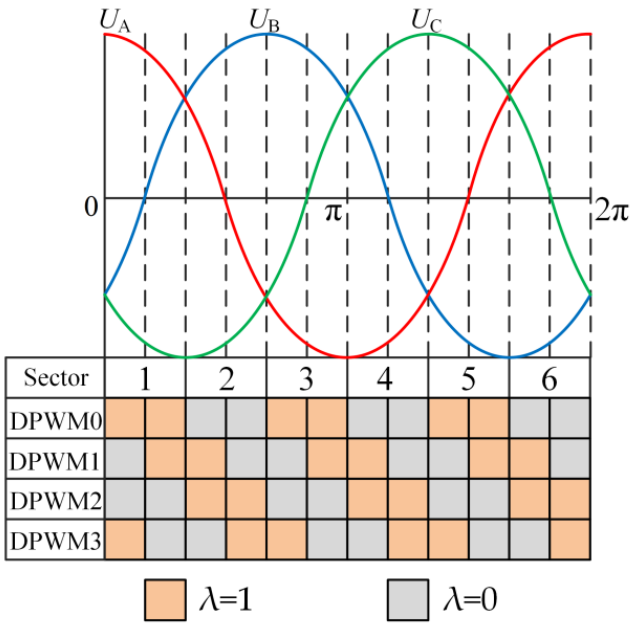

Figure 3. Clamping factor λ Schematic diagram of clamping interval.

4. Discontinuous Modulation Method with Variable Clamping Interval

Conventional discontinuous modulation methods clamp the switching state in a fixed interval in each fundamental cycle. If the power factor changes, the switching loss will be increased. In this paper, an improved discontinuous modulation strategy is proposed. Each phase can be clamped to the DC bus at the maximum value of load current by adjusting the clamping interval online. Thus, the switching loss and the voltage fluctuation of the submodule can be reduced. The overall control flow diagram of the system is shown in Figure 4.

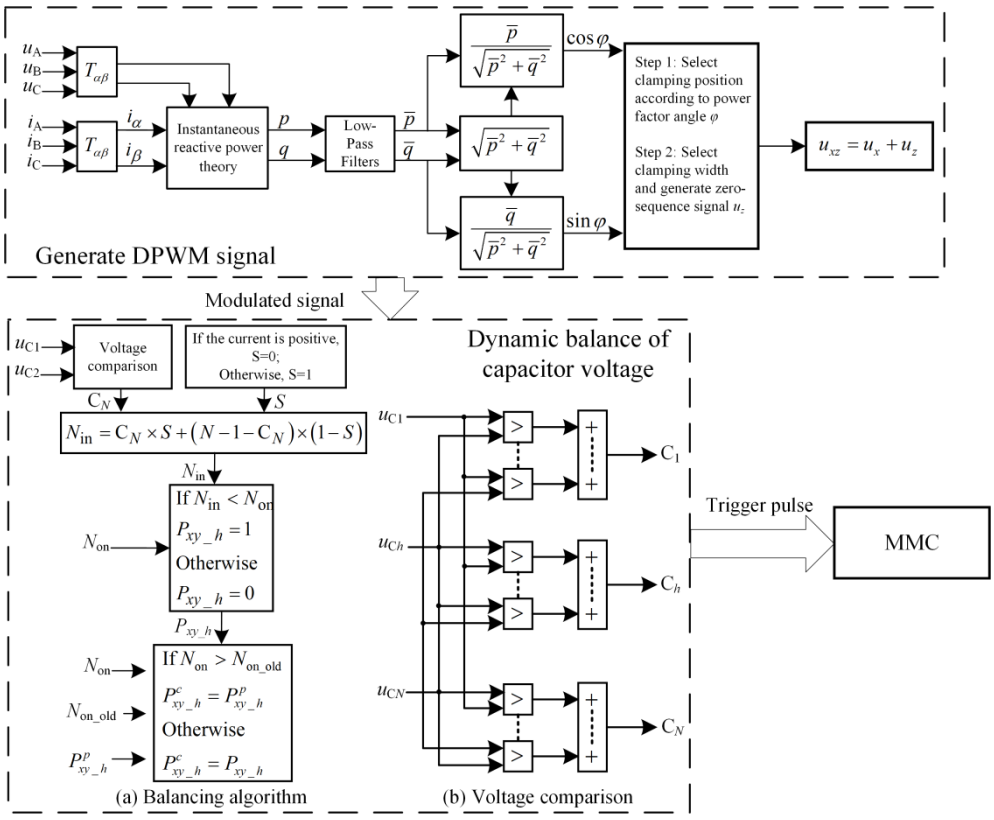

Figure 4. System control block diagram.

4.1. Calculation of Power Factor

The power factor can be calculated by the instantaneous reactive power theory [16]. The DC components of reactive power and active power can be separated and then the power factor can be calculated.

The phase of the original reference voltage signal can be shifted according to the calculated power factor angle φ. Thus:

$$\begin{cases} u^*_{\mathrm{A}}(t) = u_{\mathrm{A}}(\omega t - \varphi) \\ u^*_{\mathrm{B}}(t) = u_{\mathrm{B}}(\omega t - 2\pi/3 - \varphi) \\ u^*_{\mathrm{C}}(t) = u_{\mathrm{C}}(\omega t + 2\pi/3 - \varphi) \end{cases} . \tag{11}$$

The maximum and minimum value of the reference voltage signal after phase shifting can be defined as:

$$\begin{cases} u_{\max}(t) = \max\{u_{\mathrm{A}}, u_{\mathrm{B}}, u_{\mathrm{C}}\} \\ u_{\min}(t) = \min\{u_{\mathrm{A}}, u_{\mathrm{B}}, u_{\mathrm{C}}\} \\ u^*_{\max}(t) = \max\{u^*_{\mathrm{A}}(t), u^*_{\mathrm{B}}(t), u^*_{\mathrm{C}}(t)\} \\ u^*_{\min}(t) = \min\{u^*_{\mathrm{A}}(t), u^*_{\mathrm{B}}(t), u^*_{\mathrm{C}}(t)\} \end{cases} . \tag{12}$$

4.2. Discontinuous Modulation Method with Variable Clamping Interval

The change of clamping interval will lead to the change of switching loss and output waveform quality. In industrial applications, different widths of the clamping interval need to be selected according to the requirements of the system. To achieve variable width of the clamping interval, each sector is further divided into eight subregions with an interval of $\pi/24$, as shown in Figure 5. Each subregion can be independently set as a clamping interval or an unclamping interval.

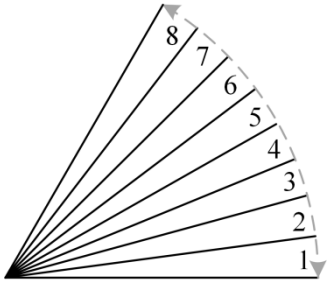

Figure 5. Sector division diagram.

In the unclamp interval, the zero-sequence component $u_z = 0$, while in the clamping interval:

$$u_z(t) = \begin{cases} 1 - u_{\max}, & |u^*_{\max}(t)| > |u^*_{\min}(t)| \\ -1 - u_{\min}, & |u^*_{\max}(t)| < |u^*_{\min}(t)| \end{cases}. \tag{13}$$

The clamping interval and the unclamping interval can be flexibly selected. It does not require complex coordinate transformation, trigonometric function calculation, vector selection and duty cycle calculation. Figure 6 shows the discontinuous modulation methods with four clamping interval widths: $\pi/12$, $\pi/6$, $\pi/4$ and $\pi/3$.

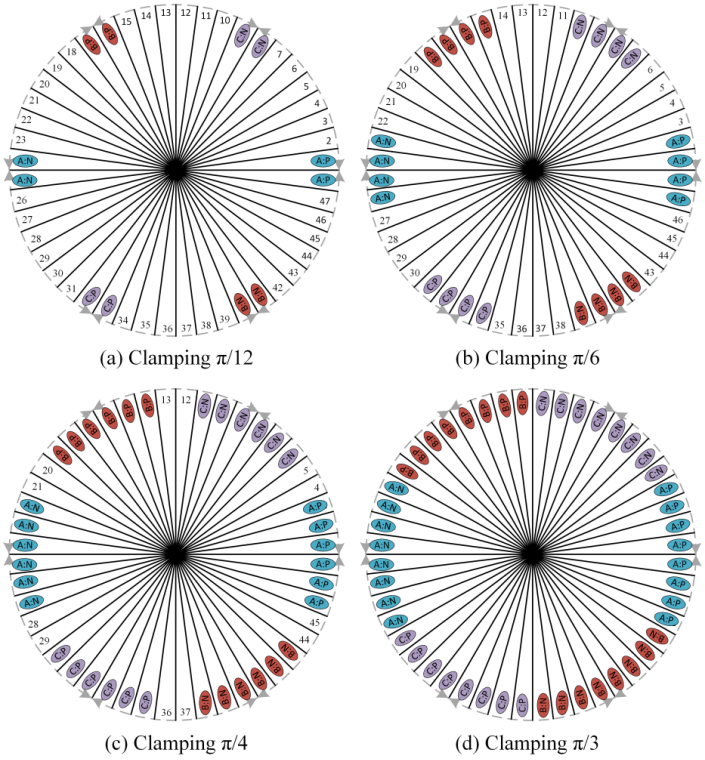

Figure 6. Four clamping interval widths.

Taking power factor angle $\varphi = \pi/9$ as an example, the variable load power factor discontinuous modulation voltage is shown in Figure 7. When the amplitude of the load current is close to its peak value, the corresponding phase is clamped to the DC bus. The switching loss can effectively be reduced.

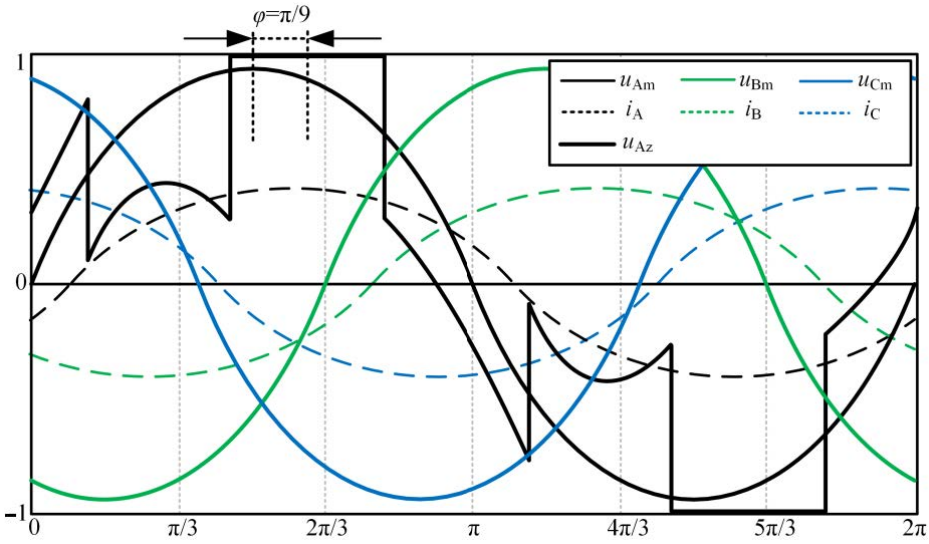

Figure 7. Example of discontinuous modulation strategy for variable load power factor.

4.3. Capacitor Voltage Dynamic Balance Algorithm

In order to solve the power imbalance problem of submodule, the capacitor voltage dynamic balance algorithm needs to be adopted. The ON and OFF of submodules are determined by the direction of the arm current and the capacitor voltage of submodules. The algorithm can be divided into the following steps (as shown in Figure 4):

(1) Determining the total number of submodules which need to be put in, then subsequently sorting the submodules into numerical order according to the amplitude of the capacitor voltage;
(2) Judging the direction of the current i_{xy}. When the direction of i_{xy} is positive, set S = 0, otherwise, set S = 1;
(3) Determining the index number of submodules according to the direction of i_{xy}. The expression of the index number is as follows:

$$N_{\text{in}} = \text{C}_N \times S + (N - 1 - \text{C}_N) \times (1 - S) \tag{14}$$

(4) The ON and OFF of each submodule is determined by the calculation result of step (3);
(5) Judging the change of the number of submodules in the ON state. If the number of submodules in the ON state is not changed, there will be no switching behavior, and the switching loss will be reduced.

In the clamping interval, the number of submodules in the ON state is constant, and the dynamic balance algorithm of the capacitor voltage is not applied.

5. Experimental Verification

In order to verify the feasibility and effectiveness of the proposed modulation method, the rapid control prototype OP5700 (OPAL-RT Co. Ltd. Montreal, Quebec, Canada) and the H-bridge power model PEH2015 (Imperix Co. Ltd., Sion, Switzerland) are adopted to establish the experimental setup, as shown in Figure 8.

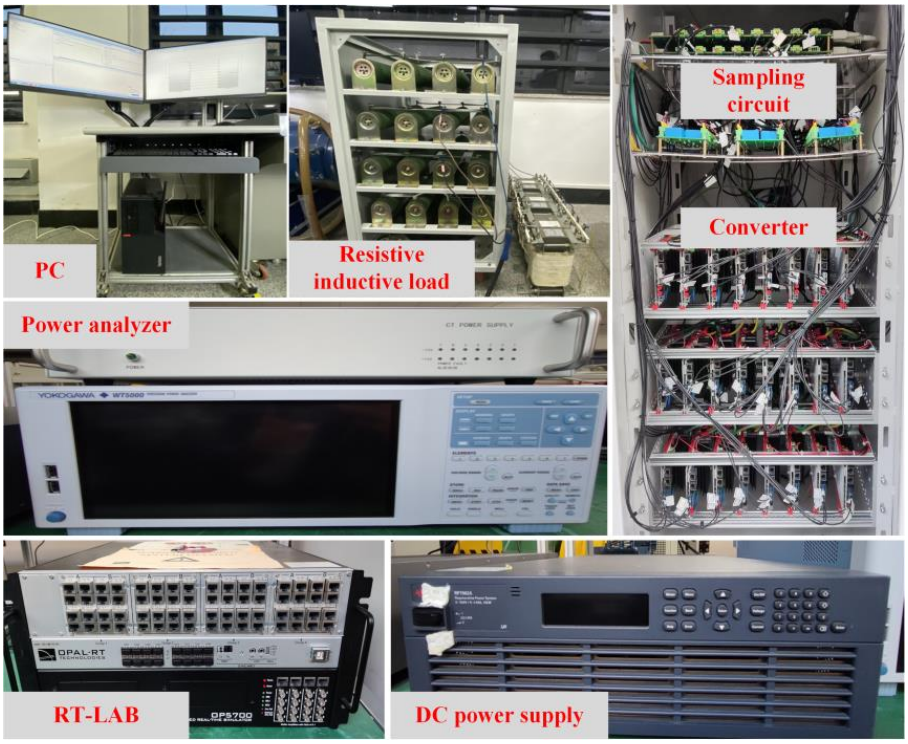

Figure 8. MMC experimental system diagram.

The proposed modulation strategy is tested under eight different clamping interval conditions ($\pi/24$, $\pi/12$, $\pi/8$, $\pi/6$, $5\pi/24$, $\pi/4$, $7\pi/24$ and $\pi/3$). The parameters of the experimental setup are listed in Table 2.

Table 2. Experimental parameters.

Parameter	Value	Unit
DC voltage U_{dc}	200	V
Number of submodules N	4	-
Submodule capacitance C	5.04	mF
arm inductance L_m	2.7	mH
Carrier frequency f_c	2	kHz
Output frequency f	50	Hz
Load resistance R	5	Ω
Load inductance L	5	mH

Figures 9 and 10 shows the output current, phase voltage and capacitor voltage ripple of eight different clamping intervals ($\pi/24$ to $\pi/3$) under the condition of m = 0.9 and m = 0.3. As can be seen, no matter how the width of the clamping interval changes, the output current remains sinusoidal. With the decrease in the width of the clamping interval, the capacitor voltage ripple of the submodule increases.

5.1. Switching Loss

The efficiency of the proposed modulation strategy under different modulation indices and clamping interval width conditions is recorded by a Yokogawa WT5000 power analyzer. The variation of efficiency with the change of the modulation index and the width of the clamping interval is shown in Figure 11.

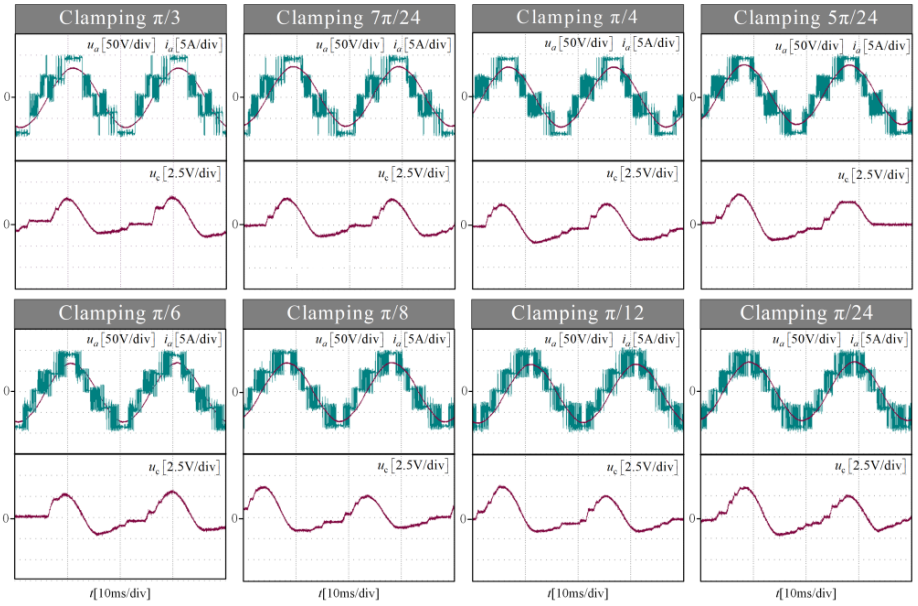

Figure 9. Experimental waveforms of eight clamping widths under the condition of m = 0.9.

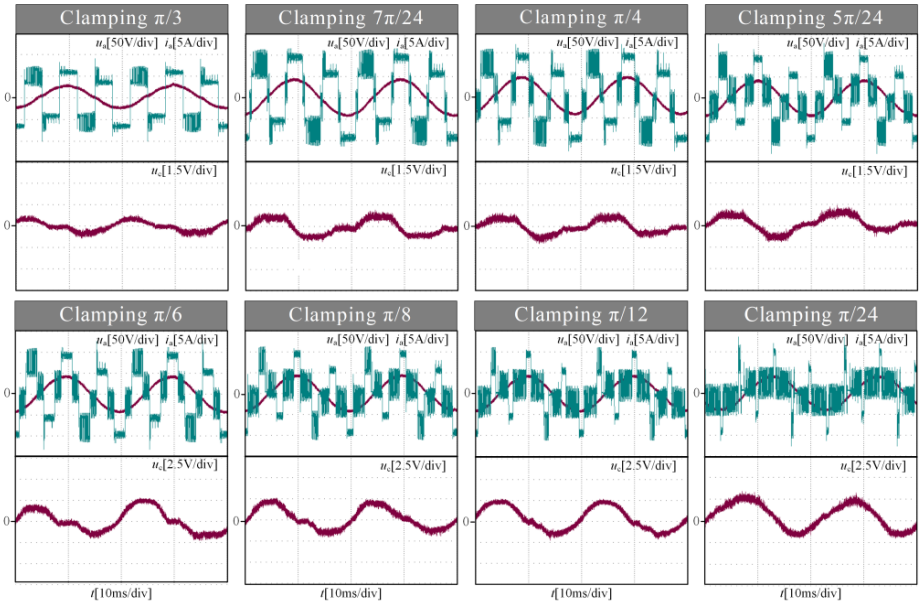

Figure 10. Experimental waveforms of eight clamping widths under the condition of m = 0.3.

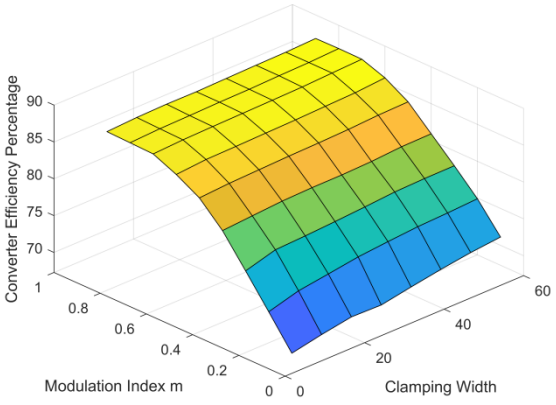

Figure 11. Converter working efficiency.

Under lower modulation index conditions, the efficiency is gradually improved with the increase in clamping width. While under higher modulation index conditions, the change of the efficiency is unobvious.

5.2. Capacitor Voltage Ripple of Submodule

The variation of the capacitor voltage ripple with the change of the modulation index and the width of the clamping interval is shown in Figure 12.

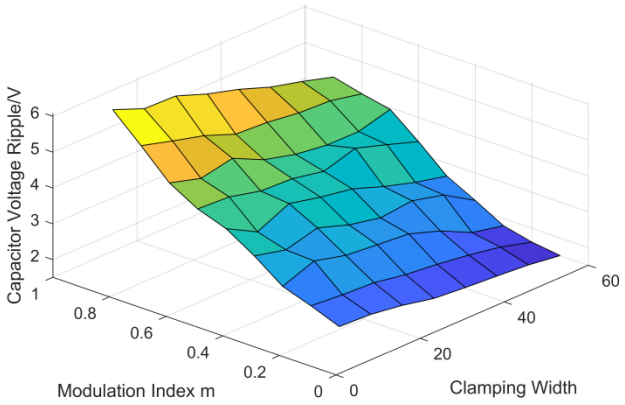

Figure 12. Capacitor voltage ripple.

As shown in Figure 12, under the same modulation index, the capacitance voltage ripple decreases continuously with the increase in the width of the clamping interval from $\pi/24$ to $\pi/3$. This is because there is no current flowing through the capacitor of the submodule during the clamping interval.

5.3. Total Harmonic Distortion

The variation of total harmonic distortion (THD) of the output current with the change of the modulation index and the width of the clamping interval is shown in Figure 13.

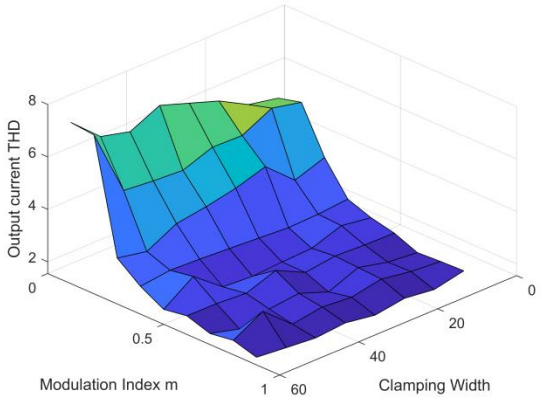

Figure 13. Output current THD.

Under lower modulation index conditions, the THD of the output current raises with the increase in clamping width. While under higher modulation index conditions, the change of the THD of the output current is unobvious.

In conclusion, under higher modulation index conditions, the change of the width of the clamping interval will not lead to a rapid variation of the THD of the output current and the switching loss. Under lower modulation index conditions, the switching loss can be effectively reduced by broadening the clamping interval. In addition, the variation of the THD of the output current is simultaneously unobvious.

5.4. Strategy Comparison

To verify the effectiveness of the algorithm in this paper, the proposed strategy is compared with the conventional strategy and the rotation strategy. Comparison experiments were performed at a clamping width of $\pi/3$ and m = 0.8. Figure 14 shows the output current, phase voltage, capacitor voltage ripple and circulating current under the condition of 5 Ω and 10 mH. The proposed strategy reduces capacitor voltage fluctuations and circulating current.

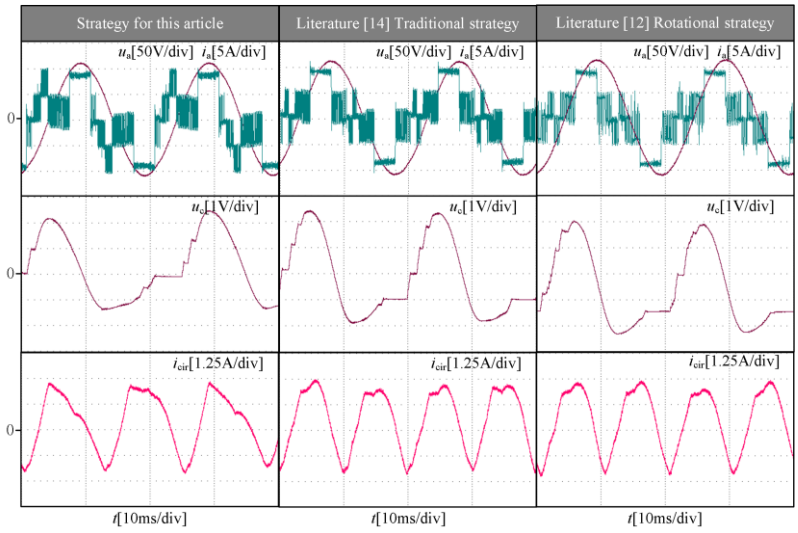

Figure 14. Comparison of experimental waveform under the condition of 5 Ω and 10 mH.

As shown in Figure 15, under the condition of 10 Ω and 30 mH, the effect of the proposed strategy is the same.

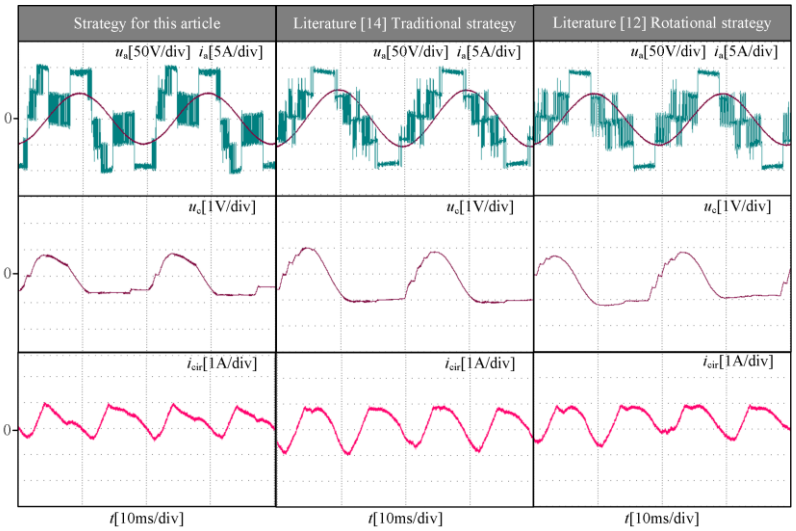

Figure 15. Comparison of experimental waveform under the condition of 10 Ω and 30 mH.

6. Conclusions

In this paper, a discontinuous modulation method with variable clamping interval width of the MMC for different load power factor conditions is proposed. The position of the clamping interval can be adjusted according to the power factor. In addition, the width of the clamping interval can also be adjusted according to the requirements of switching loss and the output waveform quality. The proposed method is tested and verified by a RT-LAB based rapid prototype development experimental system. The results show that

the switching loss can be significantly reduced without reducing the output waveform quality under lower modulation conditions.

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