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An Energy-Efficient Scheme for Waking Co-Channel TDMA in LoRa Networks via the Integration of Bidirectional Timestamp Correction and Address Recognition

Zongliang Xu [1,2], Guicai Yu [1,2,*], Yingcong Luo [1,2] and Hao Jiang [1,2]

[1] School of Intelligent Science and Engineering, Qinghai Minzu University, Xining 810000, China; xzl762564093@gmail.com (Z.X.); 15972637020@163.com (Y.L.); 19106434260@163.com (H.J.)
[2] National Demonstration Center for Experimental Teaching of Communication Engineering, Qinghai Minzu University, Xining 810007, China
* Correspondence: yuguicai@ncu.edu.cn; Tel.: +86-13767967866

Abstract

To address the issues of high energy consumption, data collisions, and invalid wake-ups of nontarget nodes in large-scale node-deployment scenarios of long-range (LoRa) star networks, this paper proposes an energy-saving wake-up scheme that combines (i) time-division multiple access (TDMA) slot allocation based on bidirectional timestamp correction with (ii) a sensing and communication integrated (ISAC) scheme proposed for physical address identification of LoRa nodes operating on the same channel. The scheme incorporates parameter estimation of the LoRa channel, which effectively enhances the identification accuracy and improves the system's robustness. The proposed scheme consists of two parts: First, in case nodes briefly lose power, a bidirectional timestamp calibration algorithm and GPS-assisted timing are used to synchronize the gateway and each node with high precision, ensuring the accurate scheduling of the TDMA mechanism. Second, based on time synchronization, a "slot–LoRa module address" mapping table is constructed to set the communication time points between the gateway and each node. The gateway can wake the target nodes at specific, precise communication time points. Experimental results show that the proposed method maintains the error range within ±1 ms. The significant decrease in the rate of unnecessary node wake-up decreases data collisions and energy waste in the same channel environment. Energy savings scale with network size, thereby significantly extending the network life cycle.

Keywords: LoRa; TDMA; bidirectional timestamp; low-power data acquisition; ISAC; parameter estimation

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Academic Editor: Jose I. Moreno Novella

Received: 10 July 2025
Revised: 4 August 2025
Accepted: 12 August 2025
Published: 14 August 2025

Citation: Xu, Z.; Yu, G.; Luo, Y.; Jiang, H. An Energy-Efficient Scheme for Waking Co-Channel TDMA in LoRa Networks via the Integration of Bidirectional Timestamp Correction and Address Recognition. *Future Internet* **2025**, *17*, 369. https://doi.org/10.3390/fi17080369

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1. Introduction

As Internet of Things (IoT) applications continue to expand in areas such as smart agriculture, environmental monitoring, and remote sensing, long-range (LoRa) communication modules have become a pivotal technology for low-power wide-area networks (LPWANs) due to their ability to combine long-range transmission with low power consumption [1–3]. However, in scenarios involving the dense deployment of large-scale terminal nodes—particularly under master–slave network architectures—conventional LoRa systems face significant challenges related to co-channel resource contention. These challenges manifest as frequent unnecessary wake-ups of LoRa nodes, data transmission collisions, and substantial increases in energy consumption [4]. Such issues have limited the

scalability and energy efficiency of LoRa networks, gradually becoming critical technical barriers that hinder their practical deployment and widespread adoption [5–7].

To enable effective time-slot scheduling and polling-based directional communication among multiple nodes operating on the same channel, a stable and high-precision clock synchronization mechanism is essential to prevent communication collisions. However, LoRa nodes are typically driven by low-power microcontroller units (MCUs) [8]. The implementation of the TDMA algorithm supported by the STM32 will be elaborated and explained in detail in Section 2; for instance, the STM32F103 series is subject to inherent clock drift caused by oscillator inaccuracies, temperature fluctuations, aging effects, and low-power wake-up offsets [9]. Without proper compensation, this drift can accumulate over time during the scheduling process, eventually causing timing overlaps, incorrect wake-ups, and erroneous data transmissions [10].

In addition to mitigating co-channel interference and ensuring reliable synchronization, the integration of energy-aware scheduling mechanisms has emerged as a critical requirement for next-generation IoT systems, particularly those operating under stringent energy constraints [11]. As the number of battery-powered and energy-harvesting edge devices continues to grow, conventional always-on or periodic listening approaches are becoming increasingly inefficient and unsustainable [12]. To address these limitations, the proposed framework incorporates low-power wake-up signal recognition, selective and context-aware node activation, and adaptive transmission scheduling based on real-time network status and channel conditions [13]. These strategies not only significantly reduce idle listening and redundant transmissions but also enable differentiated quality-of-service (QoS) provisioning for heterogeneous IoT applications [14]. As a result, the system achieves extended node lifetime, reduced energy imbalance across the network, and enhanced scalability and robustness in complex or large-scale deployment scenarios [15].

To address these challenges, this work integrates a sensing–communication integrated (ISAC) framework with advanced parameter estimation techniques tailored for the LoRa channel. The ISAC framework enhances signal detection and physical address recognition, thereby enabling precise node wake-up control under co-channel conditions [16,17]. Meanwhile, parameter estimation improves the accuracy of channel state information, thereby enhancing synchronization precision and mitigating the adverse effects of clock drift. Together, these methods effectively reduce redundant energy consumption and reinforce robust clock synchronization, significantly improving the stability, adaptability, and scalability of LoRa networks in large-scale IoT deployments [18].

The system experiment is implemented based on STM32F103 hardware for networked communication, and the power consumption, false wake-up rate, and time-synchronization range are displayed on the MATLAB R2024a platform.

Targeted point-to-point transmission in co-channel environments is implemented on the hardware testbed, and the overall power consumption and energy-saving metrics are computed via experimental simulation based on the predefined hardware parameters. The main contributions of this work are summarized as follows:

(a). A mapping mechanism between TDMA slots and physical node addresses on the same channel in LoRa networks has been constructed. By precisely mapping time slots to node physical addresses, data collisions and false wake-ups are significantly reduced, resulting in improved network capacity and enhanced energy efficiency in large-scale deployment scenarios.

(b). A directional activation and scheduling framework is proposed, in which integrated sensing and communication (ISAC) is combined with LoRa channel-feature estimation. Through this integration, energy efficiency and scheduling accuracy under co-channel conditions are significantly enhanced.

(c). A lightweight algorithm for bidirectional timestamp synchronization and physical address identification, which is specifically tailored to the resource constraints of low-power STM32 microcontrollers, thereby making it well-suited for edge-node deployment, is designed.

(d). The physical address of the target node is embedded in the LoRa wake-up code. A low-complexity address recognition and node authentication mechanism is employed at the physical layer to enhance system security, whereby interference caused by spoofed nodes and unauthorized access is effectively prevented.

(e). The proposed system is evaluated through comparative simulations and field deployment experiments and is demonstrated to outperform existing approaches in terms of false wake-up rate, data collision rate, and average power consumption. These results provide novel insights into the sustainable operation of LoRa networks in large-scale IoT scenarios.

2. Network Topology and Distribution of Co-Channel Nodes

The method proposed in this study is verified by comparing its performance with that of a typical star-shaped LoRa network with a conventional topology. To verify the feasibility of the proposed method, the STM32F103C8T6 MCU (hereinafter referred to as STM32) is employed as the core controller. The system architecture comprises a LoRa gateway consisting of an STM32 main control module, a LoRa wireless communication module, and a 4G communication module, which collectively handle protocol conversion and cloud connection. The LoRa nodes comprise an STM32 main control unit, a LoRa communication module, and a sensor array, collectively tasked with on-site data acquisition. In this architecture, the integration of a sensing and communication integrated (ISAC) framework and advanced parameter estimation techniques is implemented to enhance the overall performance of the system [19].

The ISAC framework is designed to jointly process sensing and communication tasks, thereby significantly improving signal detection and transmission reliability [20]. Meanwhile, the accuracy of channel state information is refined through parameter estimation, which enables precise physical address identification and robust synchronization under co-channel conditions.

The fundamental capabilities required for TDMA operations are supported by the STM32 microcontroller [21]. Precise time-slot scheduling is enabled by its built-in timers, and rapid response to communication events is facilitated by the interrupt controller, ensuring that the requirements of time synchronization and real-time performance in TDMA systems are satisfied. Table 1 shows the hardware conditions of the STM32 that meet the requirements for TDMA.

Table 1. STM32F103 hardware features that support TDMA operation.

Resource Category	STM32F103 Specifications	Lightweight TDMA Requirements	Is It Satisfied?
CPU clock frequency	72 MHz	<30 MHz	Satisfied
DMIPS	90 DMIPS	5–10 DMIPS	Satisfied
Flash capacity	64/128 KB	12–18 KB	Satisfied
Timer	4 × 16-bit + RTC	1 × 16-bit	Satisfied
Clock accuracy	±20–50 ppm (≤1 ppm after software compensation)	≤5 ppm	Satisfied
SRAM capacity	20 KB	2–4 KB	Satisfied

In large-scale LoRa networks, sensor nodes typically complete data acquisition and reporting via timed triggers or channel switching, then enter a low-power sleep mode during nonoperational periods. Hua-Wei et al. [22]. identified the issue of communication performance in LoRa networks as an urgent problem requiring further investigation. They pointed out that the ALOHA protocol, which adopts a random access mechanism, promotes transmission collisions between devices under the same channel, thereby causing conflicts and degrading the stability of the network. Da-Tao et al. [23]. combined the air wake-up strategy with the channel switching mechanism to reduce network energy consumption. However, their method still employs a collective wake-up approach, which wastes energy when operating under the same channel.

Figure 1 illustrates the distribution of nodes within the same channel area as the gateway, with all communication links being shorter than 1 km. In the experiment, the communication period of a single node is defined as the time, T (in seconds), between the test gateway and a node 1 km away.

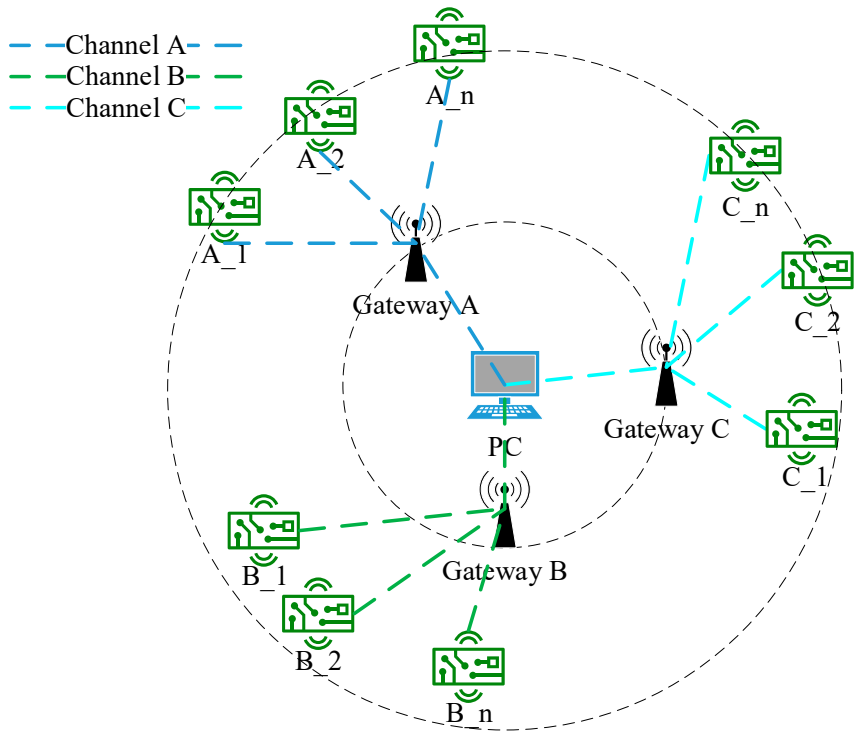

Figure 1. Distribution of nodes within the gateway's co-channel area.

To address this problem, we designed a LoRa same-channel time-division multiple-access (TDMA) slot energy-saving wake-up scheme based on a bidirectional timestamp correction algorithm to address recognition for multisensory low-power polling acquisition scenarios under the same channel with a communication radius of less than 1 km. The scheme primarily addresses two core technical challenges: (i) resolving the time-synchronization error between the gateway and nodes and (ii) mapping between TDMA slots and physical node addresses to mitigate data collisions and unnecessary wake-ups on the same channel.

The hardware of the system operates under a supply voltage of 3.3 V, with 50 nodes configured and a communication packet size of 40 bytes. The MATLAB Simulink platform was used to simulate an urban environment for a communication distance not exceeding 1 km. Physical-layer data transmission and reception at the 915 MHz band are implemented by the SX1278 LoRa module. The LoRa transmission power is set to 14 dBm, with a transmission current of 120 mA and a reception current of 16.8 mA. The MCU idle current

is 15 mA, and the sensor module current—comprising temperature, humidity, GPS, and other modules—is approximately 51 mA. The lowest current consumption occurs in sleep mode, approximately 1.1 mA. The system adopts a time-slot length of 0.5 s (hereinafter denoted as T). Within each time slot, time is allocated to the gateway wake-up phase (M_1) and the data interaction phase (M_2) between the gateway and nodes, while the remaining duration is dedicated to sleep mode. A buffer time of 10 ms between nodes (denoted as T_b hereafter) is configured. Through the rational allocation of duty cycles, efficient switching between active and low-power states is achieved, effectively reducing overall energy consumption. The time-slot length, T; buffer time, T_b; gateway wake-up slot, M1; and data interaction slot, M2, will be elaborated in detail in Section 3.

The following sections of this paper elaborate on the causes of these issues, their solutions, and the implementation process. In addition, the effectiveness of the proposed method is experimentally verified.

3. Key Challenges and Proposed Solutions for the Scheme

3.1. Clock Synchronization Between Gateway and Nodes

3.1.1. Synchronization Problem Between Gateway and Nodes

In LoRa master–slave ad hoc networks, implementing TDMA slot scheduling between the gateway and nodes relies on a high-precision time-synchronization mechanism. However, in large-scale LoRa communication networks, time drift in communication nodes is inevitable. The sources of error are compounded by multiple factors: at the hardware level, the external crystal oscillator of the STM32 has an initial frequency difference (±20–50 ppm), which can be further exacerbated by environmental temperature variations and reduced frequency stability due to long-term use [24].

At the software level, operations such as MCU clock switching, interrupt delays, and low-power wake-up can cause jitter in the timer timestamps. Moreover, if the clock-correction update cycle is too long or the adjustment parameters are incorrect, synchronization errors will persist [25]. Table 2 shows the main factors and typical values of MCU clock drift.

Table 2. Main factors and typical values of MCU clock drift.

Cause of Clock Drift	Typical Error Range
Initial frequency variation of crystal oscillator	±20–50 ppm
Ambient temperature variation	±2 ppm (°C)
Crystal ageing	±0.5 ppm (year)
Low-power wake-up timing	50 ppm
Interrupt latency	0.166 ppm

In the LoRa networking system, the STM32 real-time clock is based on an external 32.768 kHz crystal oscillator (±20 ppm) as the time reference, with the main frequency provided by an 8 MHz crystal oscillator. The time drift is primarily determined by the frequency error of the crystal oscillator; Table 3 shows the typical time drift of a ±20 ppm crystal oscillator. Note that even a slight frequency deviation can accumulate to become a significant synchronization offset over time. Ensuring the long-term stable operation of the TDMA system requires constructing a high-precision, low-power, and periodically correctable time-synchronization mechanism that suppresses the timing deviations caused by crystal-oscillator errors, temperature drift, and long-term aging [26,27]. If the synchronization error exceeds the slot tolerance, it will cause conflicts in the same channel and affect the stability of communication.

Table 3. Typical time drift of a ±20 ppm crystal oscillator.

Duration	Time (s)	Drift Duration (s)
One day	86,400	≈1.728
One month	2,592,000	≈51.84
Half a year	15,552,000	≈311.04
One year	31,536,000	≈630.72

3.1.2. Solutions to Synchronization Problems Between Gateway and Nodes

To achieve time synchronization between the gateway and nodes, the system employs periodic communication time-point setting and a bidirectional timestamp correction algorithm. The gateway acts as the "master clock" for the entire network and is responsible for time calibration of all nodes. The nodes, as subordinate devices, adjust their own timers based on the correction results to align with the gateway's time.

3.1.3. Explanation of Individual Time Slots

The system is based on the STM32 multi-threading architecture and employs the TIM2 timer (32-bit counting, supports capture and compare, and a maximum period of approximately 71 min to prevent frequent overflows) to construct periodic communication moments. The timing trigger mechanism causes the timer interrupt to wake the gateway and nodes at the preset communication time points. These network elements execute TDMA slot data interaction and generate timestamps, thereby achieving initial time synchronization across the entire network. The process involves the following two steps:

Step 1: The communication time points between the gateway and each node are set. The gateway and nodes utilize homogeneous STM32 control boards (which can achieve a resolution of 1 μs when the clock is multiplied to 72 MHz). After initialization, the communication thread is initiated with a unified time reference, T_0, as the starting point. To enhance the system robustness, a buffer time, Tb, is set between two adjacent single-node communication cycles to initialize the LoRa module and avoid slot overlap, thereby ensuring the stability and reliability of communication. On this basis, the communication time points are set with a period equal to the "single-node communication time, T, plus buffer time, T_b." To have orderly slot scheduling, the node slots are allocated in sequence through polling. Figure 2 shows the communication time points between the gateway and nodes.

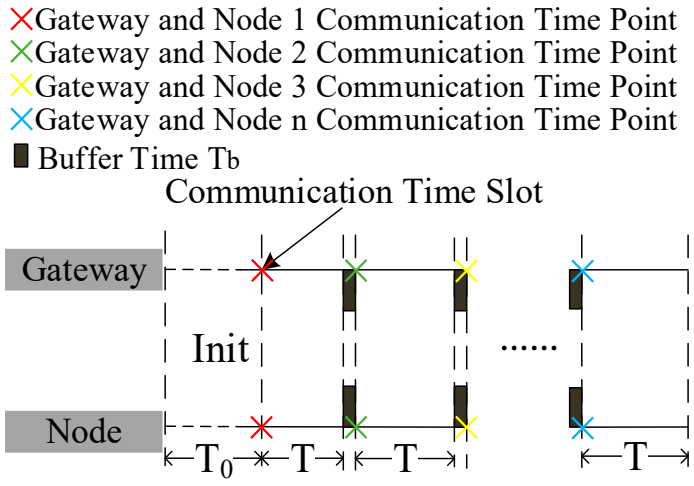

Figure 2. Communication time points between gateway and nodes.

Step 2: Bidirectional timestamp correction algorithm [28]. With this mechanism, the gateway and nodes exchange two rounds of request and response messages to achieve

high-precision time synchronization. More specifically, at the reference time, T_0 (the same as T0 in Step 1), the gateway sends a wake-up code to the target node and records the transmission time as T1_send. The target node records the time at which it receives the wake-up code as T2_recv and then sends a response message via the LoRa communication. The time at which the response is sent is recorded as T2_send. The gateway records the reception time of the response as T1_recv.

3.1.4. Detailed Process of the Bidirectional Timestamp Correction Algorithm

Based on the four key timestamps T1_send, T2_recv, T2_send, and T1_recv, the system applies the symmetric delay assumption and relevant algorithms to calculate the time deviation between the node and the gateway. The local clock is then adjusted accordingly to achieve precise time synchronization between the node and the gateway. This bidirectional timestamp mechanism compensates somewhat for the delay caused by link transmission, thereby improving the synchronization between the gateway and the nodes. Figure 3 illustrates a schematic diagram that describes the bidirectional timestamp correction, providing an intuitive representation of the processes involved in time synchronization and timestamp acquisition.

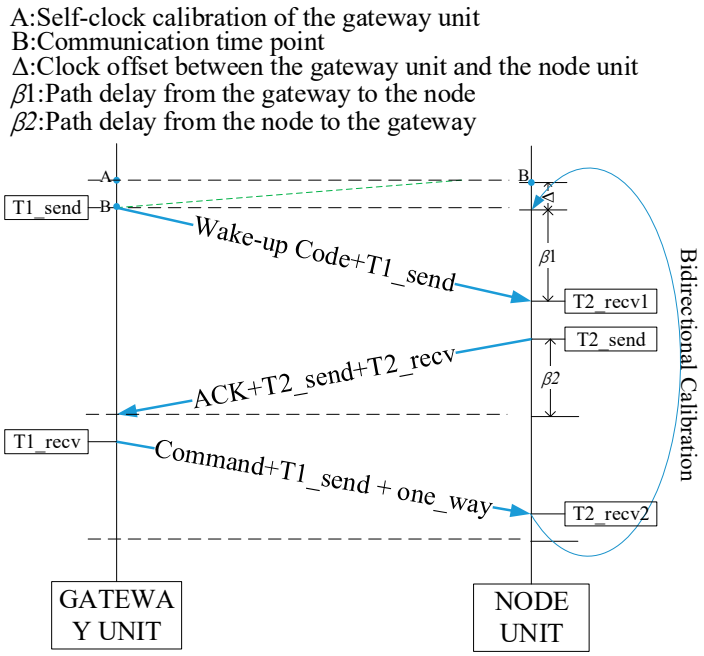

Figure 3. Bidirectional timestamp correction.

The round-trip delay can be calculated by determining $\beta 1$ (propagation delay from gateway to node) and $\beta 2$ (propagation delay from node to gateway) using the four timestamps. $\beta 1$ and $\beta 2$ are calculated as follows:

$$\beta 1 = \mathrm{T2_{recv}} - \mathrm{T1_{send}} + \Delta \tag{1}$$

$$\beta 2 = \mathrm{T1_recv} - \mathrm{T2_send} - \Delta \tag{2}$$

$\beta 1$ is the propagation delay from the gateway's signal transmission to the node's signal reception, $\beta 2$ is the propagation delay from the node's signal transmission to the gateway's signal reception, and Δ is the clock offset between gateway and node. If the round-trip path is symmetric, we obtain

$$\beta 1 = \beta 2 \tag{3}$$

The clock offset, Δ, between gateway and node can then be calculated as follows:

$$\Delta = [(T1_{send} - T2_{recv}) + (T1_recv - T2_send)]/2 \quad (4)$$

Based on the measured time offset between the gateway and the node, the deviation can be dynamically corrected in the subsequent communication. The TIM2 timer is reconfigured for compensation, thereby ensuring the consistency and synchronization of the system clock.

3.1.5. Description of GPS Time Synchronization and Its Alternative Solutions

During actual communication, nodes may experience local clock deviations from the gateway due to brief power outages, thereby causing gateway–node desynchronization. To enhance the system's capability to resynchronize under abnormal conditions, the node unit can be integrated with a GPS module, utilizing its provided high-precision UTC time as the clock reference. By parsing the time field in the NMEA sentences output by the GPS, the node writes the UTC time into the STM32′s internal real-time clock, thereby rapidly recovering and precisely calibrating the node clock. Combined with the timestamp correction mechanism, TDMA slot scheduling can be optimized in terms of synchronization and stability, which helps to reduce the probability of slot overlap and minimize communication conflicts caused by clock drift. Table 4 details the advantages of GPS time synchronization.

Table 4. Description of GPS time synchronization.

Advantages of GPS Time Synchronization	Application Notes
High accuracy (<1 ms)	Suitable for strict TDMA synchronization demands
Independent of network	Suitable for outdoor scenarios and pastoral and mountainous areas
Single alignment maintains long-term accuracy	Avoids frequent broadcast synchronization
Globally unified	Enables cross-regional deployment

Due to frequent GPS signal obstructions in indoor environments, underground spaces, or densely built urban areas, time synchronization may become unreliable. To overcome this limitation, the LoRa central node can periodically broadcast synchronization beacons embedded with precise timestamps. After receiving these signals, terminal nodes estimate the signal propagation delay and subsequently adjust their local clocks using internal timers. Consequently, clock alignment with the gateway can be achieved without relying on GPS, thereby enabling robust TDMA operation in GPS-denied scenarios [29].

3.2. Collective Invalid Wake-Up in LoRa Nodes and Associated Countermeasures

3.2.1. Collective Invalid Wake-Up in LoRa Nodes

In master–slave communication networks, the gateway that sends a synchronous wake-up command via broadcasting activates all nodes within the same channel. This broadcast leads to numerous invalid wake-ups and increases the system's energy consumption. For example, assume that 100 nodes are deployed in the same channel; during a single communication cycle, the 99 nontarget nodes are unnecessarily woken, resulting in a redundant power consumption overhead that is 99 times the required amount [30]. In LoRa-based co-channel scenarios, adaptive channel estimation is employed to accurately detect changes in the number of communicating nodes within the link [31,32]. Figure 4 shows a typical power consumption composition diagram for a LoRa node.

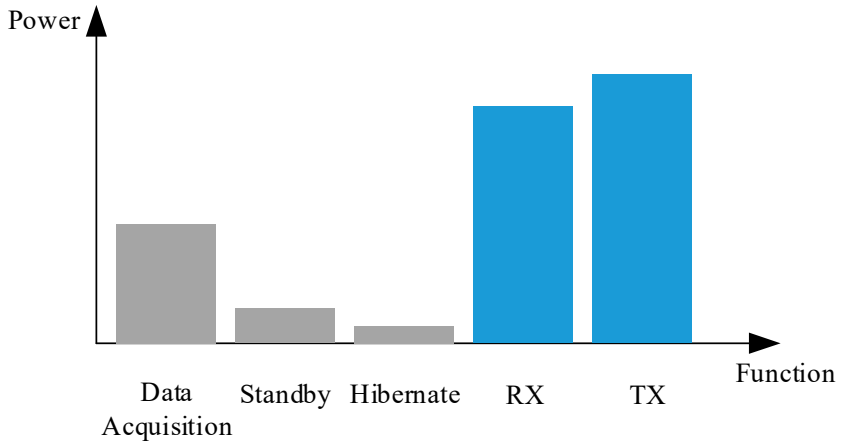

Figure 4. Schematic diagram showing typical power consumption composition for a LoRa node.

3.2.2. Countermeasures for Collective Invalid Wake-Up of LoRa Nodes

A static time-slot allocation strategy based on TDMA is used to synchronize the clocks of the LoRa gateway and LoRa nodes. The single-node communication period, T, (the same T as mentioned earlier) is divided into two functional time slots: the gateway wake-up time slot, M1, and the data interaction time slot, M2, between the gateway and the node. Each node is scheduled in a predefined sequence to form a periodic polling communication mechanism.

To precisely manage and directionally wake multiple nodes, the communication system incorporates an address-slicing mechanism. To uniformly configure channel parameters, network identifiers (NetIDs), and air rate, a unique LoRa module address is assigned to each terminal node, ensuring unique and recognizable NetIDs at the address level. Within the wake-up time slot, M1, a wake-up frame data packet is sent downstream by the gateway with a payload consisting of the unique module address of the target node. As shown in Figure 5, the wake-up data frame has the following fields: preamble (for channel synchronization), synchronization byte (for protocol synchronization between devices), flag byte (containing communication configuration flags), length byte (indicating the length of the subsequent payload), payload (containing the address of the LoRa module of the target node), and a cyclic redundancy check (CRC, for data packet verification).

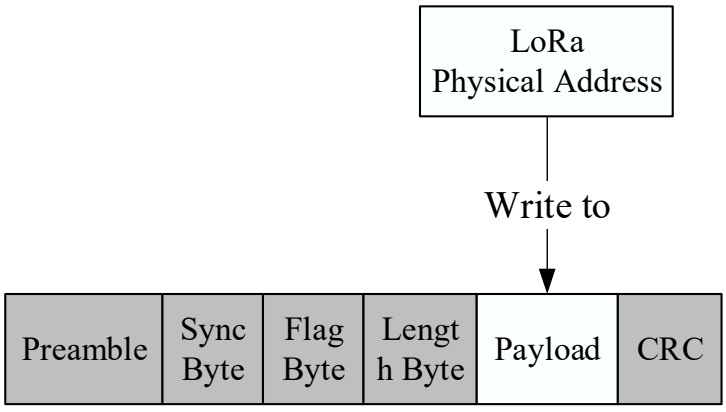

Figure 5. Wake-up data frame with the target node's module address embedded.

3.2.3. MCU-Based Wake-Up Frame Parsing with ISAC-Driven Coordination

At the preset communication time point, the corresponding target node is awakened and switched to working mode to monitor the downstream wake-up frame. Once the MCU receives a complete data packet, it parses and extracts the module address field

for comparison. Subsequently, it responds and enters the data transmission phase. In this process, the signal detection and address recognition are jointly optimized by the sensing and communication integrated (ISAC) framework, thereby enhancing the accuracy of the target-node identification. Meanwhile, the timing synchronization is refined by the parameter estimation techniques, ensuring precise wake-up control and reliable data transmission. Nontarget nodes not in the current communication time slot remain in sleep mode, with the wireless communication module and noncritical peripherals disabled to minimize the overall system power consumption to the greatest extent. Figure 6 shows the status of the target node at the communication time point.

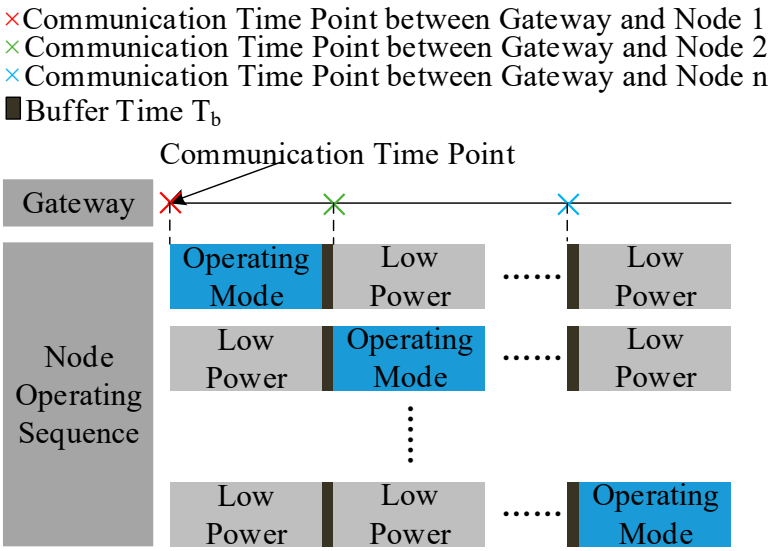

Figure 6. Status of the awakened node at the communication time.

3.2.4. Binding of M1/M2 Time Slots to LoRa Module Addresses

Given that the peripheral configurations and main control MCUs of the nodes are consistent, the duration of the two functional time slots, M1 and M2, can be set based on the relative relationship between the wake-up time point and the data transmission deadline. On this basis, the system achieves directional transmission of wake-up commands and data interaction between nodes through time-slot division, thereby reducing the interference issues caused by collective wake-up in the same channel environment. Figure 7 shows 100 nodes in the same channel as an example of the "time slot–LoRa block address" mapping relationship.

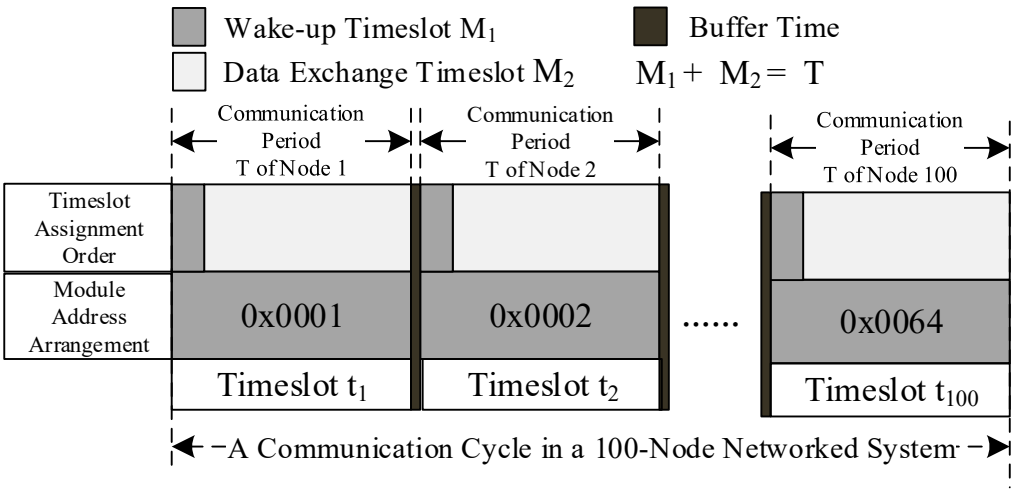

Figure 7. Mapping of time slots to LoRa block addresses.

3.3. Detailed Procedure for Time Synchronization Between Gateway and Nodes

3.3.1. End-to-End Communication Workflow of the LoRa System

With the bidirectional timestamp correction mechanism and the "time slot–LoRa module address" mapping strategy, communication between the gateway and nodes is characterized by high efficiency and temporal consistency. Figure 8 shows the interaction flowchart for the communication between the gateway and nodes. It illustrates the communication and time calibration between the gateway and nodes. The gateway takes the initiative to wake the nodes, issue commands, and receive data. The nodes respond, record timestamps, and report back to the gateway. The gateway corrects the time drift caused by factors such as interrupt response and transmission delay by applying a bidirectional timestamp correction algorithm. In each communication cycle (the pre-compensation period preceding single-node communication), this closed "wake-up, response data, transmission calibration" loop is repeated to precisely synchronize the gateway time, which is consistent with the periodic calibration mechanism to ensure temporal accuracy.

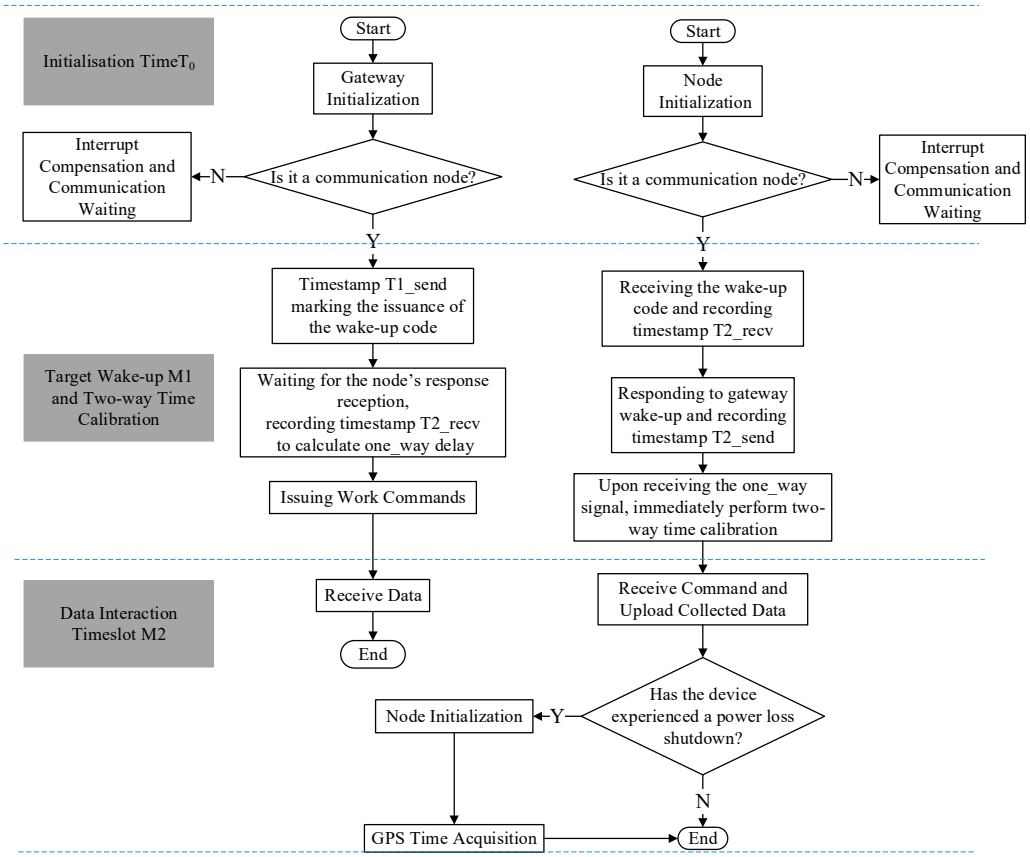

Figure 8. Flowchart of gateway–node interaction.

3.3.2. Communication Time Synchronization Process Between Adjacent Nodes

The gateway corrects the time drift caused by factors such as interrupt response and transmission delay by applying a bidirectional timestamp algorithm. Throughout the LoRa master–slave topology, the closed-loop "wake-up–response–timestamp calibration" procedure is cyclically executed. In this process, the sensing and communication tasks are jointly processed by the sensing and communication integrated (ISAC) framework, and the timing synchronization is refined by the parameter estimation techniques, thereby enhancing the reliability of node identification and the precision of wake-up scheduling.

Taking as an example two adjacent nodes (Node 1 and Node 2), the gateway broadcasts a wake-up frame carrying the target address (Node 1) at the preset communication time

point. At this time, only Node 1 listens to the matching address within its time slot, thereby waking the main control unit and realizing a point-to-point mesh communication architecture. The bidirectional time synchronization is executed to precisely correct the time. During this process, the gateway and the node respectively record four key timestamps (T1_send, T2_recv, T2_send, and T1_recv), which are used to calculate the time offset based on the symmetric delay model corrected to deliver high-precision time alignment. After completing synchronization, the node enters the data acquisition and uplink phase, and the gateway switches to the next node for polling communication. Figure 9 shows the process for communication calibration between adjacent nodes.

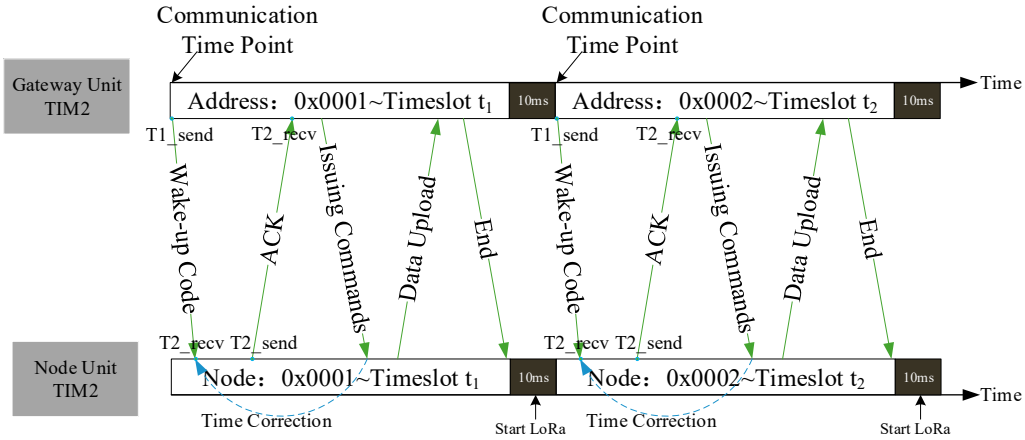

Figure 9. Neighboring-node communication calibration process.

For Node 2 and the remaining nodes not currently scheduled, the LoRa module remains in sleep mode, and the main controller remains in a low-power standby state outside the preset communication time points, thereby reducing the system's overall power consumption. Before the communication rotation reaches the time slot corresponding to Node 2, the system reserves a buffer time of approximately 10 ms to initialize the LoRa module, ensuring seamless access to the next time slot and thereby organically integrating precise node scheduling with low-power operation.

4. Experimental Results

The MATLAB Simulink platform was used to simulate an urban environment for a communication distance not exceeding 1 km. The simulation comprised one gateway and 50 nodes sharing the same channel. The communication distance was incremented in 20 m steps, with 5000 iterations conducted at each distance to statistically evaluate the time-synchronization error between the gateway and nodes. In this study, key performance metrics—such as overall energy consumption and node wake-up frequency—are systematically compared for LoRa networking under three typical communication modes: traditional broadcast, ALOHA, and LoRaWAN Class B.

Figure 10 shows the synchronization errors between the gateway and nodes at different distances. Although path loss, obstruction, and channel fading may introduce delay jitter, the system effectively suppresses physical-layer interference by combining bidirectional timestamp calibration with exponential moving average filtering. As a result, synchronization errors are primarily determined by the timestamping algorithm and the stability of the node clocks.

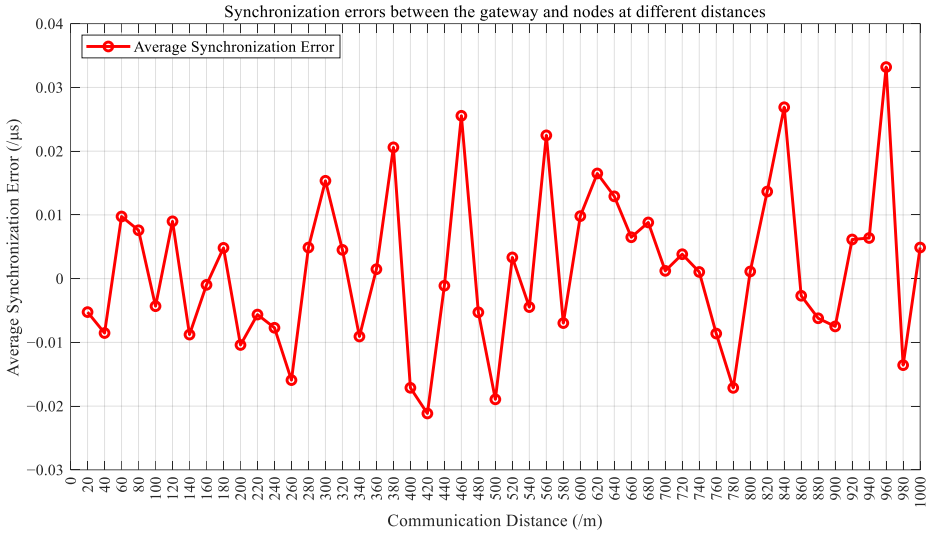

Figure 10. Synchronization errors between the gateway and nodes at different distances.

The simulation results show the range of the synchronization error of 50 nodes sharing the same channel as a function of communication distance. For each distance, 5000 iterations were performed to obtain stable and statistically significant results. Using a step size of 100 m, the system recorded the synchronization-time error of all nodes relative to the gateway during each simulation round. After completion, the minimum and maximum synchronization errors of all nodes at each distance point were extracted to determine the range of variation in the error at the given communication distance. Table 5 shows the range of synchronization error extrema at different distances.

Table 5. Range of synchronization error extrema at different distances.

Co-Channel Node Count	Distance (m)	Range of Synchronization Error (μs)
50	1000	[−91.4, 124.1]
50	900	[−98.1, 113.3]
50	800	[−128.8, 120.2]
50	700	[−130.7, 212.0]
50	600	[−135.6, 169.3]
50	500	[−112.7, 111.5]
50	400	[−117.3, 139.7]
50	300	[−130.9, 126.1]
50	200	[−102.5, 169.5]
50	100	[−129.1, 159.3]

The synchronization errors in Table 4 are defined as "node time minus gateway time," so negative (positive) values indicate that the node's clock precedes (lags behind) the gateway's clock.

In a typical LoRa networking scenario with nodes sharing the same channel, this study compares the "time slot–LoRa address mapping" mechanism with the traditional broadcast-based wake-up method in terms of the number of erroneously awakened nodes. Figure 11 compares invalid wake-ups. In conventional LoRa gateway communication, wake-up commands are broadcast to all terminal nodes sharing the same channel. Although only a few nodes actively participate in communication, all other nodes are passively woken upon receiving the signal, resulting in unnecessary activation and a significant waste of energy. As the network scale expands, the number of falsely woken nodes increases linearly, significantly increasing the system's total energy consumption.

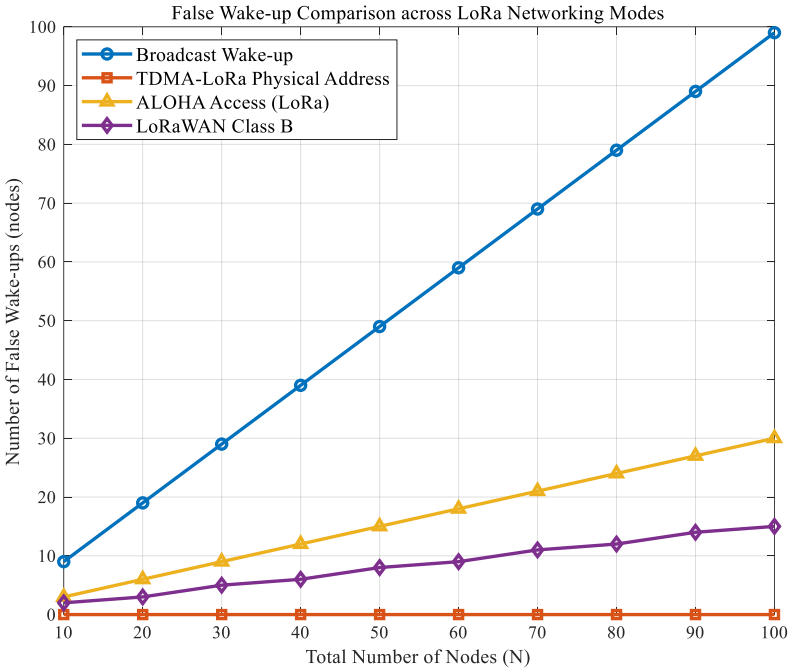

Figure 11. The number of erroneously woken nodes for broadcast wake-up compared with the same for TDMA directional wake-up.

Compared with the traditional broadcast approach, the proposed directional wake-up mechanism based on TDMA time-slot and node address mapping enables precise control of target nodes, while nontarget nodes remain in sleep mode during unassigned slots, thereby reducing the system's overall energy consumption. Experimental results demonstrate that, for networks of varying scales, the proposed mechanism consistently maintains the number of falsely awakened nodes at zero, effectively preventing collective activation issues in same-channel environments. For same-channel LoRa networking, Figure 12 compares (i) the overall network power consumption between the proposed "TDMA time slot–LoRa address mapping" mechanism and (ii) the traditional LoRa gateway broadcast communication and (iii) the overall network power consumption under the LoRaWAN Class B and ALOHA communication modes. In the traditional broadcast mode, all nodes are simultaneously awakened for each communication, causing the system's overall energy consumption to accumulate linearly with the number of nodes. In LoRaWAN Class B mode, wake-up timeouts are frequently experienced by nodes during the scheduled beacon periods. In ALOHA mode, due to the random access nature of nodes, a high probability of collisions is encountered, resulting in increased energy consumption. In contrast, under the TDMA-based directional wake-up mechanism, nontarget nodes operate only in low-power sensing mode, significantly reducing energy consumption. After data collection from 50 nodes, the energy consumption under the traditional acquisition mode is approximately 4.9 times that of the TDMA-based directional wake-up mechanism. The simulation results indicate that the energy savings increase with the number of LoRa nodes sharing the same channel.

The total energy consumption of a node is obtained by summing the products of current, voltage, and duration across its operating states. Specifically, energy consumed during the sensor's sleep state is calculated as the product of the sleep current, sleep voltage, and sleep time. Similarly, the LoRa module's transmission and reception energy are computed by multiplying their respective currents, voltages, and durations. Energy consumption during the sensor's active state is calculated likewise. Summing these components yields the total energy consumption for the communication cycle. All electrical parameters are

in amperes and volts and the time is in seconds, resulting in energy expressed in joules (J). This approach effectively profiles node energy use across states, facilitating accurate system-level efficiency evaluation.

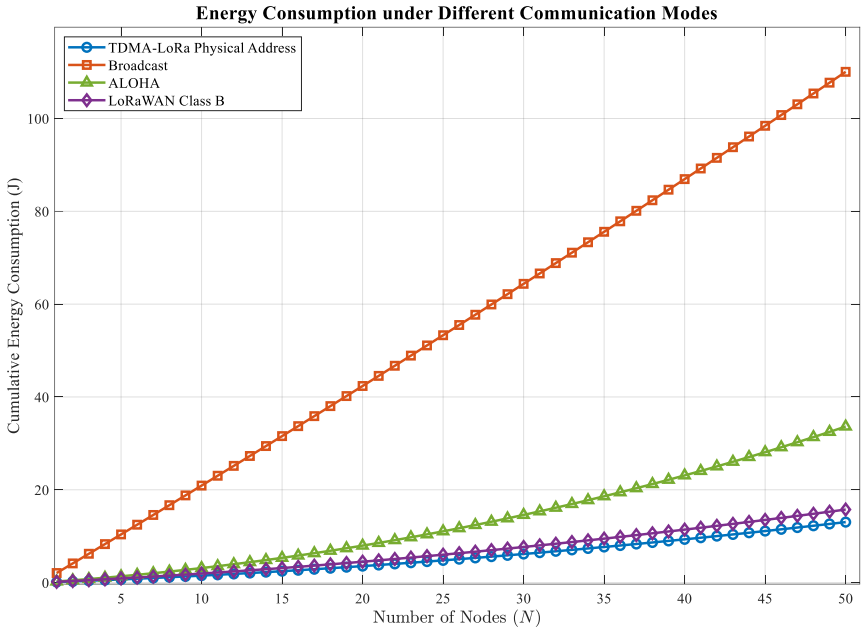

Figure 12. Comparison of overall network power consumption.

Networks of varying scales sharing the same channel were constructed with increments of 30 nodes. For each network size, 5000 simulations were conducted to minimize random errors. Table 6 presents the cumulative energy consumption of the network system, which forms the basis for evaluating the energy efficiency of the TDMA mechanism versus the traditional broadcast mechanism over different network scales.

Table 6. Cumulative energy consumption of the network system.

Number of Nodes	Traditional Method Cumulative Energy (J)	TDMA Cumulative Energy (J)
20	84.42	
50	538.35	17.52
80	1385.00	281.44
110	2624.50	532.28
140	4256.60	862.37

5. Conclusions

This paper proposes a LoRa same-channel TDMA wake-up mechanism that integrates a bidirectional timestamp correction algorithm with physical address recognition. Additionally, buffer scheduling and GPS-assisted time calibration are employed to enhance synchronization accuracy and communication stability in large-scale deployments. The scheme incorporates sensing and communication integration (ISAC) alongside parameter estimation of the LoRa channel, which collectively improves signal detection and target-node identification accuracy. By implementing a "time slot–LoRa module address" mapping, the gateway can selectively wake specific nodes, effectively reducing interference and redundant energy consumption compared to traditional broadcast methods. The bidirectional timestamp calibration algorithm ensures precise clock synchronization between nodes and the gateway, maintaining synchronization errors within ± 1 ms. Overall, the proposed approach effectively mitigates collective wake-up, channel conflicts, and

high energy consumption in large-scale LoRa deployments, making it well-suited for IoT applications such as livestock farming and environmental monitoring.

Author Contributions: System design, algorithm proposal, and theoretical analysis: Z.X. and H.J. Implementation of bidirectional timestamp correction and address recognition mechanism: Z.X. and Y.L. Simulation construction, data collection, and result evaluation: Z.X., Y.L. and G.Y. Manuscript writing, editing, and review: Z.X. and G.Y. All authors have read and agreed to the published version of the manuscript.

Funding: This work was partly supported by the National Natural Science Foundation of China (Grant No: 62261056) and the Qinghai Minzu University Key Scientific Research Project in Science and Engineering (Grant No: 2024XJZD01).

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

Abbreviations

The following abbreviations are used in this manuscript:

LoRa	Long-range
ISAC	Sensing and communication integrated
TDMA	Time-division multiple access
IoT	Internet of Things
LPWAN	Low-power wide-area networks
MCU	Microprocessor control units

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