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NBTI-Aware Transient Fault Rate Analysis Method for Logic Circuit Based on Probability Voltage Transfer Characteristics

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Abstract: The reliability of Very Large Scale Integration (VLSI) circuits has become increasingly susceptible to transient faults induced by environmental noise with the scaling of technology. Some commonly used fault tolerance strategies require statistical methods to accurately estimate the fault rate in different parts of the logic circuit, and Monte Carlo (MC) simulation is often applied to complete this task. However, the MC method suffers from impractical computation costs due to the size of the circuits. Furthermore, circuit aging effects, such as negative bias temperature instability (NBTI), will change the characteristics of the circuit during its lifetime, leading to a change in the circuit's noise margin. This change will increase the complexity of transient fault rate estimation tasks. In this paper, an NBTI-aware statistical analysis method based on probability voltage transfer characteristics is proposed for combinational logic circuit. This method can acquire accurate fault rates using a discrete probability density function approximation process, thus resolving the computation cost problem of the MC method. The proposed method can also consider aging effects and analyze statistical changes in the fault rates. Experimental results demonstrate that, compared to the MC simulation, our method can achieve computation times that are two orders of magnitude shorter while maintaining an error rate less than 9%.

Keywords: VLSI circuit; transient fault; aging effects; voltage transfer characteristics; discrete probability density function approximation

1. Introduction

Reliability issues have become a vital concern for Very Large Scale Integration (VLSI) design due to the continued scaling of VLSI technology and supply voltage. Among these reliability issues, transient faults caused by environmental effects, such as electrical noise, particle strikes, and electromagnetic coupling, are primary failure mechanisms [1]. In contrast to permanent faults, transient faults are temporary deviations of a circuit's state from its correct or reference state. The occurrence of transient faults has certain random characteristics; therefore, statistical analysis methods are required to accurately analyze the effects of such faults on circuit performance [2]. In the past, environmental induced transient faults used to be a concern only in regarding memory because of the following two reasons. Firstly, the density of memory circuits is much higher than logic circuits, which makes the memory circuits contain the largest number and density of bits susceptible to transient fault. Secondly, the three masking factors affect the propagation of a transient fault through combinational circuit, which include logical masking, electrical masking and latching-window masking. However, in the last decade, supply voltage continues to diminish in value with current scaling trends, causing a decrease in the impact of these masking factors on logic circuits [3,4]. Furthermore, the high density and high

speed of VLSI circuits also make the digital logic circuit more susceptible to transient faults induced by noise [5]. This trend will become more severe as the feature size of Complementary Metal Oxide Semiconductor (CMOS) devices approaches 22 nm, or even smaller scales, in the near future. Therefore, it is critical to model, analyze, and mitigate the impact of transient faults on VLSI circuits.

Existing transient fault mitigation methods can be generally classified into two categories: fault avoidance and fault correction methods. The first category generally exploits device fabrication processes to reduce the transient fault occurrence. These methods include the silicon-on-insulator process [6], the gate resizing strategy [7], and various other methods. The second category of methods functions at the circuit level or system level of abstraction to alleviate transient fault effects. Partial duplication [8], redundancy addition/removal [9], Delay Filtered Dual Interlocked storage Cell (DF-DICE) [10], and algorithmic noise tolerance (ANT) [11] are some typical methods used to address this issue. All of the above techniques suffer from area and energy overhead; therefore, to effectively and efficiently implement these mitigation methods, circuit designers require an accurate and fast transient fault modeling and analysis method to identify the part of a VLSI circuit that is most sensitive to transient faults. However, transient fault analysis has been difficult to implement due to the random characteristics of circuit design specifications, such as supply noise and input signal distribution. Therefore, statistical estimation methods are required to encapsulate all of these design conditions. Monte Carlo (MC) simulation is often applied to accomplish this task. However, the MC method suffers from an impractical computation cost due to the size of the circuits, and more efficient analysis methods are required.

In addition to transient faults, aging effects, such as hot carrier injection (HCI), time-dependent dielectric breakdown (TDDB), electro-migration (EM), and negative bias temperature instability (NBTI), are also major causes of VLSI reliability issues. Among these aging effects, NBTI is the main mechanism of circuit failure when the feature size approaches the 65 nm scale. NBTI occurs when positive-channel Metal Oxide Semiconductor (pMOS) transistors are negatively biased, which causes a shift in the threshold voltages (Vth) [12]. The reaction-diffusion (R-D) model is a widely used physical model for NBTI effect [13]. Yu Cao *et al.* developed a long-term Vth calculation formula based on the R-D model and noted that degradation caused by NBTI effect could cause a delay fault [14]. Moreover, NBTI may cause significant noise margin changes for digital circuits during the entire lifetime of circuits [15], and thus, transient fault rates are difficult to estimate. In [16], the authors proposed a methodology for modeling the transient fault propagation characteristics in the presence of process variation effect and obtained accurate estimation of transient fault rates for logic circuits. However, transient fault rate analysis under the influence of both environmental noise and aging effects has not yet been investigated in detail.

In this paper, we propose an NBTI-aware statistical analysis method to address transient fault rate estimation for combination logic circuit that considers both environmental noise and the NBTI effect. Our work is based on probability voltage transfer characteristics (PVTC) analysis and statistical modeling, which can provide accurate and efficient estimation of NBTI-aware transient fault rates, along with available statistical static timing analysis tools (SSTA) [17]. It should be noted that by introducing high-k/metal gate transistors in sub-45-nm technology, the PBTI effect becomes comparable to the NBTI effect [18]. Since the degradation effect of PBTI is similar to that of NBTI, the proposed approach can be easily extended to consider the PBTI effect as well.

The remainder of the paper is organized as follows. In Section 2, the principle of PVTC method is described. The procedure for performing PVTC analysis for single- and multi-gate circuits is presented. The NBTI-aware transient fault rate estimation is also introduced. Verification of the effectiveness of the proposed method by comparing the transient fault rate estimation results between the PVTC method and MC simulation is presented in Section 3. Moreover, the NBTI effect on changes in circuit characteristics and transient fault rates are also discussed. Conclusions are presented in Section 4.

2. Methodology

In recent years, noise-induced transient faults and circuit aging effects are two main mechanisms of VLSI circuit failure during its lifetime. These effects will change the timing and voltage levels of logic gates and can induce timing errors, voltage level distortion, or bit-flips when the influence accumulates to a certain degree. Most of the current transient fault analysis methods model the noise induced fault as a transient glitch and analyze the propagation characteristics of the glitch in the logic circuit. They focus on the timing errors of the circuit and apply the state-of-art statistical static timing analysis method to evaluate the timing effect. However, with respect to the voltage level, efficient analysis methods have not yet been studied in detail.

In VLSI design, sequential logic circuits are typically partitioned into pipeline stages separated by latches, as shown in Figure 1.

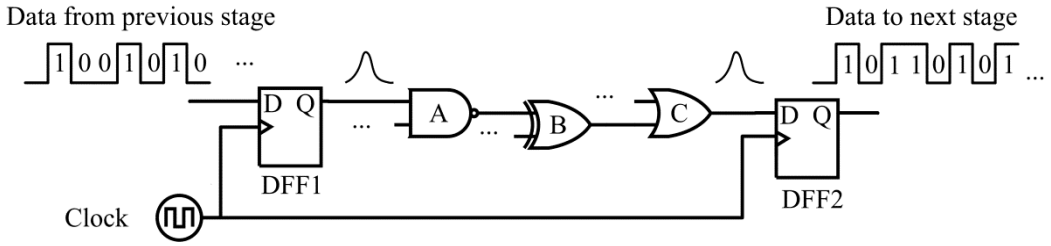

Figure 1. Pipeline stage structure of digital sequential circuits.

As shown in Figure 1, a noise-induced voltage transient (at the input port of NAND gate A) can become a voltage or timing fault only if it propagates to the end of one pipeline stage (at the input port of DFF2) and is stored in the latch. Thus, although hundreds of logic gates may exist in one pipeline stage, only the gates connected to the latch inputs are required to estimate the transient fault rates at the gates, and the computational complexity can be dramatically reduced. According to the characteristics of a CMOS logic circuit, the probability that a logic state is stored in the latch depends on the voltage level at the data input of that latch during the sampling time window. Because the noise-induced voltage transient arrives at the input of the latch at any point in the clock cycle with an equal probability, a high occurrence probability for the voltage transient will result in a high probability that the wrong logic state is captured by the latch. Therefore, the statistical analysis method proposed in this paper is applied to estimate the probability density function (pdf) of the voltage level at the end of one pipeline stage in the presence of noise effects. In a digital system, considering the low-pass characteristics of the logic gates and the central limit theorem, the effects of noise can be generally modeled as variations following a normal distribution in terms of the supply voltage and input signal of the pipeline stages, and MC simulation is commonly used to analyze these effects on circuit performance. However, the computational cost of MC is extremely high due to the complexity of the circuit. Some improved MC methods have effectively decreased the computational costs for transient fault rate analysis [19,20] and have shortened the MC computation time. However, these methods do not consider the effects of some potential circuit characteristic changes in the analysis framework, such as aging effects, which undermine the accuracy of the analysis results during the lifetime of the circuit. Thus, in this paper, we propose a new NBTI-aware statistical analysis method to acquire accurate transient fault rates for different parts of the circuit to resolve the high computational cost problem of MC method. The design flow of the proposed method is shown in Figure 2.

As shown in Figure 2, when the random effects of circuit characteristics are not considered, the input and output relationship of VLSI circuits can be determined by the conventional static voltage transfer characteristics (SVTC) method. However, the input signal and supply voltage of the logic circuits are random variables instead of static values due to the effects of environmental noise. Therefore, the SVTC method is not sufficient to accurately calculate the output of logic circuits, and a statistical analysis method based on probability voltage transfer characteristics (PVTC) is proposed.

Moreover, our method can also consider the effect of NBTI aging on circuit characteristics and analyze statistical changes in transient faults under NBTI effect such that the transient fault rates for different parts of VLSI circuits can be estimated accurately.

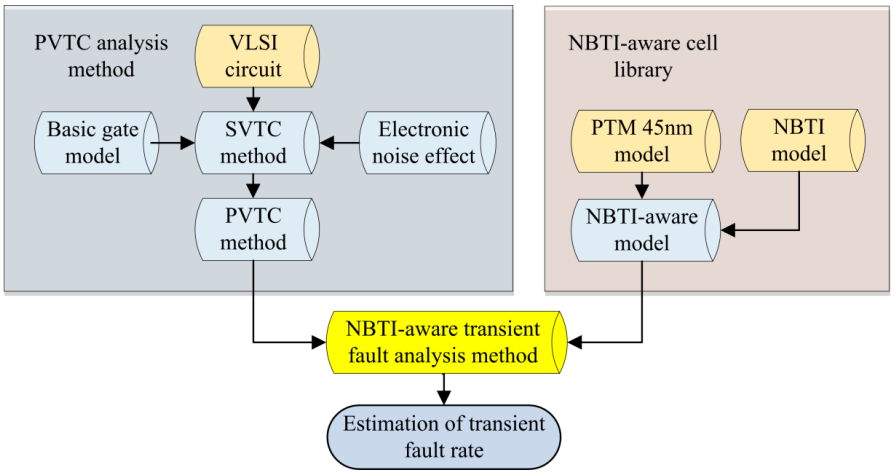

Figure 2. NBTI-aware transient fault rate analysis framework based on the PVTC method.

2.1. PVTC-Based Analysis for Single Logic Gates

In VLSI design, a combinational circuit is composed of basic logic gate cells; thus, the transient fault analysis method begins with a single logic cell. In this paper, to describe the random characteristics of noise-induced effects, we apply a voltage level probability density function (pdf) to describe the input signal and supply and propose a PVTC method to establish the relationship between the input and output voltage pdf distributions of the logic gates. The basic scheme of the PVTC modeling method for logic gates is shown in Figure 3.

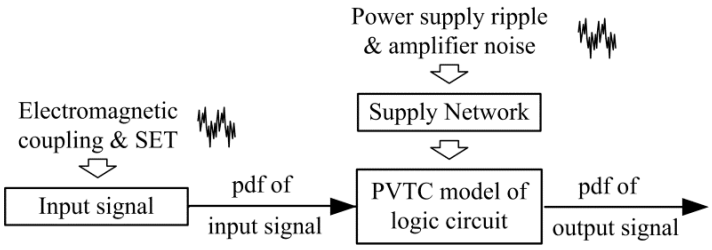

Figure 3. Diagram of the PVTC modeling method.

As shown in Figure 3, the function relationship between the voltage level of the input signal and output signal can be acquired by the PVTC model. Figure 4 provides an illustration of the procedure for establishing the PVTC model for an inverter gate.

Figure 4a presents an SVTC curve for an inverter gate by SPICE DC analysis, and the pdf of the input signal can be modelled as a random variable following a normal distribution due to the environmental noise effects, as shown in Figure 4c. Figure 4a,c show that the probability of the input signal falling into the shaded area $[V_{in1}, V_{in2}]$ is equal to the probability of the output signal falling into the shaded area $[V_{out1}, V_{out2}]$, and this relationship can be expressed as

$$P\left(V_{out2} < V_{out} \leqslant V_{out1}\right) = P\left(V_{in1} \leqslant V_{in} < V_{in2}\right) \tag{1}$$

However, Figure 4b illustrates that in the practical construction of an SVTC curve, instead of a continuous curve, only a series of discrete points can be acquired because of the actual characteristics

of DC analysis. Therefore, the corresponding output signal point V_o for any input signal point V_i may not be found exactly in the discrete SVTC curve, which is necessary for the probability calculation in Equation (1). Thus, a discrete pdf approximation process must be used to implement the calculation. First, the input range of the signal is divided into a sequence of equal-length intervals by DC analysis, and the length of each interval is dV_{in}, which can be set in the analysis process. We assume that, for each point ($V_{in,i}$, $V_{out,i}$) in the SVTC curve (e.g., point D in Figure 4b), input signals falling into area $[V_{in,i} - dV_{in}/2, V_{in,i} + dV_{in}/2]$ or the corresponding output signal of area $[V_A, V_C]$ all have the same voltage $V_{out,i}$. Furthermore, the approximation error can be tolerated because the division interval of dV_{in} is small. Then, the probability of the output voltage level being equal to $V_{out,i}$ can be calculated as

$$P\left(V_{out,i}\right) = \int_{V_A}^{V_C} p\left(V_{in}\right) dV_{in} \tag{2}$$

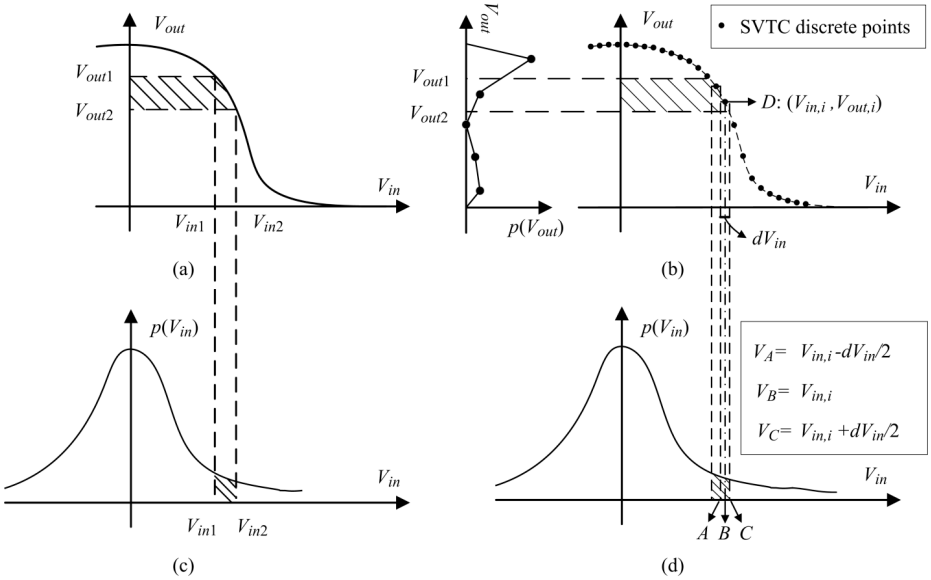

Figure 4. Principle of the PVTC method for an inverter gate. (**a**) SVTC curve for an inverter gate; (**b**) Calculation of output signal's pdf; (**c**) Voltage pdf for input signal V_{in}; (**d**) Division of V_{in}'s pdf.

Subsequently, to calculate the probability of the output signal falling into area $[V_{out2}, V_{out1}]$, we search for all points ($V_{in,i}$,$V_{out,i}$) having an output signal belonging to this area in the SVTC curve. All of the $P(V_{out,i})$ of these points are then accumulated, and the probability of the output signal falling into the given area can be acquired. In the pdf calculation process, the gap between V_{out1} and V_{out2} is set to a small interval dV_{out}; therefore, the pdf of area $p(V_{out})$ can be estimated as

$$p\left(V_{out}\right) \cdot dV_{out} \cong P\left(V_{out2} < V_{out} \leqslant V_{out1}\right) \cong \sum_i P\left(V_{out,i}\right) \cong \sum_i \int p\left(V_{in,i}\right) dV_{in} \tag{3}$$

where ($V_{in,i}$, $V_{out,i}$) is the *ith* point on the SVTC curve with $V_{out2} < V_{out,i} \leqslant V_{out1}$.

PVTC analysis for gates with multiple input ports, such as NAND and NOR gates, can be modelled by a similar method. However, the SVTC curves for these gates are extended to three-dimensional curves (two or more input axes and one output axis), as shown in Figure 5.

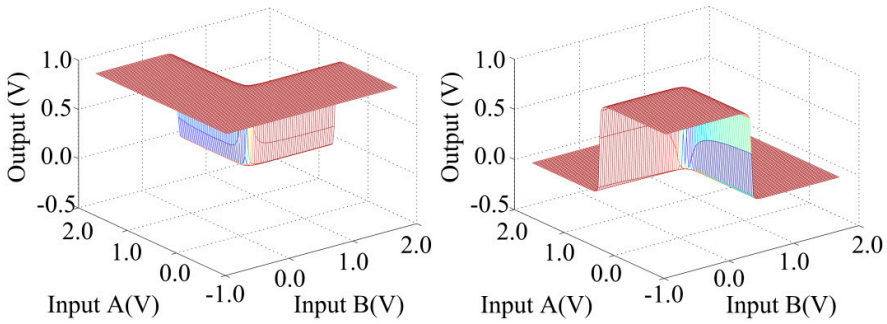

Figure 5. Three-dimensional SVTC curves for multi-input gates. (**a**) SVTC of NAND gate; (**b**) SVTC of NOR gate.

In Figure 5, the x- and y-axes are the two input voltage levels, and the z-axis is the output voltage level. The pdf calculation for the output signal V_{out} is expressed as

$$p\left(V_{out}\right)\cdot dV_{out} \cong P\left(V_{out2} < V_{out} \leqslant V_{out1}\right) \cong \sum_i P\left(V_{out,i}\right) \cong \sum_i \int p\left(V_{in1,i}\right) dV_{in1} \cdot \int p\left(V_{in2,i}\right) dV_{in2} \quad (4)$$

where ($V_{in1,i}$,$V_{in2,i}$,$V_{out,i}$) is the *ith* point on the three-dimensional SVTC curve with $V_{out2} < V_{out,i} \leqslant V_{out1}$.

Accurate analysis of transient fault occurrence probabilities, or transient fault rates for different parts of circuits, is an important step for the effective implementation of transient fault mitigation techniques. Therefore, after acquiring the pdf of a circuit's output ports, we can calculate the transient fault rate P_{error} for these ports. Figure 6 presents an illustration of the transient fault rate calculation for an inverter gate whose normal state is input "one" and output "zero".

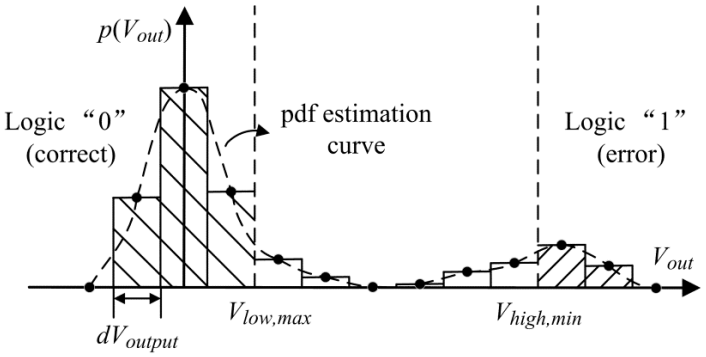

Figure 6. Transient fault rate calculation for an inverter with input "one".

As shown in Figure 6, the two shaded areas in the figure are the probability of logic "0" and logic "1". Then, P_{error} can be calculated according to Equation (5):

$$P_{error} = P\left(V_{out} > V_{high,\min} \middle| V_{nom} = 0\right) = \sum_i p(V_{out,i}) dV_{out} \quad (5)$$

where $V_{high,min}$ is the voltage threshold for logic "one", V_{nom} is the expected correct voltage for the output signal, and $p(V_{out,i})$ is the estimated pdf of the points whose $V_{out,i}$ is greater than $V_{high,min}$.

2.2. PVTC-Based Analysis for Multi-Gate Circuits

Transient fault analysis for single gates is clearly not sufficient. Digital logic circuits typically consist of hundreds of gates, and there is complex logic dependency between them, meaning that the

pdf of the output of one gate is the pdf of the input of another gate. The pdf calculation result for the single gate obtained in Section 2.1 is a series of discrete points, which is not suitable for estimating the pdf for gates in the next stage. Therefore, some approximation procedures are required, and the Riemann sum $p(V_{in})dV_{in}$ is applied to substitute for the integration $\int p(V_{in})dV_{in}$ in Equations (3) and (4). We then obtain the modified pdf calculation equation for single- and multi-input gates in Equations (6) and (7), respectively.

$$p\left(V_{out}\right)\cdot dV_{out} \cong P\left(V_{out2} < V_{out} \leqslant V_{out1}\right) \cong \sum_{i} p\left(V_{in,i}\right) dV_{in} \tag{6}$$

$$p\left(V_{out}\right)\cdot dV_{out} \cong P\left(V_{out2} < V_{out} < V_{out1}\right) \cong \sum_{i} P\left(V_{out,i}\right) \cong \sum_{i} p\left(V_{in1,i}\right) dV_{in1} p\left(V_{in2,i}\right) dV_{in2} \tag{7}$$

where $(V_{in,i}, V_{out,i})$ or $(V_{in1,i}, V_{in2,i}, V_{out,i})$ is the *ith* point on the SVTC curve with $V_{out2} < V_{out,i} \leqslant V_{out1}$.

However, the functional complexity of actual circuits usually results in re-convergent fan-out characteristics, which causes different input ports of one gate to be interdependent. The full adder in Figure 7 is an illustration of re-convergent fan-out characteristics.

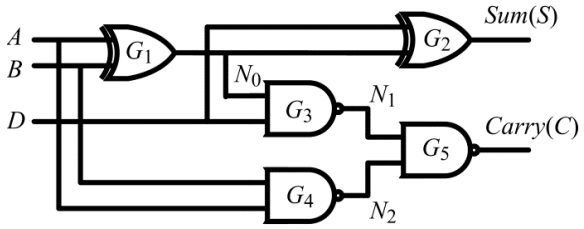

Figure 7. Illustration of the re-convergent fan-out characteristics in a multi-gate circuit.

As shown in Figure 7, the output signal C for the full adder circuit is determined by the inputs of gate G_5, N_1 and N_2. Port N_1 is the output of NAND gate G_3 and is determined by the root input signals A, B, and D. Port N_2 is the output of NAND gate G_4 and is determined by A and B. Therefore, the two input ports of gate G_5 are not independent. Thus, in the pdf calculation of the output signal C of G_5, the correlation between input ports N_1 and N_2 must be considered, as the calculation may otherwise lead to inaccurate results. To solve this problem, the pdf calculation formula Equation (7) is adapted by considering the dependence between N_1 and N_2 because these two signals are both related to root inputs A and B. The total probability formula Equation (8) is applied to estimate the pdf of the output signal C, which considers conditional probability of input ports N_1 and N_2 of gate G_5 on the root input signals V_A and V_B.

$$\begin{aligned} p\left(V_C\right)\cdot dV_C &\cong P\left(V_{C2} < V_C \leqslant V_{C1}\right) \cong \sum_{i} P\left(V_{C,i}\right) \\ \cong \sum_{V_{A,j},V_{B,j}} \sum_{i} & p\left(V_{N1,i} \middle| V_A = V_{A,j}, V_B = V_{B,j}\right) dV_{N1} \cdot p\left(V_{N2,i} \middle| V_A = V_{A,j}, V_B = V_{B,j}\right) dV_{N2} \end{aligned} \tag{8}$$

In Equation (8), point $(V_{N1,i}, V_{N2,i}, V_{C,i})$ is the *ith* point on the SVTC curve of gate G_5 with $V_{C2} < V_{C,i} \leqslant V_{C1}$. $(V_{A,j}, V_{B,j})$ is each input voltage pair of the discrete three-dimensional SVTC curve acquired by SPICE DC analysis, as shown in Figure 5. The conditional probability $p(V_{N2,i} \mid V_A = V_{A,j}, V_B = V_{B,j})$ can be calculated directly because V_{N2} is determined by V_A and V_B only, whereas V_{N1} is determined by D and N_0, and the pdf estimate of the conditional probability $p(V_{N0,i} \mid V_A = V_{A,j}, V_B = V_{B,j})$ can be acquired by a similar method to that of N_2. The conditional probability $p(V_{N1,i} \mid V_A = V_{A,j}, V_B = V_{B,j})$ can then be found by calculating the pdf estimate of gate G_3, and the final result of the pdf calculation for gate G_5's output C can be determined. The pdf estimation for other logic circuits can also be obtained by a similar method.

2.3. NBTI Effect and Its Impact on the PVTC Method

At present, the NBTI effect is the dominant aging mechanism for VLSI circuits; this effect occurs when pMOS transistors are negatively biased, which causes a shift in the threshold voltages (V_{th}) and in turn causes changes in circuit characteristics during its lifetime. Grasser *et al.* [21] noted that in small-sized devices in CMOS logic circuits, the threshold voltage change induced by the NBTI effect is dominated by stochastic charging/discharging events of individual oxide defects; therefore, each device shows a different degradation curve. Clearly, this type of NBTI model will greatly complicate the analysis process. Because our aim was to estimate the transient fault rate that considers both environmental noise and the NBTI effect and provide a design basis for transient fault mitigation techniques, in this paper, pMOS transistors are assumed to suffer the same degree of degradation during the lifetime of the circuits, and the R-D model is applied to analyze the NBTI effect. According to the R-D model, the V_{th} degradation of pMOS transistors caused by NBTI has two phases: the stress phase and the recovery phase. The magnitude of V_{th} increases during the stress phase (*i.e.*, $V_{gs} = -V_{dd}$), whereas the magnitude of V_{th} partially decreases towards its initial value during the recovery phase (*i.e.*, $V_{gs} = 0$); however, recovery can only partially alleviate the effect of NBTI. The threshold voltage change during stress and recovery cycles is illustrated in Figure 8.

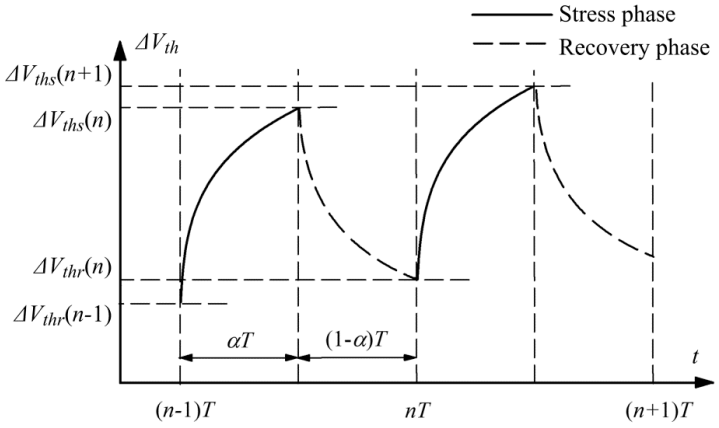

Figure 8. Threshold voltage change during stress and recovery cycles.

Therefore, the magnitude of V_{th} degradation is strongly dependent on the duty cycle (α) of the input signal, which reflects the fraction of time that the pMOS transistor spent in the stress state in one clock period. In this paper, we apply the long-term prediction model proposed in [14] to calculate the V_{th} degradation effect as follows

$$|\Delta V_{th}| = \left(\sqrt{K_v^2 \cdot T_{clk} \cdot \alpha} / \left(1 - \beta_t^{1/2n} \right) \right)^{2n} \tag{9}$$

where $\beta_t = 1 - \left(2\xi_1 t_e + \sqrt{\xi_2 C \left(1 - \alpha\right) T_{clk}} \right) / \left(2t_{ox} + \sqrt{Ct} \right)$, and T_{clk} is the clock period. According to the formula Equation (9), we simulate the NBTI effect of a pMOS transistor using the PTM 45 nm model [22] in HSPICE. The increase in V_{th} after working 10^8 s (approximately 3 years) is presented in Figure 9. The duty cycle (α) of the NBTI effect is set from 0.05 to 0.95, with a step of 0.3.

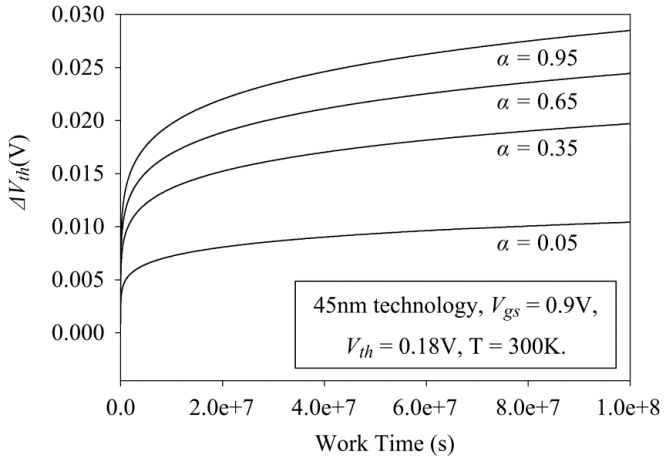

Figure 9. Change of V_{th} *vs.* work time under different duty cycles of an input signal.

The change in the SVTC curve for an inverter gate caused by the V_{th} increase is shown in Figure 10; this change, in turn, affects the occurrence probability of transient faults. Therefore, to acquire accurate transient fault rate estimations during the lifetime of circuits, changes in circuit characteristics caused by NBTI effect should be considered in the PVTC analysis framework.

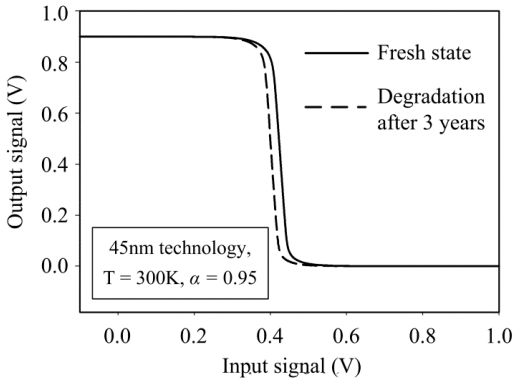

Figure 10. Changes in the SVTC of an inverter in the fresh and degraded states.

3. Results and Discussion

3.1. Experimental Setup

We divide the noise sources into two categories to simulate the actual working conditions of circuits in a noise-filled environment: input noise and supply noise. Considering the low-pass characteristics of logic gates and the central limit theorem, these two types of noise are modelled as random variables following a normal distribution. The input noise represents external noise effects, such as single event transient and electromagnetic coupling, and the amplitudes of these noises are relatively large. Additionally, as the probability of error in actual circuits is very small, an extremely long time is required for the MC simulation to obtain the overall transient fault rate. Therefore, the standard deviation of the noise on the input signal is set to 300 mV such that the MC simulation can be implemented within a reasonable time to verify the effectiveness of the PVTC method. Supply noises, which represent noise effects inside the VLSI circuit system, such as power supply ripple and amplifier noise of the linear regulator, are also considered; the amplitudes of these noises are relatively small, and thus, their standard variation is set to 20 mV. The supply noise and the input noise are assumed to be independent. In our experiment, dV_{out} and dV_{in} are set to the same value to simplify the experiment, and dV_{out} and dV_{in} are set to the small value of 30 mV to guarantee accuracy.

The predictive technology model (PTM) [22] for 45 nm general-purpose pMOS and nMOS transistors is exploited to evaluate the PVTC method, and the power supply of the logic circuit is set to 0.9 V. In NBTI effect simulation, the duty cycle for the pMOS transistor is set to 0.95, as in [23] by the MDS method, temperature T is set to 300 K. In the transient error rate calculation, $V_{high,min}$ in Equation (5) is set to 0.7 V, which represents logic "1", whereas $V_{low,max}$ is set to 0.2 V, which represents logic "0". The number of iterations for MC simulation is set to 10,000. The above configuration is the same for all of the experiments.

3.2. The PVTC Method for the Logic Circuit

First, we build the voltage level pdf at the output of the basic logic gate cell based on the PVTC method and MC simulation. Figure 11 presents the voltage pdf curve for the NAND gate with an input of "11" by these two methods.

As shown in Figure 11, the majority of the output is distributed around "0", which is a correct result for the NAND gate. However, due to the influence of noise effects, a minority of the output voltage level is distributed around "1". We can also find that the pdf estimation results by two methods are highly similar. Furthermore, Figure 12a–f presents the level pdf for the NAND gate and NOR gate with different input combinations. In Figure 12, the dashed lines are the pdf curve estimated by the PVTC method, and the solid lines are the pdf curve acquired by the MC method. Figure 12 illustrates that the voltage pdf estimation curves obtained by the two methods are all highly similar for different input combinations, thus verifying the effectiveness of the proposed method. Moreover, Figure 12a,c illustrate that the probability of occurrence for a transient fault is less when the input is "00" compared to when the input is "11" for the NAND gate due to the logical masking effect of combinational circuits. We can observe similar phenomena based on the results of the NOR gate.

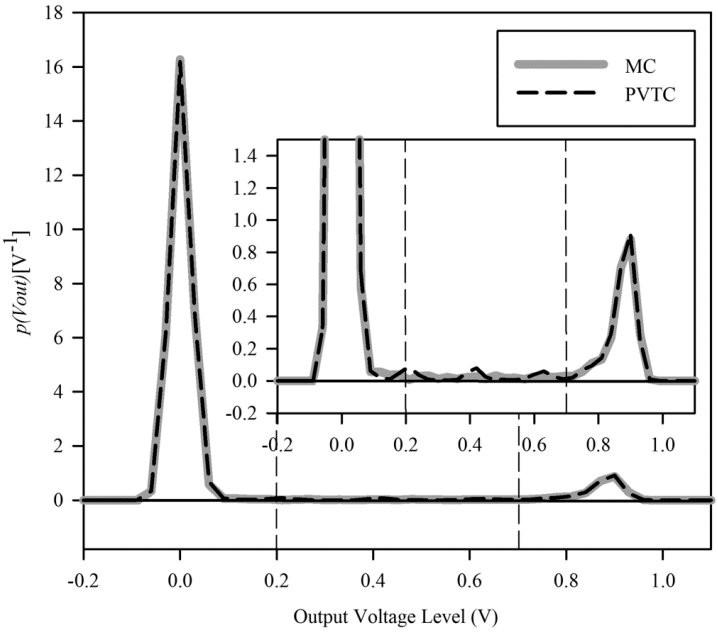

Figure 11. The pdf estimation of the output of the NAND gate with input "1, 1".

To fully investigate the effectiveness of the PVTC method, a multi-gate circuit is also tested. Here, the full adder in Figure 7 is selected, which is a frequently used structure in pipeline stages. Because the result of N_2 is determined by inputs A and B and node N_1 is also related to inputs A and B, there is a correlation between N_1 and N_2. Conditional probability should be considered. Figure 13a,b present the level pdf curve for the sum signal and carry signal of the full adder circuit, respectively. To provide

a brief illustration of the result, only the result with an input of "000" is listed. We also implemented experiments using other input combinations and obtained similar results.

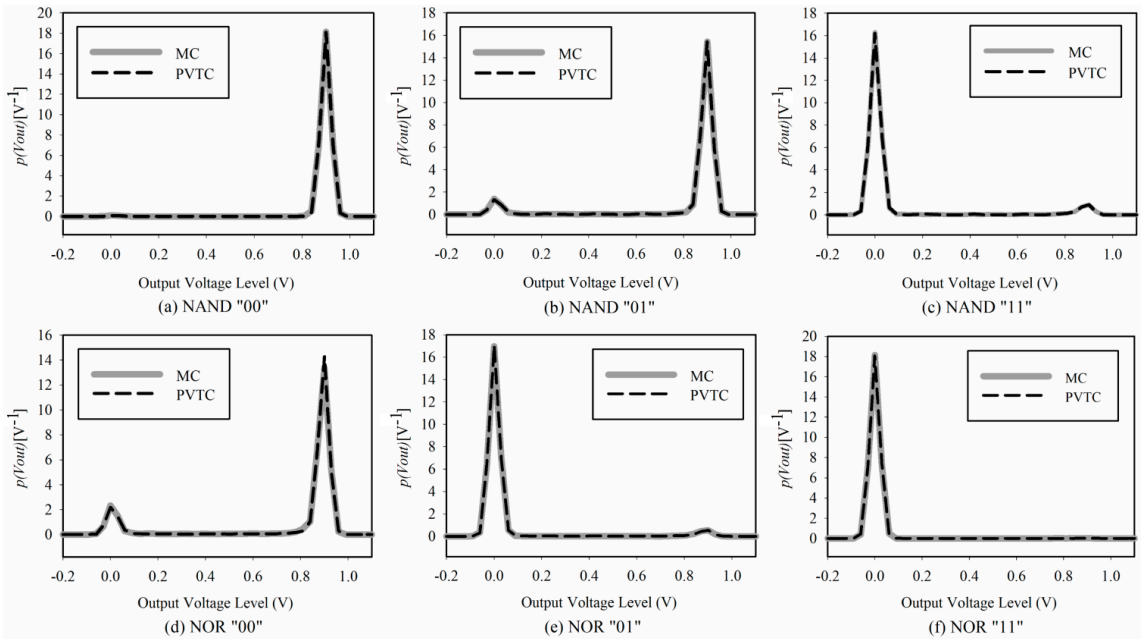

Figure 12. The level pdf for the NAND and NOR gates with different inputs. (**a**) NAND "00"; (**b**) NAND "01"; (**c**) NAND "11"; (**d**) NOR "00"; (**e**) NOR "01"; (**f**) NOR "11".

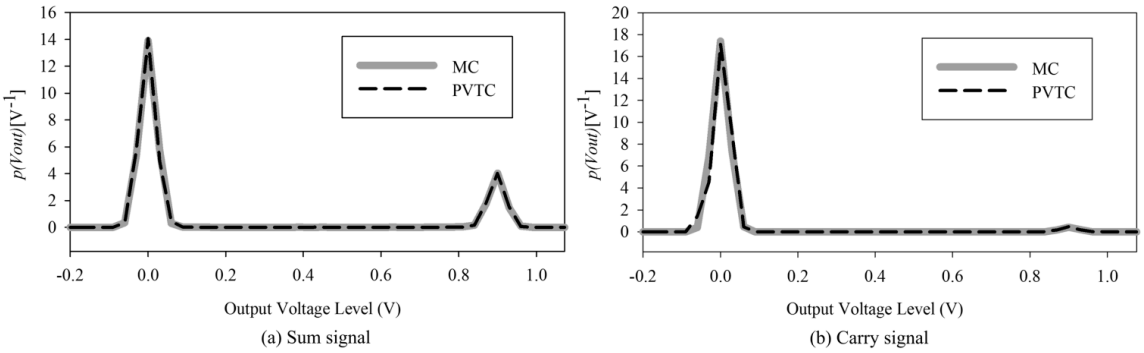

Figure 13. PVTC analysis for a full-adder circuit. (**a**) Sum signal; (**b**) Carry signal.

A comparison of the results of the transient fault rate and the runtime between the PVTC and MC simulations is shown in Table 1. We also calculate the error between the results obtained by the PVTC and MC simulations, which is defined as follows: (PVTC-MC)/MC. The experiments are conducted on a PC with a 3.30 GHz Intel Core i3-2120, 3GB RAM, and the 32-bit Windows 8 operating system. The PVTC method is implemented in a Matlab R2011b simulation environment, and the MC simulations are implemented in an HSPICE C-2009.9 environment. Table 1 shows that the error between the two methods is less than 9%, which is sufficient for the transient fault mitigation design requirement. Moreover, the computational cost of the PVTC method is far less than that of the MC simulation, as the PVTC method is approximately two orders of magnitude faster than the MC method. As the transient fault rate when the input is "01" is the same as the rate when the input is "10" for the NAND gate, we only list the transient fault rate when the input is "01" for the NAND and NOR gates in Table 1.

Table 1. Comparison of the results of the probability voltage transfer characteristics (PVTC) method and Monte Carlo (MC) simulation.

Logic Circuit	Input	Transient Fault Rate (%)		Error (%)	Runtime (s)	
		MC	PVTC		MC	PVTC
NAND Gate	00	0.81	0.88	8.6	220	0.41
	01	8.98	9.11	1.4		
	11	7.52	7.46	−0.8		
NOR Gate	00	15.47	14.80	−4.3	230	0.39
	01	4.77	4.41	−7.5		
	11	0.23	0.21	−8.7		
FA Sum	000	22.71	22.88	0.7	452	1.0
FA Carry	000	2.57	2.55	−0.8	452	1.8

3.3. NBTI-Aware PVTC Method Analysis

To explore how the NBTI effect can affect the transient fault rate of digital circuits, we add the NBTI model to the PVTC analysis framework. Table 2 presents the transient fault estimation results for NAND and NOR gates and the full adder circuit when the circuit is in a fresh state and after three years of NBTI degradation. We also calculate the change rate before and after degradation, which is defined as follows: (Degraded-Fresh)/Fresh.

As shown in Table 2, the NBTI effect causes a significant transient fault rate change for different parts of the VLSI circuit during its lifetime. Moreover, as the feature size, supply voltage and threshold voltage continue to decrease, this change will become more severe in the future. These results also illustrate that the transient fault rate will increase for certain gates with a certain input pattern, but the opposite situation is observed for other gates with the same input pattern combination (Table 2). A detailed illustration of the fault rate change for the NAND and NOR gates with the same input pattern, in a fresh state and degraded state, respectively, is provided in Figure 14.

Table 2. Comparison of the transient fault rate before and after negative bias temperature instability (NBTI) degradation.

Logic Circuit	Input	Transient Fault Rate (%)		Change Rate (%)
		Fresh	Degraded	
NAND Gate	00	0.88	1.03	+17.1
	01	9.11	10.11	+11.0
	11	7.46	6.51	−12.7
NOR Gate	00	14.80	16.89	+14.1
	01	4.41	3.78	−14.3
	11	0.21	0.16	−23.8
FA Sum	000	22.88	25.11	+9.8
FA Carry	000	2.55	3.22	+26.3

As shown in Figure 14a, the gate will be more sensitive to transient faults after degradation when the input pattern of the NAND gate is “01”; in contrast, the same pattern “01” results in a transient fault rate decrease for the NOR gate, as shown in Figure 14b. This result is mainly due to the different functions of the logic gates. When the threshold voltage of the pMOS increases, an input of “0” will be more likely to be recognized as “1”; thus, the transient fault rate will be more likely to increase with an input of “00”, whereas the transient fault rate will be more likely to decrease with an input of “11” for both the NAND and NOR gates. If the input is “01”, the NOR gate is more likely to logically mask the error, whereas the NAND gate is not, which creates the different trends in the change rate. Thus, during the entire lifetime of a VLSI circuit, we can provide more accurate fault rate estimation results if NBTI effect is considered.

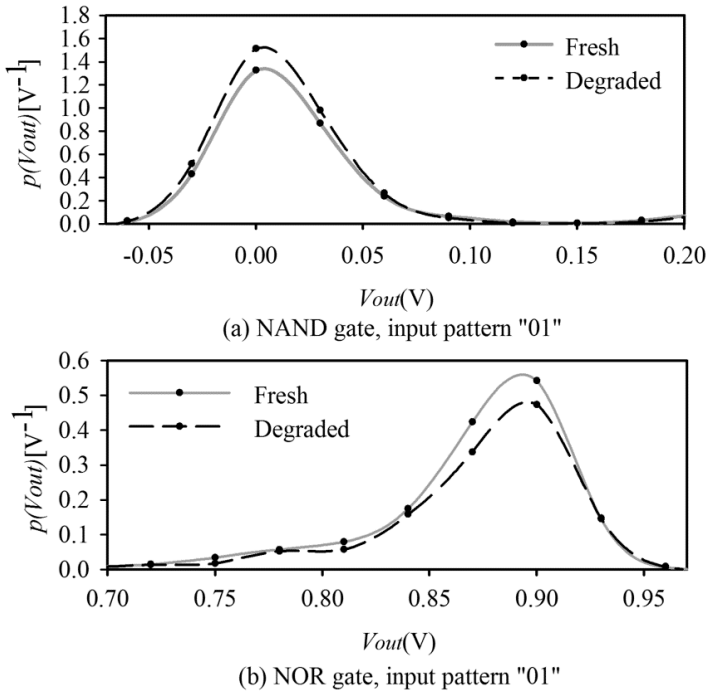

Figure 14. Transient fault rate change before and after degradation. (**a**) NAND gate, input pattern "01"; (**b**) NOR gate, input pattern "01".

4. Conclusions

Transient faults and the NBTI aging effect are two main failure mechanisms for modern VLSI systems. In this paper, an NBTI-aware statistical analysis method is proposed to analyze the transient fault rates of combinational logic circuits induced by environmental noise. The new method is based on PVTC, which can acquire accurate fault rates using a discrete probability density function approximation method with a reasonable computational cost. Moreover, the proposed method also considers the NBTI effect on the estimation process of the transient fault rate and analyzes the impact of input combinations on the highest transient fault rate for different parts of the circuit. Experimental results at different levels of abstract circuit design have demonstrated the effectiveness of the proposed method. The NBTI-aware PVTC method can provide a design basis for different transient fault mitigation methods and improve long-term reliability during the lifetime of VLSI circuits.

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Author Contributions: Zhiming Yang conceived and designed the experiments; Yang Yu performed the experiments; Junbao Li analyzed the data; Zhiming Yang and Xiyuan Peng wrote the paper.

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