

Article

A Mayfly-Based Approach for CMOS Inverter Design with Symmetrical Switching

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Abstract: This paper presents a novel approach to designing a CMOS inverter using the Mayfly Optimization Algorithm (MA). The MA is utilized in this paper to obtain symmetrical switching of the inverter, which is crucial in many digital electronic circuits. The MA method is found to have a fast convergence rate compared to other optimization methods, such as the Symbiotic Organisms Search (SOS), Particle Swarm Optimization (PSO), and Differential Evolution (DE). A total of eight different sets of design parameters and criteria were analyzed in Case I, and the results confirmed compatibility between the MA and Spice techniques. The maximum discrepancy in fall time across all design sets was found to be 2.075711 ns. In Case II, the objective was to create a symmetrical inverter with identical fall and rise times. The difference in fall and rise times was minimized based on Spice simulations, with the maximum difference measuring 0.9784731 ns. In Case III, the CMOS inverter was designed to achieve symmetrical fall and rise times as well as propagation delays. The Spice simulation results demonstrated that symmetry had been successfully achieved, with the minimum difference measuring 0.312893 ns and the maximum difference measuring 1.076540 ns. These Spice simulation results are consistent with the MA results. The results conclude that the MA is a reliable and simple optimization technique and can be used in similar electronic topologies.

Keywords: Mayfly Optimization Algorithm (MA); CMOS inverter; cost function; rise time; fall time; Spice



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1. Introduction

The inverter is known as the basic logic gate of any digital Integrated Circuit (IC) technology, and it is an integral part of all digital systems. With the emergence of new technologies, designers are focusing on building the basic blocks, such as inverters [1,2]. Much work has been conducted to overcome the performance bottleneck in CMOS inverters [3]. The inverters' performance has been investigated in order to come up with robust circuits [4]. As technology has been sized down, circuit design has become more challenging, and the need for designing accurate and fast circuits with low time delay has become an important issue [5,6]. The switching characteristics of the inverter are the fundamental parameters used to describe the inverter's performance. Thus, the switching speed of the inverter's circuit should be optimized before the design steps to achieve symmetrical switching. Switching time from high to low or from low to high depends on the channel width, length of the transistors, and load capacitance C_L .

The physical structure of the transistors in the CMOS inverter causes parasitic capacitances, because of the segregation of mobile charges across different regions within the device. The value of parasitic capacitances in a transistor depends on its width (W) and the length (L) of its channel. The currents charging and discharging these capacitances are I_{Ch} and I_{Dis} , respectively. I_{Ch} is responsible for the rise time and I_{Dis} is responsible for the fall time. The flow of I_{Ch} is through the pull-up section and the flow of I_{Dis} flow is through the pull-down section [7]. The significance of output rise and fall time has been discussed on numerous occasions [8–12]. To ensure symmetrical sequence many techniques have

been developed. In Ref. [7] two additional transistors were added to regulate the same amount of current from V_{dd} to match I_{Ch} with I_{Dis} . The problem with this method is that the addition of new transistors will lead to larger size circuits and can introduce more noise to the circuit. Others have used time-delay elements to correct the mismatch in the time delay on a chip [13,14]. Nevertheless, creating delay elements can be a challenging task due to their extensive design specifications and various trade-offs involved. In this work, instead of adding any new transistors, we focus on matching the rise time and the fall time by finding the optimum values of W and L using the Mayfly Algorithm.

Optimization algorithms use mathematical techniques to iteratively refine the solution until the optimal value is achieved. There are various optimization algorithms available in the literature. Gradient descent [15,16], genetic algorithms [17–19], RMSProp [20], and many other optimization algorithms have been used to improve the efficiency and accuracy of solving complex problems. In the published literature, different evolutionary optimization methods have been used to design inverters with optimal switching characteristics. For instance, the PSO technique was used to design the CMOS inverter and its transient performance [21,22]. The authors investigated the overall performance of the PSO technique. In [23,24], the PSO algorithm was used to design a nano-scale CMOS inverter to improve its symmetrical switching. The results of the PSO method were compared to Spice simulation results.

In [25–29], De, Bishnu Prasad, et al., implemented different optimization techniques to obtain the symmetrical switching characteristic of CMOS inverters. In [25], the PSO with constriction factor and inertia weight approach PSO-CFIWA was used to get the optimal symmetrical switching properties of the CMOS inverter. The performance of the PSO-CFIWA method was compared to that of the real coded genetic algorithm (RGA) and the results showed an improved performance of the PSO-CFIWA. Two different evolutionary optimization methods (DE and RGA) were used in [26] to obtain an optimal global design. The DE and RGA methods were applied to three different studies with different design parameter ranges and the comparison between them was presented. The DE method was found to be the least cost-effective function compared to other design methods. The Crazy-fitness-based Particle Swarm Optimization (CRPSO), presented in [27], was used to design the CMOS inverter with the optimal switching speed characteristics. The results of the CRPSO method were compared to the RGA method results and the CRPSO method gave better symmetrical switching for the CMOS inverter. In [28], a hybrid meta-heuristic search method was suggested with a harmony search algorithm (HS) and DE algorithm. This method was called HS–DE and it was used in CMOS inverter design with symmetrical switching properties to find an improved global solution. The results of HS–DE were compared with PSPICE results. In [29], the PSO with an aging leader and challenger (ALCPSO) method was employed to design the CMOS inverter with the optimal symmetrical switching characteristics. The simulation results of the ALCPSO method were compared with the simulation results of the RGA. In [30], a Cuckoo Search Algorithm (CSA), inspired by the parasitic nature brood of a few cuckoo types, was used to optimize the CMOS inverter and to achieve equal values of both the fall time (t_f) and rise time (t_r). The CSA algorithm was also used to achieve equal propagation delay time when switching from low to high and from high to low. The results of the CSA were compared with different methods such as the PSO, the RGA, and the PSO-CFIWA methods. The authors in [31] used different optimization methods to derive the accuracy equation for the propagation delay time of a ring oscillator. In [32], the SOS was presented to determine the best values of the channel width (W), length (L), and the output-load's capacitance (C_L) to achieve symmetrical switching characteristics for the CMOS inverter. The modified approach for Multi-Objective Optimization of Heat Transfer Search (MOMHTS) was presented in [33]. The MOMHTS method was applied to five problem sets. The modified optimizer method was compared to Multi-Objective Symbiotic Organism Search (MOSOS), Multi-Objective Synchronous Heat Transfer (MOHTS), Multi-Objective Ant System (MOAS), and Multi-Objective Ant Colony System (MOACS).

A novel MA was presented in [34]. The MA is an optimization algorithm used to find the best solution to a problem in terms of the convergence position and convergence speed. The authors in [34] compared the results of the MA with the PSO and Firefly Algorithm (FA) algorithms. The MA was improved in [35]. The equations of the velocity were updated to achieve better results. In [36], the authors conducted research to examine the key role of the oppositional mayfly optimization for the use in tasks scheduling technique (OMO-TST) related to the cloud computing environment (CC). The OMO-TST was implemented, and the cloud computing environment performance was optimized and controlled. The results showed that implementing the OMO-TST technique for CC can contribute to a significant reduction in the level of complexity related to the computations required for processing data in a cloud system. In addition, the results of their analysis revealed that utilizing the OMO technique for CC can achieve practical usage of resources and enhance the performance of CC at the level of individuals and companies. In [37], the performance of the negative mayfly optimization method is presented to get the best positions and velocities of the mayflies.

The MA was utilized by researchers to solve various problems and obtain optimal solutions. In a study conducted by Bhattacharyya, et al., the role of MA in machine learning was evaluated for reducing the dataset dimension by eliminating redundant and excessive characteristics [38]. A novel feature collection method, MA-HS, was developed to achieve this goal [38]. The MA-HS was employed to enhance feature selection performance by improving the search space and fitness function. The experimental results showed that it outperformed other algorithms such as the genetic algorithm (GA), binary dragonfly algorithm (BDA), binary salp swarm algorithm (BSSA), and whale optimization algorithm (WOA) [38]. Work was conducted to employ the initial center frequency-guided filter (ICFGF) approach to detect bearing faults through a two-phase process [39]. In the first phase, energy spectrum distributions were assessed using a variation analysis scale. In the second phase, a modified Mayfly optimization method (MMA) was used to determine the optimal resonance demodulation frequency. Employing the MMA in the ICFGF was found to be effective in detecting faults with high accuracy, as evidenced by results from [39]. The study also compared ICFGF to other techniques such as conditional variation selection and fast kurtogram, demonstrating its superior performance. The Mayfly method was also used to optimize the model of combined cooling heat and power (CCHP) systems [40]. The authors in [40] were able to obtain the optimal size of the components and minimum fuel consumption in the system. It was noted that the Mayfly Algorithm was more effective in providing the required solution in a shorter time. Researchers carried out a study assessing the major contribution of implementing the MA to conduct optimization of the performance of solar photovoltaic thermal collectors PVTC that are integrated with an electric hydrogen generation system [41]. To achieve the study goal, a solar (PVTC) with a hydrogen generation system has been modeled for predicting several factors related to the performance of the system using artificial intelligence and the Mayfly Algorithm. The MA has been used to improve the forecasting accuracy in the model.

The aim of this research is to utilize the Mayfly Algorithm to determine the ideal circuit parameters that result in minimal rise time in Case I. In Case II, the goal is to use the same algorithm to find the optimal circuit parameters that produce symmetrical fall and rise times for the inverter. In Case III, the focus will be on finding the optimal circuit parameters that lead to an output waveform with symmetrical rise and fall times, as well as a symmetrical propagation delay time. The rest of this paper is organized as follows: the MA is briefly described in Section 2; the switching characteristics of the CMOS inverter are presented in Section 3; Section 4 explains the formulation of the problem; results and Spice simulations are provided in Section 5; finally, Section 6 concludes the paper.

2. Mayfly Optimization Algorithm

Optimization problem-solving techniques can be classified into two categories. The first category is heuristic methods, such as kinetic gas molecules, evolutionary program-

ming, particle swarm optimization, simulated annealing, genetic algorithm, and Mayfly Algorithm [38]. The second category is mathematical methods, such as linear programming, nonlinear programming, and mixed-integer linear programming [42].

The main goal of an optimization algorithm is to determine the optimal solution to an optimization problem. The MA is a recently proposed algorithm by Zervoudakis and Tsafarakis in 2020 [34]. The MA is based on the mayfly's mating procedure and the flight behavior that combines the evolutionary algorithms and the best features of the swarm intelligence optimization algorithms [34]. In MA, two population sets are randomly generated to represent the female and male sets of the mayflies. The position of each mayfly in the problem space represents a candidate solution to the optimization problem. The mayfly's position is given by an n -dimensional vector $x = (x_1, x_2, \dots, x_n)$, where the objective function is computed to evaluate each mayfly's performance. Each mayfly's position is updated using its velocity, given by the vector $v = (v_1, v_2, \dots, v_n)$, and flying direction. The mayfly's flying direction is determined by the best individual flying experiences of each mayfly's p_{best} and the best swarm's social flying experiences g_{best} [34].

The individuals in the MA update their location in the problem space based on their current positions p_i^t and their velocity v_i^t for each iteration using Equation (1) [34].

$$P_i^{t+1} = P_i^t + V_i^{t+1} \quad (1)$$

In the Mayfly Algorithm, a mayfly's velocity can be explained as the alteration in its location. The flight path of a mayfly is influenced by a complex interplay of its own and the group's flying encounters. Every mayfly modifies its flight path to get closer to its optimal position (" p_{best} ") and the most favorable position acquired by any mayfly in the swarm (" g_{best} ").

The working mechanism of the MA is presented in the following discussion.

2.1. Movement of Male Mayflies

In each iteration, the male mayflies continue the exploring process in swarms. The position of a male mayfly is updated using Equation (2) [34].

$$x_i^{t+1} = x_i^t + v_i^{t+1} \quad (2)$$

where x_i^t is the current position of the male mayfly at time step t , and v_i^{t+1} is the mayfly's velocity. The male mayflies fly a few meters above the water's surface and evolve at high speeds. The velocity of a male mayfly is calculated as in Equation (3) [34].

$$v_{ij}^{t+1} = v_{ij}^t + a_1 e^{-\beta r_p^2} (p_{best_{ij}} - x_{ij}^t) + a_2 e^{-\beta r_g^2} (g_{best_{ij}} - x_{ij}^t) \quad (3)$$

where a_1 and a_2 are the personal and global positive coefficients, respectively, r_p and r_g are the Cartesian distance for personal and global positions, respectively, β represents visibility coefficient, p_{best} is the best position of a mayfly and g_{best} is the best global position of a mayfly.

The velocity of the best male mayflies in the current iteration is updated using Equation (4) [34].

$$V_{ij}^{t+1} = v_{ij}^t + d \times r \quad (4)$$

where d is the nuptial dance parameter and r is a random number in the range $[-1, 1]$.

2.2. Movement of Female Mayflies

The female mayflies' velocity depends on the distance between the females and the males. The female mayflies fly to the male mayflies for mating. The position of a female Mayfly is updated using Equation (5) [34].

$$Y_i^{t+1} = y_i^t + v_i^{t+1} \quad (5)$$

where y_i^t is the current position of the female mayfly at time step t . In the MA, the best female. The velocity of the female is calculated using Equation (6) [34].

$$v_{ij}^{t+1} = \begin{cases} v_{ij}^t + a_2 e^{-\beta r_{mf}^2} (x_{ij}^t - y_{ij}^t) & \text{if } f(y_i) \geq f(x_i) \\ v_{ij}^t + f_1 * r & \text{if } f(y_i) \leq f(x_i) \end{cases} \quad (6)$$

where v_{ij}^t is a female mayfly's velocity in dimension j at time t , y_{ij}^t is the position of female mayfly in the dimension j at time t , x_{ij}^t is the position of male mayfly in j at time t , β and a_2 represent visibility coefficient, and a positive constant, respectively, r_{mf} is the Cartesian distance between female and male mayflies, while f_1 and r represent a random walk coefficient and a random number in the range $[-1, 1]$, respectively.

2.3. Mating of Mayflies

In MA, each couple of mayflies produces two offspring. One is added to the female population arbitrarily and the other is added to the male population. Two offspring are generated after mating as shown in Equations (7) and (8) [34].

$$\text{Offspring}_1 = L \times \text{male} + (1 - L) \times \text{female} \quad (7)$$

$$\text{Offspring}_2 = L \times \text{female} + (1 - L) \times \text{male} \quad (8)$$

where L is a random number with a Gaussian distribution. The procedure of the MA is described in the flow chart shown in Figure 1 below [36].

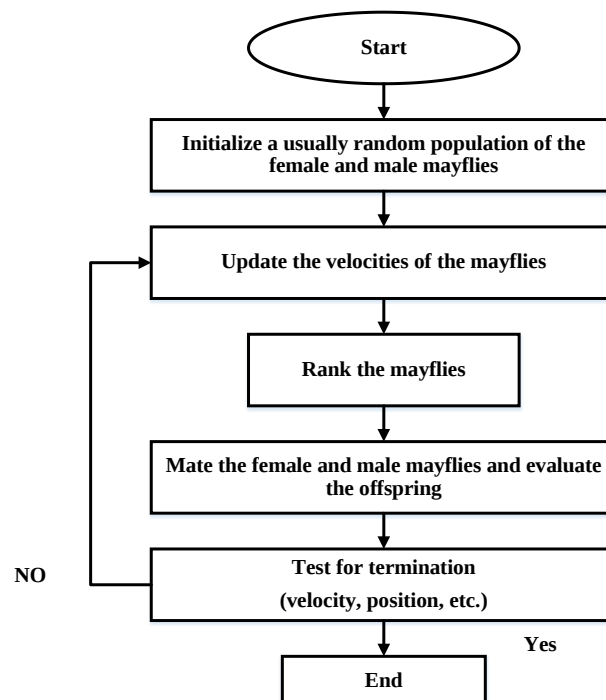


Figure 1. Flowchart of the MA [36].

3. Switching Characteristics of the CMOS Inverter

The fundamental technology of any digital IC relies on the inverter. The inverter serves as the basic block. Its switching characteristics play a critical role in describing the technology. The performance speed of a digital system is contingent on the switching characteristics of the logic gates. This study employs the MA technique to derive the optimal switching characteristics of CMOS inverters. By analyzing the switching operation of the CMOS inverter, the fall and rise time (t_f and t_r) and propagation delay times (t_{PHL}

and t_{PLH}) are determined [11–16,18]. Figure 2 shows the CMOS inverter, while Figure 3 displays the voltage waveforms.

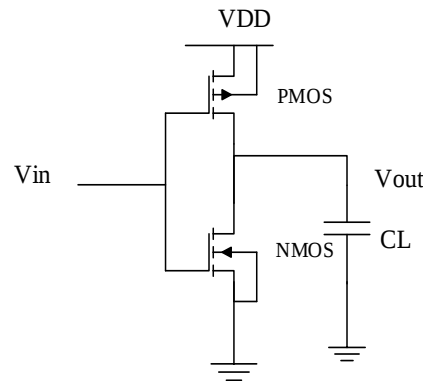


Figure 2. CMOS inverter circuit.

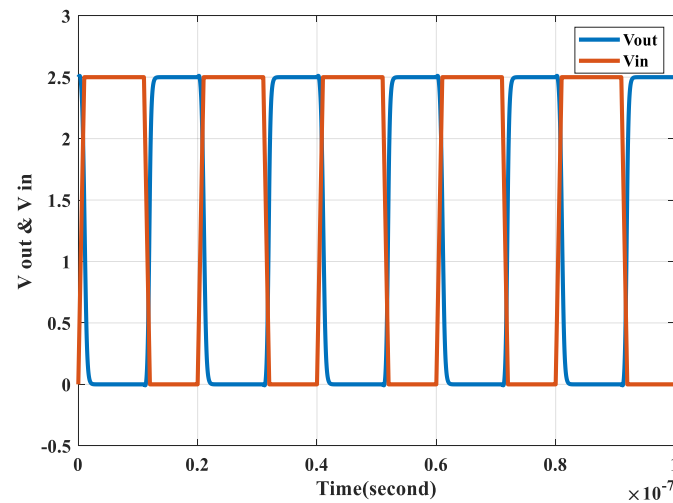


Figure 3. Voltage waveforms of the CMOS inverter.

To determine the fall time, one must measure the duration necessary for the output voltage to decrease from 90% to 10% levels. Conversely, the rise time pertains to the time required for the output voltage to increase from 10% to 90% levels. These values can be calculated using Equations (9) and (10), respectively [11–16,18].

$$t_f = \frac{C_L}{\mu_n C_{OX} \left(\frac{W}{L} \right) n (V_{DD} - V_{tn})} \left[\frac{2(V_{tn} - 0.1V_{DD})}{(V_{DD} - V_{tn})} + \ln \left(\frac{(2(V_{DD} - V_{tn})) - 0.1V_{DD}}{0.1V_{DD}} \right) \right] \quad (9)$$

$$t_r = \frac{C_L}{\mu_p C_{OX} \left(\frac{W}{L} \right) p (V_{DD} - |V_{tp}|)} \left[\frac{2(|V_{tp}| - 0.1V_{DD})}{(V_{DD} - |V_{tp}|)} + \ln \left(\frac{(2(V_{DD} - |V_{tp}|)) - 0.1V_{DD}}{0.1V_{DD}} \right) \right] \quad (10)$$

The duration between the 50% in the rising input voltage and the 50% in the falling output voltage represents the high to low propagation delay. On the other hand, the low to high propagation delay pertains to the time delay between the 50% transition of the falling input voltage and the 50% transition of the rising output voltage. These values can be determined using Equations (11) and (12), respectively [11–16,18].

$$t_{pHL} = \frac{C_L}{\mu_n C_{OX} \left(\frac{W}{L} \right) n (V_{DD} - V_{tn})} \left[\frac{2V_{tn}}{(V_{DD} - V_{tn})} + \ln \left(\frac{(4(V_{DD} - V_{tn}))}{V_{DD}} - 1 \right) \right] \quad (11)$$

$$t_{pLH} = \frac{C_L}{\mu_p C_{OX} \left(\frac{W}{L}\right)_p (V_{DD} - |V_{tp}|)} \left[\frac{2|V_{tp}|}{(V_{DD} - |V_{tp}|)} + \ln\left(\frac{4(V_{DD} - |V_{tp}|)}{V_{DD}} - 1\right) \right] \quad (12)$$

4. Problem Formulation

This paper presents three different case studies to obtain the optimal switching characteristics and the optimal performance of the CMOS inverter. In the first one, the fall time t_f of the output voltage for the CMOS inverter is evaluated. The second case study aims to design a CMOS inverter with a symmetrical output voltage where values for both rise time's t_r and fall time's t_f are equal. In the third one, the CMOS inverter is designed to achieve a symmetrical output voltage and also to obtain equal propagation delay times (t_{PHL} and t_{PLH}).

4.1. Case I

In this case, the aim is to evaluate the fall time of the output voltage for the CMOS inverter, as previously shown in 9, with the minimum values of the cost function CF. During the design phase, the values of the design parameters—which include the output load capacitance C_L , the ratio between channel width and length W/L for both the NMOS and the PMOS structures' fall-time t_f —should be within a specific range. The MA is implemented to find the optimal design parameters C_L , W/L , and the t_f is needed to minimize the cost function given in Equation (13). The fitness function can be written as in Equation (14) [25–30,32].

$$CF = \left| \mu_n C_{OX} \left(\frac{W}{L}\right)_n t_f - \frac{C_L}{(V_{DD} - V_{tn})} \left[\frac{2(V_{tn} - 0.1V_{DD})}{(V_{DD} - V_{tn})} + \ln\left(\frac{(2(V_{DD} - V_{tn}) - 0.1V_{DD})}{0.1V_{DD}}\right) \right] \right| \quad (13)$$

$$J = 10\log_{10}(CF) \quad (14)$$

The TSMC 0.25 μm CMOS model in the three case studies. Table 1 shows the eight different design sets which are considered in Case I.

Table 1. Lower and upper bounds for the eight design sets of Case I [25–30,32].

Set Number	C_L (pF)	W/L	T_f (ns)
1.0	0.10–2.40	0.30–3.30	0.50–6.70
2.0	0.20–5.60	0.40–2.30	0.30–6.00
3.0	0.60–3.40	0.90–5.00	0.60–8.60
4.0	0.50–3.60	1.20–4.10	0.90–11.00
5.0	0.70–1.80	0.70–4.90	1.20–15.00
6.0	0.30–2.40	2.20–3.20	1.40–12.00
7.0	0.70–2.30	0.70–3.00	1.60–5.70
8.0	0.60–1.90	1.50–3.50	1.00–8.150

4.2. Case II

To obtain an optimal symmetrical switching response, the fall time must equal the rise time of the output voltage. The main objective, in this case, is to find the inverter design parameters, C_L , $(W/L)_p$, and $(W/L)_n$ that minimize the cost function given in Equation (15) [25–30,32]. This cost function measures the difference between the fall time and rise times of the CMOS inverter.

$$CF = \left| (t_f(C_L, \left(\frac{W}{L}\right)_n) - (t_r(C_L, \left(\frac{W}{L}\right)_p)) \right| \quad (15)$$

Subject to the following constraints as in Equations (16)–(20) [25–30,32].

$$(t_f)_{\min} \leq t_f \leq (t_f)_{\max} \quad (16)$$

$$(t_r)_{\min} \leq t_r \leq (t_r)_{\max} \quad (17)$$

$$(C_L)_{\min} \leq C_L \leq (C_L)_{\max} \quad (18)$$

$$\left(\left(\frac{W}{L}\right)_n\right)_{\min} \leq \left(\frac{W}{L}\right)_n \leq \left(\left(\frac{W}{L}\right)_n\right)_{\max} \quad (19)$$

$$\left(\left(\frac{W}{L}\right)_p\right)_{\min} \leq \left(\frac{W}{L}\right)_p \leq \left(\left(\frac{W}{L}\right)_p\right)_{\max} \quad (20)$$

Table 2 shows the eight different design sets considered with the corresponding bound constraints. In this case, the evaluation of the fall time (t_f), and the rise time (t_r) of the output voltage is implemented for the eight different design sets of the parameters C_L , $(W/L)_p$ and $(W/L)_n$.

Table 2. Lower and upper bounds for the eight design sets of Case II [25–30,32].

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_f (ns)	t_r (ns)
1.0	0.33–2.3	1.0–3.0	2.0–18	1.0–12.0	1.0–12.0
2.0	0.6–1.5	0.5–2.5	1.60–19.3	0.5–7.6	0.5–7.6
3.0	0.3–3.0	0.3–1.9	1.76–7.56	0.56–8.7	0.56–8.7
4.0	0.11–1.34	1.5–3.5	2.65–18.9	0.77–7.89	0.77–7.89
5.0	0.5–1.5	1.0–2.5	2.0–13.75	0.1–15.0	0.1–15.0
6.0	0.5–1.5	1.0–3.0	2.0–21.0	0.1–15.0	0.1–15.0
7.0	1.0–3.0	1.5–3.5	3.75–21.0	0.1–15.0	0.1–15.0
8.0	1.5–3.5	1.5–3.0	3.0–19.2	0.1–10.0	0.1–10.0

4.3. Case III

In this case, the main objective is to obtain the symmetrical switching characteristics for the CMOS inverter with equal fall time (t_f) and rise time (t_r), and equal propagation delay times. The cost function that needs to be minimized is formulated as in Equation (21) [25–30,32].

$$CF = \left| (t_f(C_L, \left(\frac{W}{L}\right)_n)) - (t_r(C_L, \left(\frac{W}{L}\right)_p)) \right| + \left| (t_{pHL}(C_L, \left(\frac{W}{L}\right)_n)) - (t_{pLH}(C_L, \left(\frac{W}{L}\right)_p)) \right| \quad (21)$$

Subject to the following constraints as in Equations (16)–(20), (22) and (23) [25–30,32].

$$(t_{pHL})_{\min} \leq t_{pHL} \leq (t_{pHL})_{\max} \quad (22)$$

$$(t_{pLH})_{\min} \leq t_{pLH} \leq (t_{pLH})_{\max} \quad (23)$$

The optimization problem depends on three variables: the load capacitance C_L , the ratio between the channel width and length of NMOS and PMOS transistor $(W/L)_p$, and $(W/L)_n$. The eight different design sets are considered with the lower and upper bounds of the constraints and they are shown in Table 3 for Case III.

Table 3. Lower and upper bounds for the eight design sets of Case III [25–30,32].

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_f (ns)	t_r (ns)	t_{PHL} (ns)	t_{PLH} (ns)
1.0	0.20–4.0	1.10–6.10	2.80–19.30	1.10–13.0	1.10–13.0	0.50–10.0	0.50–10.0
2.0	0.10–5.10	1.60–7.10	1.80–18.0	1.10–15.0	1.10–15.0	0.50–8.0	0.50–8.0
3.0	0.470–20	1.40–6.70	3.20–38.0	0.50–12.0	0.50–12.0	0.20–9.0	0.20–9.0
4.0	0.10–1.10	1.20–7.0	1.50–17.50	0.50–5.0	0.50–5.0	0.20–4.0	0.20–4.0
5.0	0.20–14.0	1.90–50	2.70–17.0	0.70–6.0	0.70–6.0	0.40–5.0	0.40–5.0
6.0	0.30–3.60	1.30–3.50	3.50–16.20	0.250–7.0	0.250–7.0	0.30–4.50	0.30–4.50
7.0	0.20–4.90	1.10–5.80	2.20–25.30	0.50–6.60	0.50–6.60	0.20–7.70	0.20–7.70
8.0	0.20–3.50	0.30–7.60	1.30–39.0	0.30–6.60	0.30–6.60	0.10–4.40	0.10–4.40

5. Results

In this section, the optimal switching characteristics of the CMOS inverter are obtained using the Mayfly Optimization Algorithm. A total of eight different design sets are considered with the lower and upper bounds for the design parameters of each design set as seen in Tables 1–3 for the three different case studies. TSMC 0.25 μm CMOS model is used in the LT-Spice simulation to get simulation results. The model parameters are $V_{DD} = 2.5\text{ V}$, $V_{tn} = 0.3655\text{ V}$, $V_{tp} = 0.5466\text{ V}$, $\mu_p C_{ox} = 51.6\text{ }\mu\text{A/V}^2$ and $\mu_n C_{ox} = 243.6\text{ }\mu\text{A/V}^2$ [25–30,32].

For Case I, the MA is implemented using MATLAB to find the design parameters needed to minimize the fall time of the output voltage for the CMOS inverter with an identical size of PMOS and NMOS transistors. For each design set in Table 1, the MA parameters are population size (males and females) equal 20 and number of iterations equal 50. The result of the MA gives the optimal design parameters, i.e., C_L , (W/L) and (t_f) , for the CMOS inverter with the minimum fall time. These results are summarized in Table 4. The results show that the design parameters are within the limits given in Table 1.

Table 4. MA results for Case I.

Set Number	C_L (pF)	W/L	T_f (ns)	CF (s)
1.0	0.6610313	3.2691838	1.122116	$8.4500086 \times 10^{-20}$
2.0	0.6817429	2.2553382	1.6775056	$8.2739268 \times 10^{-20}$
3.0	0.6	2.7507903	1.2104557	$6.3245267 \times 10^{-20}$
4.0	0.7064141	2.4468083	1.6021919	$5.3510907 \times 10^{-20}$
5.0	0.8389162	3.8796487	1.2	$8.6812836 \times 10^{-20}$
6.0	0.7272609	2.4489382	1.6480392	$9.6705203 \times 10^{-20}$
7.0	0.7122034	1.8113496	2.1820107	$2.7473019 \times 10^{-20}$
8.0	0.8179995	2.3458135	1.9351501	$5.5974648 \times 10^{-20}$

Figure 4 shows the convergence of the objective function, given in 13, with the iterations for the seventh design set. In Figure 4, it can be seen that the objective function reaches an optimal value of $2.7473019 \times 10^{-20}\text{ s}$. The 7th design set was chosen since it has the lowest value of the cost function. Figures 5–7 show the convergence plots of the inverter design parameters, C_L , (W/L) , and (t_f) , for the same design set. In Figure 5, the optimum value for the load capacitance is 0.7122034 pF and it starts to converge after 24 iterations. The aspect ratio (W/L) optimum value for the seventh set is shown in Figure 3 to be equal to 1.8113496. The optimum value for the fall time is equal to 2.1820107 ns as shown in Figure 7.

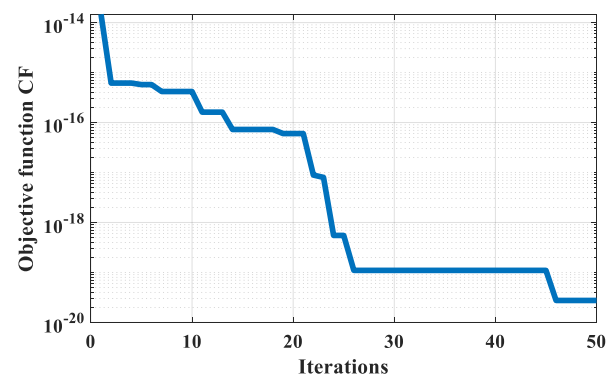


Figure 4. MA results for the seventh design set of Case I.

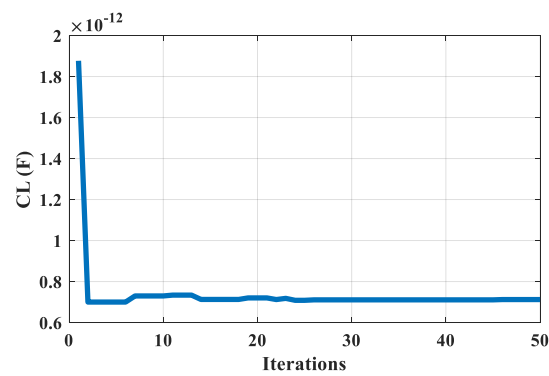


Figure 5. Plot of C_L with iterations for the seventh design set of Case I.

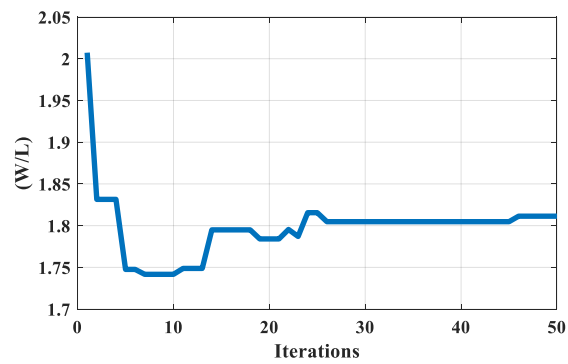


Figure 6. Plot of (W/L) with iterations for the seventh design set of Case I.

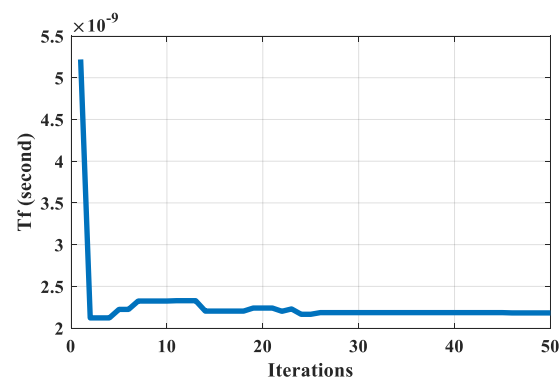


Figure 7. Plot of t_f with iterations for the seventh design set of Case I.

The MA is stochastic by its nature. Therefore, different simulation runs will give different design results. The MA has been run 50 times for the best design set of all the case studies and the resulting CF values have been utilized for the box and whisker plots. Figure 8 shows the box and whisker plot for the seventh design set of the MA; the green square represents the maximum value, the purple star represents upper whisker, the blue triangle represents median value, the red diamond represents the lower whisker, and the orange circle represents the minimum value. The median value of the CF is found to be equal to 5.95×10^{-20} , the maximum value is 9.98×10^{-20} , and the minimum value is 2.75×10^{-20} , the lower whisker is 4.32594×10^{-20} and the upper whisker is 7.8561×10^{-20} .

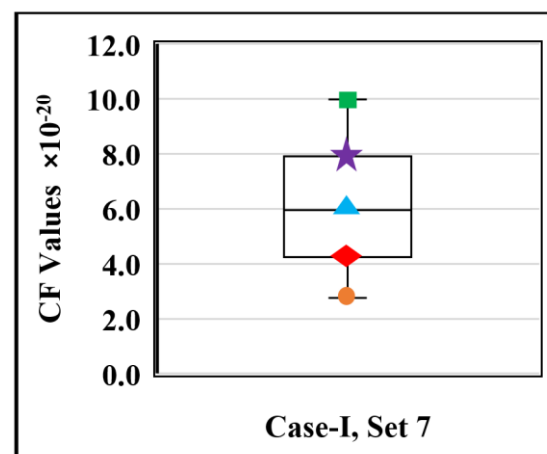


Figure 8. Box and whisker plot of the MA for the seventh design set of Case I.

Table 5 shows the simulation results for each design set in case studies I. Spice simulation results show that the MA method is very accurate with small variations due to MOSFET junction capacitance.

Table 5. Spice results for Case I.

Set Number	C _L (pF)	W/L	T _f (ns)
1.0	0.6610313	3.3	2.5000779
2.0	0.6817429	2.3	2.8601715
3.0	0.6	2.8	2.6132502
4.0	0.7064141	2.5	3.2513576
5.0	0.8389162	3.9	2.7435698
6.0	0.7272609	2.5	3.4637568
7.0	0.7122034	1.9	4.1925571
8.0	0.8179995	2.4	4.0108611

The fall time for the seventh design set of Case I using Spice simulation is shown in Figure 9. As shown in Figure 9, using the values obtained using the MA, an optimum value of the fall time equal to 4.1925571 ns is achieved.

For Case II, the optimal CMOS inverter design with symmetrical operation (fall time equals rise time) is found using the MA for the eight different design sets in Table 2. The MA gives the optimal design parameters needed to minimize the cost function in 15. Table 6 gives the optimal design parameters needed for the CMOS inverter with a symmetrical operation for the eight design sets of Case II. It is apparent that in Table 6 the symmetry in the fall time and rise time has been achieved.

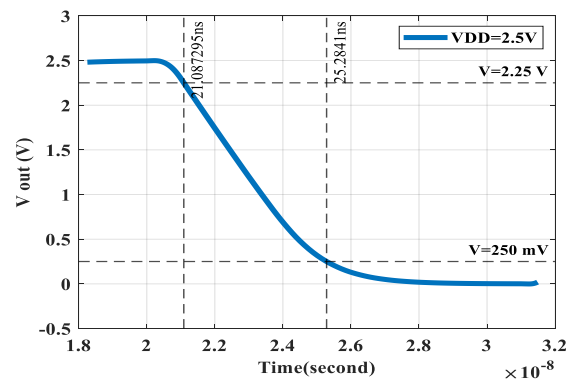


Figure 9. Fall time using Spice for the seventh design set of Case I.

Table 6. MA results for Case II.

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_r (ns)	t_f (ns)	CF(s)
1.0	0.6596316	2.1756359	11.6161245	1.6825590	1.6825590	4.1359×10^{-25}
2.0	0.7279563	2.4977102	13.3357389	1.6174035	1.6174035	8.2718×10^{-25}
3.0	1.0019859	1.3927859	7.43634260	3.9923848	3.9923848	7.4446×10^{-25}
4.0	0.6085469	2.4734372	13.206141	1.3653634	1.3653634	2.068×10^{-25}
5.0	0.8989244	1.8138884	9.68468758	2.7502217	2.7502217	4.1359×10^{-25}
6.0	1.0894291	2.3886778	12.7535949	2.5310252	2.5310252	4.1359×10^{-25}
7.0	1.2756814	2.9565994	15.7858338	2.3944450	2.3944450	4.1359×10^{-25}
8.0	1.7737612	2.8189517	15.0509072	3.4919065	3.4919065	8.2718×10^{-25}

In Figure 10, a plot of the objective function convergence with MA iteration for the fourth design set is shown; the objective function converges after 160 iterations. Figures 10–12 show the convergence plots of the inverter design parameters, C_L , $(W/L)_n$, and $(W/L)_p$, for the same design set. In Figure 11, convergence is achieved after the 25th iteration with an optimum value of 0.6085469 pF for the load capacitance. Figure 12 shows the convergence of the NMOS transistor aspect ratio for the fourth set which is equal to 2.4734372. On the other hand, the optimum value for PMOS aspect ratio is equal to 13.206141, as shown in Figure 13.

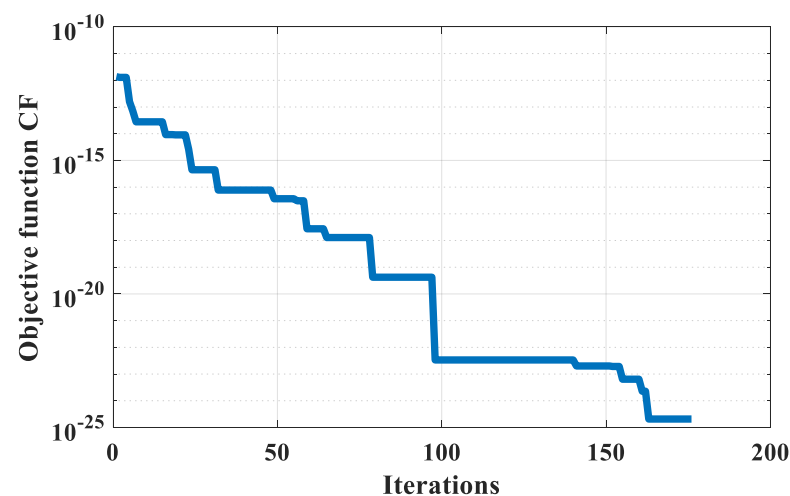


Figure 10. The MA results for the fourth design set of Case II.

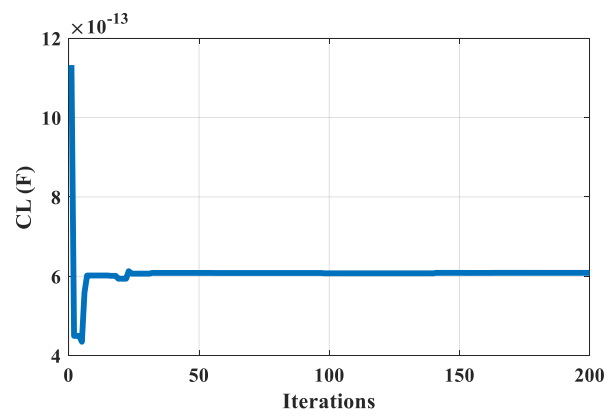


Figure 11. Plot of C_L with iterations for the fourth design set of Case II.

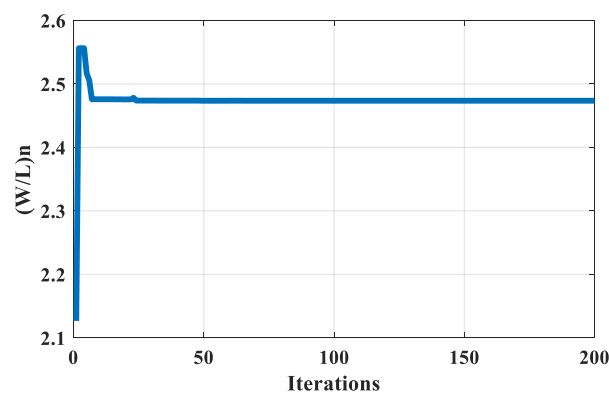


Figure 12. Plot of $(W/L)_n$ with iterations for the fourth design set of Case II.

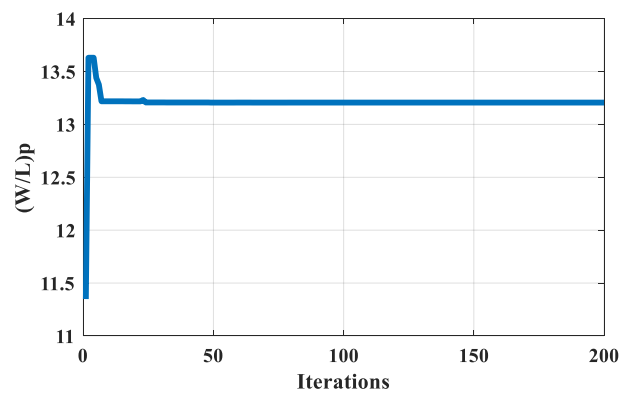


Figure 13. Plot of $(W/L)_p$ with iterations for the fourth design set of Case II.

Figure 14 shows the box and whisker plot for the fourth design set of Case II. The green square represents the maximum value, the purple star represents upper whisker, the blue triangle represents median value, the red diamond represents the lower whisker, and the orange circle represents the minimum value. The median value is found to be 4.14×10^{-25} , the maximum value is 9.31×10^{-25} , the minimum value is 2.07×10^{-25} , the lower whisker is 2.6366×10^{-25} , and the upper whisker is 8.2718×10^{-25} .

Table 7 shows the simulation results for each design set in case studies II. Spice simulation results show that the MA method is very accurate with small variations due to MOSFET junction capacitance.

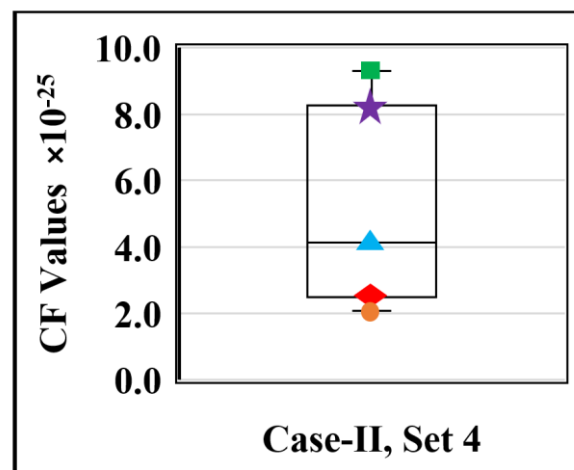


Figure 14. Box and whisker plot of the MA for the fourth design set of Case II.

Table 7. Spice results for Case II.

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_r (ns)	t_f (ns)	CF (ns)
1.0	0.6596316	2.2	11.6	2.8782002	3.4201091	0.5419089
2.0	0.7279563	2.5	13.3	2.7835531	3.4020265	0.6184734
3.0	1.0019859	1.4	7.4	6.7656613	6.6977397	0.0679216
4.0	0.6085469	2.5	13.2	2.3658613	2.8699922	0.5041309
5.0	0.8989244	1.8	9.7	4.6454616	5.2847168	0.6392552
6.0	1.0894291	2.4	12.8	4.3289372	5.2544608	0.9255236
7.0	1.2756814	3	15.8	4.1247077	5.1031808	0.9784731
8.0	1.7737612	2.8	15	5.9821567	6.9487975	0.9666408

The rise and fall times for the fourth design set of Case II using Spice simulation are shown in Figure 15. Spice simulations in Figure 15 show that the designed inverter has a fall time and rise time with only fractions of nano second difference.

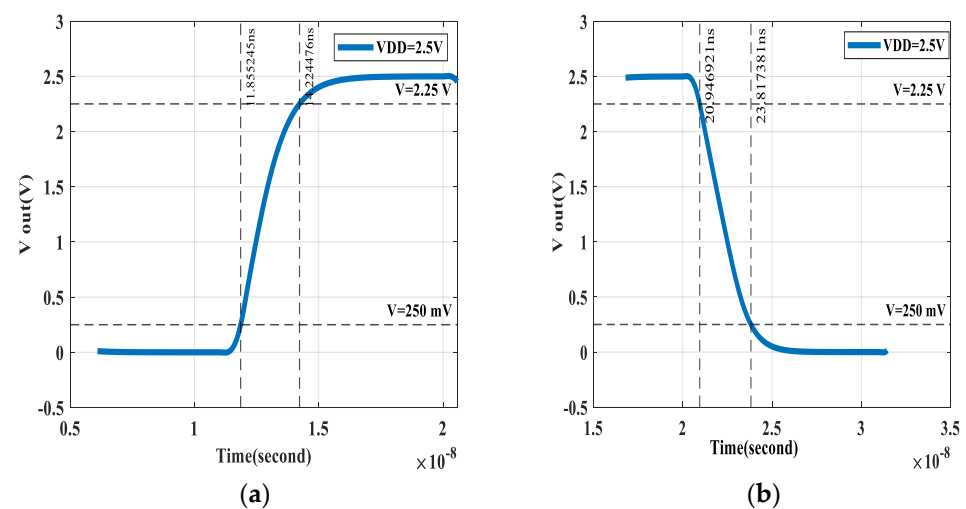


Figure 15. Spice simulation for the fourth design set of Case II. (a) Rise Time (b) Fall Time.

In Case III, the optimal CMOS inverter design for each design set in Table 3 is found using the MA with population size (males and females) equals 20 and 100 iterations. The results give the optimal design parameters. $(W/L)_p$, $(W/L)_n$, and C_L of the CMOS inverter,

which minimizes the objective function given in Equation (21). Then, these optimal values of the CMOS inverter parameters are used to calculate the fall time (t_f), the rise time (t_r), and the propagation delay times (t_{PHL} and t_{PLH}). Table 8 summarizes the results obtained using the MA for each design set in Case III, which satisfies the symmetrical output waveform with equal rise and fall times, and the symmetrical propagation delay time (t_{PHL} equal t_{PLH}).

Table 8. MA results for Case III.

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_f (ns)	t_r (ns)	t_{PHL} (ns)	t_{PLH} (ns)	CF (ps)
1.0	0.767635	3.61478	19.2999	1.17849	1.17849	0.5	0.518353	18.3537
2.0	0.715929	3.37130	18	1.17849	1.17849	0.5	0.518353	18.3537
3.0	0.603656	6.7	35.7725	0.5	0.5	0.212134	0.219921	7.78695
4.0	0.239064	2.65338	14.1668	0.5	0.5	0.212134	0.219921	7.78695
5.0	0.368314	2.16798	11.5752	0.942796	0.942796	0.4	0.414683	14.6830
6.0	0.386602	3.03417	16.2	0.707097	0.707097	0.3	0.311012	11.0122
7.0	0.414941	4.60544	24.5893	0.5	0.5	0.2121134	0.219921	7.78695
8.0	0.394871	7.30448	39	0.3	0.3	0.12728	0.131953	4.67217

Table 9 shows a comparison of the MA results with results obtained by different optimization algorithms. The optimal value of the CF (in ps) of the MA is compared to the optimal value of CF using PSOCFIWA [25], DE [26], ALC-PSO [29], CRPSO [27], PSO [30], HS-DE [32], and SOS [32]. The results show that the suggested MA outperforms most of the widely used optimization methods in finding the optimal CMOS inverter design with the lowest CF value.

Table 9. Comparison of the MA results with other optimization methods for Case III.

Set Number	MA	HS-DE [32]	SOS [32]	DE [26]	PSO-CFIWA [25]	RGA [27]	CRPSO [27]	ALCPSO [29]	PSO [30]
1.0	18.35	17.74	18.35	23.94	14.91	47.52	18.41	17.83	17.7
2.0	18.35	17.92	18.35	26.17	11.91	46.23	21.74	17.85	15.9
3.0	7.78	7.81	7.79	10.25	7.88	44.83	9.68	7.8	15.9
4.0	7.78	7.81	7.79	10.08	7.78	42.86	9.36	13.68	18.7
5.0	14.68	14.19	14.68	26.47	8.08	46.44	19.38	14.19	26.4
6.0	11.01	22.95	11.01	14.88	11.52	48.03	11.95	10.96	19.3
7.0	7.78	7.81	7.79	10.16	7.89	44.06	8.54	7.79	8
8.0	4.67	4.67	4.67	5.91	7.67	46.88	5.25	4.67	9.9

Figure 16 shows the convergence plot of the objective function for the eighth design set. The optimum value of the objective function is 4.67217 ps and it converges after 18 iterations. Figures 17–19 show the convergence plots of the inverter design parameters: C_L , $(W/L)_n$ and $(W/L)_p$ for the same design set. Figure 17 shows that the capacitance load optimum value for the eighth set is equal to 0.394871 pF. The aspect ratio for the NMOS transistor converges at a value of 7.30448 after 16 iterations as shown in Figure 18. On the other hand, Figure 19 shows that the optimum aspect ratio for the PMOS transistor is 39.

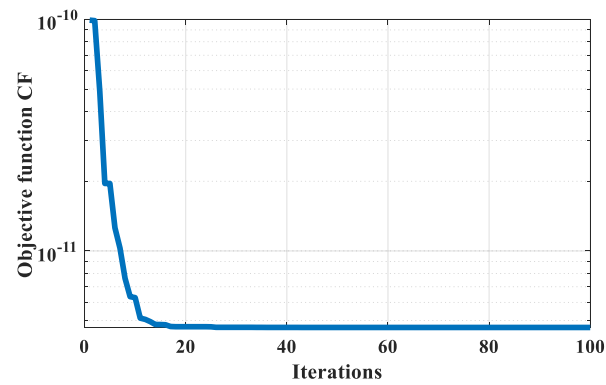


Figure 16. The MA results for the eighth design set of Case III.

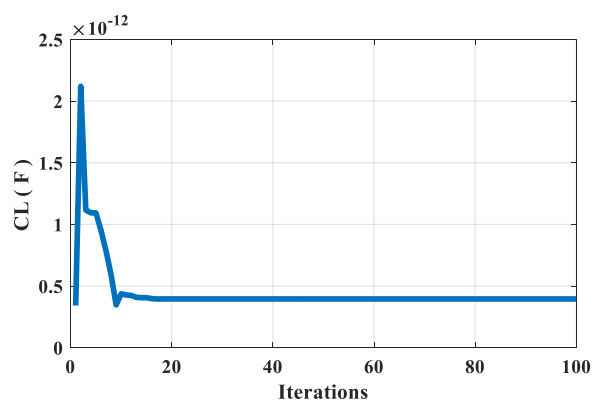


Figure 17. Plot of C_L with iterations for the eighth design set of Case III.

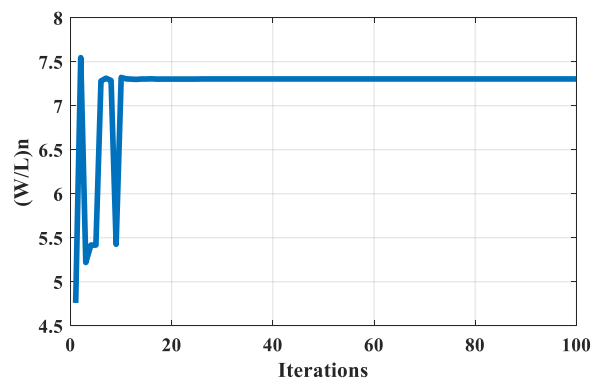


Figure 18. Plot of $(W/L)_n$ with iterations for the eighth design set of Case III.

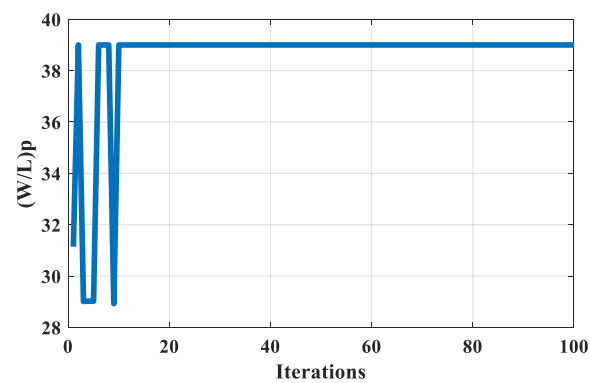


Figure 19. Plot of $(W/L)_p$ with iterations for the eighth design set of Case III.

Figure 20 shows the box and whisker plot for the eighth design set of the MA. The green square represents the maximum value, the purple star represents upper whisker, the blue triangle represents median value, the red diamond represents the lower whisker, and the orange circle represents the minimum value.

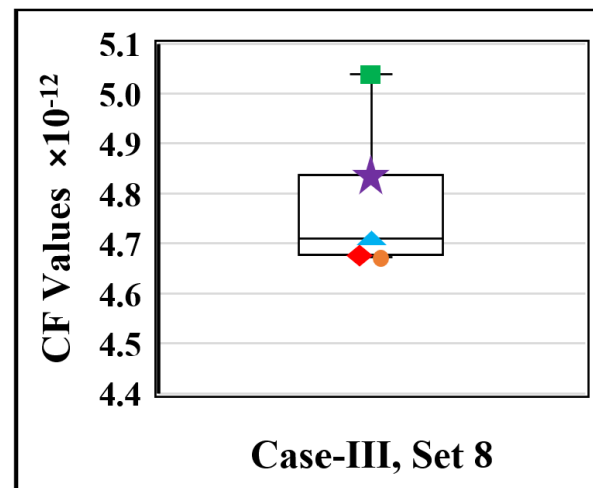


Figure 20. Box and whisker plot of the MA for the eighth design set of Case III.

The median value is found to be 4.71×10^{-12} , the maximum value is 5.04×10^{-12} , the minimum value is 4.67×10^{-12} , the lower whisker is 4.67727×10^{-12} , and the upper whisker is 4.81995×10^{-12} .

To verify the results obtained using MA optimization, the optimal values of the design parameters are used in the inverter Spice simulations. The simulated circuit is shown in Figure 21. Table 10 shows the simulation results for each design set in the three case studies. Spice simulation results show that the MA method is very accurate with small variations due to MOSFET junction capacitance.

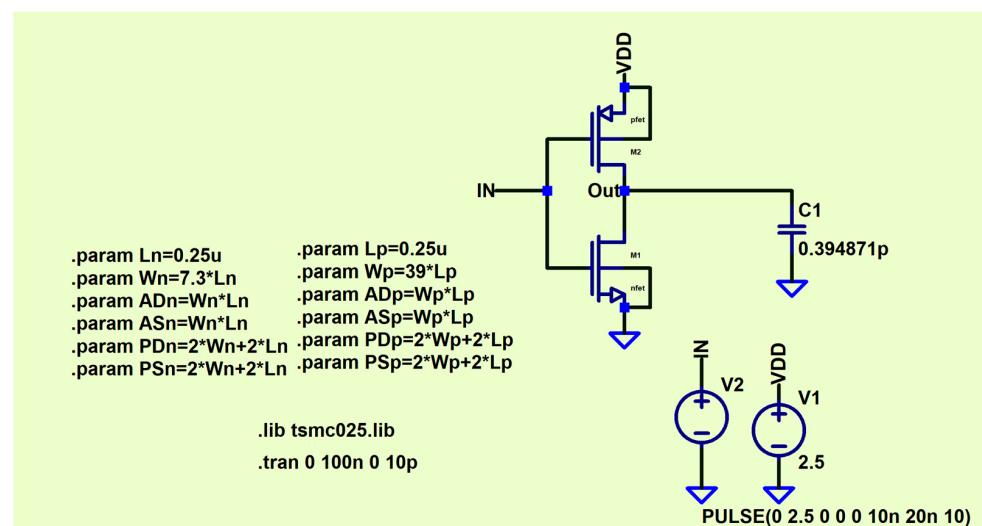
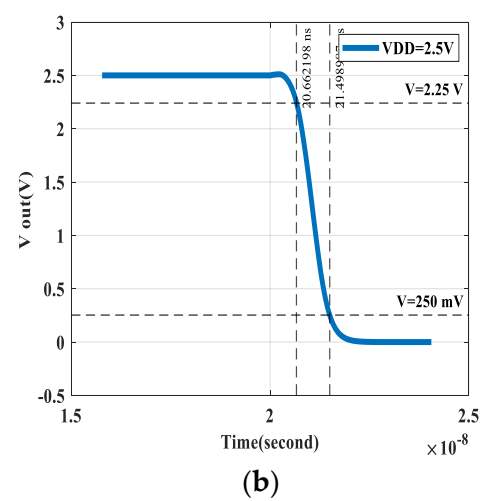
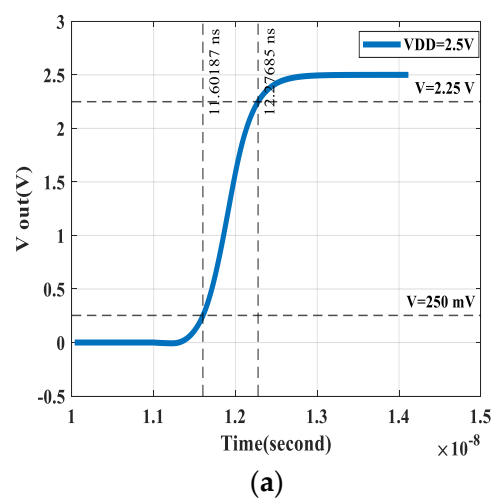
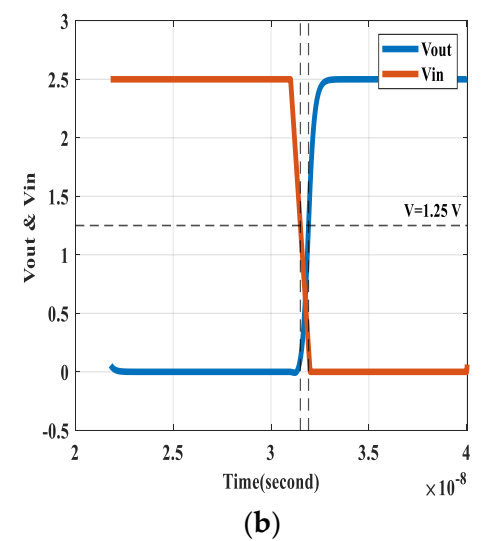
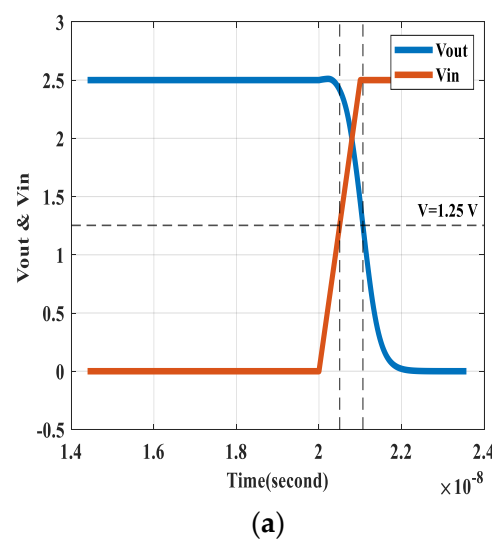


Figure 21. The Spice schematic used to simulate the eighth design set for Case III.

Spice simulations for the rise and fall times and the propagation delay times for the eighth design set of Case III are shown in Figures 22 and 23, respectively. Rise time and fall time in Figure 22 are 0.840474 ns and 0.6761915 ns with a difference less than 0.2 ns. propagation delay high to low and low to high for the eighth set are shown in Figure 23 to be equal to 0.565393 ns and 0.416783 ns, respectively.

Table 10. Spice results for Case III.

Set Number	C_L (pF)	$(W/L)_n$	$(W/L)_p$	t_f (ns)	t_r (ns)	t_{PHL} (ns)	t_{PLH} (ns)	CF (ns)
1.0	0.767635	3.6	19.3	2.664692	2.076923	1.556271	1.0675	1.076540
2.0	0.715929	3.4	18	2.638971	2.03107	1.543645	1.065625	1.043884
3.0	0.603656	6.7	35.8	1.275526	0.9818394	0.806703	0.570023	0.530366
4.0	0.239064	2.7	14.2	1.145440	0.9706936	0.738426	0.567141	0.346031
5.0	0.368314	2.2	11.6	1.946853	1.6663289	1.184149	0.884956	0.579717
6.0	0.386602	3	16.2	1.594699	1.301161	0.985	0.718125	0.472680
7.0	0.414941	4.6	24.6	1.234606	0.978176	0.785312	0.569062	0.472680
8.0	0.394871	7.3	39	0.840474	0.6761915	0.565393	0.416783	0.312893

**Figure 22.** Rise time and fall time using Spice for the eighth design set of Case III. (a) Rise Time (b) Fall Time.**Figure 23.** Propagation delay times using Spice for the eighth design set of Case III. (a) High to low (b) Low to high.

6. Conclusions

This paper employs the Mayfly Algorithm (MA), one of the latest optimization algorithms, to find the optimal design of the CMOS inverter. The design problem is mathematically formulated as an optimization problem. Three case studies with different constraints and design criteria are presented to illustrate the effectiveness of the proposed optimization algorithm to find the global solution of the objective function. The results of the three case studies were used in the spice simulations in order to verify the results. In Case I, estimating of the fall time is found depending on the design parameters and 0.25 μm TSMC CMOS technology manufacturing parameters. Case I is performed for eight different sets with different ranges of design parameters and design criteria. The results show compatibility between MA results and Spice results. The maximum fall time difference between Mayfly Algorithm and Spice Simulation for all design sets is equal to 2.075711 ns. In the second case, the goal is to design an inverter with symmetrical fall and rise times. In Case II, the MA is performed for eight design sets. The difference between the fall time and rise time is minimized as shown Spice simulations, where the maximum difference between fall time and rise time is equal to 0.9784731 ns. In Case III, the CMOS inverter is designed to achieve a symmetrical fall time and rise time and a symmetrical propagation delay time. Spice simulations show that symmetry was achieved in Case III with minimum difference equal to 0.312893 ns and maximum difference equal to 1.076540 ns. Negligible variations between the MA outcomes and the spice results are observed due to more complicated models used in Spice simulations compared to the theoretical mathematical equations used in the optimization method. When comparing optimization methods, the MA contains very simple approximate expressions, and it has fast convergence and a better chance to find the global best solution of the cost function.

The values of the width to length ratio have to be slightly modified to meet design rules for the process technology used in fabricating the circuit. This modification will have an almost negligible effect on the rise and fall times. In the future, more work will be conducted to identify the optimal width to length ratio of CMOS transistors used in a CMOS inverter to achieve the minimum power dissipation and time delay. Achieving this optimal ratio is critical for developing more energy-efficient and high-performance electronic devices. The Mayfly Algorithm can not only help in optimizing the CMOS inverter but can also be extended to optimize more complex circuits, such as Schmitt trigger circuits. Schmitt trigger circuits are commonly used in applications such as signal processing, noise filtering, and waveform generation.

Author Contributions: Conceptualization, F.N.Z.; Methodology, A.A.; Software, F.N.Z.; Validation, H.A.; Formal Analysis, F.N.Z. and H.A.; Investigation, A.A. and H.A.; Resources, F.N.Z.; Data Curation, H.A.; Writing-Original Draft Preparation, F.N.Z. and H.A.; Writing-Review & Editing, A.A. and F.N.Z.; Visualization, A.A.; Supervision, F.N.Z.; Project Administration, F.N.Z. All authors have read and agreed to the published version of the manuscript.

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