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GaN Vertical Transistors with Staircase Channels for High-Voltage Applications

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Abstract: In this study, we propose and simulate the design of a non-regrowth staircase channel GaN vertical trench transistor, demonstrating an exceptional threshold and breakdown characteristic for high power and high frequency applications. The unique staircase design provides a variable capacitance through the gate-dielectric-semiconductor interface, which results in a high breakdown voltage of 1.52 kV and maintains a channel on-resistance of 2.61 mΩ·cm^2. Because of the variable length and doping profile in the channel region, this model offers greater flexibility to meet a wide range of device application requirements.

Keywords: vertical transistor; vertical GaN transistor; high power transistor; GaN-based high power transistor; staircase channel GaN transistor; GaN on GaN technology

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1. Introduction

Current telecommunications rely on the availability of power supplies. With the explosive demand for high bandwidth and 24/7 connectivity, the electrical infrastructure is facing the challenges of increasing the power conversion efficiency. In recent years, wide bandgap (WBG) materials and their corresponding power devices are attracting much attention. Gallium Nitride (GaN) is a critical WBG material for high-power, high-speed electronics. Compared to other mature devices based on Si or GaAs, GaN-based transistors exhibit exceptional properties, such as low specific on-resistance (R_{on}), high breakdown-voltage (V_{br}), and high operating frequency, giving a fixed device geometry [1–5]. Lateral GaN transistors on Si substrate have been widely studied. They are currently adopted in commercial power electronics due to their cost-effectiveness, as compared with GaN-based devices grown on GaN, SiC or other substrates. However, lateral transistors have two main limitations. First, to sustain high voltage, a large lateral gate to drain spacing is required [6], which inevitably increases the chip size. Second, thermal energy is generated and distributed primarily in the top epilayers because they are where current flow occurs [7,8], making the corresponding thermal resistance per unit chip area higher than vertical type transistors. Therefore, similar to Si power MOSFETs (metal-oxide semiconductor field-effect transistors), GaN vertical transistors have been studied by growing GaN epilayers on GaN substrate. Because lateral GaN power devices on Si substrate suffer from current collapse during high-voltage operation due to carrier trapping in the buffer region [9,10]. GaN on GaN devices have additional advantages. They avoid buffer-induced carrier trappings, making operating voltage much higher than 600 V feasible.

Several works have been reported in the last few years to develop GaN-based vertical transistors [11–13]. Based on the device architecture, there are primarily two types of structures [14,15]. The first one is the current aperture vertical electron transistor (CAVET) [16,17], consisting of a 2DEG channel induced by polarization in the AlGaN/GaN interface. In contrast, the second is the vertical GaN trench MOSFET [18,19],

which is operated based on the inversion layer. Since the fundamental vertical structure consists of a vertical p-n junction, material regrowth is crucial for most of the above vertical transistors. The pattern etching followed by the regrowth process induces impurities in the interface [20]. Although a post thermal annealing and the in-situ cleaning process can neutralize most impurities [21,22], the regrowth limits the device performance and production yield. For example, the breakdown performance is limited to around 600 V for the trench CAVET [23] and the regrowth-based MOSFET [24]. On the other hand, for a GaN vertical fin-power transistor [25,26] in which material regrowth isn't required, a higher V_{br} (>1kV) is demonstrated.

In this work, we propose and simulate a novel staircase trench design that can attain higher V_{br} and low R_{on}. The design is based on an n^+-i-P-n-n^+ non-regrowth layer structure with a unique staircase-like channel region. The staircase side wall can be realized with a non-regrowth process, which is one of the essential criteria for minimizing interface defects.

2. Design and Simulation

In order to obtain an in-depth study of the device, a systematic approach to performance analysis is carried out. The model is simulated based on standard semiconductor device physics using Poisson's equation, carrier continuity equation, and transport equation. Moreover, the breakdown characteristic is calculated by considering Selberherr's impact ionization model [27–29]. The staircase device structure is shown in Figure 1a. In practice, the fabrication of a staircase channel device can be realized by first performing three ICP-RIE (Inductively Coupled Plasma–Reactive Ion Etching) steps; each stops at i-GaN, p-GaN, and n-type drift layer. The etched thickness (though there is tolerance of an over-etch of each step) can be precisely monitored with plasma end-point detection during ICP-RIE etching. Multi-dielectric layer coating with a total thickness higher than 900 nm is proposed to fill up the staircase trench followed by source contact VIA hole etching and source electrode deposition. The gate electrode can be then deposited after the gate VIA hole definition. The drain contact is coated after the drift layer is grinded to the desired thickness. Multiple etching steps increase surface roughness and induce defects which may degrade the carrier mobility. Such surface defects can be effectively passivated with a proper recipe of GaN etching and dielectric deposition. Additionally, some advanced etching methods, such as digital etching with N_2 plasma treatment, can minimize exposed defects [30]. Parametric analysis is performed based on two major parameters: device geometry and doping concentrations. As shown in Figure 1, the model is studied by varying the drift length (L_{drift}) of the drift layer between 2 and 20 μm and drift doping concentration (n_{drift}) between 5×10^{15} and $5 \times 10^{16}/cm^3$. The gate to n^+-GaN, i-GaN, and p-GaN length, t_1, t_2, t_3, is 300, 200, and 100 nm, respectively. The typical value of p-GaN doping concentration (n_p), source contact n^+-GaN doping concentration (n^+), and n_{drift} is kept at 2×10^{17}, 8×10^{18}, and 1×10^{16} cm^{-3}, respectively. To highlight the dependence of electrical properties on the device profile near the gate-source region, we compared the proposed staircase structure with the traditional straight channel trench gate (see Figure 1b) and multi-stage staircase (see Figure 1c) structures. The purpose of the multi-stage staircase profile is to understand the electrical field and current distribution when multiple-step etching is applied to the staircase device. It can be considered as a tapered structure if the number of staircase steps is infinite. The gate to channel distance is 200 nm for a straight channel device while that of a multi-stage channel device decreases from 300 to 100 nm as labeled in Figure 1e,f. The epi-structures of all three types of devices are the same throughout the study.

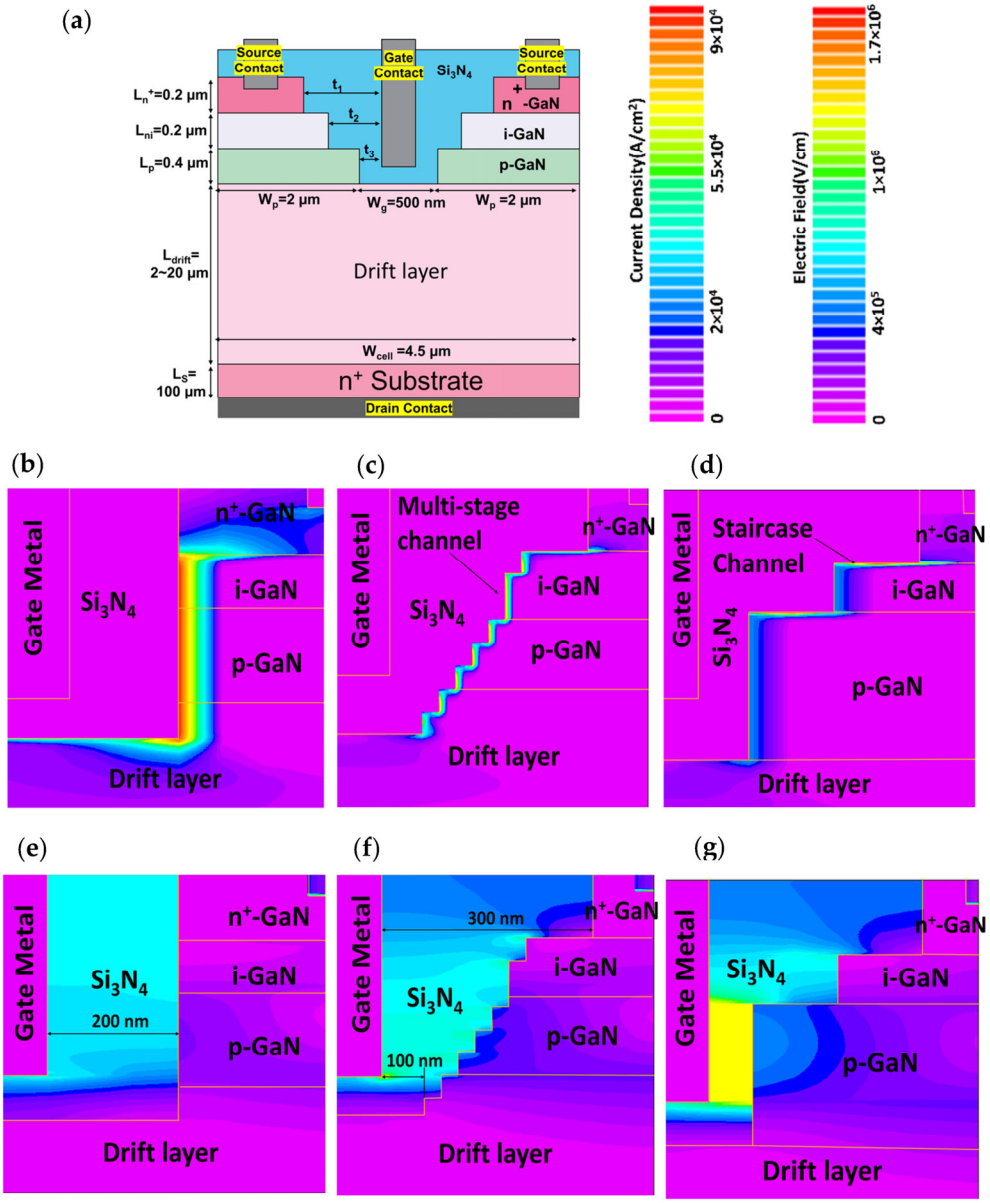

Figure 1. (**a**) Device structure of the proposed staircase channel transistor. Comparison of current density distributions in traditional straight channel (**b**), multi-stage staircase channel (**c**), and staircase channel (**d**) transistors. (**e**–**g**) Comparison of Electric field profiles of the traditional straight channel, multi-stage staircase channel, and staircase channel transistors respectively.

The on-state channel current density of the traditional straight channel trench gate, multi-stage staircase, and staircase channel device are plotted in Figure 1b–d, respectively. The above channel formation is investigated by applying a gate to source voltage higher than the threshold voltage (V_{th}) (7 V in this work). Among the devices, current density along the vertical sidewall of the traditional straight channel trench gate (Figure 1b) is the highest and the most uniform, with the current distribution deep into the sidewall. For a multi-stage device (Figure 1c), the current density increases with the depth of the channel due to the gradually reduced distance from gate metal. As for the staircase channel, current density depends on the corresponding gate-channel dielectric spacing (e.g., t_1, t_2, t_3) of each step (see Figure 1d). For instance, because of a smaller dielectric thickness between the gate metal and p-GaN, t_3, a stronger electric field in the channel leads to narrower carrier confinement, thus a better gate bias control and a higher channel transconductance.

Comparative electric field distribution of the devices is shown in Figure 1e–g. For the staircase design (shown in Figure 1g), due to the shortest spacing between the gate and p-GaN region, the electric field in the p-GaN layer is the strongest. It creates a strong inversion at the interface of the p-GaN region for the staircase channel. It is observed that the electric field at the dielectric/semiconductor interface is strong and exponentially decays away from the interface. The e-field gradient is lower in the intrinsic region than in the p-GaN region, which is one of the reasons for a broader carrier distribution in the intrinsic region.

V_{th} is one of the key parameters to understanding the device's switching and leakage performance. A greater value of V_{th} (generally greater than 3 V) is always expected in high-power applications. Conceptually, it is mainly determined by the p-type and n-type drift layers. The comparative transfer characteristics between straight, multistage, and staircase channels are shown in Figure 2a, in which staircase structure exhibits a higher threshold voltage than the other two types of transistors. For the staircase channel transistor, the variation of V_{th} with respect to different values of n_p is plotted in Figure 2b. It is observed that the V_{th} significantly increases with n_p. Since a higher n_p has a stronger depletion and reverse field, it requires a larger gate to source potential (V_{gs}) to accumulate carriers at the dielectric-semiconductor interface and to switch on the device. Hence a large V_{th}, extracted from linear extrapolation of the transfer curve, around 6.6 V can be achieved at n_p of 1×10^{17} cm^{-3} while keeping n_{drift}, L_p, L_{drift} at 1×10^{16} cm^{-3}, 200 nm, and 12 µm, respectively. Figure 2c also shows a slight dependence of V_{th} on the n_{drift}. Variations of V_{th} to t_1, t_2, and t_3 of the staircase device are explored in Figure 2d. The thickness of a certain parameter is varied by keeping the rest two to their original assigned values. V_{th} is calculated using linear extrapolation of the transfer curves. It demonstrates that V_{th} increases with layer thickness.

The output characteristics were obtained by sweeping the drain voltage with fixed gate voltages. Figure 3a–c represent the output characteristics of straight, multi-stage, and staircase channels, respectively. Sharp increase of linear current reflects very low R_{on} values of 1.54 mΩ·cm^2, 1.63 mΩ·cm^2, and 1.77 mΩ·cm^2 for the straight, multistage, and staircase devices, respectively. For this study, the thickness and doping concentration of each layer were kept constant throughout all types of devices. The breakdown characteristics are obtained by sweeping the drain to source voltage and keeping the V_{gs} less than V_{th}. A comparative breakdown analysis was carried out among the devices and is plotted in Figure 3d, where the L_{drift} is 9 µm and all other structural parameters were kept the same among devices. V_{br}, defined as the voltage at which the reverse current is 10^{-10} A/µm^2, of the traditional straight channel trench, multi- stage staircase, and staircase channel transistor is 880, 972, and 1086 V, respectively. It is shown that the staircase design can have superior breakdown performance compared to the other two types of vertical design. This phenomenon can be explained by considering the channel current density depicted in Figure 1b. Moreover, with a careful design of L_{drift} (~20 µm), a large V_{br} around 2.12 kV can be achieved while keeping n_p, n_{drift}, and L_p at 2×10^{17} cm^{-3}, 1×10^{16} cm^{-3}, and 400 nm, respectively.

However, the threshold voltage predominantly depends on t_3.

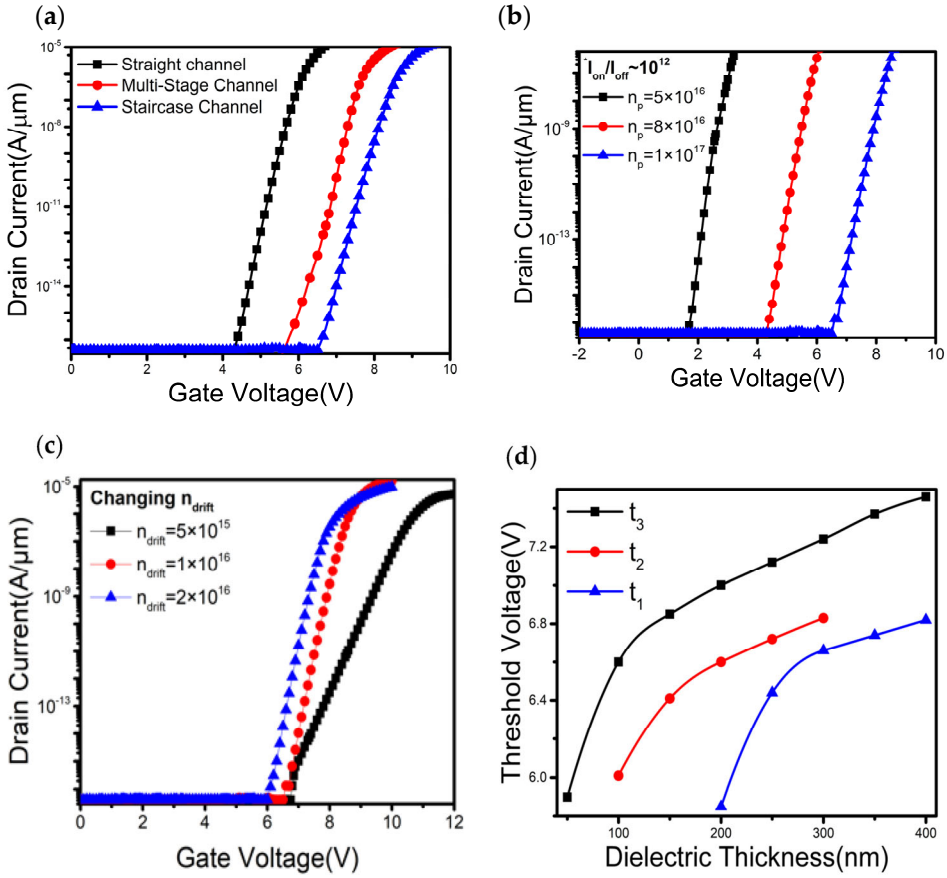

Figure 2. Transfer characteristics of the devices (**a**) Transfer curves of different types of vertical transistors with the same layer thickness and doping concentration. (**b**) Transfer curves of the staircase channel transistor at various n_p. (**c**) Variation of transfer curves of the staircase channel transistor with n_{drift}. For (**a**–**c**), the drain voltage for demonstrating transfer curves is 5V. (**d**) Variations of threshold voltage to the lateral dielectric layer (staircase) thickness.

Conceptually, a larger L_{drift} with a smaller n_{drift} can help distribute the field generated by large drain voltage so that the effective field is lower than the critical field for avalanche breakdown. Therefore, parameter optimization is crucial to satisfy different application requirements. The variation of the staircase channel potential is depicted in Figure 4a. It is observed that the channel potential at dielectric/semiconductor interface is strong and exponentially decays away from the interface. The channel potential gradient is lower in the intrinsic region than that in the p-GaN region, which is one of the reasons for a broader carrier distribution in the intrinsic region. The breakdown occurs as a result of an avalanche process triggered by impact ionization. At a very high drain to source potential, electrons at p-GaN and drift n-GaN interface obtain high kinetic energy and undergo scattering events, where the excess energy transferred to neighboring atom, generating new electron-hole pairs. This process continues and rapid carrier multiplication occurs. Sudden surge in generated carriers results a direct current flow between n^+ source and drain terminal, hence the gate loses its control over the channel and avalanche breakdown occurs. The generation rate of interface charges by impact ionization is represented in Figure 4b. It is observed that the impact ionization rate is maximum at the edges as indicated as point P_1.

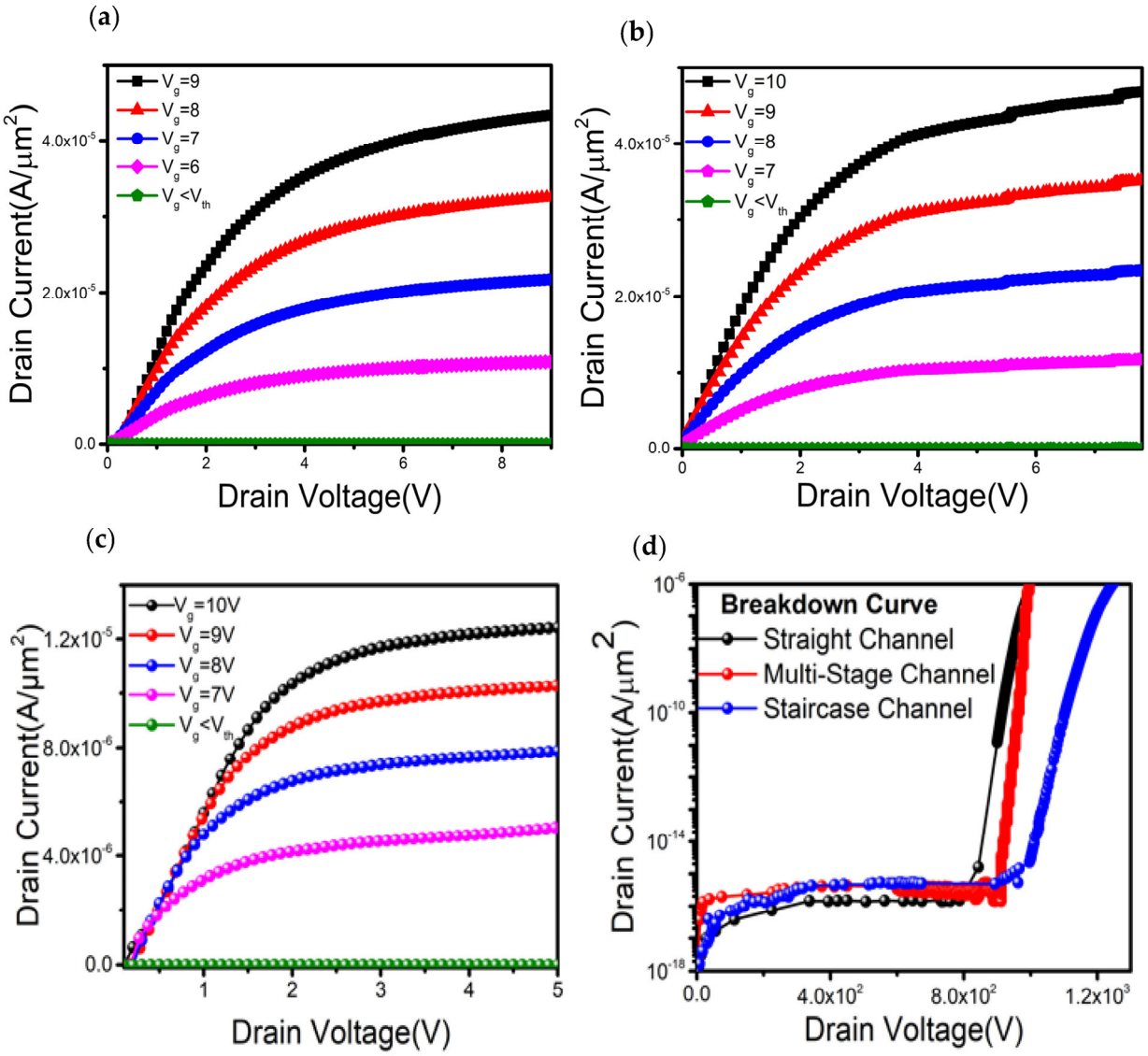

Figure 3. (**a**) Output characteristics of the straight channel trench channel transistor. (**b**) Output characteristics of the multi-stage channel transistor. (**c**) Output characteristics of the staircase channel transistor. (**d**) Comparisons of breakdown characteristics of the straight channel trench gate, multi-stage staircase and staircase channel transistors, where the layer thickness and corresponding doping concentration are kept the same for all structures.

In general, the optimization is performed based on the desired application. In this study, optimization is carried out to achieve balanced performance between high V_{br} and low R_{on}. First, the L_{drift} is optimized while maintaining other parameters, n_p, L_p, and n_{drift}, constant at 2×10^{17} cm^{-3}, 400 nm, and 1×10^{16} cm^{-3}, respectively. The L_{drift} varies from 2 to 20 μm. As shown in Figure 5a, the V_{br} increases with L_{drift} but gradually saturated when L_{drift} exceeds 16 μm. On the other hand, the R_{on} increases linearly with L_{drift}. By setting L_{drift} to be 12 μm, we can obtain a R_{on} of 2.61 mΩ·cm^2 and a V_{br} of 1.52 kV. Next, the n_{drift} is optimized by keeping L_{drift} at 12 μm, as plotted in Figure 5b. By increasing n_{drift}, the V_{br} is reduced. The result is due to the reduced R_{on} when the carrier density between the source and drain increases. When the n_{drift} is larger than 1×10^{16} cm^{-3}, a sharp decrease of V_{br} but a slow decrease of R_{on} is observed. Hence, the n_{drift} around 1×10^{16} cm^{-3} or lower is most acceptable for high-power applications.

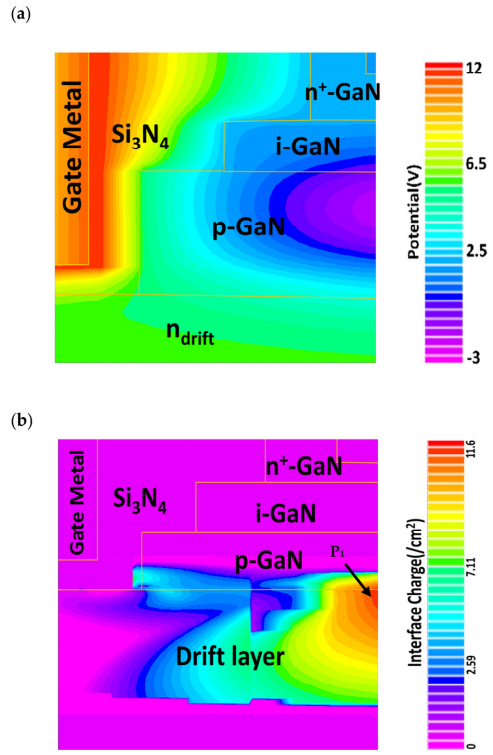

Figure 4. (**a**) Variation of channel potential of the staircase channel transistor.; (**b**) Generation rate of charge carriers by impact ionization.

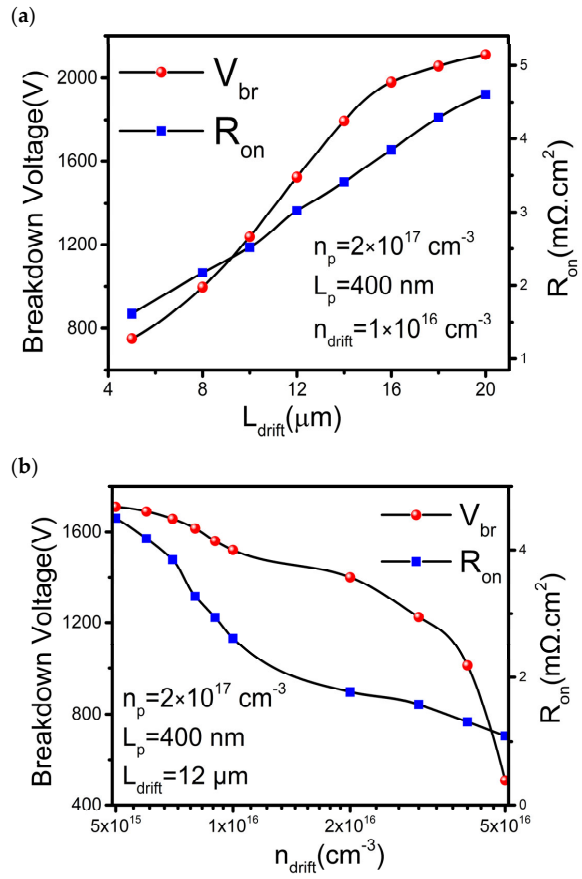

Figure 5. Optimization of V_{br} with various parameters: (**a**) drift length (L_{drift}), (**b**) Drift doping concentration (n_{drift}), with constant n_p, L_p and L_{drift} at 2×10^{17} cm^{-3}, 400 nm and 12 µm respectively.

Moreover, the p-type region is vital for switching performance and breakdown characteristics. Optimization is carried out by correlating n_p to L_p. Generally, a thicker p-layer with a higher doping concentration leads to an increase of channel resistance. It improves the breakdown voltage but the channel resistance increase slows down the switching operation. As plotted in Figure 6a, when n_p increases, the V_{br} increases linearly and saturates at n_p around 2×10^{17} cm^{-3}. Similarly, the R_{on} increases slowly until n_p reaches 1×10^{17} cm^{-3}. In such a case, the optimized np is around 2×10^{17} cm^{-3}. In addition, the R_{on} and V_{br} increase with the thickness of the p-type layer, L_p (see Figure 6b). The optimum V_{br} and R_{on} are achieved for L_p around 300~400 nm.

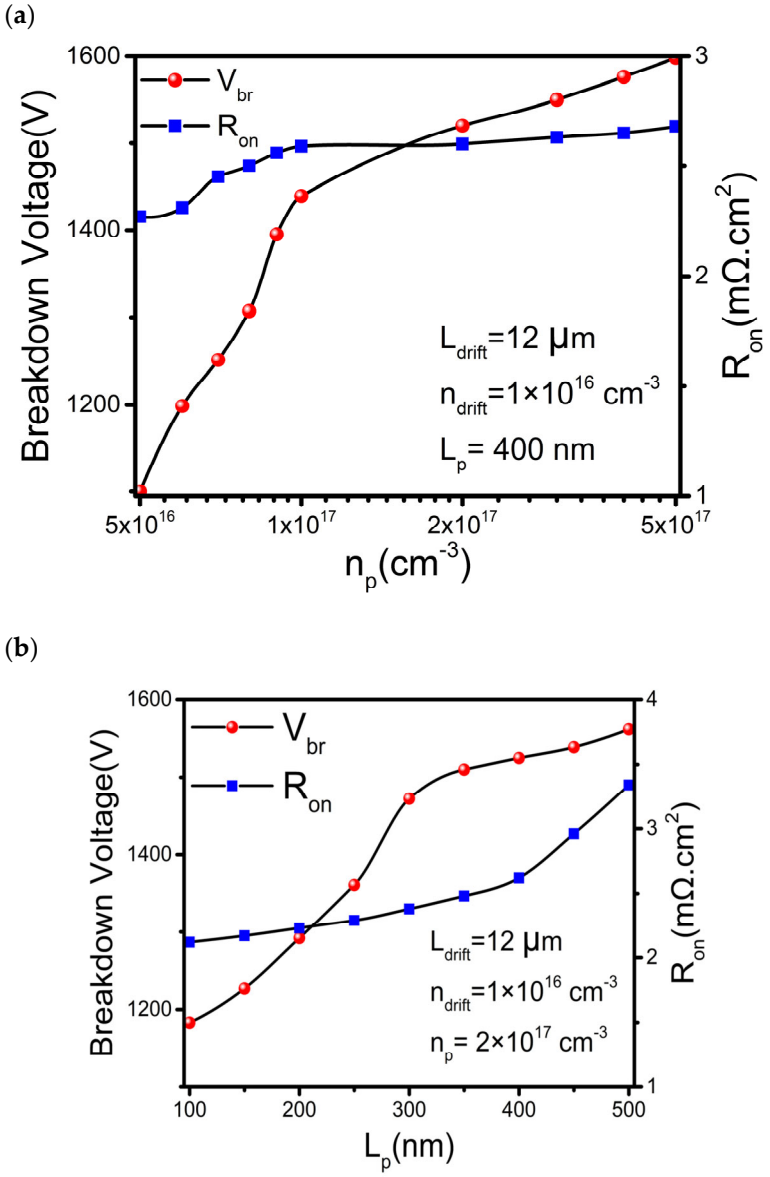

Figure 6. Optimization of V_{br} with respect to (**a**) p-doping concentration (n_p) and (**b**) P-layer thickness (Lp).

3. Conclusions

In this study, a novel staircase design of a vertical GaN transistor without regrowth is demonstrated. The variable gate dielectric thickness along the channel helps to achieve a V_{th} of 6.6 V. A comparative study has been made with respect to traditional straight channel trench and multi-stage channel structures. The current density and the electric field profile in the channel of the staircase design show a superior control over channel

carrier density compared to other two type of design. By adjusting the layer thickness and doping concentration, a specific device performance is accomplished, which provides adequate design flexibility for a wide range of applications. The stronger off-state effective channel resistance of the staircase structure leads to a high V_{br} of up to 2.12 kV and a R_{on} of 4.21 mΩ·cm^2 at a L_{drift} of 20 µm. For a balanced performance between R_{on} and V_{br}, a V_{br} of 1.52 kV and a R_{on} of 2.61 mΩ·cm^2 can also be achieved at L_{drift} of 12 µm. The high breakdown voltage with low on-resistance suggests that the devices have the potential for high-voltage applications.

Author Contributions: K.B. and J.-J.H. conceived the idea and planned the research. K.B. and D.-J.L. performed the theoretical modelling. K.B. and C.-K.C. performed the simulation and optimization. K.B., J.-J.H. and R.G. wrote the original draft of the paper, and all authors contributed to the review and editing of the paper. J.-J.H. acquired the funding and supervised the study. All authors have read and agreed to the published version of the manuscript.

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