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Improved I_{on}/I_{off} Current Ratio and Dynamic Resistance of a p-GaN High-Electron-Mobility Transistor Using an $Al_{0.5}GaN$ Etch-Stop Layer

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Abstract: In this study, we investigated enhance mode (E-mode) p-GaN/AlGaN/GaN high-electron-mobility transistors (HEMTs) with an $Al_{0.5}GaN$ etch-stop layer. Compared with an AlN etch-stop layer, the $Al_{0.5}GaN$ etch-stop layer not only reduced lattice defects but engendered improved DC performance in the device; this can be attributed to the lattice match between the layer and substrate. The results revealed that the $Al_{0.5}GaN$ etch-stop layer could reduce dislocation by 37.5% and improve device characteristics. Compared with the device with the AlN etch-stop layer, the p-GaN HEMT with the $Al_{0.5}GaN$ etch-stop layer achieved a higher drain current on/off ratio (2.47×10^7), a lower gate leakage current (1.55×10^{-5} A/mm), and a lower on-state resistance (21.65 Ω·mm); moreover, its dynamic R_{ON} value was reduced to 1.69 (from 2.26).

Keywords: etch-stop layer; high selectivity ratio; normally off; p-GaN gate HEMT

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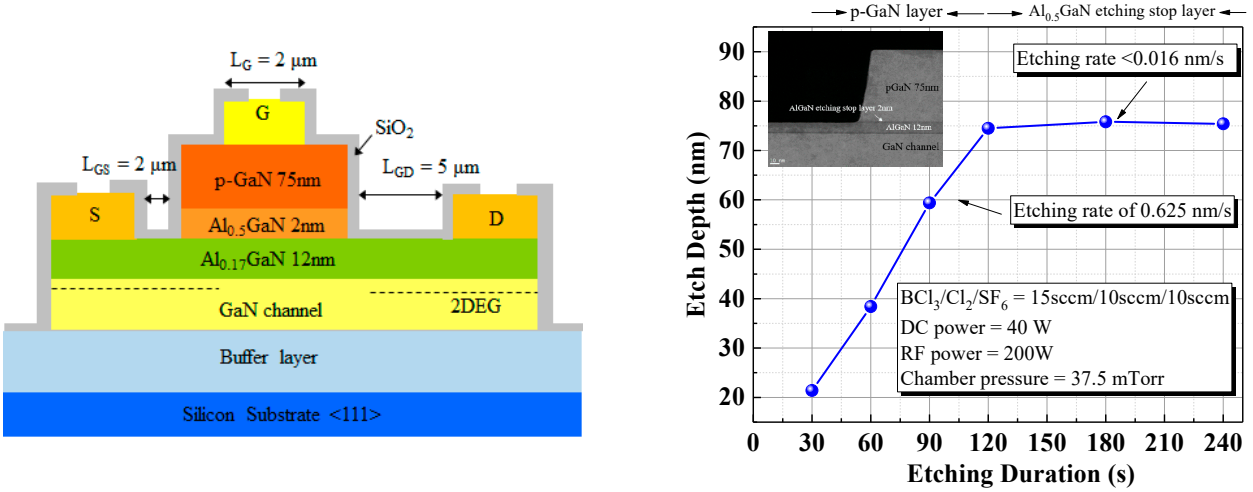
1. Introduction

In recent years, the wide bandgap (WBG) GaN-based high-electron-mobility transistors (HEMTs) have attracted much attention for high-radio-frequency (RF) and high-power semiconductor device applications owing to their excellent performance of high electric field strength (3.3 MV/cm), high mobility (>1200 cm^2/Vs), and favorable thermal conductivity [1–3]. To get realistic power supply applications, the normally off behavior of GaN-based HEMTs must be implemented. Thus, several methods have attempted to realize the positive threshold voltage (V_{TH}) of AlGaN/GaN HEMTs, such as ultrathin barriers, gate-recessed structures, fluorine treatment, and p-type gates [4–8]. However, structures involving p-type gates have drawn increasing attention in industry owing to their low on-state resistance and high threshold voltage. The precision and lower damage etching process is a key factor in device fabrication, and outstanding etching depth control is imperative because the residual p-GaN layer in the out-of-gate area makes the 2DEG channel depleted and leads to a low forward current. Moreover, if the p-GaN layer is overetched in to the AlGaN barrier layer and reduces the AlGaN barrier thickness in this process, the channel carrier density is decreased because of the decrease in spontaneous polarization. In tradition structures, an AlN layer is used as an etch-stop layer; however, high-quality thin AlN has difficulty achieving epitaxy control, and problems related to lattice mismatch can arise [9,10]. In this study, we applied an $Al_{0.5}GaN$ etch-stop layer

between p-GaN and AlGaN barriers and compared its performance with that of an AlN etch-stop layer. The experimental results indicated that the dynamic R_{ON} was improved and that the leakage current was suppressed. Transmission electron microscopy (TEM) images revealed the etch-stop layer to be smooth and highly selective. Therefore, high-performance normally off p-GaN/AlGaN/GaN HEMTs can be realized using an AlGaN etch-stop layer for high-speed and high-power electronic applications.

2. Device Structure

As illustrated in Figure 1a, we present a new p-GaN/AlGaN/GaN HEMT structure with an $Al_{0.5}GaN$ etching stop design grown through metal organic chemical vapor deposition (MOCVD) on a 6 in silicon (111) wafer. The epistructure was composed, from bottom to top, of a 4 µm-thick C-doped GaN buffer layer, a 300 nm-thick undoped GaN channel layer, a 12 nm-thick undoped $Al_{0.17}GaN$ barrier layer, a 2 nm $Al_{0.5}GaN$ etch-stop layer, and a 75 nm-thick p-type GaN top layer whose active Mg concentration was 1×10^{18} cm^{-3}.



(**a**) (**b**)

Figure 1. (**a**) Schematic cross-sectional structure of the p-GaN gate HEMT with an $Al_{0.5}GaN$ etch-stop layer design. (**b**) p-GaN etch depth versus the etch duration and TEM image after etching (inset).

For device fabrication, we used standard photolithography and lift-off technology, the active region was defined by a photoresist and etched to a depth of 200 nm using BCl_3/Cl_2 mixed-gas plasma by reactive ion etching (RIE). A 5 µm-long p-type GaN gate platform was formed through a mixture of $BCl_3/Cl_2/SF_6$ gas plasma 120 s to remove p-GaN by inductively coupled plasma (ICP). The F radicals from the SF_6 plasma and Al atoms from the $Al_{0.5}GaN$ barrier layer created a fluorination reaction and formed a thin aluminum fluoride (AlF_3) etch-stop layer [11]. The resulting etching rate was 0.625 nm/s. Moreover, the $A_{0.5}GaN$ layer was etched at an etching rate of <0.016 nm/s, implying a high-selectivity etching process in the p-GaN/$Al_{0.5}GaN$ layer. Subsequently, the formed AlF_3 can be removed by diluted HF/NH_4OH chemical solution [12]. As indicated in Figure 1b the p-GaN removal depth was measured using an atomic force microscope (AFM) and the inset of that figure presents a TEM image after p-GaN etching. This was followed by the source and drain ohmic contact formation where a Ti/Al/Ni/Au (25 nm/120 nm/25 nm/150 nm) ohmic metal stack was deposited by electron beam evaporation and thermally annealed at 875 °C for 30 s in ambient nitrogen (N_2) by rapid thermal annealing system (RTA). Third, the device was fabricated with implant isolation through oxygen implantation. Finally, the Ni/Au (25 nm/120 nm) gate electrode (gate length: 2 µm) was deposited through electron beam evaporation, and 100 nm of SiN was passivated.

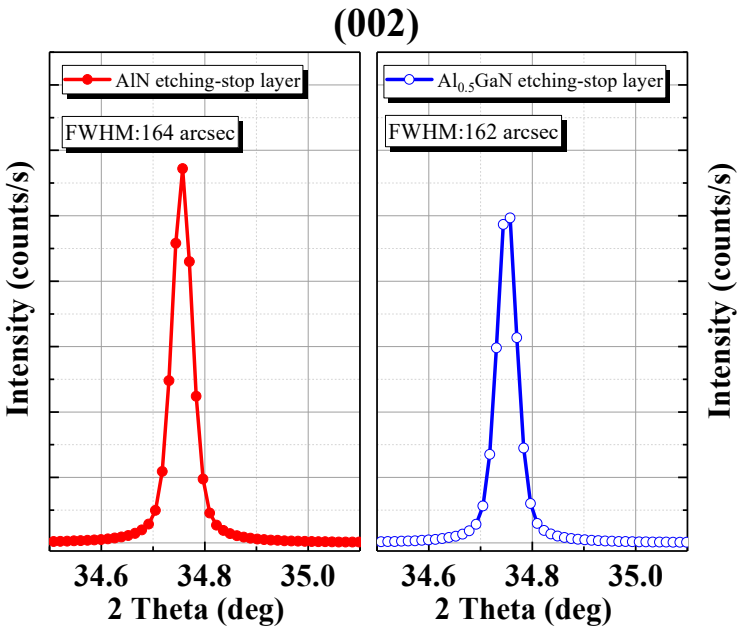
3. Experimental Results and Discussion

X-ray diffraction (XRD) was used to investigate the dislocation density, and the results are presented in Figure 2. The full width at half-maximum (FWHM) values of the (002) symmetric and (102) asymmetric reflection were used to measure crystal quality. In our device surface measurements, we mainly investigated the crystal quality on the device surface. The FWHM values for the (002) and (102) planes of the AlN and AlGaN etch-stop layer designs were 164/239 and 162/179 arcsec, respectively. In general, the rocking curve scan of a (002) reflection provides information on the degree of tilt with respect to the surface of a device, and the FWHM of this reflection is a qualitative measure of screw dislocation density (N_{screw}) [13,14]. The rocking curve scan of a (102) reflection provides information on the degree of twist with respect to the surface of a device, and the FWHM of this reflection is a measure of edge dislocation density (N_{edge}). The dislocation density can be calculated using XRD-derived FWHM results as follows:

$$N_{screw} = \frac{FWHM_{002}^2}{4.35 \times b_{screw}^2}, N_{edge} = \frac{FWHM_{102}^2}{4.35 \times b_{edge}^2}, \quad (1)$$

$$N_{total} = N_{screw} + N_{edge} \quad (2)$$

where N_{screw} and N_{edge} are the screw and edge dislocation densities, respectively, and b is Burger's vector. In this study, these equations were used for calculation, and the results revealed that the total dislocation (N_{total}) values of the $Al_{0.5}GaN$ etch-stop layer and AlN etch-stop layer were $2.23 \times 10^8/cm^2$ and $3.57 \times 10^8/cm^2$, respectively. As indicated in Figure 2, the screw dislocation density and edge dislocation density were lower when the $Al_{0.5}GaN$ etch-stop layer was used than when the AlN etch-stop layer was used.



(**a**)

Figure 2. *Cont.*

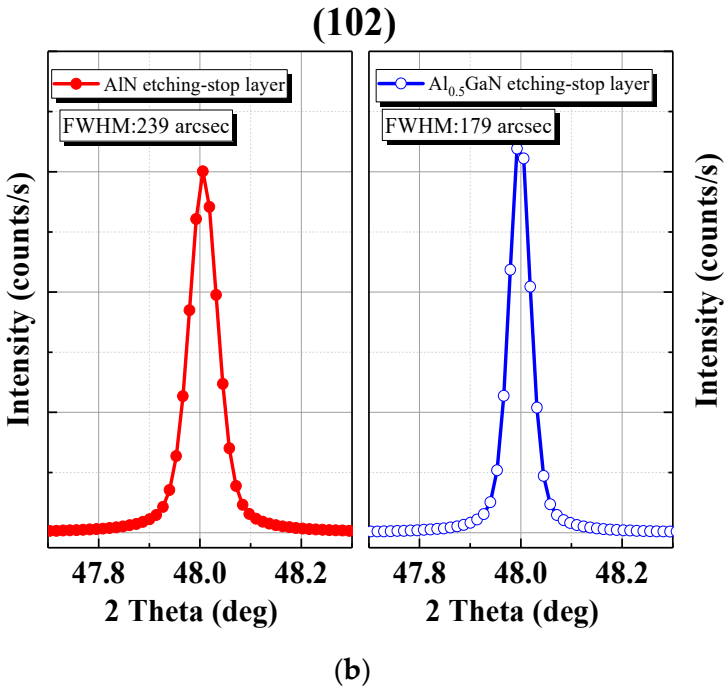


Figure 2. XRD measurement of the FWHM at the $Al_{0.5}Ga$ N etch-stop layer and AlN etch-stop layer. (**a**) (002) symmetric reflection and (**b**) (102) asymmetric reflection.

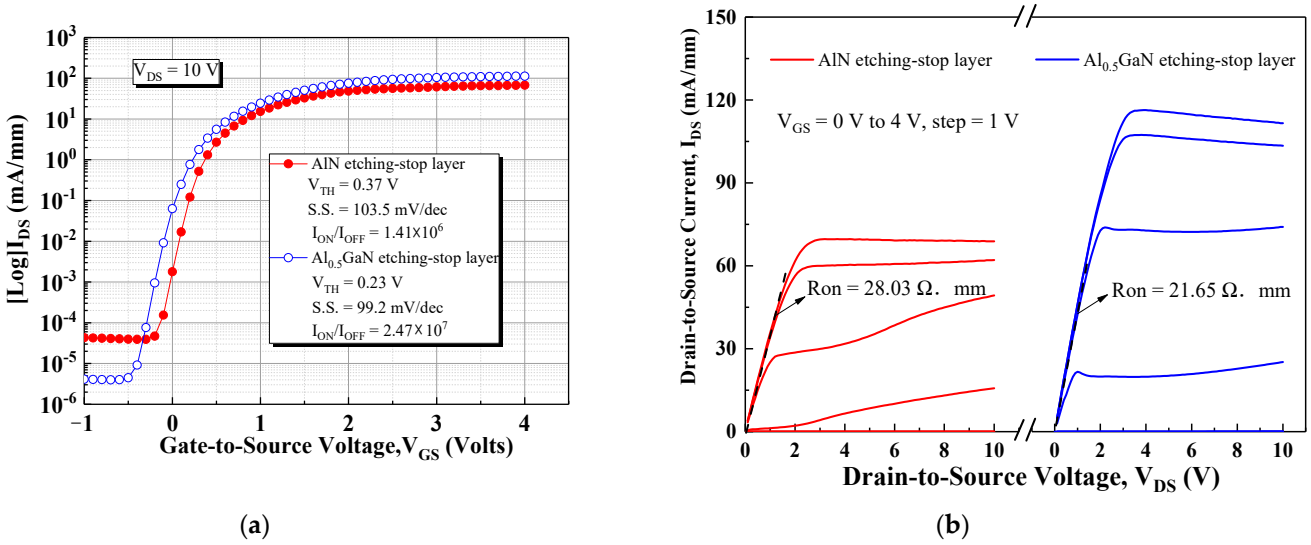
To study the effects of the layers on DC performance, we measured the transfer (I_{DS}–V_{GS}) and output (I_{DS}–V_{DS}) characteristics of the devices by using an Agilent 4142B monitor. Figure 3a presents a plot of the log-scale I_{DS}–V_{GS} curve as a function of gate-to-source voltage (V_{GS}) under biasing at a drain-to-source voltage (V_{DS}) of 10 V. The threshold voltage (V_{TH}) of the devices was defined as the V_{GS} level at which I_{DS} reached 1 mA/mm. We observed that threshold voltage (V_{TH}) values of the devices with the AlN etch-stop layer and AlGaN etch-stop layer were 0.37 and 0.23 V, respectively. At a gate bias of 4 V, the maximum output current density (I_{Dmax}) values of the devices with the AlN and AlGaN etch-stop layers were 67 and 121 mA/mm, respectively. At a gate bias of −1 V, the off-state current values of the devices with the AlN and AlGaN etch-stop layers were 4.31×10^{-5} and 4.11×10^{-6} mA/mm, respectively. The device with the $Al_{0.5}GaN$ etch-stop layer had a superior I_{on}/I_{off} ratio to the device with the AlN etch-stop layer, which increased from 1.41×10^{6} to 2.47×10^{7}. Moreover, the subthreshold swing (S.S.) values of the devices with the AlN and $Al_{0.5}GaN$ etch-stop layers were 103.5 and 99.2 mV/dec, respectively. The subthreshold swing (S.S.) is expressed by the analytical equation given below [15]

$$\text{S.S.} = (\ln 10)\left(\frac{kT}{q}\right)\left(1 + \frac{Cd + Cit}{Cox}\right) \tag{3}$$

$$Dit = \frac{Cit}{q} \tag{4}$$

where kT/q is the thermal voltage, C_{ox} is the capacitance of the gate dielectric, C_d the depletion capacitance, C_{it} is the capacitance of gate and semiconductor interface state, D_{it} is interface charge densities, and q is the electronic charge. The capacitance of the gate dielectric (C_{ox}) for the AlN stop layer and $Al_{0.5}GaN$ stop layer was measured to be 222 nF/cm^2 and 184 nF/cm^2 under a frequency of 1M Hz. Therefore, the interface charge densities (Dit) can be calculated and the D_{it} values of the AlN stop layer and $Al_{0.5}GaN$ stop layer device were 1.02×10^{12} and 7.64×10^{11} cm^{-2} eV^{-1}, respectively. This indicated the device with the $Al_{0.5}GaN$ stop layer had better defect density suppression. The $Al_{0.5}GaN$ stop layer design was determined to be suitable for device switching owing to its favorable I_{on}/I_{off} ratio and gate drive-control capability. Figure 3b illustrates the I_{DS}–V_{DS} curves as

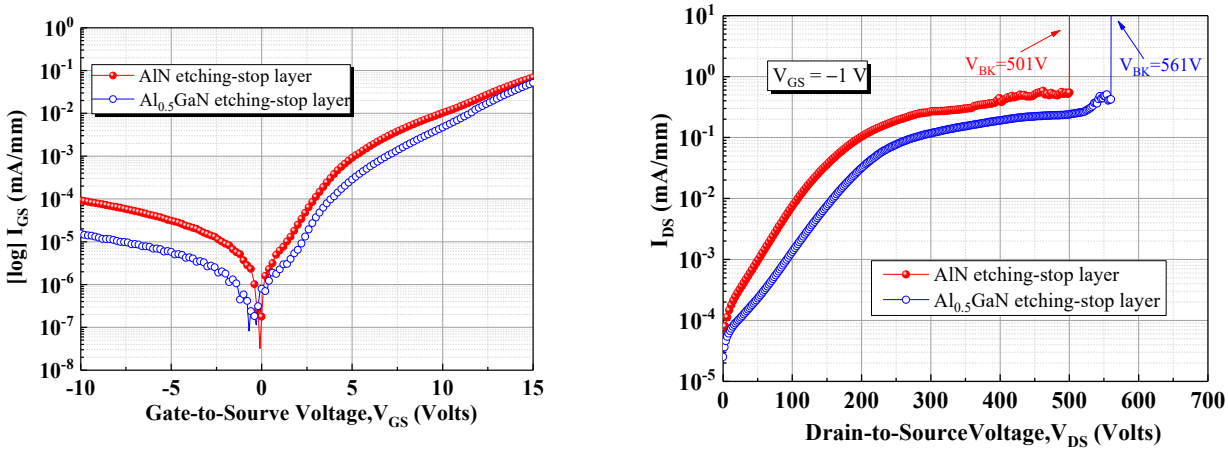
functions of the gate-to-source voltage (V_{GS}) bias ranging from 0 to 4 V in steps of 1 V and of the drain-to-source voltage (V_{DS}) sweep ranging from 0 to 10 V. The ON-resistance (R_{ON}) could be reduced from 28.03 to 21.65 Ω mm owing to the lower dislocation trap density and the suppressed trap density effect in the channel.



(**a**) (**b**)

Figure 3. I–V characteristic comparison of both devices (device dimension: $L_{GS}/L_G/L_{GD}/W_G$ = 2 μm/2 μm/5 μm/100 μm). (**a**) Transfer characteristics and (**b**) output characteristics.

The gate leakage curve presented in Figure 4a was used to investigate the leakage current mechanism. The device with the $Al_{0.5}GaN$ etch-stop layer exhibited a lower gate leakage current than did the other device. This low gate leakage current not only increased the device breakdown voltage but also improved the gate operator voltage. The off-state breakdown voltage (V_{BR}) was measured using an Agilent B1505 analyzer; the V_{GS} was 1V and the drain leakage current reached 1 mA/mm. As displayed in Figure 4b, the V_{BR} values of the devices with the AlN and $Al_{0.5}GaN$ etch-stop layers were 501 and 561 V, respectively. Moreover, Baliga's figure of merit ($BFOM = {V_{BR}}^2/R_{DS\_on}$) for various power transistors was calculated to evaluate the overall performance of these devices [16,17]. The *BFOM* values of the devices with the AlN and $Al_{0.5}GaN$ etch-stop layers were 44.37 and 83.11 MW/cm^2, respectively.



(**a**) (**b**)

Figure 4. (**a**) Gate leakage characteristics and (**b**) off-state breakdown voltage measurement of both devices.

The Maury AMCAD pulse IV system was used to further investigate trapping/detrapping phenomena and the dynamic behavior of the devices [18,19]. Furthermore, the I_{DS}–V_{DS} characteristics were also measured from different quiescent bias points at V_{GS} = 4 V to investigate the influence of off-state gate bias stress on dynamic R_{ON} and I_{DS}, as illustrated in Figure 5. The reference off-state was set to (V_{GSQ}, V_{DSQ}) = (0 V, 0 V); this setting did not induce any relevant trapping. The device was switched with a 2 µs pulse width and 200 µs period. The quiescent gate bias (V_{GSQ}) was swept from 0 to −3 V. The current collapse in the device with the AlN etch-stop layer was worse than that in the device with the $Al_{0.5}GaN$ etch-stop layer, and the high gate lag of the device with the AlN layer under gate voltage stress resulted in a decrease in the *I*–*V* slope, indicating that the surface defect trap density of this device was higher than that of the device with the $Al_{0.5}GaN$ etch-stop layer. The dynamic R_{ON} ($R_{ON}/R_{ON(0,0)}$) of the device with the $Al_{0.5}GaN$ etch-stop layer slightly increased with the gate bias stress from 0 to −3 V because of the low electron injection into the surface trap states from the gate electrode [20]. The dynamic R_{ON} ratio increased to 2.26 and the dynamic drain current decreased to 41.4% when the off-state gate bias stress was −3 V for the device with the AlN etch-stop layer.

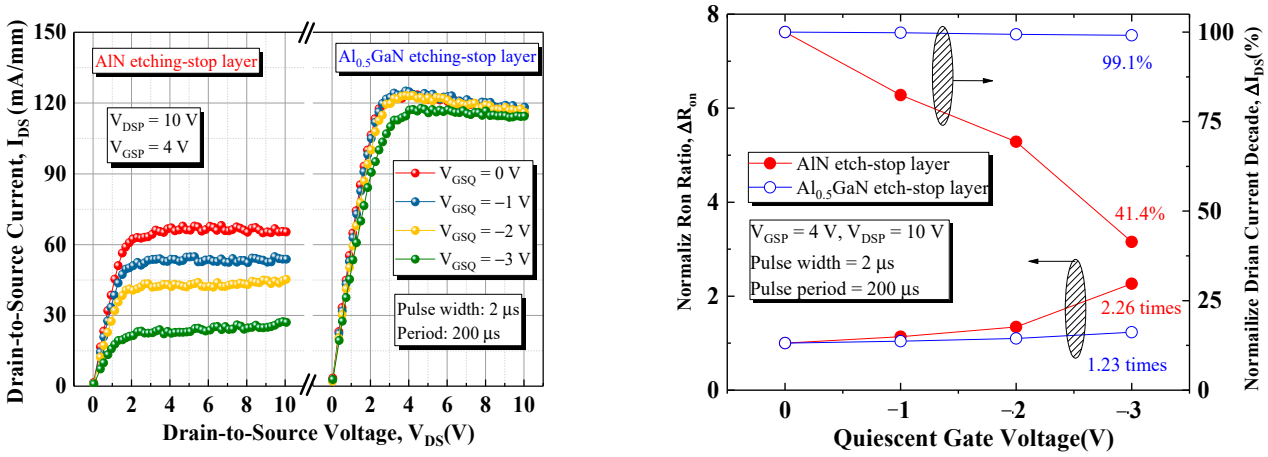


Figure 5. (**a**) Pulsed I_{DS}–V_{DS} characteristics after quiescent gate bias (V_{GSQ}) stress and (**b**) dependence of the R_{ON} collapse ratio and I_{DS} decay versus various quiescent gate voltages of both devices.

4. Conclusions

In this study, a highly selective $Al_{0.5}GaN$ etch-stop layer was applied to a p-GaN/AlGaN/GaN HEMT. Compared with the traditional AlN etch-stop layer structure, the $Al_{0.5}GaN$ etch-stop layer had a lower dislocation density, according to our XRD results; dynamic R_{ON} and dynamic I_{DS} were significantly lower in the device with the $Al_{0.5}GaN$ etch-stop layer. Furthermore, the device with the $Al_{0.5}GaN$ etch-stop layer had superior DC characteristics to the other device, including a lower off-state current, lower gate leakage, lower on-resistance, higher on/off ratio, good subthreshold swing, and higher off-state breakdown voltage. A *BFOM* assessment revealed that applying an $Al_{0.5}GaN$ etch-stop layer is a promising method for fabricating high-performance normally off p-GaN HEMTs.

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Conflicts of Interest: The authors declare no conflict of interest.

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