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New Power MOSFET with Beyond-1D-Limit R_{SP} - BV Trade-Off and Superior Reverse Recovery Characteristics

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Abstract: The application of conventional power metal-oxide-semiconductor field-effect transistor (MOSFET) is limited by the famous one-dimensional “silicon limit” (1D-limit) in the trade-off relationship between specific on-resistance (R_{SP}) and breakdown voltage (BV). In this paper, a new power MOSFET architecture is proposed to achieve a beyond-1D-limit R_{SP} - BV trade-off. Numerical TCAD (technology computer-aided design) simulations were carried out to comparatively study the proposed MOSFET, the conventional power MOSFET, and the superjunction MOSFET. All the devices were designed with the same breakdown voltage of ~550 V. The proposed MOSFET features a deep trench between neighboring p-bodies and multiple p-islands located at the sidewall and bottom of the trench. The proposed MOSFET allows a high doping concentration in the drift region, which significantly reduces its R_{SP} compared to the conventional power MOSFET. The multiple p-islands split the electric field into multiple peaks and help the proposed MOSFET maintain a similar breakdown voltage to the conventional power MOSFET with the same drift region thickness. Another famous device technology, the superjunction MOSFET (SJ-MOSFET), also breaks the 1D-limit. However, the SJ-MOSFET suffers a snappy reverse recovery performance, which is a notorious drawback of SJ-MOSFET and limits the range of its application. On the contrary, the proposed MOSFET presents a superior reverse recovery performance and can be used in various power switching applications where hard commutation is required.

Keywords: power MOSFET; deep trench; p-islands; beyond-1D-limit; reverse recovery

1. Introduction

The power metal-oxide-semiconductor field-effect transistor (MOSFET) is a commonly used power switch in power switching applications. To obtain a higher breakdown voltage (BV) in the conventional power MOSFET, the drift region has to be thicker and more lightly doped, which leads to a higher specific on-resistance R_{SP} ($= R_{DS-ON} \times \text{area}$). Thus, there is a trade-off relationship between R_{SP} and BV , which is often referred to as the “silicon limit” or “1D-limit”: $R_{SP} \propto BV^{2.5}$ [1–3]. As a consequence, when the blocking voltage of the power MOSFET increases, its R_{SP} rises quickly. For blocking voltages above 200–300 V, conventional power MOSFETs are not preferred due to the high R_{SP} .

The superjunction MOSFET (SJ-MOSFET) features laterally repeated p/n pillars, which assists the voltage blocking capability by lateral depletion [4–7]. Thus, the doping concentration of the pillars can be much higher than that of the drift region in conventional power MOSFET. In off-state, the electric field in the SJ-MOSFET keeps almost constant along the depth of the n/p pillars, so the pillars can be much shorter than the drift region of the conventional power MOSFET for the same BV .

Therefore, the SJ-MOSFET breaks the 1D-limit in R_{SP} - BV trade-off, owing to the shorter and more heavily doped n-pillar compared to the drift region of conventional power MOSFET [8–11]. The first SJ-MOSFET was demonstrated in 1998 [9]. A key to the development of SJ-MOSFET is the scaling of the p/n-pillars, which has been steadily advancing with the progress of fabrication technology. After around twenty years' development, the most advanced SJ-MOSFET boasts a R_{SP} as low as $10 \text{ m}\Omega\cdot\text{cm}^2$ for a 600-V voltage rating, which is over five times lower than the theoretical R_{SP} according to the silicon limit [4,12]. However, the large aspect PN junction area of the SJ-MOSFET leads to snappy reverse recovery performance and prohibits its adoption in many applications [13–15]. Although various approaches have been proposed to improve the performance of body diode in conventional power MOSFETs and SJ-MOSFETs, such as carrier lifetime control [16,17], integration of Schottky diodes [18–20], usage of anti-parallelled freewheeling diode [21–23], and injection control using channel diode [24,25], the snappy reverse recovery of the SJ-MOSFET remains an unsolved issue since it is intrinsic to the SJ-MOSFET structure.

In this paper, a new power MOSFET is proposed to obtain a beyond-1D-limit R_{SP} - BV trade-off and a superior reverse recovery performance. The proposed MOSFET features a deep trench and multiple p-islands located at the trench sidewall. The proposed MOSFET was comprehensively studied using numerical TCAD (technology computer-aided design) device simulations and mixed-mode circuit simulations and compared with a conventional power MOSFET and a SJ-MOSFET. All the MOSFETs were designed with a breakdown voltage of $\sim 550 \text{ V}$. The proposed MOSFET allows a higher doping concentration in the drift region, which significantly reduces the R_{SP} . The multiple p-islands split the electric field peak of the conventional power MOSFET into multiple peaks so that a high breakdown voltage is maintained. A beyond-1D-limit R_{SP} - BV trade-off was achieved in the proposed MOSFET. Furthermore, the notorious snappy reverse recovery performance of a SJ-MOSFET is avoided in the proposed MOSFET, which allows the proposed MOSFET to be adopted in a much wider range of applications.

The simulations are based on Sentaurus TCAD [26]. The Sentaurus Structure Editor is used for structure and mesh construction. The Sentaurus Device is used for device simulations and mixed-mode circuit simulations. The mesh of the structures contains four parts: an overall mesh for the whole device structure with lateral/vertical mesh sizes of $0.4/0.5 \text{ }\mu\text{m}$; a refined mesh with much smaller lateral/vertical mesh sizes ($0.1/0.2 \text{ }\mu\text{m}$) is placed at the top $2\text{-}\mu\text{m}$ region; a further refined mesh with a size of $0.01 \text{ }\mu\text{m}$ is placed around the PN junctions; the oxide/silicon interface is refined with a mesh size of $0.002 \text{ }\mu\text{m}$ along the direction perpendicular to the interface. In the Sentaurus Device simulations, the electron/hole continuity equations and Poisson equations are solved self-consistently. The mixed-mode circuit simulations are carried out with the circuit equations solved in the same manner as traditional SPICE tools. Shockley-Reed-Hall and Auger combination, impact ionization (Okuto model), doping-dependent transport, high-field saturation effects, band narrowing, are all considered.

2. Device Structure and R_{SP} - BV Trade-Off

Figure 1 plots the schematic cross-sectional structures of the conventional power MOSFET, the SJ-MOSFET, and the proposed MOSFET. The proposed MOSFET has a deep trench between neighboring p-bodies. Multiple p-islands are located at the sidewall and bottom of the trenches. The number of p-islands was designed according to the requirement of BV . In this study, 5 p-islands were adopted. The doping concentration of the p-islands is $2.5 \times 10^{18} \text{ cm}^{-3}$. The distance between adjacent p-islands is $6.6 \text{ }\mu\text{m}$. The deep trench is filled with an insulator (silicon oxide is used in this paper). All the studied MOSFETs include a $1\text{-}\mu\text{m}$ -wide gate in one cell pitch. The gate oxide thickness is 80 nm . The channel length is $0.7 \text{ }\mu\text{m}$. The n/p-pillars in SJ-MOSFET have a doping concentration of $4 \times 10^{15} \text{ cm}^{-3}$, and a thickness of $42 \text{ }\mu\text{m}$. The key device parameters of the studied MOSFETs are listed in Table 1.

Figure 1. Schematic cross-sectional structures of (a) conventional power MOSFET (metal-oxide-semiconductor field-effect transistors), (b) SJ-MOSFET, and (c) proposed MOSFET featuring deep trench and p-islands.

Table 1. Key parameters of the studied MOSFETs.

	Parameters	Value	Unit
Conventional MOSFET	doping of n-drift	3.8×10^{14}	cm^{-3}
	thickness of n-drift	42	μm
	cell pitch	3	μm
Superjunction MOSFET	doping of n/p-pillar	4×10^{15}	cm^{-3}
	thickness of n/p-pillar	28	μm
	pitch of n/p-pillar	3	μm
Proposed MOSFET	doping of n-drift	4×10^{15}	cm^{-3}
	thickness of n-drift	42	μm
	pitch of n-drift	3	μm
	pitch of trench oxide	3	μm

To understand the mechanism for the proposed MOSFET to break the 1D-limit, the two-dimensional electrostatic potential contours of the studied MOSFETs are plotted in Figure 2, and the electric field along the depth of the devices are plotted in Figure 3. The devices are in off-state under $V_{DS} = 500$ V. For the conventional power MOSFET, the electrostatic potential lines are crowded around p-body/n-drift junction, and the distance between adjacent equal-potential lines is gradually increasing towards the lower side of the drift region. From Figure 3, the electric field in the conventional power MOSFET has a triangle shape, peaking near the top of the device. When the electric field peak reaches the critical breakdown field, the breakdown voltage is the integration of the triangle-shaped electric field distribution along the depth.

For the SJ-MOSFET, the p/n pillars are fully depleted laterally with a low off-state voltage, even though the doping concentration in the p/n pillars of SJ-MOSFET are much higher than conventional power MOSFET. At higher off-state voltage, the fully depleted p/n pillars behave like dielectrics. From Figure 2, the equal-potential lines in the SJ-MOSFET at $V_{DS} = 500$ V are more evenly distributed along the depth compared to conventional power MOSFET. The electric field in the SJ-MOSFET has a rectangle shape; thus, for the same BV , the SJ-MOSFET can have a much thinner drift region. The thinner and more heavily doped n-pillar significantly reduces the R_{SP} of the SJ-MOSFET.

Figure 2. Electrostatic potential contour under $V_{DS} = 500$ V in off-state: (a) conventional MOSFET, (b) SJ-MOSFET, and (c) the proposed MOSFET.

Figure 3. Electric field along the depth of the studied MOSFETs at $V_{DS} = 500$ V in off-state.

In the proposed MOSFET, the n-drift region is heavily doped for a reduced R_{SP} , which leads to a quick rise of the electric field peak. To obtain a higher BV , the proposed MOSFET uses multiple p-islands at the sidewall of the trench. The equal-potential lines of the proposed MOSFET, shown in Figure 2c, are crowded at not only the p-body/n-drift junction but also every p-island/n-drift junction. Hence, the electric field in the proposed MOSFET has multiple peaks. The proposed MOSFET was designed by first assuming that there is no p-island. When a drain voltage V_{DS} is applied, a depletion region is formed in the drift region until breakdown occurs at $V_{DS} = BV_0$. At BV_0 , if the width of the

depletion region is W_0 , the distance between the p-body and the 1st p-island is slightly smaller than W_0 to allow some design margin. Therefore, the 1st p-island starts to support the off-state voltage before the p-body/n junction sees the critical breakdown field. Following the same manner, the second p-island, third p-island, etc. are designed until the required blocking voltage is obtained. In the design of the p-islands, the p-island should be located within the previous p-island's depletion region by a certain margin to allow some process variation. If the p-island is placed out of the previous p-island's depletion region, the electric field around the previous p-island will reach the critical breakdown field before the next p-island starts to clamp the voltage. These voltage clamping effects of the p-islands are similar to those in the floating field rings widely adopted for the edge termination of power devices [27,28]. Figure 4 shows the potential of the p-islands in the proposed MOSFET as a function of the off-state drain voltage.

Figure 4. The voltage of the 1st to 5th p-island from top to bottom in the proposed MOSFET vs. V_{DS} in off-state.

Unlike traditional MOSFET, which reduces the doping concentration when a higher BV is required, the proposed MOSFET structure uses a high doping concentration even for increased BV . According to the above analysis, to increase the BV of the proposed MOSFET, the doping concentration of the n-drift region can be kept unchanged, and the thickness of the n-drift region roughly scales with BV . The proposed MOSFET roughly follows $R_{SP} \propto BV$ as contrasted by $R_{SP} \propto BV^{2.5}$ for the conventional power MOSFET. Thus, the R_{SP} of the proposed MOSFET rises much slower as BV increases. Figure 5 benchmarks R_{SP} and BV for the conventional power MOSFET, the SJ-MOSFET, and the proposed MOSFET. The proposed MOSFETs with a different number of p-islands are benchmarked. Both the SJ-MOSFET and the proposed MOSFET achieve a R_{SP} - BV trade-off beyond the so-called 1D-limit. In this paper, the MOSFETs with $BV = \sim 550$ V were chosen for detailed study.

The output characteristics of the studied MOSFETs are plotted in Figure 6. All the three MOSFETs present the same BV of ~ 550 V. In on-state with $V_{GS} = 10$ V, and the conventional MOSFET has a high R_{SP} of $49.80 \text{ m}\Omega\cdot\text{cm}^2$. The SJ-MOSFET has a small R_{SP} of $8.52 \text{ m}\Omega\cdot\text{cm}^2$ owing to the high doping concentration and short pillars compared to the n-drift region of the conventional power MOSFET. The proposed MOSFET features the same high doping concentration for the n-drift compared to the n-pillar in the SJ-MOSFET. The thickness of the n-drift region of the proposed MOSFET is the same as that of the conventional MOSFET, but thicker compared to the n-pillar in SJ-MOSFET. Thus, the proposed MOSFET has a much lower R_{SP} ($12.74 \text{ m}\Omega\cdot\text{cm}^2$) than the conventional MOSFET, although slightly higher than the SJ-MOSFET.

Figure 5. Relationship between R_{SP} and BV of the MOSFETs and the 1D “silicon limit.”

Figure 6. I - V characteristics of the studied MOSFETs.

3. Body Diode Characteristics

Figure 7 shows the reverse conduction characteristics of the studied MOSFETs under $V_{GS} = 0$ V. The reverse conduction takes place through the internal parasitic PN junction. The reverse conduction voltage ($V_{RC} = |V_{DS}|$ at $I_D = -100$ A/cm²) of the conventional power MOSFET is 0.79 V, and that for the SJ-MOSFET is 0.78 V. The V_{RC} of the proposed MOSFET (0.85 V) is slightly higher than the other two MOSFETs since a portion of its device area is taken by the trench, which does not contribute to the reverse conduction. In a practical application with an optimized dead time design, the influence of this slightly higher V_{RC} is limited.

Figure 8 plots the minority carrier density along the depth of the studied MOSFETs at the reverse conduction current of 100 A/cm². All the studied MOSFETs have a similar level of minority carrier density.

In modern power switching applications, the reverse recovery performance of the power MOSFETs is of crucial importance [13,29–31]. During reverse conduction, a large amount of minority carriers is injected into the drift region of the MOSFETs. Before the power MOSFETs are switched to sustain the forward off-state voltage, the polarity of the voltage across the device is reversed, and the devices experience the reverse recovery process. During this process, the minority carriers have to be removed from the drift region so that the device can be able to block the forward off-state voltage.

The reverse recovery performance of the MOSFETs was studied using the testing circuit in Figure 9a. The supply voltage is 400 V, and a load current of 100 A is adopted. The device-under-test (DUT) is at the high-side of the circuit. A conventional MOSFET is employed as the switch in the circuit for all reverse recovery tests. Both the DUT and the switch have an area of 1 cm².

Figure 7. The reverse conduction characteristics of the studied MOSFETs.

Figure 8. Hole density along the depth of the studied MOSFETs at $I_D = -100 \text{ A/cm}^2$.

Figure 9b illustrates a typical reverse recovery behavior of a power MOSFET. The reverse recovery charge (Q_{RR}) is the integration of the reverse recovery current. The reverse recovery in the DUT causes an appreciable switching loss not in the DUT itself, but in the low-side power transistor. The reverse recovery current of the DUT adds up with the load current during the switching transient, leading to an increase of the switching current in the low-side transistor, which consequently causes an increase of power loss. The reverse recovery charge (Q_{RR}) of the DUT is an integration of its reverse recovery current over the switching time duration and is a critical parameter to evaluate the power MOSFET [13]. The softness of the reverse recovery process is defined by $S = t_f/t_s$, where the t_f and t_s are illustrated in Figure 9b. The softness of the reverse recovery process is also of crucial importance. A snappy reverse recovery (i.e., a reverse recovery with very small S , marked by a sharp falling of current after the peak reverse recovery current) causes a very sharp change of current in the power loop of the circuit, which is very like to induce voltage spikes and oscillations due to the existence of parasitic inductances in the circuit. Therefore, a relatively softer reverse recovery (with larger S) is usually desired [13,32].

Figure 9c plots the reverse recovery performances of the studied MOSFETs. The reverse recovery charge Q_{RR} of the conventional power MOSFET is $14.3 \mu\text{C/cm}^2$, with a softness of 0.57. The SJ-MOSFET has a smaller Q_{RR} of $9.85 \mu\text{C/cm}^2$ owing to the thinner drift region. However, the softness of the SJ-MOSFET is as low as 0.07. Such a snappy reverse recovery is caused by the large aspect PN junction area in the SJ-MOSFET; the large-area PN junction extracts the minority carriers through the whole depth of the drift region. When all the minority carriers are quickly removed, the reverse recovery

current falls abruptly. The snappy reverse recovery is deleterious for the system reliability and prevents the SJ-MOSFET technology to be adopted in many power switching applications. The proposed MOSFET has a Q_{RR} of $8.88 \mu\text{C}/\text{cm}^2$. Q_{RR} of the proposed MOSFET is smaller than the conventional power MOSFET, although they have a similar level of minority carrier density because a portion of the active area of the proposed MOSFET is consumed by the trench that does not store minority carriers. The softness of the proposed MOSFET is 0.90, larger than both the SJ-MOSFET and the conventional power MOSFET.

Figure 9. (a) Test circuit configuration for the reverse recovery characteristics. (b) Schematic of reverse recovery waveforms. (c) Reverse recovery characteristics of the studied MOSFETs.

The main performances of the studied MOSFETs are listed in Table 2 for a comparison. Both the SJ-MOSFET and the proposed MOSFET can obtain a beyond-1D-limit R_{SP} - BV trade-off. However, the superior reverse recovery performance of the proposed MOSFET makes it a preferable candidate for power switching applications where hard commutation is required [30,33].

Table 2. Comparison of the device characteristics.

	Conv.	SJ.	Proposed	Unit
R_{SP}	49.80	8.52	12.74	$\text{m}\Omega \cdot \text{cm}^2$
BV	550	550	550	V
V_{RC}^a	0.79	0.78	0.85	V
t_{RR}	116	80	114	ns
t_s	74	75	60	ns
t_f	42	5	54	ns
$S(t_f/t_s)$	0.57	0.07	0.90	-
Q_{RR}	14.30	9.85	8.88	$\mu\text{C}/\text{cm}^2$
I_{RRM}	177	216	114	A/cm^2

^a $V_{RC} = |V_{DS}|$ at $I_D = -100 \text{ A}/\text{cm}^2$.

4. Proposed Process Flow

The proposed MOSFET can be realized using a similar approach as a conventional power MOSFET. The key difference between the proposed MOSFET and the conventional power MOSFET is the trench and the p-islands. Figure 10 presents a proposed fabrication approach for the new device structure. In Figure 10a, with a patterned hard mask (e.g., silicon oxide), the epitaxial n-drift layer is dry-etched for a designed depth. The deep trench can be formed using the deep reactive ion etching (DRIE) technology, which is widely used in MEMS, memory, and power devices. The DRIE process consists of multiple cycles of dry etching and passivation. The passivation layer suppresses the lateral etching of the silicon material and helps to form fine vertical trenches [34–38]. A p-type ion implantation is performed, which creates a p-type region under the trench with a certain lateral spread. Then, in Figure 10b, the above etch and implantation processes are repeated to form the second p-island. In Figure 10c, the above processes are repeated multiple times to obtain the targeted number of p-islands. At last, thermal annealing will be performed to further enhance the lateral spread of the dopants. In Figure 10d, the trench is filled with oxide, and the surface is planarized. In Figure 10e, the surface implantations are carried out to form the p-body and n+ source region. Finally, in Figure 10f, the gate structure and metallization are implemented. According to the proposed process, the new structure can be realized using mature silicon fabrication technology.

Figure 10. Proposed process flow for the MOSFET featuring trench oxide and p-islands: (a) patterned silicon oxide and the topmost p-island formation by etching and ion-implantation; (b) second topmost p-island definition in the same manner; (c) the other p-islands formation by repeated etching and ion-implantation, and a thermal process to activate the dopants and further enhance the lateral spread of the dopants; (d) trench oxide growth and etching back; (e) p-body, p+-source, n+-source as well as (f) trench gate and contact formation in the same manner as the conventional trench MOSFET.

5. Conclusions

The performance of the conventional power MOSFET is limited by the R_{SP} - BV trade-off relationship: $R_{SP} \propto BV^{2.5}$, which is also known as the 1D-silicon-limit. The SJ-MOSFET breaks the 1D-limit but suffers a snappy reverse recovery that limits its application in many applications, where hard commutation is required. In this work, a new power MOSFET architecture is proposed, which simultaneously offers a beyond-1D-limit R_{SP} - BV trade-off and a superior reverse recovery performance. The proposed MOSFET has a much higher doping concentration compared to the conventional power MOSFET, which reduces the R_{SP} . A high breakdown voltage is obtained in the proposed MOSFET by splitting the single electric field peak into multiple peaks using multiple p-islands along a deep trench. The snappy reverse recovery inherent to SJ-MOSFET is avoided in the newly proposed MOSFET. Therefore, the proposed MOSFET can be used in various power switching applications where hard commutation is required.

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References

- Chen, X.; Sin, J.K.O. Optimization of the specific on-resistance of the COOLMOS. *IEEE Trans. Electron Devices* **2001**, *48*, 344–348. [\[CrossRef\]](#)
- Baliga, B.J. *Fundamentals of Power Semiconductor Device*; Springer: New York, NY, USA, 2008.
- Williams, R.K.; Darwish, M.N.; Blanchard, R.A.; Siemienieć, R.; Rutter, P.; Kawaguchi, Y. The trench power MOSFET: Part I-history, technology, and prospects. *IEEE Trans. Electron Devices* **2017**, *64*, 674–691. [\[CrossRef\]](#)
- Udrea, F.; Deboy, G.; Fujihira, T. Superjunction power devices, history, development, and future prospects. *IEEE Trans. Electron Devices* **2017**, *64*, 713–727. [\[CrossRef\]](#)
- Cao, Z.; Duan, B.; Shi, T.; Yuan, S.; Yang, Y. A superjunction U-MOSFET with SIPOS pillar breaking superjunction silicon limit by TCAD simulation study. *IEEE Electron Device Lett.* **2017**, *38*, 794–797. [\[CrossRef\]](#)
- Park, J.; Lee, J. A 650 V super-junction MOSFET with novel hexagonal structure for superior static performance and high BV resilience to charge imbalance: A TCAD simulation study. *IEEE Electron Device Lett.* **2017**, *38*, 111–114. [\[CrossRef\]](#)
- Zhang, W.; Zhang, B.; Qiao, M.; Li, Z.; Luo, X.; Li, Z. Optimization and new structure of superjunction with isolator layer. *IEEE Trans. Electron Devices* **2017**, *64*, 217–223. [\[CrossRef\]](#)
- Shirota, S.; Kaneda, S. New type of varactor diode consisting of multilayer p-n junctions. *J. Appl. Phys.* **1978**, *49*, 6012–6019. [\[CrossRef\]](#)
- Deboy, G.; Marz, M.; Stengl, J.P.; Strack, H.; Tihanyi, J.; Weber, H. A new generation of high voltage MOSFETs breaks the limit line of silicon. In Proceedings of the 1998 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 6–9 December 1998; pp. 683–685.
- Chen, X. Semiconductor Power Devices with Alternating Conductivity Type High-Voltage Breakdown Regions. U.S. Patent 5216675, 1 June 1993.
- Coe, D.J. High Voltage Semiconductor Devices. U.S. Patent 4754310, 1 June 1988.
- Deboy, G.; Treu, M.; Haeberlen, O.; Neumayr, D. Si, SiC and GaN power devices: An unbiased view on key performance indicators. In Proceedings of the 2016 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 3–7 December 2016; pp. 532–535.
- Linder, S. *Power Electronics*; EPFL Press: Lausanne, Switzerland, 2006.

14. Zhang, J.; Lai, J.S. A synchronous rectification featured soft switching inverter using CoolMOS. In Proceedings of the 2006 IEEE Applied Power Electronics Conference and Exposition, Dallas, TX, USA, 19–23 March 2006; pp. 810–815.
15. Conrad, M.; Deconcker, R.W. Avoiding reverse recovery effects in super junction MOSFET based half-bridges. In Proceedings of the 2015 IEEE International Symposium on Power Electronics for Distributed Generation Systems, Aachen, Germany, 22–25 June 2015; pp. 1–5.
16. Schmitt, M.; Schulze, H.J.; Schlogl, A.; Vosseburger, M.; Willmeroth, A.; Deboy, G. A comparison of electron, proton and helium ion irradiation for the optimization of the CoolMOS™ body-diode. In Proceedings of the 2002 IEEE International Symposium on Power Semiconductor Devices and ICs, Sante Fe, NM, USA, 7 June 2002; pp. 229–232.
17. Saito, W.; Ono, S.; Yamashita, H. Influence of carrier lifetime control process in superjunction MOSFET characteristics. In Proceedings of the 2014 IEEE International Symposium on Power Semiconductor Devices and ICs, Waikoloa, HI, USA, 15–19 June 2014; pp. 87–90.
18. Lin, Z.; Hu, S.; Yuan, Q.; Zhou, X.; Tang, F. Low-reverse recovery charge superjunction MOSFET with a p-type Schottky body diode. *IEEE Electron Device Lett.* **2017**, *4*, 176–178. [[CrossRef](#)]
19. Cheng, X.; Liu, X.M.; Sin, J.K.O.; Kang, B.W. Improving the CoolMOSTM body-diode switching performance with integrated Schottky contacts. In Proceedings of the 2003 IEEE International Symposium on Power Semiconductor Devices and ICs, Cambridge, UK, 14–17 April 2003; pp. 304–307.
20. Wei, J.; Zhang, M.; Jiang, H.; Zhou, X.; Li, B.; Chen, K.J. Superjunction MOSFET with dual built-in schottky diodes for fast reverse recovery: A numerical simulation study. *IEEE Electron Device Lett.* **2019**, *40*, 1155–1158. [[CrossRef](#)]
21. DeWitt, D.B.; Brown, C.D.; Robertson, S.M. System and Method for Reducing Body Diode Conduction. U.S. Patent 7508175, 24 March 2009.
22. DeWitt, D.; Brown, C.; Robertson, S. The pinch-off circuit: Reducing noise and component stresses by eliminating body diode conduction in synchronous rectifiers. In Proceedings of the 2007 IEEE Applied Power Electronics Conference and Exposition, Anaheim, CA, USA, 25 February–1 March 2007; pp. 1531–1536.
23. Xue, P.; Maresca, L.; Riccio, M.; Breglio, G.; Irace, A. Investigation on the self-sustained oscillation of superjunction MOSFET intrinsic diode. *IEEE Trans. Electron Devices* **2019**, *66*, 605–612. [[CrossRef](#)]
24. Zhang, M.; Wei, J.; Zhou, X.; Jiang, H.; Li, B.; Chen, K.J. Simulation study of a power MOSFET with built-in channel diode for enhanced reverse recovery performance. *IEEE Electron Device Lett.* **2019**, *1*, 79–82. [[CrossRef](#)]
25. Uchida, M.; Horikawa, N.; Tanaka, K.; Takahashi, K.; Kiyosawa, T.; Hayashi, M. Novel SiC power MOSFET with integrated unipolar internal inverse MOS-channel diode. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011; pp. 602–605.
26. *TCAD Sentaurus Device Manual*; Synopsys Inc.: Mountain View, CA, USA, 2013.
27. Cheng, X.; Sin, J.K.O.; Shen, J.; Huai, Y.; Li, R.; Wu, Y.; Kang, B. A general design methodology for the optimal multiple-field-limiting-ring structure using device simulator. *IEEE Trans. Electron Devices* **2003**, *50*, 2273–2279. [[CrossRef](#)]
28. Brieger, K.P.; Gerlach, W.; Pelka, J. Blocking capability of planar devices with field limiting rings. *Solid-State Electron.* **1983**, *26*, 739–745. [[CrossRef](#)]
29. Ren, Y.; Xu, M.; Zhou, J.; Lee, F.C. Analytical loss model of power MOSFET. *IEEE Trans. Power Electron.* **2006**, *21*, 310–319.
30. Huang, A. Hard Commutation of Power MOSFET. Infineon, Nuebiberg, Germany, Tech. Rep. 2014-03. Available online: https://www.infineon.com/dgdl/Infineon-Power_MOSFET_OptiMOS_FD_200V-250V_hard_diode_commutation-AN-v01_00-EN.pdf?fileId=db3a304344ae06150144b1d2f8250165 (accessed on 12 March 2014).
31. Yang, B.; Xu, S.; Korec, J.; Wang, J.; Lopez, O.; Jauregui, D.; Kocon, C.; Herbsommer, J.; Molloy, S.; Daum, G.; et al. NexFET generation 2, new way to power. In Proceedings of the 2011 International Electron Devices Meeting, Washington, DC, USA, 5–7 December 2011; pp. 583–586.
32. Jiang, H.; Wei, J.; Zhang, B.; Chen, W.; Qiao, M.; Li, Z. Band-to-band tunneling injection insulated-gate bipolar transistor with a soft reverse-recovery built-in diode. *IEEE Electron. Device Lett.* **2012**, *33*, 1684–1686. [[CrossRef](#)]

33. Haaf, P. Understanding diode reverse recovery and its effect on switching losses. *Fairchild Power Semin.* **2007**, 23–33. [[CrossRef](#)]
34. Noblecourt, S.; Tasselli, J.; Morancho, F.; Isoird, K.; Austin, P. Design and realization of deep trench superJunction diode for 600V applications. *Eur. J. Electr. Eng.* **2014**, *17*, 345–361. [[CrossRef](#)]
35. Park, W.J.; Kim, J.H.; Cho, S.M.; Yoon, S.G.; Suh, S.J.; Yoon, D.H. High aspect ratio via etching conditions for deep trench of silicon. *Surface Coat. Technol.* **2003**, *171*, 290–295. [[CrossRef](#)]
36. Yamauchi, S.; Shibata, T.; Nogami, S.; Yamaoka, T.; Hattori, Y.; Yamaguchi, H. 200V super junction MOSFET fabricated by high aspect ratio trench filling. In Proceedings of the 2006 IEEE International Symposium on Power Semiconductor Devices and ICs, Naples, Italy, 4–8 June 2006; pp. 1–4.
37. Moens, P.; Bogman, F.; Ziad, H.; De Vleeschouwer, H.; Baele, J.; Tack, M.; Loechelt, G.; Grivna, G.; Parsey, J.; Wu, Y.; et al. UltiMOS: A local charge-balanced trench-based 600V super-junction device. In Proceedings of the 2011 IEEE International Symposium on Power Semiconductor Devices and ICs, San Diego, CA, USA, 23–26 May 2011; pp. 304–307.
38. Tilli, M.; Motooka, T.; Airaksinen, V.; Franssila, S.; Paulasto-Kröckel, M.; Lindroos, V. *Handbook of Silicon Based MEMS Materials and Technologies*; William Andrew Publishing: Norwich, NY, USA, 2015.

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