

Article

InGaAs FinFETs Directly Integrated on Silicon by Selective Growth in Oxide Cavities

Clarissa Convertino , Cezar Zota, Heinz Schmid *, Daniele Caimi, Marilyne Sousa, Kirsten Moselund and Lukas Czornomaz

IBM Research GmbH Zürich, Säumerstrasse 4, CH-8803 Rüschlikon, Switzerland; zot@zurich.ibm.com (C.Z.); cai@zurich.ibm.com (D.C.); sou@zurich.ibm.com (M.S.); kmo@zurich.ibm.com (K.M.); luk@zurich.ibm.com (L.C.)

* Correspondence: ino@zurich.ibm.com (C.C.); sih@zurich.ibm.com (H.S.)

Received: 30 November 2018; Accepted: 22 December 2018; Published: 27 December 2018



Abstract: III-V semiconductors are being considered as promising candidates to replace silicon channel for low-power logic and RF applications in advanced technology nodes. InGaAs is particularly suitable as the channel material in n-type metal-oxide-semiconductor field-effect transistors (MOSFETs), due to its high electron mobility. In the present work, we report on InGaAs FinFETs monolithically integrated on silicon substrates. The InGaAs channels are created by metal-organic chemical vapor deposition (MOCVD) epitaxial growth within oxide cavities, a technique referred to as template-assisted selective epitaxy (TASE), which allows for the local integration of different III-V semiconductors on silicon. FinFETs with a gate length down to 20 nm are fabricated based on a CMOS-compatible replacement-metal-gate process flow. This includes self-aligned source-drain n⁺ InGaAs regrown contacts as well as 4 nm source-drain spacers for gate-contacts isolation. The InGaAs material was examined by scanning transmission electron microscopy (STEM) and the epitaxial structures showed good crystal quality. Furthermore, we demonstrate a controlled InGaAs digital etching process to create doped extensions underneath the source-drain spacer regions. We report a device with gate length of 90 nm and fin width of 40 nm showing on-current of 100 $\mu\text{A}/\mu\text{m}$ and subthreshold slope of about 85 mV/dec.

Keywords: III-V; TASE; MOSFETs; Integration

1. Introduction

Compound semiconductors based on arsenides ($\text{In}_{1-x}\text{Ga}_x\text{As}$) [1] are considered promising candidates to replace silicon in nFETs for advanced and ultra-scaled CMOS technology nodes. These materials offer a significant advantage in terms of electron mobility compared to silicon and are suitable for low-power applications [2–5]. Nevertheless, to enable large-scale and cost-effective integration, the challenge of transferring high quality III-V material on silicon must be overcome. Recently, different strategies for III-V on silicon integration have been proposed. Strain-relaxed buffer layer growth and direct wafer bonding (DWB) [6,7], can enable large-area III-V-on-insulator substrates, as well as 3D heterogeneous integration on processed substrates [8]. Selective epitaxial techniques make possible, instead, local integration of III-V crystals in pre-defined regions [9,10]. This approach can potentially reduce the costs associated with III-V substrates and simplify the integration process. Defect density can be engineered by tuning multiple aspects such as cavity geometry, nucleation seed or growth direction. Aspect-ratio trapping (ART) technique [11,12], for instance, aims to filter crystals defects propagating along (111) planes but lacking in defects confinement along the trench direction. We have previously developed an integration approach called template-assisted selective epitaxy (TASE) [13–15], based on the growth of different III-V materials within arbitrarily shaped oxide

cavities. This technique has been employed to demonstrate various devices such as tunnel FETs [16,17] ballistic nanowires [18] as well as optically active devices [19].

In this work we demonstrate InGaAs n-FinFETs integrated on a silicon (100) substrate. Due to the presence of a buried oxide layer (BOX), our InGaAs-on-insulator devices share the benefits as SOI technologies. Furthermore, we implement here a replacement-metal-gate process (RMG) on selectively grown structures with a CMOS compatible III-V process. The fabrication flow includes n-doped InGaAs contacts regrowth as well as SiN_x spacers. Source-drain doped extensions are obtained by digital etching of the InGaAs channel and regrowth, in order to mitigate the access resistance increase introduced by the presence of spacers. InGaAs material quality is investigated through STEM analysis (JEOL ARM-200F, Tokyo, Japan). Electrical characteristic of FinFETs devices at two different gate length is shown, as well as the effect of scaling on the transistor subthreshold operation.

2. Materials and Methods

The InGaAs devices are fabricated by TASE. First, a SiO₂ thermal oxide layer 50 nm thick is deposited on a silicon wafer (Figure 1a). Seed-area openings, with a diameter of 50 nm, are patterned on the oxide layer by e-beam lithography using PMMA resist (Figure 1b). A sacrificial layer 30 nm thick is then deposited on top of the BOX. Thickness and morphology of this layer will define the features of the final grown semiconductor structure. Next, the sacrificial material is patterned by e-beam lithography and the structures to be transferred into III-V are dry etched (Figure 1c). A second oxide layer, 100 nm thick, referred to as the oxide template, is deposited above the patterned structures. Afterward, openings are patterned by e-beam lithography using PMMA resist and vias are dry etched down to the sacrificial material layer (Figure 1d). The latter is therefore selectively etched, exposing the silicon seed that was previously formed (Figure 1e). Thus, the as-formed cavities contain a small seed opening to the silicon substrate. The nucleation point is perpendicular to the growth direction (Figure 1f), enabling efficient defect filtering in multiple directions [15]. A short dip in diluted HF is performed to remove the native oxide formed on the Si seed. The sample is then immediately loaded into a metal–organic–chemical–vapor–deposition (MOCVD) reactor and In_{0.53}Ga_{0.47}As is grown into the patterned structures. Trimethylgallium (TMGa), trimethylindium (TMIn) and tertiarybutylarsine (TBAs) are used as precursors for the InGaAs growth, performed at 550 °C. The growth is geometrically confined into the formed template cavities. Afterwards, the template is removed by a combination of dry reactive ion etching (RIE) and HF wet etching. The replacement-metal-gate (RMG) process starts with the deposition and patterning of a dummy gate (Figure 2a). 3 nm Al₂O₃ (working as etch-stop layer) and 150 nm amorphous silicon are deposited and patterned by using HSQ resist. The smallest physical gate length measured is 20 nm. The amorphous silicon is dry etched by inductively-coupled-plasma (ICP) RIE with an optimized process for vertical sidewalls. The silicon etching stops on the Al₂O₃ layer. Next, 4 nm thick SiN_x spacers are deposited and dry etched by RIE. The Al₂O₃ on the InGaAs areas not covered by the dummy gate is then removed by wet etching in HF solution. As schematized in Figure 2c, the InGaAs channel is recessed underneath the sidewall spacers. This is achieved by several cycles of III-V digital etching (DE). The cycle consists in placing the sample in ozone atmosphere for 8 min and subsequently removing the as-formed III-V oxide in an HCl dilution with de-ionized water (1:10) for 15 s. The estimated etch rate per DE cycle is about 1.5 nm. Following, the sample is immediately loaded in the MOCVD reactor to perform raised-source-drain (RSD) epitaxy of n-doped In_{0.53}Ga_{0.47}As. The dopant used is Sn and the estimated doping level is $1 \times 10^{19} \text{ cm}^{-3}$. A SEM (Hitachi SU8000, Tokyo, Japan) micrograph of the InGaAs device after RSD epitaxy is shown in Figure 2d. RSD epitaxy is followed by an inter-layer dielectric deposition (250 nm of SiO₂) that is subsequently planarized by chemical mechanical polishing (CMP). The oxide planarization allows to expose the top part of the dummy gate that is then removed by a selective XeF₂-based etch. The dummy high-k oxide is hence removed by HF etching and the sample is immediately loaded in the ALD chamber for the gate-stack deposition. The gate-stack consists of 5 nm Al₂O₃/HfO₂ bilayer high-k dielectric and TiN metal-gate. Right after, 150 nm of W are sputtered

and planarized by CMP. A second ILD (Interlayer dielectric) layer (50 nm of SiO₂) is deposited and vias down to source/drain/metal are opened and filled with tungsten. Metal pads are patterned with negative e-beam resist and dry etched with RIE. Prior to measuring the devices, a forming gas anneal (FGA) at 300 °C is performed.

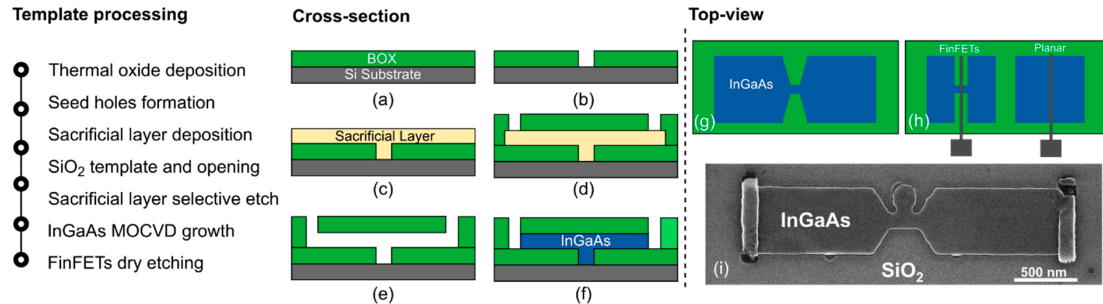


Figure 1. Overview of the fabrication process. (left) process flow up to the InGaAs fin formation. Cross-section schematic of (a) thermal oxide formation on silicon substrate, (b) patterning and opening of seed area in the oxide layer, (c) sacrificial layer deposition, (d) oxide template deposition and patterning of opening areas, (e) selective removal of sacrificial material, (f) III-V MOCVD growth. Top-view schematic of (g) as-grown InGaAs structure after SiO₂ template strip and (h) planar and FinFETs structures after dry etching. (i) SEM top-view image of grown InGaAs structure from a seed positioned off-center.

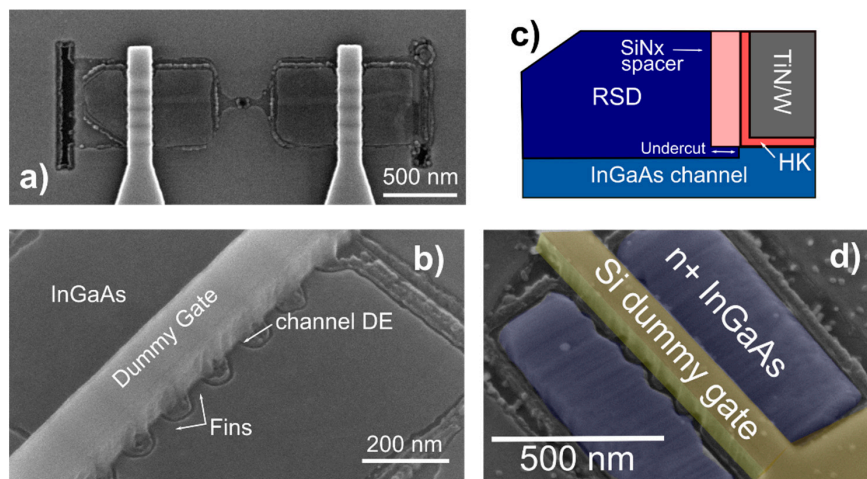


Figure 2. Device fabrication steps. (a) Top-view SEM image of InGaAs FinFET device after dummy gate patterning and dry etch. Fins are visible underneath the gate. (b) SEM picture showing InGaAs fins after digital etching (DE). The channel recess underneath the dummy gate is performed to allow for doped extensions regrowth. This is schematized in (c) with a cross-section drawing zooming on the channel/RSD interface. (d) InGaAs transistor SEM top-view after MOCVD RSD growth.

3. Results and Discussion

A schematic of the device cross-section is shown in Figure 3a with the corresponding STEM cross-sections of the finished device shown in Figure 3b and a magnified view of the spacer/RSD/channel corner (Figure 3c). The RSD and channel interface are clearly distinguishable. This is possibly due to an undesired drift in indium content between the two growth runs. The presence of planar stacking faults along a (111) plane are visible as well, originating from the growth process. Extensive study of growth dynamic and defects in InGaAs structures grown by TASE can be found in [20]. Electrical I_{DS} - V_G characteristics of 90 nm and 150 nm gate length devices as measured after FGA are shown in Figure 4. The shorter gate length (L_G) device with fin width of $W_{FIN} = 40$ nm, exhibits 85 mV/dec and 95 mV/dec subthreshold slopes (SS) at $V_{DS} = 0.05$ V and $V_{DS} = 0.5$ V, respectively.

SS is overall improved compared to devices reported in [15], where a SS of 190 mV/dec is achieved for $L_G = 100$ nm and $W_{FIN} = 50$ nm. The same device shows a transconductance peak value in saturation of $350 \mu\text{S}/\mu\text{m}$ and a maximum transconductance efficiency around 20 V^{-1} at 0.3 V. The R_{ON} of this device, measured from the output characteristics, is about $1 \text{ k}\Omega \cdot \mu\text{m}$. Compared to our previously reported InGaAs FinFETs [15] fabricated using a similar scheme, we achieved significant improvement in off-state performance as well as better $I_{ON}/I_{OFF} = 10^4$. This can be attributed to the presence of extended source-drain RSD contacts reaching underneath the spacer region, limiting the access resistance increase introduced by ungated channel area. The short L_G device shows an $I_{ON} = 100 \mu\text{A}/\mu\text{m}$, at fixed $I_{OFF} = 100 \text{ nA}/\mu\text{m}$ at $V_{DS} = 0.5 \text{ V}$ (Figure 4a) and a V_{GS} voltage swing of 0.5 V, which is the intended bias point for III-V MOSFETs. The two reported L_G , with a comparable slope, illustrate the positive impact of scaling on the on-state performance. The transfer characteristic of a planar device is shown in Figure 4b. For the same L_G , planar devices show higher SS due to degraded electrostatic control, and lower maximum on-current due to smaller normalized gate width compared to FinFET devices. Figure 5a, shows average SS values versus L_G for FinFETs with $W_{FIN} = 40$ nm. For L_G smaller than 40 nm, both linear and saturation SS increase substantially, due to short-channel effects. In Figure 5b, SS versus W_{FIN} for fixed L_G is plotted, showing that SS will benefit from further fin width scaling, due to improvement of the electrostatic control. The performance improvement achieved in this work compared to previously reported devices [15] are attributed to the use of an RMG scheme instead of a gate-first (GF) one. Here, the high-k/channel interface is less exposed to thermally induced degradation from the high-temperature RSD growth step, resulting in a lower density of interface traps.

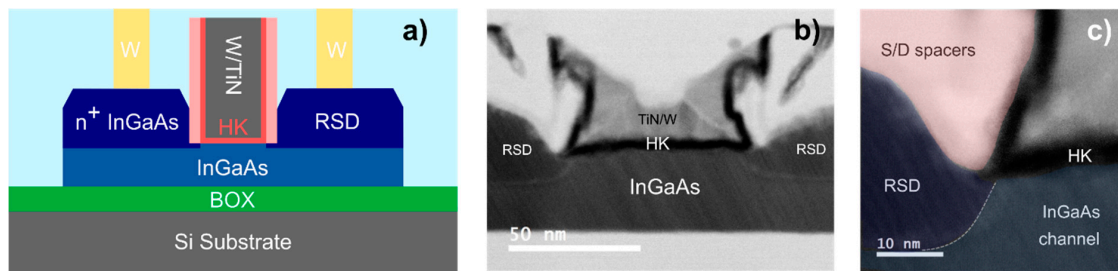


Figure 3. (a) STEM structural analysis. Cross-section schematic of completed InGaAs FET device, after final M1 metallization step. (b) STEM cross-section image for a device with $L_G = 60$ nm. The RSD/channel interface is clearly distinguishable due to difference in indium content between the two. A false-colored zoomed view on the sidewall spacer/HK/RSD/channel interface is shown in (c).

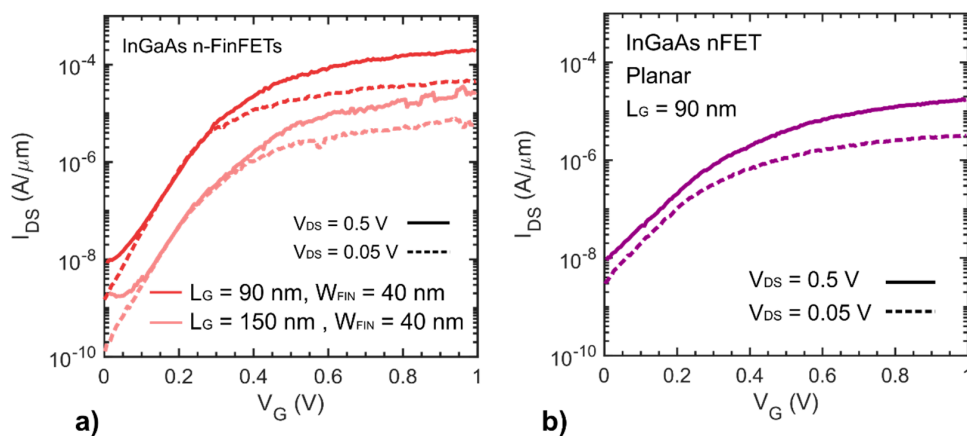


Figure 4. (a) Transfer characteristic of InGaAs FinFET device with $L_G = 90$ nm and $L_G = 150$ nm. Fin width is in both cases 40 nm. The shorter gate length device shows an on-current of $100 \mu\text{A}/\mu\text{m}$ and SS of 85 mV/decade. The gate leakage current (not shown) is at the limit of the measurement equipment, less than 1 pA. (b) Representative transfer characteristic of a planar InGaAs device with $L_G = 90$ nm.

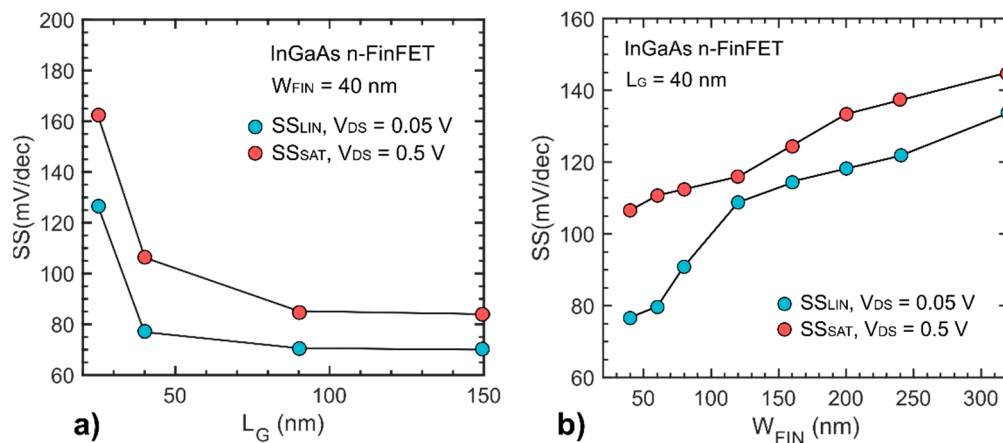


Figure 5. (a) Subthreshold slope values versus gate length for devices with $W_{FIN} = 40$ nm. For L_G smaller than 40 nm, short channel effects start dominating the device behavior. (b) Average SS versus W_{FIN} for devices with $L_G = 40$ nm. The trend indicates that subthreshold performance benefits from further reducing fin width.

4. Conclusions

In this work, we have demonstrated InGaAs n-FinFETs devices using a novel III-V integration technique based on TASE. A full RMG process flow was developed including an improved RDS process with underlapping extensions. Devices with gate length of 90 nm and fin width of 40 nm show on-current of $100 \mu A/\mu m$ and subthreshold slope of about 85 mV/dec, demonstrating good electrostatic control. The strong off-state performance is due to the introduction of source-drain sidewall spacers combined with doped extensions achieved by digital etching. Results indicate that future performance improvements could be achieved by further scaling of gate length and fin width.

Author Contributions: H.S. performed the MOCVD InGaAs growth. C.C., C.Z., D.C., and L.C. fabricated the InGaAs FinFETs devices. C.C. and C.Z. performed the electrical characterization. K.M., H.S., and L.C. initiated the work on InGaAs epitaxy in oxide cavities. M.S. performed the STEM analysis and material characterization. C.C. conducted the electrical data analysis. C.C., with the support of all authors, wrote the manuscript.

Funding: This research was funded by INSIGHT grant number 688784 and REMINDER grant number 687931.

Acknowledgments: The authors want to acknowledge the BRNC staff for technical support.

Conflicts of Interest: The authors declare no conflict of interest.

References

1. Del Alamo, J.A. Nanometre-scale electronics with III–V compound semiconductors. *Nature* **2011**, *479*, 317–323. [[CrossRef](#)] [[PubMed](#)]
2. Hahn, H.; Deshpande, V.; Caruso, E.; Sant, S.; O'Connor, E.; Baumgartner, Y.; Sousa, M.; Caimi, D.; Olziersky, A.; Palestri, P.; et al. A scaled replacement metal gate InGaAs-on-Insulator n-FinFET on Si with record performance. In Proceedings of the 2017 IEEE International Electron Devices Meeting, San Francisco, CA, USA, 2–6 December 2017; pp. 17.5.1–17.5.4.
3. Zota, C.B.; Convertino, C.; Deshpande, V.; Merkle, T.; Sousa, M.; Caimi, D.; Czomomaz, L. InGaAs-on-Insulator MOSFETs Featuring Scaled Logic Devices and Record RF Performance. In Proceedings of the 2018 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 18–22 June 2018.
4. Sun, X.; D'Emic, C.; Cheng, C.-W.; Majumdar, A.; Sun, Y.; Cartier, E.; Bruce, R.L.; Frank, M.; Miyazoe, H.; Shiu, K.-T.; et al. High performance and Low Leakage Current InGaAs-on-Silicon FinFETs with 20 nm Gate Length. In Proceedings of the 2017 Symposia on VLSI Technology and Circuits, Kyoto, Japan, 5–8 June 2017; pp. 40–41.
5. Vardi, A.; del Alamo, J. Sub-10-nm fin-width self-aligned InGaAs FinFETs. *IEEE Electron Device Lett.* **2016**, *37*, 1104–1107. [[CrossRef](#)]

6. Czornomaz, L.; Daix, N.; Kerber, P.; Lister, K.; Caimi, D.; Rossel, C.; Sousa, M.; Uccelli, E.; Fompeyrine, J. Scalability of ultra-thin-body and BOX InGaAs MOSFETs on silicon. In Proceedings of the 2013 European Solid-State Device Research Conference, Bucharest, Romania, 16–20 September 2013; pp. 143–146.
7. Djara, V.; Deshpande, V.; Uccelli, E.; Daix, N.; Caimi, D.; Rossel, C.; Sousa, M.; Siegwart, H.; Marchiori, C.; Lubyshev, D.; et al. An InGaAs on Si platform for CMOS with 200 mm InGaAs-OI substrate, gate-first, replacement gate planar and FinFETs down to 120 nm contact pitch. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015; pp. T176–T177.
8. Convertino, C.; Zota, C.B.; Caimi, D.; Sousa, M.; Czornomaz, L. InGaAs FinFETs 3D Sequentially Integrated on FDSOI Si CMOS with Record Performance. In Proceedings of the 48th European Solid-State Device Research Conference (ESSDERC), Dresden, Germany, 3–6 September 2018; pp. 162–165.
9. Zota, C.B.; Lindelow, F.; Wernersson, L.E.; Lind, E. InGaAs tri-gate MOSFETs with record on-current. In Proceedings of the 2016 IEEE International Electron Devices Meeting (IEDM), San Francisco, CA, USA, 3–7 December 2016; pp. 3.2.1–3.2.4.
10. Lindelow, F. Gated Hall effect measurements on selectively grown InGaAs nanowires. *Nanotechnology* **2017**, *28*, 205204. [[CrossRef](#)] [[PubMed](#)]
11. Li, J.Z.; Bai, J.; Park, J.-S.; Adekore, B.; Fox, K.; Carroll, M.; Lochtefeld, A.; Shellenbarger, Z. Defect reduction of GaAs epitaxy on Si (001) using selective aspect ratio trapping. *Appl. Phys. Lett.* **2007**, *91*, 021114. [[CrossRef](#)]
12. Waldron, N.; Merckling, C.; Guo, W.; Ong, P.; Teugels, L.; I, S.A.; Tsvetanova, D.; Sebaai, F.; van Dorp, D.H.; Milenin, A.; et al. An InGaAs/InP quantum well finfet using the replacement fin process integrated in an RMG flow on 300 mm Si substrates. In Proceedings of the 2014 Symposia on VLSI Technology & Circuits, Honolulu, HI, USA, 9–13 June 2014; pp. 26–27.
13. Schmid, H.; Borg, M.; Moselund, K.; Gignac, L.; Breslin, C.M.; Bruley, J.; Cutaia, D.; Riel, H. Template-assisted selective epitaxy of III–V nanoscale devices for co-planar heterogeneous integration with Si. *Appl. Phys. Lett.* **2015**, *106*, 233101. [[CrossRef](#)]
14. Borg, M.; Schmid, H.; Moselund, K.E.; Cutaia, D.; Riel, H. Mechanisms of template-assisted selective epitaxy of InAs nanowires on Si. *J. Appl. Phys.* **2015**, *117*, 144303. [[CrossRef](#)]
15. Czornomaz, L.; Uccelli, E.; Sousa, M.; Deshpande, V.; Djara, V.; Caimi, D.; Rossel, M.D.; Erni, R.; Fompeyrine, J. Confined epitaxial lateral overgrowth (CELO): A novel concept for scalable integration of CMOS compatible InGaAs-on-insulator MOSFETs on large-area Si substrates. In Proceedings of the 2015 Symposium on VLSI Technology (VLSI Technology), Kyoto, Japan, 16–18 June 2015.
16. Cutaia, D.; Moselund, K.E.; Schmid, H.; Borg, M.; Olziersky, A.; Riel, H. Complementary III–V heterojunction lateral NW Tunnel FET technology on Si. In Proceedings of the 2016 IEEE Symposium on VLSI Technology, Honolulu, HI, USA, 14–16 June 2016; p. 403.
17. Convertino, C.; Zota, C.B.; Schmid, H.; Ionescu, A.M.; Moselund, K.E. III–V heterostructure tunnel field-effect transistor. *J. Phys. Condens. Matter* **2018**, *30*, 264005. [[CrossRef](#)] [[PubMed](#)]
18. Gooth, J.; Schaller, V.; Wirths, S.; Schmid, H.; Borg, M.; Bologna, N.; Karg, S.; Riel, H. Ballistic one-dimensional transport in InAs nanowires monolithically integrated on silicon. *Appl. Phys. Lett.* **2017**, *110*, 083105. [[CrossRef](#)]
19. Mauthe, S.; Mayer, B.; Sousa, M.; Villares, G.; Staudinger, P.; Schmid, H.; Moselund, K. Monolithically integrated InGaAs microdisk lasers on silicon using template-assisted selective epitaxy. *SPIE* **2018**. [[CrossRef](#)]
20. Borg, M.; Gignac, L.; Bruley, J.; Malmgren, A.; Sant, S.; Convertino, C.; Rossel, M.D.; Sousa, M.; Breslin, C.; Riel, H. Facet-selective group-III incorporation in InGaAs Template Assisted Selective Epitaxy. *IOP Nanotechnol.* **2018**. [[CrossRef](#)] [[PubMed](#)]

