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Study on the Current-Limiting-Capable Control Strategy for Grid-Connected Three-Phase Four-Leg Inverter in Low-Voltage Network

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Academic Editor: Gabriele Grandi

Received: 7 July 2016; Accepted: 5 September 2016; Published: 8 September 2016

Abstract: The three-phase four-leg inverter can produce balanced voltages even with unbalanced loads, yet its controller design is quite complicated. Based on the analysis on time domain equations, a decoupled sequence control strategy for the three-phase four-leg inverter in a low-voltage network is proposed. A negative sequence controller and a zero sequence controller are added to the control strategy besides the positive sequence controller. Furthermore, considering the output limit of the inverter, a current limit design scheme is raised through the analysis on each sequence current in synchronous rotating frame. In the case of asymmetry, the limit value of each sequence current can be adjusted dynamically according to the design scheme. The output currents in each sequence can be controlled and limited for different purposes respectively. Finally, simulation results based on PSCAD/EMTDC V4.5.0 verify the validity of the control strategy.

Keywords: three-phase four-leg inverter; sequence control strategy; current-limiting scheme; low-voltage network

1. Introduction

In the low-voltage distribution network there are many single-phase loads, which of each phase cannot achieve absolute balance, so the voltages of the three phases are not completely symmetrical. To solve this problem as well as to improve power quality, the three-phase four-leg inverter is recommended to be used for the connection of the distributed generator to grids with a high power quality requirement [1–3]. In order to achieve a three-phase symmetrical output voltage, a bridge arm is applied to form the neutral point in the three-phase four-leg inverter, making the inverter more complex than the traditional one. Due to its special function, the control strategy is also very different from that of the traditional three-phase inverter [2,4]. Furthermore, studying the current-limiting scheme is meaningful for exerting the maximum capability in the case of limited inverter capacity. Unlike the three-phase inverter, this inverter's three phase currents are different from each other, so the current limit cannot be simply determined by only one phase current in the traditional way. Besides providing a feasible method of determining the current limit, this paper also addresses the control strategy of the inverter and the way to limit the output current.

As the important role of the three-phase four-leg inverter is balancing voltage, its control strategy has been studied by many insiders. According to the analysis by using symmetrical component method and large-signal averaged modeling method, it is found that an asymmetric output voltage is generated when the three-phase inverter fails to keep the neutral point potential constant in the case of unbalanced loads [5]. The research on three-phase inverters with unbalanced loads is also widely carried out [6–10], but constrained by the structure, it is difficult to completely solve the

problem of voltage asymmetry. On this basis, the structure of neutral point clamped (NPC) inverter begins to be studied [11,12]. Its DC capacitor is split and the midpoint is connected with the neutral line. However, problems of neutral point voltage balancing and low DC voltage utilization are complicated. Another method to solve the voltage asymmetry problem is the three-phase four-leg structure. According to modeling and analyzing the load neutral point voltage (LNPV) of three-phase four-leg inverter, the factors influencing the LNPV are revealed, and the methods to mitigate the LNPV is proposed [13]. The transfer functions of open-loop control or the proportional integral (PI) controller in the synchronous frame are studied in [14], and a method of restraining current disturbances to the three-phase four-leg inverter with unbalanced load is proposed. A strategy with model predictive control is proposed and the mathematical model of the four-leg inverter is analyzed in [15]. To keep the voltage three-phase balanced, a method of eliminating the neutral current is studied [16]. Paper [17] proposes a method based on modified repetitive control (MRC) which integrates with a non-phase-shifting low-pass filter, having a better tradeoff between the performance and robustness of repetitive control, but the effectiveness of this method is highly subject to the pole placement, bandwidth, and damping coefficient of the MRC. By using the symmetrical component method, each component can be decomposed into positive, negative, and zero sequence, which can simplify the control of three-phase four leg inverter [18,19]. Space-vector-modulation strategies respectively based on ABC and 3D coordinate systems are proposed in [20–22], but they are sort of complicated. However, the papers above only focus on the control strategy of the three-phase four-leg inverter, and do not involve discussion on how to play its maximum capacity when the output current is limited.

This paper is focused on a simple control strategy of the three-phase four-leg inverter connected to the low-voltage network with unbalance loads. By decoupling the mathematical model of three-phase four-leg inverter to three-phase form and single-phase form with the symmetrical component method, a sequence-independent control scheme is presented. On this basis, the current-limiting scheme is proposed for the inverter to achieve the maximum output capability with the output current of each leg under the limit.

2. Control Strategy of the Three-Phase Four-Leg Inverter

2.1. Modeling and Analysis of the Three-Phase Four-Leg Inverter

Compared with the traditional three-phase inverter, the three-phase four-leg inverter has an extra bridge arm as the neutral point, shown as Figure 1.

Figure 1. Topological structure of three-phase four-leg inverter with LC filter.

In Figure 1, u_{dc} is the DC voltage, u_a , u_b , u_c , u_n each represent a leg voltage, i_n is the current flowing through the neutral inductor L_n , u_{sa} , u_{sb} , u_{sc} are respectively the voltages of the three phases at the point of common coupling (PCC), and i_a , i_b , i_c are the currents flowing into PCC. L_f is the three-phase inductance of filter and C_f is the filter capacitance.

It is shown in Figure 1 that the fourth leg can provide a pathway for zero-sequence current. According to the topological structure, the differential equation of the circuit can be written as

$$\begin{aligned} u_a &= L_f \left(\frac{di_a}{dt} + C_f \frac{d^2 u_{sa}}{dt^2} \right) + u_{sa} \\ u_b &= L_f \left(\frac{di_b}{dt} + C_f \frac{d^2 u_{sb}}{dt^2} \right) + u_{sb} \\ u_c &= L_f \left(\frac{di_c}{dt} + C_f \frac{d^2 u_{sc}}{dt^2} \right) + u_{sc} \\ u_n &= -L_n \frac{di_n}{dt} \end{aligned} \quad (1)$$

Since most of the high-frequency harmonic components of the output voltage and current can be filtered by the grid-connected filter, they are not discussed for the basic control strategy study in this paper. The following analyses are based on fundamental components of 50 or 60 Hz.

To achieve the decoupling of each sequence component with the symmetrical component method, (1) is transformed to the phasor Equation (2).

$$\begin{bmatrix} \dot{U}_a \\ \dot{U}_b \\ \dot{U}_c \end{bmatrix} = j\omega L_f \begin{bmatrix} \dot{I}_a \\ \dot{I}_b \\ \dot{I}_c \end{bmatrix} + (1 - \omega^2 L_f C_f) \begin{bmatrix} \dot{U}_{sa} \\ \dot{U}_{sb} \\ \dot{U}_{sc} \end{bmatrix} \quad (2)$$

Multiplying (2) by the symmetrical component transformation matrix $\mathbf{S}$, we get

$$\mathbf{S} \begin{bmatrix} \dot{U}_a \\ \dot{U}_b \\ \dot{U}_c \end{bmatrix} = j\omega L_f \mathbf{S} \begin{bmatrix} \dot{I}_a \\ \dot{I}_b \\ \dot{I}_c \end{bmatrix} + (1 - \omega^2 L_f C_f) \mathbf{S} \begin{bmatrix} \dot{U}_{sa} \\ \dot{U}_{sb} \\ \dot{U}_{sc} \end{bmatrix} \quad (3)$$

where the matrix $\mathbf{S}$ is

$$\mathbf{S} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \quad (4)$$

where the operator $a = e^{j120^\circ}$.

Then there is

$$\begin{bmatrix} \dot{U}_{a(1)} \\ \dot{U}_{a(2)} \\ \dot{U}_{a(0)} \end{bmatrix} = j\omega L_f \begin{bmatrix} \dot{I}_{a(1)} \\ \dot{I}_{a(2)} \\ \dot{I}_{a(0)} \end{bmatrix} + (1 - \omega^2 L_f C_f) \begin{bmatrix} \dot{U}_{sa(1)} \\ \dot{U}_{sa(2)} \\ \dot{U}_{sa(0)} \end{bmatrix} \quad (5)$$

It can be seen from (5) that the three-sequence components are independent of each other, so the differential equations of each sequence in time domain are

$$\begin{aligned} u_{a(1)} &= L_f \left(\frac{di_{a(1)}}{dt} + C_f \frac{d^2 u_{sa(1)}}{dt^2} \right) + u_{sa(1)} \\ u_{b(1)} &= L_f \left(\frac{di_{b(1)}}{dt} + C_f \frac{d^2 u_{sb(1)}}{dt^2} \right) + u_{sb(1)} \\ u_{c(1)} &= L_f \left(\frac{di_{c(1)}}{dt} + C_f \frac{d^2 u_{sc(1)}}{dt^2} \right) + u_{sc(1)} \end{aligned} \quad (6)$$

$$\begin{aligned} u_{a(2)} &= L_f \left(\frac{di_{a(2)}}{dt} + C_f \frac{d^2 u_{sa(2)}}{dt^2} \right) + u_{sa(2)} \\ u_{b(2)} &= L_f \left(\frac{di_{b(2)}}{dt} + C_f \frac{d^2 u_{sb(2)}}{dt^2} \right) + u_{sb(2)} \\ u_{c(2)} &= L_f \left(\frac{di_{c(2)}}{dt} + C_f \frac{d^2 u_{sc(2)}}{dt^2} \right) + u_{sc(2)} \end{aligned} \quad (7)$$

$$u_{a(0)} = L_f \left(\frac{di_{a(0)}}{dt} + C_f \frac{d^2 u_{sa(0)}}{dt^2} \right) + u_{sa(0)} \quad (8)$$

Subscripts (1) , (2) , and (0) respectively indicate the positive, negative and zero sequence components. Then (6) is the positive sequence equation of the inverter, while (7) is the negative and (8) is the zero. As the zero sequence components of three phases are exactly identical, only the equation of phase A is given.

According to the Kirchhoff's Current Law, the current i_n flowing through the neutral line must satisfy

$$i_n = (i_a + i_b + i_c) + C_f \left(\frac{du_{sa}}{dt} + \frac{du_{sb}}{dt} + \frac{du_{sc}}{dt} \right) = 3(i_{a(0)} + C_f \frac{du_{sa(0)}}{dt}) \quad (9)$$

So, the fourth equation in (1) can be written as

$$u_n = -3L_n \left(\frac{di_{a(0)}}{dt} + C_f \frac{d^2 u_{sa(0)}}{dt^2} \right) \quad (10)$$

From (9) and (10) we can know that the neutral line current i_n only contains the zero sequence component. Therefore, the output voltage of the fourth leg is just the zero sequence voltage.

Through the analysis, it is known that the positive and negative sequence components are only dependent on the voltages and currents of the first three legs, consistent with the mathematical model of the traditional three-phase inverter, but the zero sequence components are different.

According to (8) and (10), the zero sequence equation is

$$u_{an(0)} = u_{a(0)} - u_n = (L_f + 3L_n) \left(\frac{di_{a(0)}}{dt} + C_f \frac{d^2 u_{sa(0)}}{dt^2} \right) + u_{sa(0)} \quad (11)$$

where $u_{an(0)}$ is the zero sequence potential difference between the outlets of the first and fourth legs.

The zero sequence circuit topology described by (11) is shown in Figure 2.

Figure 2. Equivalent circuit topology of zero sequence.

In summary, (6), (7), and (11) can respectively describe the positive, negative, and zero sequence mathematical models of three-phase four leg inverter. To maintain the symmetry of the three-phase voltage in the low-voltage distribution network with unbalanced loads, the negative and zero sequence voltage have to be 0. In other words, the PCC voltage contains only the positive sequence component.

2.2. Control Strategy of Positive and Negative Sequence Components

For the grid-connected distributed generator (DG), the constant power control (PQ control) is widely adopted. According to the instantaneous power theory [23], the average part of instantaneous power, in which form the energy is transferred in the three-phase four-wire system, can be expressed as (12).

$$\begin{aligned} \bar{p} &= 3V_{(1)}I_{(1)}\cos\phi_{v(1)} - \phi_{i(1)} + 3V_{(2)}I_{(2)}\cos\phi_{v(2)} - \phi_{i(2)} + 3V_{(0)}I_{(0)}\cos\phi_{v(0)} - \phi_{i(0)} \\ \bar{q} &= 3V_{(1)}I_{(1)}\sin\phi_{v(1)} - \phi_{i(1)} - 3V_{(2)}I_{(2)}\sin\phi_{v(2)} - \phi_{i(2)} \end{aligned} \quad (12)$$

where $\bar{p}$, $\bar{q}$ represent the average parts of active power and reactive power respectively, and the pairs of $V_{(1)}$ and $I_{(1)}$, $V_{(2)}$ and $I_{(2)}$, as well as $V_{(0)}$ and $I_{(0)}$, represent the effective voltage and current values of positive, negative and zero sequences separately, with their corresponding phases being $\phi_{v(1)}$, $\phi_{i(1)}$, $\phi_{v(2)}$, $\phi_{i(2)}$, $\phi_{v(0)}$, and $\phi_{i(0)}$.

Assuming the negative and zero sequence voltages are 0 to achieve symmetry, $\bar{p}$ and $\bar{q}$ in (12) are determined only by the positive sequence components. Therefore, the positive sequence components can be regulated with the PQ control method as a way to control the power flow.

Through the Park transformation, both the positive sequence and the negative sequence components acquire the DC form in d-q coordinate system, and thus can be easily controlled by the PI controller without the static error [24]. Here we show the transforming process:

The Park transformation matrix is

$$C_{3s/2r} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos(\theta - \frac{2\pi}{3}) & \cos(\theta + \frac{2\pi}{3}) \\ -\sin\theta & -\sin(\theta - \frac{2\pi}{3}) & -\sin(\theta + \frac{2\pi}{3}) \end{bmatrix} \quad (13)$$

For the positive sequence,

$$\begin{bmatrix} u_{sd(1)} \\ u_{sq(1)} \end{bmatrix} = C_{3s/2r} \begin{bmatrix} u_{sa(1)} \\ u_{sb(1)} \\ u_{sc(1)} \end{bmatrix} = C_{3s/2r} \begin{bmatrix} U_{(1)m}\sin(\omega t + \alpha_1) \\ U_{(1)m}\sin(\omega t + \alpha_1 - 2\pi/3) \\ U_{(1)m}\sin(\omega t + \alpha_1 + 2\pi/3) \end{bmatrix} = U_{(1)m} \begin{bmatrix} \sin(\omega t + \alpha_1 - \theta) \\ -\cos(\omega t + \alpha_1 - \theta) \end{bmatrix} \quad (14)$$

where $u_{sd(1)}$ and $u_{sq(1)}$ are the d-axis and q-axis components of the PCC positive voltage, $U_{(1)m}$ is its amplitude and ω is the system angular frequency which is obtained by the phase-locked loop (PLL) in real time, and α_1 is the initial phase of $u_{sa(1)}$. To make $u_{sd(1)}$ and $u_{sq(1)}$ take the DC form, and to enable $u_{sq(1)} = 0$, the following condition has to be met

$$\theta = \omega t + \alpha_1 - \pi/2 \quad (15)$$

For the negative sequence, the negative sequence current is used as an example. Let $\theta' = -\theta = -(\omega t + \alpha_1 - \pi/2)$, and get $C'_{3s/2r}$ by replacing the θ in $C_{3s/2r}$ with θ' . Then,

$$\begin{bmatrix} i_{d(2)} \\ i_{q(2)} \end{bmatrix} = C'_{3s/2r} \begin{bmatrix} i_{a(2)} \\ i_{b(2)} \\ i_{c(2)} \end{bmatrix} = C'_{3s/2r} \begin{bmatrix} I_{(2)m}\sin(\omega t + \varphi_2) \\ I_{(2)m}\sin(\omega t + \varphi_2 + 2\pi/3) \\ I_{(2)m}\sin(\omega t + \varphi_2 - 2\pi/3) \end{bmatrix} = I_{(2)m} \begin{bmatrix} \cos(\varphi_2 - \alpha_1) \\ -\sin(\varphi_2 - \alpha_1) \end{bmatrix} \quad (16)$$

where $I_{(2)m}$ and φ_2 are the amplitude and initial phase of $i_{a(2)}$.

Through the transformations (14) and (16), the PI controller is introduced to the d-q frame. Because the harmonics in the primary currents and voltages will bring problems for PI controller, low pass filters should be applied to the decomposition process of sequence components.

The inner-loop and outer-loop controllers of the positive sequence components are expressed as (17) and (18), respectively.

$$\begin{aligned} u_{d(1)\text{-ref}} &= (K_{iP(1)} + \frac{K_{il(1)}}{s})(i_{d(1)\text{-ref}} - i_{d(1)}) - \omega L_f i_{q(1)} + u_{sd(1)} \\ u_{q(1)\text{-ref}} &= (K_{iP(1)} + \frac{K_{il(1)}}{s})(i_{q(1)\text{-ref}} - i_{q(1)}) + \omega L_f i_{d(1)} + u_{sq(1)} \end{aligned} \quad (17)$$

$$\begin{aligned} i_{d(1)\text{-ref}} &= (K_{oP(1)} + \frac{K_{ol(1)}}{s})(P_{\text{ref}} - P) \\ i_{q(1)\text{-ref}} &= (K_{oP(1)} + \frac{K_{ol(1)}}{s})(Q_{\text{ref}} - Q) \end{aligned} \quad (18)$$

where $i_{d(1)}$ and $i_{q(1)}$ are the d-axis and q-axis components of the positive sequence current; $K_{iP(1)}$ and $K_{oP(1)}$ the proportionality coefficients of the inner and outer loops; $K_{il(1)}$ and $K_{ol(1)}$ the integral coefficients of the inner and outer loops; $i_{d(1)\text{-ref}}$ and $i_{q(1)\text{-ref}}$ the reference currents; P_{ref} and Q_{ref} the reference powers; and, $u_{d(1)\text{-ref}}$ and $u_{q(1)\text{-ref}}$ the modulation signals.

The outer loop is used to achieve power control, while the inner loop speeds up the dynamic response.

For the negative sequence components, as they are converted to the DC form, they can also be regulated by the same control method as the positive sequence components in (17) and (18), with components P and Q replaced by the negative voltages for the outer loop control [25]:

$$\begin{aligned} i_{d(2)\text{-ref}} &= -(K_{oP(2)} + \frac{K_{ol(2)}}{s})u_{sd(2)} \\ i_{q(2)\text{-ref}} &= -(K_{oP(2)} + \frac{K_{ol(2)}}{s})u_{sq(2)} \end{aligned} \quad (19)$$

The positive and negative sequence control strategies are illustrated in Figure 3.

Figure 3. Control strategy of the three-phase four-leg inverter: (a) Positive sequence control strategy; (b) Negative sequence control strategy.

2.3. Control Strategy of Zero Sequence Component

In (11), the zero sequence model of the three-phase four-leg inverter can be regarded as a single-phase inverter, so it can be controlled by a similar strategy to that of a single-phase inverter.

Due to the static error in controlling an AC system, the PI controller fails when high precision is required, and has to give way to the proportional resonant (PR) controller, which has no static error. However, this is only in principle, for it is difficult to build an ideal PR controller and its regulating performance is subject to the fluctuations of the grid frequency [26]. Another way to avoid this disadvantage is trying to convert the single-phase AC signal to DC form to make it acceptable for the application of the PI controller.

For a single-phase voltage or current, with a delay of a quarter of the period, a new signal is created, whose vector is perpendicular to that of the former [27]. The two signals can be converted into DC components through the $\alpha\beta$ -dq transformation. Take the zero sequence current $i_{a(0)}$ for example, whose expression is

$$i_{a(0)} = I_{(0)m} \sin(\omega t + \varphi_0) \quad (20)$$

In the $\alpha\beta$ static coordinate system, let

$$\begin{aligned} i_\alpha &= i_{a(0)} = I_{(0)m} \sin(\omega t + \varphi_0) \\ i_\beta &= I_{(0)m} \sin(\omega t + \varphi_0 - 90^\circ) = -I_{(0)m} \cos(\omega t + \varphi_0) \end{aligned} \quad (21)$$

After the $\alpha\beta$ -dq transformation, two DC components $i_{d(0)}$ and $i_{q(0)}$ are obtained as

$$\begin{bmatrix} i_{d(0)} \\ i_{q(0)} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix} \begin{bmatrix} i_\alpha \\ i_\beta \end{bmatrix} = I_{(0)m} \begin{bmatrix} \sin(\omega t + \varphi_0 - \theta) \\ -\cos(\omega t + \varphi_0 - \theta) \end{bmatrix} = I_{(0)m} \begin{bmatrix} \cos(\varphi_0 - \alpha_1) \\ \sin(\varphi_0 - \alpha_1) \end{bmatrix} \quad (22)$$

where $\theta = \omega t + \alpha_1 - \pi/2$.

Figure 4 illustrates the transformation process.

Figure 4. The transformation process of zero sequence.

Through the transformation, the static error of the PI controller can be eliminated. The control method is similar to that of negative sequence components, only with L_f replaced by $(L_f + 3L_n)$ and each voltage and current replaced by its zero sequence counterpart in (17) and (19).

Finally, the control signals of the three sequences should be superimposed and modulated in the way shown in Figure 5 to achieve the control on the three-phase four-leg inverter. In this paper, sine-wave pulse-width modulation (SPWM) is chosen as the modulation strategy.

Figure 5. Superimposition of control signals.

3. Current-Limiting Scheme Embedded in Control Strategy

To maintain the PCC voltage symmetry, each phase current output by the three-phase four-leg inverter is usually unequal in magnitude with others. The method of the modulus limit on current reference value is not applicable to limiting the output current and protect the inverter. In addition, setting limit values for each sequence independently may cause the waste of the inverter capacity. It is necessary to find a method which can limit the phase currents and make full use of the capacity of the inverter.

According to the control strategy above, the controller of each sequence is independent with others. The positive sequence current is determined by the target of the output power. It takes on the role of outputting active and reactive power. The negative and zero sequence currents depend on the load condition, and they play a common role of balancing the PCC voltage. Thus, the negative and zero sequence currents can be put into one block to be discussed, and for convenience, their sum $\dot{I}_{k(2,0)}$ can be called as the balance regulating current.

$$\dot{I}_{k(2,0)} = \dot{I}_{k(2)} + \dot{I}_{(0)}, \quad (k = a, b, c) \quad (23)$$

where $\dot{I}_{k(2)}$ is the negative sequence current of phase k , and as the zero sequence components of three phases are exactly identical, the zero sequence current is written as $\dot{I}_{(0)}$.

Then, the currents are divided into two categories: the positive sequence current is for power transmission, and the balance regulating current, which is the sum of the negative and zero sequence currents, is for voltage balance.

3.1. Output Characteristic of Each Sequence

When the direction of the AC voltage vector $\mathbf{U}_{(1)}$ is selected as that of the d-axis in the synchronous rotating coordinate system, the output power and positive sequence current of the DG have such relationships [24]

$$\begin{cases} P = 1.5u_{sd(1)}i_{d(1)} \\ Q = -1.5u_{sd(1)}i_{q(1)} \end{cases} \quad (24)$$

where P and Q are the active power and reactive power output by the inverter. Since the Park transformation will not change the amplitude, $u_{sd(1)}$ has the same amplitude with $\mathbf{U}_{(1)}$.

Therefore, the d-axis and q-axis components of the positive sequence current can be obtained as

$$\begin{cases} i_{d(1)} = \frac{2}{3} \frac{P}{u_{sd(1)}} = \frac{2}{3} \frac{P}{|\mathbf{U}_{(1)}|} \\ i_{q(1)} = -\frac{2}{3} \frac{Q}{u_{sd(1)}} = -\frac{2}{3} \frac{Q}{|\mathbf{U}_{(1)}|} \end{cases} \quad (25)$$

According to Figure 6, the current vector $\mathbf{I}_{(1)}$ lags behind the voltage vector $\mathbf{U}_{(1)}$ by an angle $\Delta\theta$. Accordingly, each phase current lags behind the corresponding phase voltage by $\Delta\theta$ in abc frame. According to (14), the amplitude of each phase current is equal with that of $\mathbf{I}_{(1)}$. The A phase current phasor can be expressed as

$$\dot{I}_{a(1)} = \sqrt{i_{d(1)}^2 + i_{q(1)}^2} \angle (\theta_0 + \Delta\theta) \quad (26)$$

where $\theta_0 = \arg \dot{U}_{sa(1)}$ and $\Delta\theta = \arctan(i_{q(1)}/i_{d(1)})$.

Figure 6. Positive sequence current in d-q frame.

In addition, the control system of the inverter is generally equipped with a modulus limiter, which can limit the amplitude of the output current within a certain value $I_{(1)\max}$. Therefore, according to (25) and (26), the positive sequence current is

$$\dot{I}_{a(1)} = \frac{2}{3} \frac{\sqrt{P_{\text{ref}}^2 + Q_{\text{ref}}^2}}{|\mathbf{U}_{(1)}|} \angle (\theta_0 + \Delta\theta), \quad \frac{2}{3} \frac{\sqrt{P_{\text{ref}}^2 + Q_{\text{ref}}^2}}{|\mathbf{U}_{(1)}|} < I_{(1)\max} \quad (27)$$

When the voltage is very small, which means the $\dot{I}_{a(1)}$ will be rather large, $\dot{I}_{a(1)}$ should be limited at the maximum value $I_{(1)\max}$. The modulus limiter can limit the amplitude of the current without changing its phase [25]. Then, the positive sequence current can be written as

$$\dot{I}_{a(1)} = I_{(1)\max} \angle (\theta_0 + \Delta\theta), \quad \frac{2}{3} \frac{\sqrt{P_{\text{ref}}^2 + Q_{\text{ref}}^2}}{|\mathbf{U}_{(1)}|} \geq I_{(1)\max} \quad (28)$$

For the negative and zero sequence currents, which are introduced to maintain voltage symmetry, they are determined by loads, and only the electrical states of the negative and zero sequence components are known

$$\dot{U}_{sa(2)} = \dot{U}_{s(0)} = 0, \quad |\dot{I}_{k(2,0)}| < I_{(2,0)\max} \quad (k = a, b, c) \quad (29)$$

where the zero sequence voltage of PCC is written as $\dot{U}_{s(0)}$ for that of each phase is identical; $\dot{U}_{sa(2)}$ is the A phase negative voltage and $I_{(2,0)\max}$ is the amplitude limit of the balance regulating current $\dot{I}_{k(2,0)}$.

To keep the voltages of both the negative sequence and zero sequence being zero, the amplitude of $\dot{I}_{k(2,0)}$ cannot exceed $I_{(2,0)\max}$. It is noted that if the amplitude of $\dot{I}_{k(2,0)}$ for any phase has the trend of surpassing $I_{(2,0)\max}$, it will be limited at this maximum, but in this case, the voltages may not be maintained at 0.

$$\max |\dot{I}_{k(2,0)}| = I_{(2,0)\max} \quad (k = a, b, c) \quad (30)$$

Thus $I_{(2,0)\max}$ can be seen as an indicator of the capability of the inverter to maintain the voltage symmetry.

3.2. Current Modulus Limiters of Each Sequence

The equations in (28) and (30) can be satisfied by applying a modulus limiter to each of the outer loops.

For (28), the three-phase current is symmetrical, so the model of the modulus limiter in Figure 7 can be used [24].

Figure 7. The positive sequence modulus limiter.

However, for (30), the balance regulating current $\dot{I}_{k(2,0)}$ of each phase is unique and thus should be calculated separately.

For the negative and zero sequence currents, after the Park transformation, the d-axis and q-axis components are shown as (16) and (22) respectively.

Then make the phasor diagram of the negative and zero sequence currents as Figure 8. By selecting the direction of $\dot{U}_{sa(1)}$ as that of the x-axis, a Rectangular coordinate system is built, where the x-axis and y-axis components of each phase can be obtained.

Figure 9. The negative and zero sequence modulus limiter.

In Figure 9, $\varphi_{k(2)}$ is the included angle between $\dot{I}_{k(2)}$ and the x-axis, and $\varphi_{(0)}$ is that between $\dot{I}_{(0)}$ and the x-axis, which can be deduced by

$$\begin{aligned}\tan \varphi_{k(2)} &= I_{k(2)y} / I_{k(2)x} \\ \tan \varphi_{(0)} &= I_{(0)y} / I_{(0)x}\end{aligned}\quad (36)$$

To limit the amplitude of the balance regulating current without changing the phase angle, the redistribution of the x-axis and y-axis components can be achieved by

$$\begin{cases} I'_{k(2)y} / I'_{k(2)x} = \tan \varphi_{k(2)} \\ I'_{(0)y} / I'_{(0)x} = \tan \varphi_{(0)} \\ I'_{k(2)x} + I'_{(0)x} = I_{k(2,0)m} \cos \varphi_{k(2,0)} \\ I'_{k(2)y} + I'_{(0)y} = I_{k(2,0)m} \sin \varphi_{k(2,0)} \end{cases}\quad (37)$$

It is defined that

$$\beta_k = \frac{I_{k(2,0)m} \cos \varphi_{k(2,0)}}{\tan \varphi_{(0)} - \tan \varphi_{k(2)}}\quad (38)$$

The negative and zero sequence components output by the modulus limiter are

$$\begin{cases} I'_{k(2)x} = \beta_k (\tan \varphi_{(0)} - \tan \varphi_{k(2,0)}) \\ I'_{k(2)y} = \beta_k (\tan \varphi_{(0)} - \tan \varphi_{k(2,0)}) \tan \varphi_{k(2)} \\ I'_{(0)x} = \beta_k (\tan \varphi_{k(2,0)} - \tan \varphi_{k(2)}) \\ I'_{(0)y} = \beta_k (\tan \varphi_{k(2,0)} - \tan \varphi_{k(2)}) \tan \varphi_{(0)} \end{cases}\quad (39)$$

It is noted that (39) needs to be calculated for each of the three phases separately, and the corresponding $i'_{d(2)}$, $i'_{q(2)}$, $i'_{d(0)}$ and $i'_{q(0)}$ for each phase can be obtained through the inverse transformation of (31)–(33). The minimum of them will be used as the new references to ensure that each phase current does not exceed the limit value.

3.3. Combined Current-Limiting Method

The amplitude limit value for the positive sequence current is $I_{(1)\max}$, and that for the sum of the negative and zero sequence currents is $I_{(2,0)\max}$, but the real constriction for the inverter output current is the maximum phase current which is determined by the current-carrying capacity of the IGBT and the saturation current of the output filter. Therefore, the real current limit should be modified as

$$\begin{cases} |\dot{I}_{k(1)} + \dot{I}_{k(2)} + \dot{I}_{(0)}| < I_{\max} \\ 3|\dot{I}_{(0)}| < I_{\max} \end{cases} \quad (k = a, b, c)\quad (40)$$

where $I_{\max}$ is the amplitude of the maximum phase current the DG can endure. The first condition in (40) should be met by each of the three phases. The second condition can be easily satisfied by using a modulus limiter next to the zero sequence outer loop.

If the priority is given to balancing the voltage over outputting power, the inverter needs to maintain the voltage symmetry as possible as it can. Thus, $I_{(2,0)\max}$ should be set as $I_{\max}$, and $I_{(1)\max}$ can be calculated graphically as shown in Figure 10, where the phase A is taken for example.

Figure 10. Method to get the maximum of the positive sequence current.

When P_{ref} and Q_{ref} are known, the phase angle $\Delta\theta$ is determined. Thus $\left| \dot{I}_{a(1)} \right|$ can be calculated with the cosine theorem.

Further, the maximum of the amplitude $I_{k(1)\text{m}}$ ($k = a, b, c$) can be obtained by solving (41).

$$\begin{cases} \alpha = \cos(\varphi_{k(2,0)} - \Delta\theta_k) \\ I_{k(2,0)\text{m}}^2 + I_{k(1)\text{m}}^2 - 2\alpha I_{k(2,0)\text{m}} I_{k(1)\text{m}} = I_{\max}^2 \end{cases} \quad (41)$$

where $\Delta\theta_k$ is the phase angle of the positive sequence current of phase k , and the solutions of (41) are

$$I_{k(1)\text{m}} = \alpha I_{k(2,0)\text{m}} \pm \sqrt{(\alpha^2 - 1) I_{k(2,0)\text{m}}^2 + I_{\max}^2} \quad (42)$$

As $I_{k(2,0)\text{m}} \leq I_{\max}$ and $\alpha I_{k(2,0)\text{m}} - \sqrt{(\alpha^2 - 1) I_{k(2,0)\text{m}}^2 + I_{\max}^2} < 0$, this solution can be excluded.

Therefore,

$$I_{(1)\text{max}} = \min \{ I_{k(1)\text{max}} \} = \min \{ \alpha I_{k(2,0)\text{m}} + \sqrt{(\alpha^2 - 1) I_{k(2,0)\text{m}}^2 + I_{\max}^2} \}, \quad (k = a, b, c) \quad (43)$$

Similarly, when outputting power is the first consideration, the limit value should be set by

$$\begin{aligned} I_{(1)\text{max}} &= I_{\max} \\ I_{(2,0)\text{max}} &= \min \left\{ \alpha I_{k(1)\text{m}} + \sqrt{(\alpha^2 - 1) I_{k(1)\text{m}}^2 + I_{\max}^2} \right\}, \quad (k = a, b, c) \end{aligned} \quad (44)$$

The scheme above can provide a current-limiting method in the case that the phase currents are not equal with each other in size. It can ensure that the current of any phase would not exceed the limit. Meanwhile, according to the different functions of the inverter, the switch between output power priority and balance voltage priority can be achieved flexibly. Furthermore, the scheme has

self-adaptation capability. The limit values can be adjusted with the change of the load so that the capacity of the inverter can be fully utilized.

4. Simulation and Analysis

To verify the effectiveness of the control strategy for the three-phase four-leg inverter and the embedded current-limiting scheme, the simulation models are established in PSCAD/EMTDC, which is shown in Figure 11.

Figure 11. Distribution network with a three-phase four-leg inverter-based DG.

In Figure 11, the system power is equivalent to a 0.4 kV three-phase voltage source $\dot{E}$ and an impedance Z_s in series. Z_s is set as $0.09 + j0.5 \Omega$. The feeder line is equivalent to a PI section. The positive sequence impedance of the feeder Z_1 is $0.412 + j0.0625 \Omega$ and the zero sequence impedance of the feeder Z_0 is $1.648 + j0.2501 \Omega$. The parameters of the DG model in Figure 11 are listed in Table 1.

Table 1. Parameters of the DG.

System Parameters	Values	PI Parameters	Values
DC voltage	0.8 kV	$K_{iP(1)} / K_{iL(1)}$	0.1/0.01
system voltage	0.4 kV	$K_{oP(1)} / K_{oL(1)}$	3.0/0.001
rated power P/Q	50 kW/0 kVar	$K_{iP(2)} / K_{iL(2)}$	0.25/0.015
filter inductance	4 mH	$K_{oP(2)} / K_{oL(2)}$	2.5/0.002
filter capacitance	100 μ F	$K_{iP(0)} / K_{iL(0)}$	2.0/0.12
L_n	1.5 mH	$K_{oP(0)} / K_{oL(0)}$	5.0/0.005

The case studies are separated into two parts. The first part is done to verify the voltage-balancing capability of the control strategy, and the second part is to verify the current-limiting scheme embedded in the control strategy.

4.1. Verification of the Voltage-Balancing Capability of the Control Strategy

Voltage unbalance of the distribution network is mainly caused by load asymmetry, so the impedance change of the load is applied to verify the voltage-balancing capability of the control strategy.

Firstly, a tunable three-phase resistor R is used as the load in simulation. At the very beginning of the simulation, R_a , R_b , and R_c are all set as 10Ω . At 0.52 s in simulation, R_a increases to 20Ω and R_c decreases to 5Ω . The voltage and current waveforms can be obtained through simulation.

In Figure 12a, there is a minor disturbance to the three-phase voltage when the resistances of the load changes at 0.52 s, and the voltage regains symmetry quickly afterwards. By contrast, in Figure 12b, the three-phase current becomes asymmetric after the load change. In Figure 12c,d, where the voltage and current are decomposed into positive, negative, and zero sequence components, the negative and zero sequence voltages disappear right after its occurrence at 0.52 s, while the corresponding currents have been existing ever since this moment. This is an indication of the fast response of the control system.

Figure 12. Waveforms of the PCC voltage and output current: (a) Three-phase voltage; (b) Three-phase current; (c) The positive, negative, and zero sequence voltages; (d) The positive, negative, and zero sequence currents.

Besides the simulation with the resistive loads, simulations with inductive loads and resistively-inductive loads are also carried out. At the very beginning of the simulation, the inductive loads L_a , L_b , and L_c are all set as 30 mH. At 0.52 s, L_a grows to 60 mH and L_c falls to 15 mH. The output voltage and current performances in this case are shown in Figure 13a. The three phase resistances of the resistively-inductive loads R_a , R_b , and R_c are all set as 10 Ω while the inductance L_a , L_b , and L_c are set as 10 mH. At 0.52 s in simulation, R_a grows to 20 Ω , L_a grows to 20 mH, R_c falls to 5 Ω , and L_c falls to 5 mH. The simulation results of output voltages and currents are presented in Figure 13b.

Figure 13. Waveforms of voltages and currents with inductive and resistively-inductive loads: (a) The inductive loads change; (b) The resistively-inductive loads change.

As is shown in Figure 13, when the inductive and resistively-inductive loads change, the voltages in both cases can transition to three-phase symmetrical conditions fast. The transition period with inductive loads is slightly longer than that with resistively-inductive loads, but finally both of the voltages can get symmetrical within 0.06 s.

From the simulation results, it is concluded that the three-phase four-leg inverter with this control strategy can ensure the output voltage balance.

4.2. Verification of the Current-Limiting Scheme

The current-limiting capability of the scheme has been tested in two cases—where a large reference power is given and where a severely unbalanced load is applied. For the model in Figure 11, it is assumed that R_a is set as $10\ \Omega$, R_b is set as $5\ \Omega$, and R_c is set as $2\ \Omega$. So the load is unbalanced. The active power reference is set as 40 kW and the reactive power is 0. The amplitude limit of the phase current is set as 0.2 kA. The current-limiting scheme is designed with the priority of voltage balance.

Case (1): The case is used to test the current-limiting capability while the current increase is caused by the ascent of the output reference of inverter. In this case, the active power reference is changed to 70 kW at 0.5 s, the external load condition keeps constant. The simulation results are shown in Figure 14.

Figure 14. Simulation results of the case with the power reference changing: (a) The amplitudes of the balance regulating currents; (b) The positive sequence current and its amplitude limit; (c) The active power and reactive power outputted by the inverter; (d) The three-phase PCC voltage; (e) The three-phase output current.

In Figure 14a, the amplitude of the sum of negative and zero sequence currents for each phase is presented. When the active power reference changes to 70 kW, each of them increases slightly, but they are still under the limit of 0.2 kA. Therefore, the PCC voltage in Figure 14d is still three-phase symmetrical. Accordingly, in Figure 14b, the limit value of the positive sequence current has a slight drop. To output more power, the positive sequence current rises before it is capped at the limit value. Therefore, in Figure 14c, the active power output by the inverter fails to reach the reference, but finally stops at around 58 kW. In a word, the output power is limited to ensure the current of each phase will not go beyond the set limit. According to Figure 14e, the current of phase C is the largest whose amplitude is limited at 0.2 kA.

In case (1), the three phase currents are all no more than the limit and the three phase voltages are symmetrical throughout. The increase of the output power reference only has a minor influence on the negative and zero sequence currents through the slight variation of the voltage. Therefore, the voltage-balancing capability can be ensured by the embedded current-limiting scheme with different output reference.

Case (2): The case is used to test the current-limiting capability while the current increase is caused by the deterioration of the external load asymmetry. At 0.5 s, the resistance of phase C changes from 2 to 0.5Ω . The unbalanced load is introduced to show the adjusting process and performance of the currents while the voltage unbalance rises beyond the capacity of control strategy under the constraint of the current-limiting scheme. The simulation results are shown as Figure 15.

Figure 15. Simulation results in the case with load changing: (a) The amplitudes of the balance regulating currents; (b) The positive sequence current and its amplitude limit; (c) The active power and reactive power output by the inverter; (d) The three-phase PCC voltage; (e) The three-phase output current.

In Figure 15a, the amplitude of the sum of the negative and zero sequence currents in phase C has reached the limit. The inverter is supposed to maintain voltage symmetry to its greatest capacity yet fails to achieve the goal due to the severe asymmetry of the load. So in Figure 15d, the PCC voltage cannot keep balanced after 0.5 s. Also, in Figure 15b, the limit value of the positive sequence current drops to 0, which causes the positive sequence active power to fall to 0 in Figure 15c. According to Figure 15d, it can be seen that the largest phase current appears in phase C, and it has an impulse to exceed the amplitude limit of 0.2 kA, but finally stabilizes under the limit.

In case (2), with the asymmetry increasing, the inverter needs to output larger negative and zero sequence currents to maintain voltage symmetry, which may cause the currents to exceed the limit. As the priority of the current-limiting scheme is voltage balance, the negative and zero sequence currents are preferentially output. So the positive sequence current drops to 0 to give way to the negative and zero sequence currents in this case. The voltage finally becomes asymmetrical because

the demand of the negative and zero sequence currents to maintain the voltage symmetry is beyond the limit of the current-limiting scheme.

5. Conclusions

In the paper, a novel control strategy including an adaptive current-limiting scheme for grid-connected three-phase four-leg inverter is proposed. It has the capability to dynamically adjust the current limit of each sequence while keeping the output voltage symmetrical. The main features are listed as follows:

1. The independent control schemes for the positive, negative, and zero sequence in synchronous rotating frame are realized based on the symmetrical component method. All three sequence components are transformed into DC to make the PI controller applicative.
2. Through the coordinate transformation, all the DC components of the three sequence currents in d-q frames are unified into one coordinate system. The current limiter is designed by calculating the current reference of each sequence in this unified coordinate system.
3. The current-limiting scheme is adaptive to the output power reference and the loads asymmetry condition. It can set the current limit of each sequence reasonably while giving full play to the output capability of the inverter.

Acknowledgments: This work was supported in part by the National Natural Science Foundation of China under Grant 51677125, by the Specialized Research Fund for the Doctoral Program of Higher Education for New Teacher under Grant 20120032120085 and by National High Technology Research and Development (863 program) under Grant 2015AA050102.

Author Contributions: Botong Li put forward the research direction, organized the research activities, provided theory guidance, and completed the revision of the article. Jianfei Jia completed the principle analysis and the method design, provided the results of the simulation, and drafted the article. Valuable comments on the first draft were received from Shimin Xue and Botong Li. All three were involved in revising the paper.

Conflicts of Interest: The authors declare no conflict of interest.

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