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A Hybrid Modular Multilevel Converter with Partial Embedded Energy Storage

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Abstract: Modular and cascaded multilevel converters provide a functional solution for the integration of energy storage systems (ESSs). This paper develops a hybrid multilevel converter based on the modular multilevel converter (MMC) that can be functionally extended with partial embedded ESS as a fraction of the overall converter power rating. The configuration, which can operate as a typical DC-AC converter, enables multi-directional power flow between the DC- and AC-side of the converter, as well as the embedded energy storage elements. The use of a three-phase flying-capacitor submodule eliminates the second-order harmonic oscillations present in modular cascaded multilevel converters. Current, voltage and power control are discussed in the paper while simulation results illustrate the operation of the hybrid MMC as a DC-AC converter in a typical inverter application and the additional functions and control of the embedded ESS.

Keywords: multilevel converters; modular multilevel converter (MMC); hybrid multilevel converters; energy storage

1. Introduction

The large growth in grid-connected renewable energy resources, experienced globally, has added to the existing challenges of maintaining a reliable and efficient electricity network. Energy storage systems (ESSs) provide a solution for balancing generation with consumption and addressing issues caused by the intermittency and variability of both wind and solar photo-voltaic (PV) systems at a central and distributed level [1–3]. The additional functions that can be provided by ESSs, including voltage support, frequency regulation, power quality and reliability services, mean that they will become more of a necessity than a "luxury" in the future power system.

Power electronics converters are an important element in the integration of ESSs to the networks. Currently, two- and three-level topologies are predominantly used in grid-connected ESSs [4]. However, as the power and energy levels of installed systems are expected to increase, multilevel topologies will become more competitive solutions. Distributed energy storage can also facilitate integration with renewable energy systems, such as PV converters. The main advantages of multilevel converters are their lower semiconductor losses, higher conversion efficiency, high quality output voltages and currents, as well as the potential for fault-tolerant operation [5].

In ESS applications, cascaded and modular multilevel solutions, such as the cascaded H-bridge converter (CHB) or the modular multilevel converter (MMC) [6], offer the additional advantage of reducing the size of the battery string, offering an improved configuration and the capacity for better

control of the state of charge (SoC) for each of these strings. Both of these topologies have attracted research interest over the last couple of years [7]. An evaluation between the two topologies [7–19] in terms of conversion efficiency shows that MMC-based solutions perform slightly better compared to the CHB counterparts [4]. However, the high semiconductor and capacitance requirements, as well as more complicated voltage and energy balancing of MMCs [8,9] make the CHB a more competitive and practical application in dedicated ESS applications [10,11].

A defining characteristic of MMC-based solutions, compared to the CHB ones, is that they provide, in addition to the lower voltage DC-links of the SMs, a high voltage DC-link terminal. This means that the MMC topology can be potentially used in systems that require a combination of DC-AC power flow with integrated energy storage. The operation of the MMC with SMs that could integrate batteries together with the required voltage control was demonstrated in [12,13], while [14] extended the concept of energy storage in MMCs for traction applications.

The addition of any kind of energy storage elements in the SMs of the MMC necessitates additional controllers for energy balancing between the SMs, the arms, phase-legs and ESS within the converter [15–17], as well as considerations for the SoC of the integrated batteries [18,19]. Operational aspects of MMC-based ESSs have also been investigated in the current literature, with [20] demonstrating the fault-ride through (FRT) capabilities of the converter and [21] investigating its fault-tolerant capacity and the limitations in real and reactive power capabilities with faulty or isolated ESS SMs. In the latter, the authors calculate a limit of 33% for faulty ESSs within the SMs of the MMC. In [22], it is demonstrated that the converter can operate at even higher power imbalances for ESS within the arms and between the phases of the converter without impacting the output waveforms, if internal imbalances can be tolerated.

Based on the above, the interest for converter configurations that enable ESS integration within the MMC is high. This paper proposes (i) a hybrid modular multilevel converter (HMMC) topology with reduced capacitor voltage ripple in certain SMs and (ii) an HMMC with partial embedded ESS and multi-directional power flow. The novelty of the proposed HMMC lies in the combination of a three-phase, three-level cell with multiple half-bridge SMs (HB-SM) per arm. The advantages of the proposed approach are the partial integration of energy storage to a typical MMC and the elimination of the second harmonic voltage ripple from the SM with the ESS. The required control and limitations of the proposed approach are also discussed, and simulation results are presented for the different operating modes of the converter.

The article is structured as follows: Section 2 presents the fundamental aspects of the MMC that directly relate to the proposed HMMC, and Section 3 introduces the circuit configuration, operational aspects and control of the proposed HMMC. The integration of ESS in some of the SMs of the proposed HMMC is presented in Section 4, and Section 5 shows the simulation results of both configurations. Finally, the conclusions of the work are summarised in Section 6.

2. Modular Multilevel Converter

The MMC (Figure 1a) offers a modular power electronics solution for medium and high-voltage applications, based on SMs that are the building blocks of the converter phase-legs. The most common SM configuration in the literature is that of the HB-SM (Figure 1b), but other configurations, including the full-bridge (FB-SM), single-clamped (SC-SM), flying-capacitor (FC-SM) and cross-connected SM (CC-SM) (Figure 1c–f) and their combinations, can be used [23].

The converter consists of N series-connected SMs in the arms that behave as controllable voltage sources that, considering the fictitious mid-point of the DC-link voltage as a reference, generate the voltages v_{ux} and v_{lx} across the phase-leg inductors of phase x, where $x \in [a, b, c]$. The inductors (L) enable the control of the currents within the upper and lower arms (i_{ux} and i_{lx}).

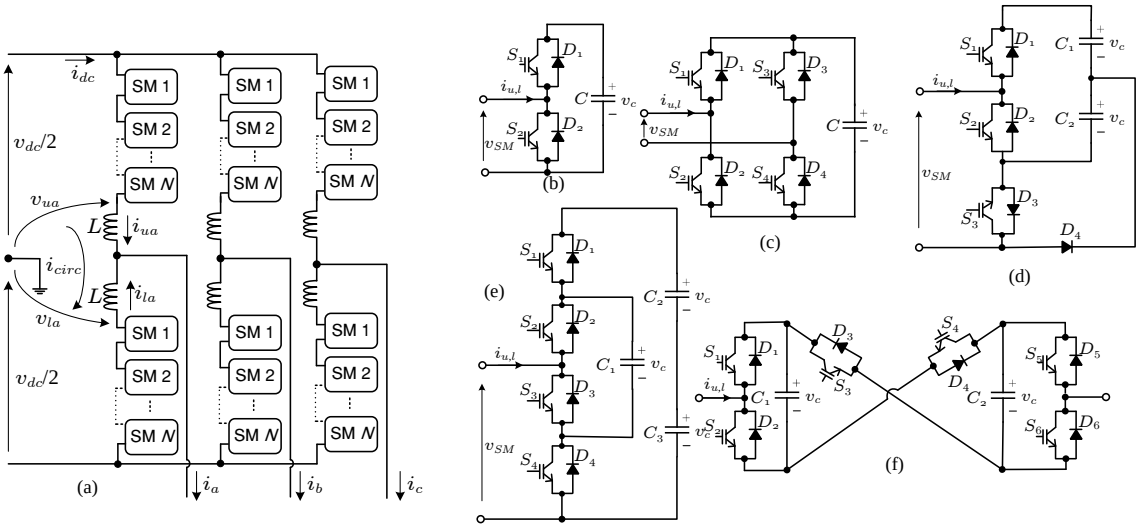

Figure 1. MMC: (**a**) Three-phase circuit configuration; (**b**) Half-bridge (HB)-SM; (**c**) Full-bridge (FB)-SM; (**d**) Single-clamped (SC)-SM; (**e**) Flying-capacitor (FC)-SM; (**f**) Cross-connected (CC)-SM.

Looking into one of the phase-legs of Figure 1a, i_{ux} and i_{lx} can be written as the sum of two distinct current components, the common-mode current (i_{comm}) that is equal to half of the total output current and the differential-mode or circulating current ($i_{circ,x}$) that circulates within the phase-leg of the converter, so that:

$$i_{ux} = i_{comm,x} + i_{circ,x} = \frac{i_x}{2} + i_{circ,x} \tag{1}$$

and:

$$i_{lx} = i_{comm,x} - i_{circ,x} = \frac{i_x}{2} - i_{circ,x} \tag{2}$$

The differential (or circulating) current will naturally include a second-order harmonic that can be eliminated in order to increase converter efficiency or defined so that it achieves additional control objectives, such as reducing the ripple in the SM capacitor voltages. The injection of higher order harmonics can also be used to improve the operation of the MMC [24].

The current that flows through the arms of the converter causes a variation in the SM capacitor voltages and is one of the defining characteristics for the sizing (in terms of capacitance, size and weight) of each individual SM. One of the main challenges with the MMC is the reduction of the required capacitance, and consequently the total energy, within the arms of the converter.

3. Hybrid Modular Multilevel Converter

Partial reduction of SM capacitance for one SM in each of the converter arms in a three-phase system can be achieved by connecting the individual DC-link voltages of the upper-most SM in the upper arm and the lower-most SM in the lower arm of the MMC as analysed in [25]. The common connection of the DC-link in the upper-most and lower-most SM transforms this particular set of SMs into a three-phase, two-level converter. As this connection can only be done for one SM per arm (extending to more is not possible due to short-circuits between SMs), it is apparent that the practical application and benefits of the method diminish with increasing number of SMs. Nonetheless, such concepts can be of interest in medium-voltage applications with a low number of SMs.

3.1. Circuit Configuration, Operation Principles and Model

In order to reduce the number of SMs that experience the relatively higher voltage ripple without impacting the number of output voltage levels, we propose the hybrid MMC of Figure 2. The topology comprises a three-phase, three-level flying capacitor (FC) converter for the upper and lower arms and

a number (N) of series-connected HB-SMs. The three-level FC substitutes two HB-SMs in each of the arms, requiring the same number of semiconductor devices, one common capacitor for the outer stage C_{fc} and a capacitor per-phase as the flying capacitors ($C_{fc,x}$).

Assuming N HB-SMs per arm, the number of levels generated by each arm with the additional two levels of the three-phase, three-level FC-SM is equal to $N + 3$. The total number of levels in the output of the converter is also equal to $N + 3$ if the SMs in the upper and lower arm switch concurrently or $2N + 5$ in the case of interleaved operation of the MMC [26].

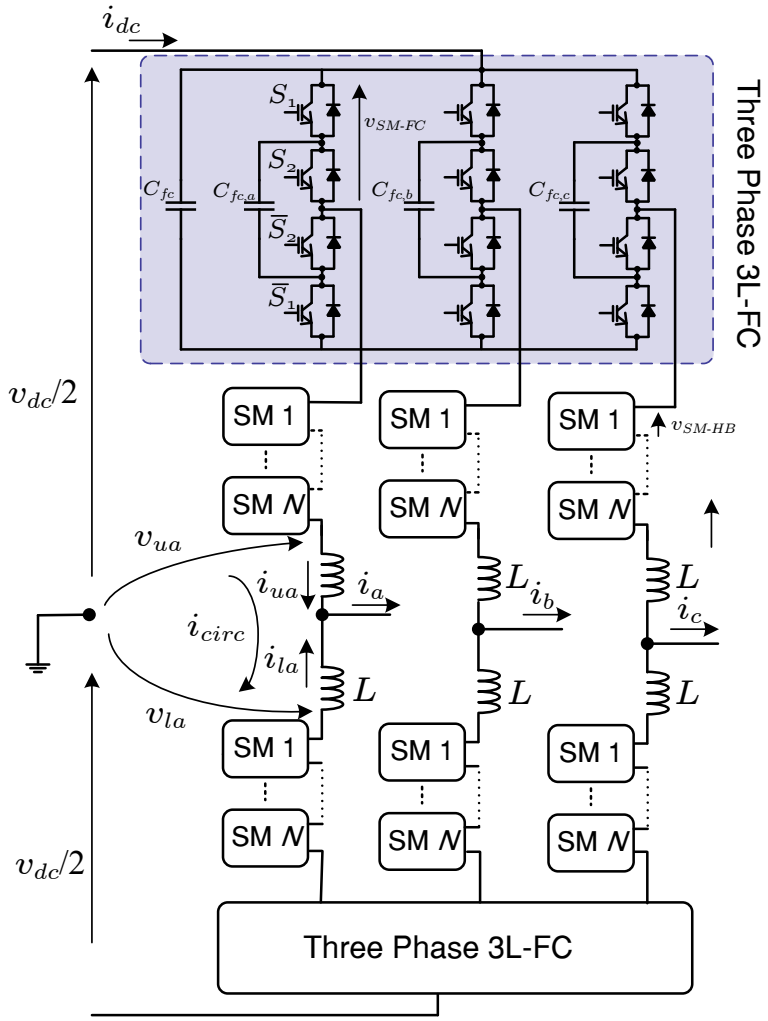

Figure 2. Proposed three-phase hybrid modular multilevel converter (MMC).

The operation of the HB-SMs in the proposed HMMC is identical to the typical MMC, while the three-level FC cell has four switching combinations that generate three different voltage levels in the output (v_{SM}). The switching states of the three-phase, three-level FC cell are given in Table 1.

Table 1. Switching states and output voltage of the three-level FC cell.

S_1	S_2	v_{SM-FC}
0	0	$2v_C$
0	1	v_C
1	0	v_C
1	1	0

A relative reduction in components is achieved, because fewer capacitors are required in the overall system. However, this is not the main objective of the proposed HMMC with benefits derived from the reduced capacitor voltage ripples. As the FC cell is connected across all three phases of the converter, the voltage oscillations cancel out between the three phases, reducing the voltage ripple to a minimum. Furthermore, the three-level FC converter offers redundant switching stages in generating the v_C voltage level, as shown in Table 1. These redundancies can be utilised in the proposed HMMC in order to maintain the voltages of capacitors $C_{fc,x}$ to the reference voltage by selecting the appropriate switching state depending on both the deviation of the capacitor voltage and the direction of the arm current.

The behaviour of the proposed HMMC as seen from the output remains similar to the standard MMC topology. The output voltage of the converter ranges in the $[-v_{DC}/2, +v_{DC}/2]$ interval, and the output voltage (v_x) and current (i_x) of phase x, $x \in \{a, b, c\}$ are given by:

$$v_x = \frac{V_{DC}}{2} v_{mx} = m_x \frac{V_{DC}}{2} \cos(\omega t) \tag{3}$$

$$i_x = \hat{I}_x \cos(\omega t + \phi) \tag{4}$$

where $v_{mx} = m_x cos(\omega t)$ represents the normalised reference signal ($v_{mx} \in [-1, 1]$) and m_x is the modulation index ($m_x \in [0, 1]$). The controllable voltages generated by the upper and lower arm are given by:

$$v_{ux} = \frac{V_{DC}}{2} - \sum_{j=1}^{N} s_{uj} v_c - s_{ufc} v_c \tag{5}$$

$$v_{lx} = \frac{-V_{DC}}{2} - \sum_{j=1}^{N} s_{lj} v_c - s_{lfc} v_c \tag{6}$$

where v_{SMfc} is the capacitor voltage of the SMs, $s_{uj} \in \{0, 1\}$ is the switching state of the HB-SMs and $s_{u,lfc} \in \{0, 1, 2\}$ is the switching state of the FC-cell. Based on Kirchoff's voltage law and (5) and (6), the equations for the upper and lower arm of phase x can be written as:

$$L \frac{di_{ux}}{dt} = v_{ux} - R i_{ux} - v_x \tag{7}$$

$$L \frac{di_{lx}}{dt} = -v_{lx} - R i_{lx} + v_x \tag{8}$$

By adding (7) and (8):

$$L \left[\frac{di_{ux}}{dt} + \frac{di_{lx}}{dt} \right] = v_{ux} - v_{lx} - R \left(i_{ux} + i_{lx} \right) \tag{9}$$

and as $i_x = i_{ux} + i_{lx}$, Equation (9) becomes:

$$L \frac{di_x}{dt} = v_{ux} - v_{lx} - R i_x \tag{10}$$

Substituting (5) and (6) in (10),

$$L \frac{di_x}{dt} = V_{DC} - \sum_{j=1}^{N} s_{ujx} v_c - s_{ufcx} v_c - \sum_{j=1}^{N} S_{ljx} v_c - s_{lfcx} v_c - R i_x \tag{11}$$

By subtracting (7) and (8):

$$L\left[\frac{di_{ux}}{dt}-\frac{di_{lx}}{dt}\right]=v_{ux}+v_{lx}-R\left(i_{ux}-i_{lx}\right)-2v_x \tag{12}$$

Defining the circulating current based on (1) and (2):

$$i_{circ,x}=\frac{i_{ux}-i_{lx}}{2} \tag{13}$$

Equation (12) can be re-written as:

$$L\frac{di_{circ,x}}{dt}=\frac{v_{ux}+v_{lx}}{2}-2Ri_{circ,x}-v_x \tag{14}$$

Now, by substituting (5) and (6) in (14):

$$L\frac{di_{circ,x}}{dt}=\frac{1}{2}\left[-\sum_{j=1}^{N}s_{ujx}v_c-s_{ufcx}v_c-\sum_{j=1}^{N}s_{ljx}v_c-s_{lfcx}v_c\right]-Ri_{circ,x}-v_x \tag{15}$$

Assuming that:

$$V_{cu}^{\Sigma}=\sum_{j=1}^{N}s_{uj}v_{cu}=Nv_{cu}m_u \tag{16}$$

and:

$$V_{cl}^{\Sigma}=\sum_{j=1}^{N}S_{lj}v_{cl}=Nv_{cl}m_l \tag{17}$$

where v_{cu} and v_{cl} are the averaged upper/lower voltage capacitor for one SM, (11)–(15) become:

$$L\frac{di_x}{dt}=V_{DC}-Nv_{cu}m_u-s_{ufc}v_c-Nv_{cl}m_l-s_{lfc}v_c-Ri_x \tag{18}$$

$$L\frac{di_{circ,x}}{dt}=\frac{1}{2}\left[Nv_{cu}m_u-s_{u,fc}v_c-Nv_{cl}m_l-s_{lfc}v_c\right]-Ri_{circ,x}-v_x \tag{19}$$

The SM capacitor charging/discharging is modelled by:

$$C_{SM}\frac{dv_{cu}}{dt}=m_ui_{ux}=m_u\left(i_{circ}+\frac{i_x}{2}\right) \tag{20}$$

for the upper SMs and

$$C_{SM}\frac{dv_{cl}}{dt}=m_li_{lx}=m_l\left(i_{circ}-\frac{i_x}{2}\right) \tag{21}$$

for the lower SMs.

The FC-SM voltage is given by:

$$v_{SM_{fc}}=2\left(1-m_{fc}\right)v_c \tag{22}$$

and the internal dynamics of the flying capacitors $C_{fc,x}$ described by [27]:

$$C_{fc,x}\frac{dv_{SM_{fc}}}{dt} = 2\left(1 - m_{ufc}\right) i_{ux} \tag{23}$$

$$C_{fc,x}\frac{dv_{SM_{fc}}}{dt} = 2\left(1 - m_{lfc}\right) i_{lx} \tag{24}$$

where m_{ufc} and m_{lfc} are the duty cycles corresponding to the FC-SM of the upper and the lower arms. The dynamics of the common capacitor in the three-phase FC C_{fc} are defined by the currents in the upper and lower arms of all three phases as $i_{C_{fc}} = i_{DC} - s_{1a}i_u a - s_{1b}i_u b - s_{1c}i_u c \approx 0$, so the dynamics of capacitor C_{fc} can be omitted in an averaged model.

Summarizing the prior analysis, the HMMC averaged model can be described by the following equations:

$$L\frac{di_x}{dt} = V_{DC} - Nv_{cux}m_{ux} - 2\left(1 - m_{ufcx}\right) v_{cux} - Nv_{cl}m_{lx} - 2\left(1 - m_{lfcx}\right) v_{clx} - Ri_x \tag{25}$$

$$L\frac{di_{circ,x}}{dt} = \frac{1}{2}\left[Nv_{cux}m_{ux} - 2\left(1 - m_{ufcx}\right) v_{cux} - Nv_{clx}m_{lx} - 2\left(1 - m_{lfcx}\right) v_{clx}\right] - Ri_{circ,x} - v_x \tag{26}$$

$$L\frac{di_{circ,x}}{dt} = \frac{1}{2}\left[Nv_{cux}m_{ux} - m_{ufcx}v_{SM_{fc}} - Nv_{clx}m_{lx} - m_{lfcx}v_{SM_{fc}}\right] - Ri_{circ,x} - v_x \tag{27}$$

$$C_{SM}\frac{dv_{cux}}{dt} = m_{ux}i_{ux} = m_{ux}\left(i_{circ,x} + \frac{i_x}{2}\right) \tag{28}$$

$$C_{SM}\frac{dv_{clx}}{dt} = m_{lx}i_{lx} = m_{lx}\left(i_{circ,x} - \frac{i_x}{2}\right) \tag{29}$$

$$C_{fc,x}\frac{dv_{fc,x}}{dt} = 2\left(1 - m_{ufcx}\right) i_{ux} \tag{30}$$

$$C_{fc,x}\frac{dv_{fc,x}}{dt} = 2\left(1 - m_{lfcx}\right) i_{lx} \tag{31}$$

The first equation models the output current dynamics, while the remaining equations represent the internal dynamics of the HMMC. The state variables are $\mathbf{x} = \left[i_x\ i_{circ,x}\ v_{cux}\ v_{clx}\ v_{fc,x}\ \ v_{fc,x}\right]$; the control input variables $\left[m_{ux}\ m_{lx}\ m_{ufcx}\ m_{lfcx}\right]$ and $[v_{DC}\ v_x]$ are considered as the perturbations of the system.

3.2. Circulating Current Control and Voltage Balancing

It was analysed in the previous section that it is necessary to control the circulating current of the MMC and eliminate the higher order harmonic components that are naturally present in i_{circ}. The behaviour of the HMMC, with the exception of the voltage balancing for the FC-SM, is similar to the MMC, as analysed in Section 2. Control of the circulating current (i_{circ}) is achieved by modifying the upper and lower arm references (usually by adding and subtracting a reference voltage from an appropriate controller) in order to achieve the control objectives. This results in a variation of the voltages v_{ux} and v_{lx} that controls the current through the inductors L.

As control of the circulating current is a higher-level objective for the operation of the MMC and does not have a direct impact to the generation of the switching signals for the SMs, most of the current

controllers that have been proposed for the MMC can be readily applied to the proposed HMMC. In the current work, a proportional-resonant controller with a DC-current reference [28] has been implemented. The circulating current controller is shown in Figure 3.

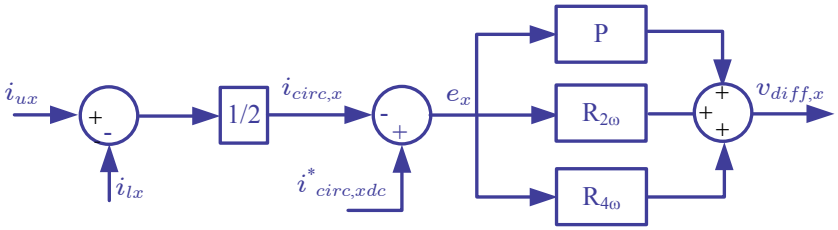

Figure 3. Circulating current controller implementation.

A second requirement for the operation of the MMC is balancing of the SM capacitor voltages, which can be implemented either with the use of sorting algorithms or by making use of the natural balancing property of phase-shifted pulse-width modulation (PS-PWM). In the case of the proposed HMMC, the capacitors of the FC SM will exhibit significantly lower voltage oscillations requiring modifications to the existing sorting algorithms. On the other hand, PS-PWM can be implemented directly if individual reference signals are generated for each of the SMs, including the FC-cell, compensating appropriately for the voltage imbalances between the measured SM capacitor voltage ($v_{Cu,j}$) and the SM capacitor reference voltage ($v_{C,ref}$). The additional balancing component is multiplied with the sign of the arm current $sgn\{i_{ux}\}$ so that the SM capacitor voltages are regulated towards the reference depending on the direction and amplitude of the arm current. The combined voltage balancing and modulation stage of the converter, based on PS-PWM (Figure 4a), is shown in Figure 4b.

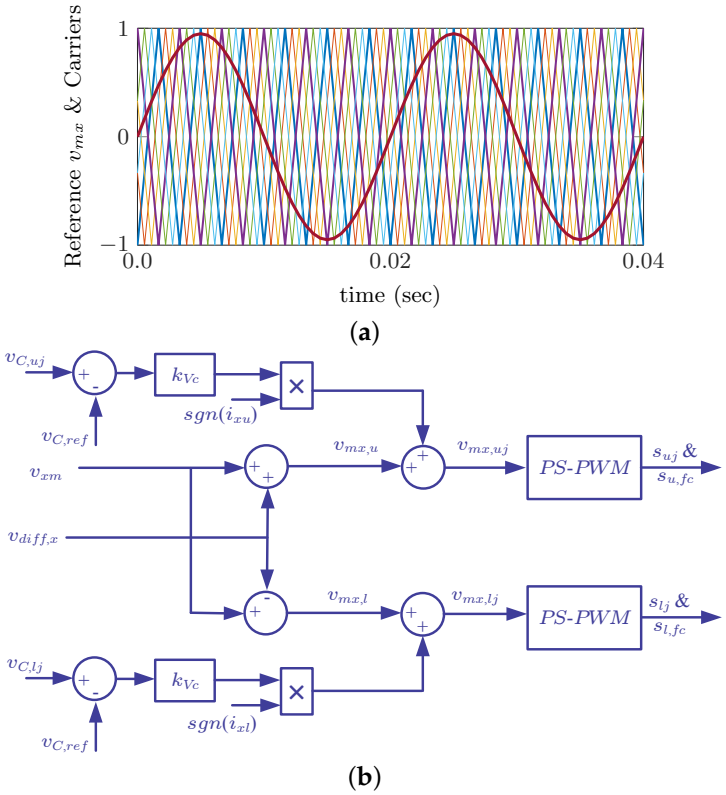

Figure 4. Modulation of the proposed hybrid modular multilevel converter (HMMC): (**a**) phase-shifted (PS)-PWM carriers and reference signal ($v_{mx,uj}$); (**b**) Generation of the references and switching signals.

4. Hybrid Modular Multilevel Converter (HMMC) with Embedded Energy Storage

ESS can be directly connected to the DC-side of the SMs in the MMC and the proposed HMMC. However, the SM capacitor voltage ripple appears directly across the ESS, and the low order harmonic oscillations have a detrimental effect to the lifetime and reliability of the ESS, while the SM voltage is directly linked to the SoC of its ESS. It is, therefore, preferable to use a DC-DC converter as an interface between the ESS and the SM capacitors.

4.1. Circuit Configuration

The DC-DC stage present between the ESS and the SM capacitors in MMC-based converters should operate in a manner so that the voltage at the ESS side is kept constant and without low-order harmonics. This task is simplified if the ESS is connected to the three-level FC-SM, as the voltage of the capacitor does not have low-order oscillations. Integration of the ESS in the proposed HMMC is shown in Figure 5a, with a bidirectional boost converter used at the DC-DC stage of the topology. This stage is also drawn with two devices in series, as that part of the circuit needs to withstand double the voltage of the devices in the FC-SM. Various other configurations can be used [12], including high-ratio boost DC-DC converters, interleaved (Figure 5b) and multilevel DC-DC converters. In the case that isolation between the ESS and the SMs is required, the dual-active bridge (DAB) of Figure 5c with a high-frequency transformer stage can also be utilised.

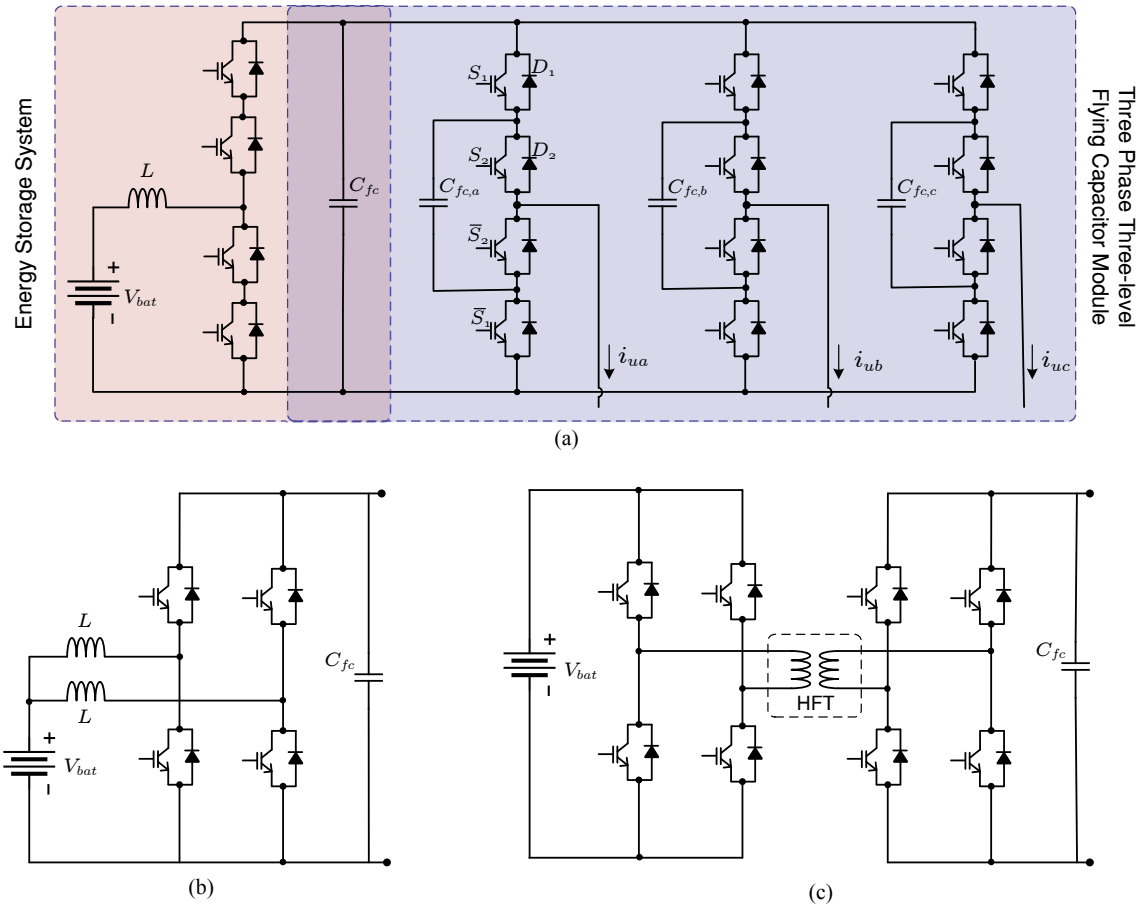

Figure 5. (**a**) FC-SM with embedded energy storage; (**b**) interleaved DC-DC stage; (**c**) isolated DC-DC stage based on the dual-active bridge (DAB) converter.

With the configurations of Figure 5, one ESS, common between the three phases of the converter, can be connected at each arm of the HMMC. An additional advantage of the configuration is that the SoC is common between the three phases, simplifying the energy balancing and control of the system.

The possible operating modes of the HMMC with the partial embedded ESS are: (i) DC to AC mode and vice versa; (ii) DC to ESS and AC mode; (iii) DC and ESS to AC mode; (iv) AC to DC and ESS mode; and (v) AC and ESS to DC mode. The first mode represents a typical DC-AC converter operation as analysed in Section 3; however, in the remaining modes of operation, additional controllers are required in order to achieve simultaneous energy balancing between all of the SMs. These modes are illustrated in Figure 6. As ESS is not included in any of the remaining HB-SMs, power flow solely from the ESS to the AC system (such as the case of a dedicated ESS converter) is not possible with the partial ESS configuration, as the converter cannot generate sufficiently high voltage at the AC terminals.

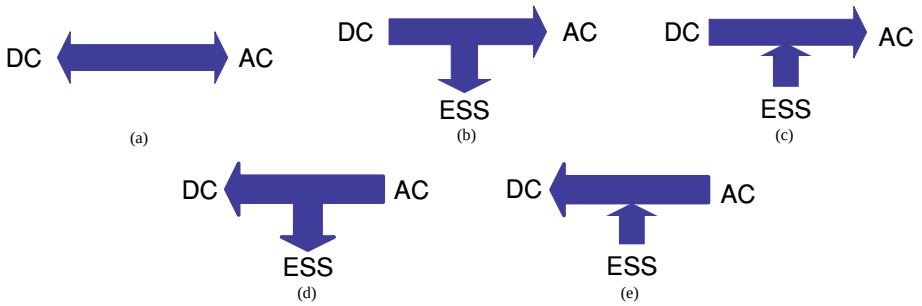

Figure 6. Power flow modes of the proposed hybrid modular multilevel converter (HMMC): (**a**) DC to AC mode and vice versa; (**b**) DC to the energy storage system (ESS) and AC mode; (**c**) DC and ESS to AC mode; (**d**) AC to DC and ESS mode; and (**e**) AC and ESS to DC mode.

4.2. Power and Energy Balancing

In the case of the proposed HMMC and other topologies with partially-embedded ESS, the circulating current cannot be used to directly control the power and energy balance between the DC-, the AC-side and the ESS. The active power injection from the FC-SM DC-side will introduce an imbalance with non-ESS SMs. In order to achieve the required voltage balancing, the reference signal of the FCSM with the embedded ESS is modified to compensate for the power flow in or out of the ESS. This means that the conduction period of the FCSM increases or decreases based on whether the ESS is charging or discharging, while the currents within the arms remain the same. The current of the ESS ($i_{bat,meas}$) is used in the control of both the DC-DC converter stage, as well as the voltage balancing of the HMMC, as shown in Figure 7.

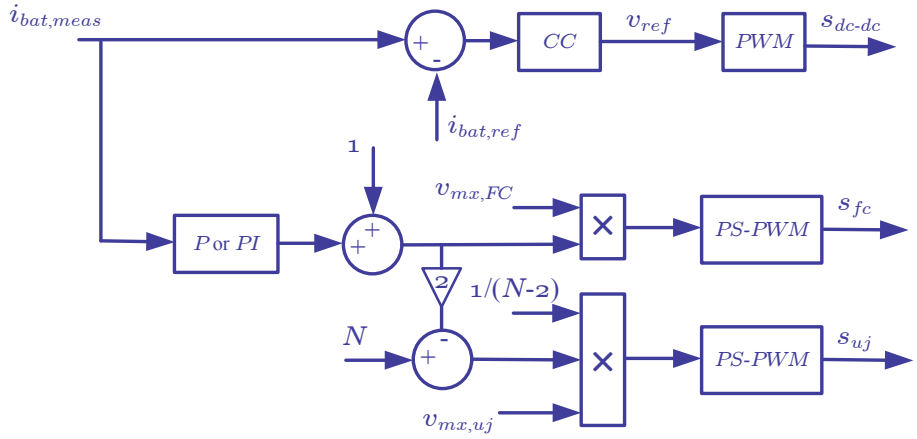

Figure 7. Energy control for the HMMC with embedded ESS.

The variation of the conduction interval for the FCSM means that the voltage generated by the HMMC arm is no longer equal to the reference. In order to compensate for the imbalance, the references of the remaining SMs need to be appropriately scaled, as well, avoiding a distortion of the output waveforms (Figure 7). This requirement sets some additional limitations on the proposed converter, as the maximum power that can be extracted out of the ESS is a function of the operating point of the converter, so that none of the references saturate.

5. Results

In order to demonstrate the operation of the converter, three different sets of simulation results are provided, one for the typical DC-AC converter operation and two with the partial embedded ESS in both charging and discharging modes supplying an *RL* load. The simulated converter consists of one three-level FC-SM and four HB-SMs per arm, generating a seven-level output voltage. The parameters of the simulation are given in Table 2.

Table 2. Parameters of the simulation.

Parameter	Value
Number of HB-SMs, N	4
DC-link voltage, V_{DC}	6000 V
HB-SM Capacitor Voltage, $V_{C,HB}$	1000 V
Arm Inductors, L	9 mH
SM Capacitors, C	3.6 mF
Load Resistance, R_{load}	20 Ω
Load Inductance, L_{load}	10 mH
ESS Voltage, V_{bat}	600 V
Carrier Frequency, f_{car}	550 Hz
Modulation Index, m_a	0.8

5.1. DC-AC Converter Operation

When there is no power exchange between the ESS and the HMMC, the converter operates as a typical MMC-like converter. The seven-level output voltages and corresponding load currents are shown in Figure 8a,b, respectively. As expected, the multilevel output of the converter provides high quality output currents with a total harmonic distortion (%THD) of approximately 2.6%. The capacitor voltage of the HB-SMs are regulated to the reference voltage, while the voltages of the FC-SM capacitors exhibit a very small voltage ripple, as shown in Figure 8c. The higher order harmonics are eliminated from the circulating current, which only has a DC component (Figure 8d).

To further illustrate the major difference of the proposed HMMC compared to a standard MMC, Figure 9a shows the voltage of the internal capacitor of the FC-SM compared to the voltage of a normal HB-SM, demonstrating the elimination of the fundamental frequency harmonic ripple in the FC-SM. Assuming a maximum of 10% ripple on each SM capacitor voltage, Figure 9b shows the average SM voltage ripple across all SMs as the number of SMs increases. It becomes apparent that the advantages of the proposed HMMC are more apparent for a low number of SMs with the average SM voltage ripple converging towards that of the MMC as the number of HB-SMs increases.

Figure 10 shows the low-order harmonics of the SM capacitor voltage for the FC-SM and the HB-SM of the proposed HMMC. The capacitors within the three-phase, three-level FC-SM do not have any low-order harmonic ripple, while the HB-SM have both a fundamental and a second-order harmonic ripple in their capacitor voltages as a result of the current (Figure 8d) that flows through the arm and contains a fundamental frequency component and the fundamental frequency switching function of the SM.

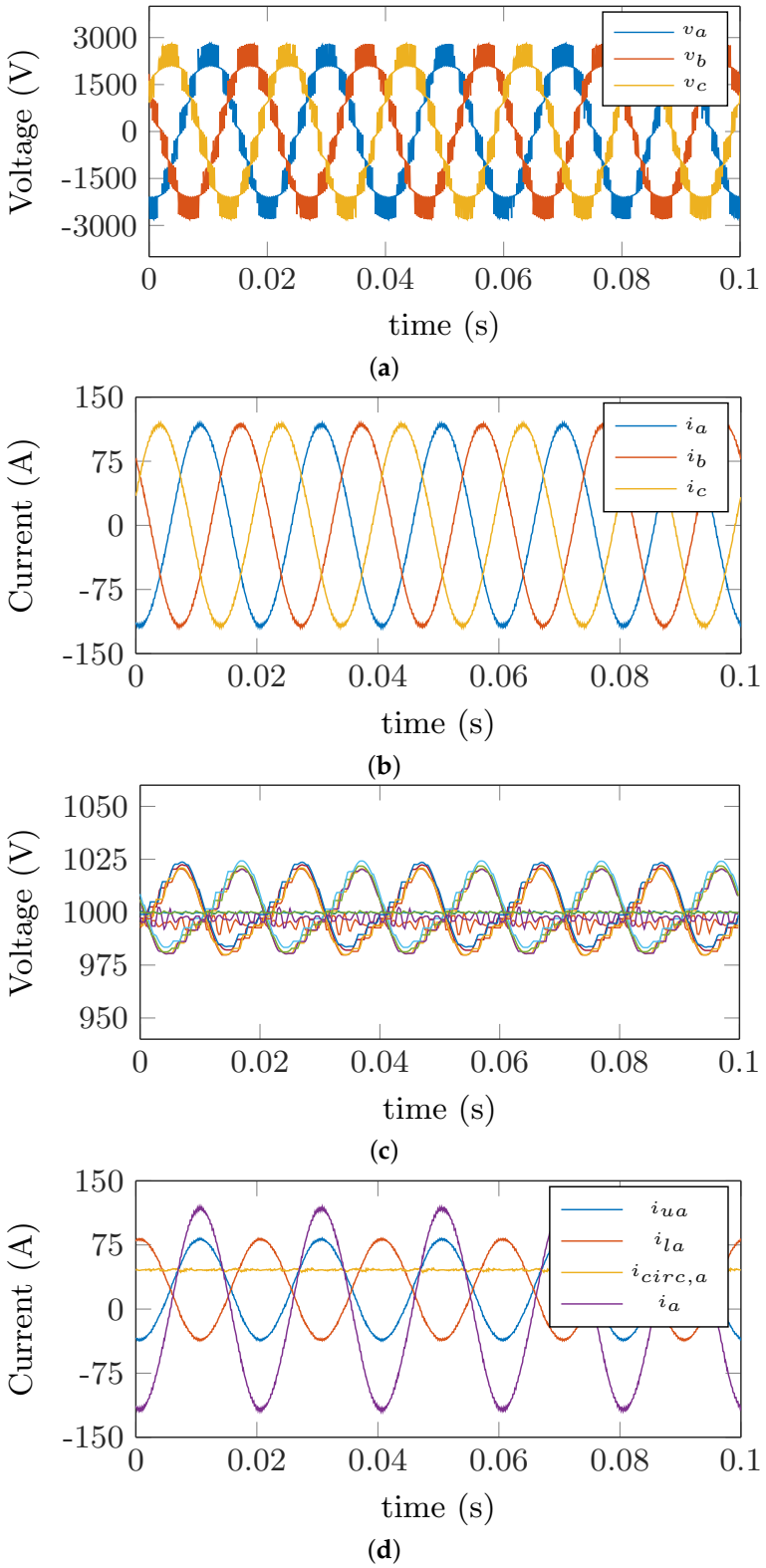

Figure 8. Output waveforms under Mode *i*: (**a**) three-phase load voltages; (**b**) three-phase load currents; (**c**) SM capacitor voltages of Phase A; (**d**) load, circulating and arm currents of Phase A.

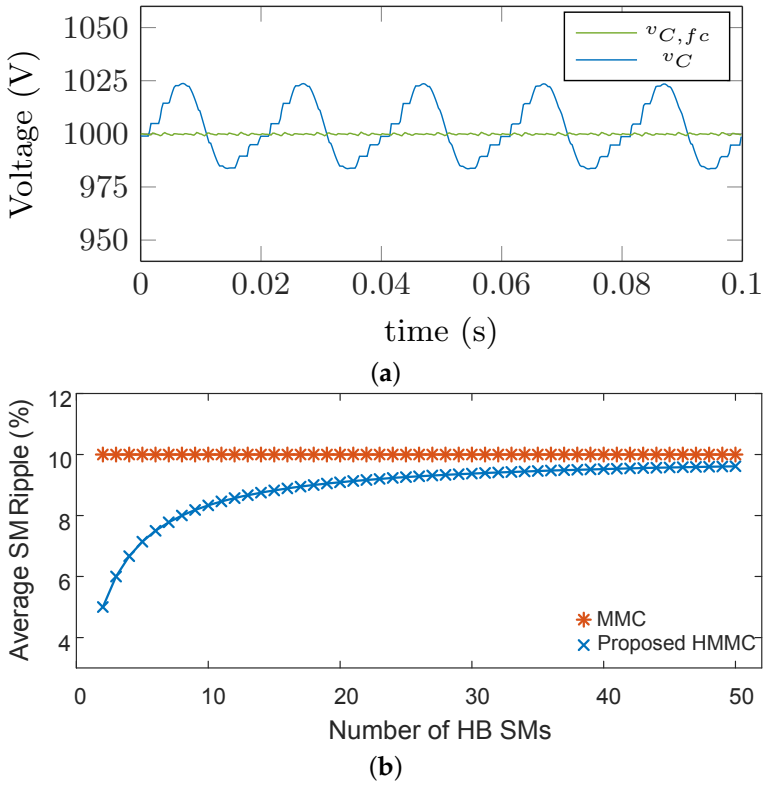

Figure 9. (**a**) Comparison of FC-SM capacitor voltage and (**b**) HB-SM capacitor voltage in the HMMC.

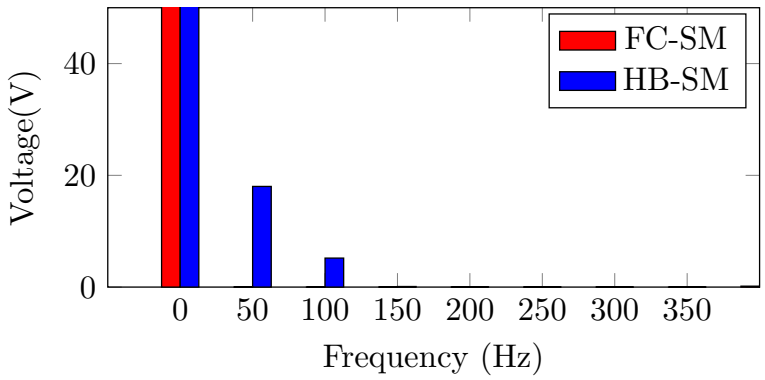

Figure 10. Harmonic spectra of the FC and HB-SM capacitor voltages.

5.2. Embedded ESS

Charging and discharging of the ESS is regulated from the DC-DC controller that acts as an interface between the ESS and the capacitor of the FC-SM. The voltage of the capacitor does not exhibit any significant ripple, and there is no need for the second harmonic ripple to be compensated by the DC-DC converter. This is not the case when ESSs are connected to HB-SMs individually per-phase.

Figure 11a,c shows the instantaneous and average power flow into the ESS that is connected to the FC-SM when the ESS is charging (Figure 11a) or discharging (Figure 11c). These results correspond to the power flow from the ESS connected to the FC-SM of the upper arms, while the same reference is used for the ESS in the lower arms. Extraction of unequal power out of the upper and lower ESS is outside of the scope of this paper and left for future work. The reference signals for the SMs of the upper arm of phase *a* when the ESS is charging and discharging are given in Figure 11b,d, respectively.

The conduction time of the FC-SM is adjusted accordingly to compensate for the additional power flow from the ESS in order to maintain the voltage balancing of the FC and HB SMs.

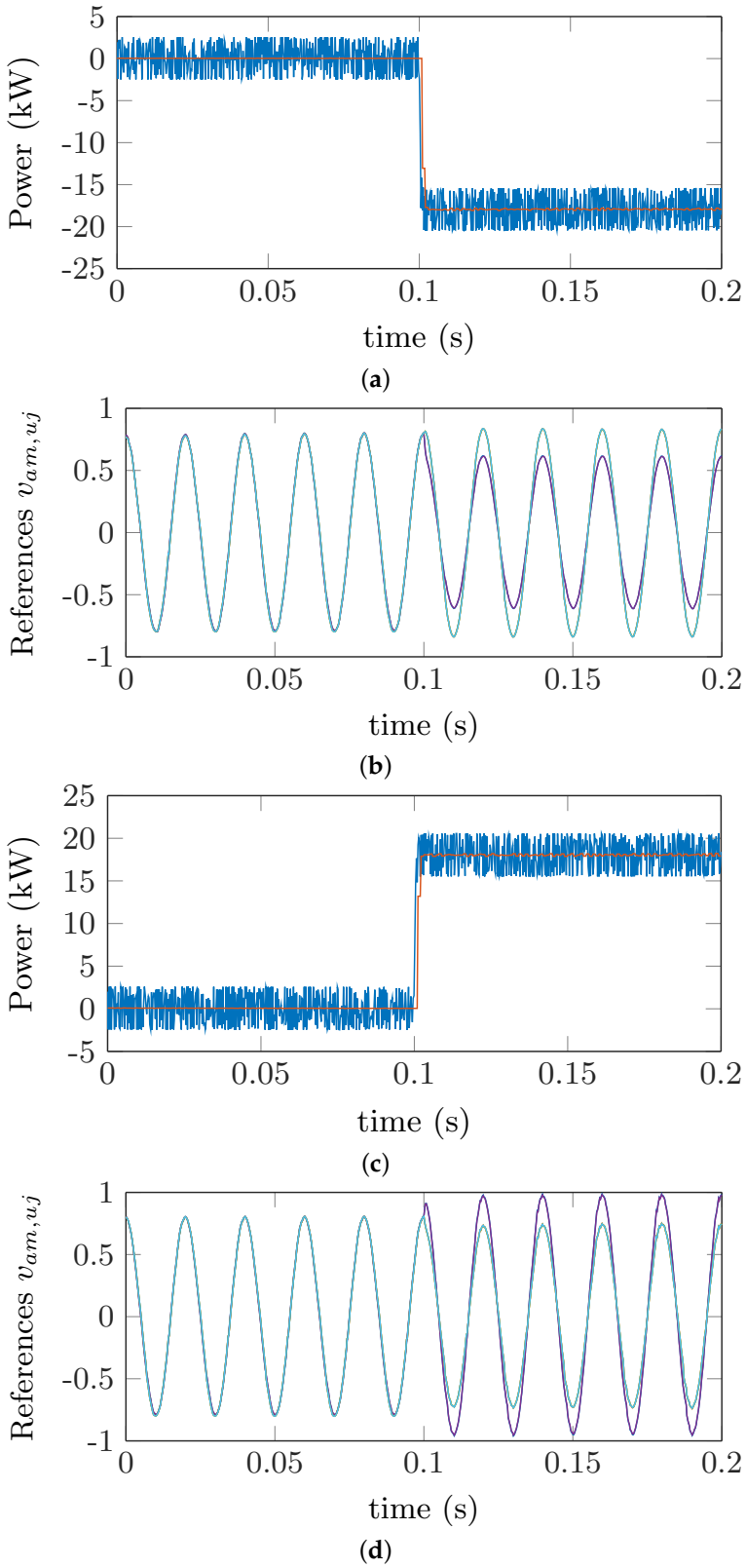

Figure 11. (**a**) Power flow during ESS charging; (**b**) reference signals; (**c**) power flow during ESS discharging; (**d**) reference signals.

The variation in the reference signals, as shown in Figure 11b,d, has a small effect on the output voltage harmonics; however, this effect is negligible due to the relatively large number of levels the HMMC is capable of generating. Figure 12a,b shows the load voltages generated by the converter when the ESS is charging and discharging, respectively. Similarly, the load currents are shown in Figure 12c,d. The %THD of the load currents is approximately 2.6%.

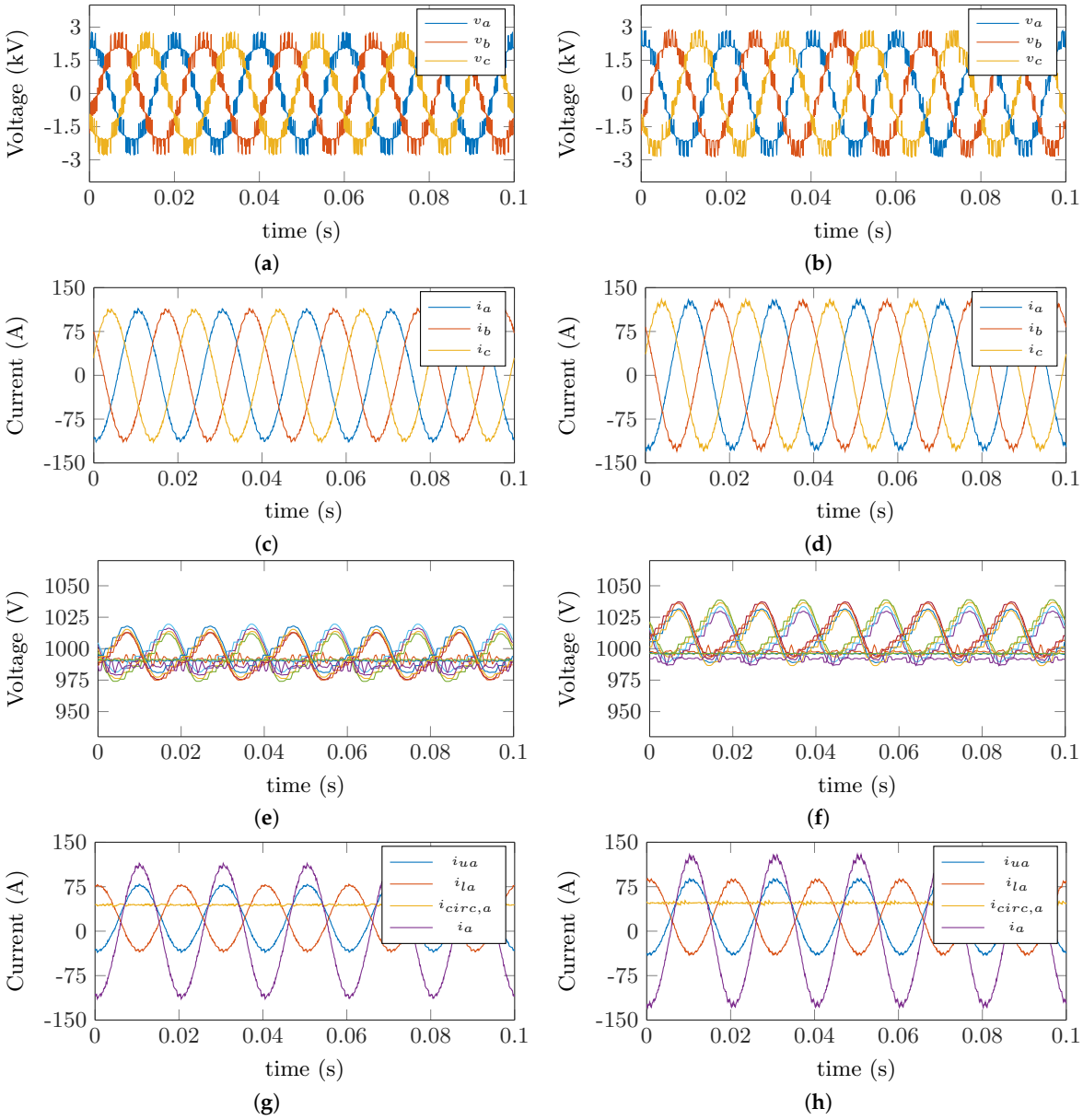

Figure 12. Output waveforms: (**a**) load voltages during ESS charging; (**b**) load voltages during ESS discharging; (**c**) load currents during ESS charging; (**d**) load currents during ESS discharging; (**e**) SM capacitor voltages during ESS charging; (**f**) SM capacitor voltages during ESS discharging; (**g**) load, circulating and arm currents during ESS charging; (**h**) load, circulating and arm currents during ESS discharging.

The capacitor voltages of the FC and HB-SMs of the HMMC are shown in Figure 12e,f. The voltage of the FC-SM that the ESS is connected to is regulated from the controllers that perform the energy and voltage balancing tasks of the MMC. This leads to a decoupling between the control of the FC-SM and the ESS; however, the different time constants of the two controllers need to be taken into consideration.

The DC component of the circulating current can be used to control the power flow from the DC to the AC side and vice versa, while the presence of the ESS does not have an effect in eliminating the higher order harmonics of i_{circ}. As can be seen from Figure 12g,h, the circulating current only contains a DC component with all of the higher order harmonics not present. Similarly to the MMC with or without ESS, injection of higher-order harmonics can be used to achieve additional control functions.

6. Conclusions

This paper proposed an hybrid modular multilevel converter (HMMC) as a combination of a three-phase FC-SM with single-phase HB-SMs. The main advantages of the proposed HMMC are the elimination of low-frequency voltage ripple in the capacitors of the FC-SM without introducing any further complexity into the circuit. This reduces the overall energy variation within the arms of the converter, compared to a typical MMC with HB-SMs for the same number of output voltage levels. As the three-phase configurations can only be used in the uppermost and lowermost location in the upper and lower arm, respectively, the proposed HMMC is well suited in applications with a relatively low number of SMs per arm.

The proposed HMMC is then extended to include a common energy storage element within the three-phase FC-SM. It is shown that the converter can provide multi-directional power flows from and to the DC-side, AC-side and ESS. The placement of the ESS within the three-phase FC-SM means that the DC-DC converter that interfaces with the ESS with the SM does not experience low-order voltage ripple. The power flow from and to the ESS is regulated from the DC-DC converter, while energy and power balancing within the arms is handled from the HMMC controllers. However, due to the partial embedded ESS in the converter, the operation of the HMMC without the DC-side (as an ESS system supporting the AC network) is not possible.

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Author Contributions: Georgios Konstantinou developed the HMMC topology and the simulation models with input from Josep Pou on the partial integration of energy storage and Salvador Ceballos, Daniel Pagano developed the mathematical models for the converter and contributed to the control algorithms. Georgios Konstantinou wrote the article with input from all the authors.

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References

1. Hill, C.A.; Such, M.C.; Chen, D.; Gonzalez, J.; Grady, W.M. Battery Energy Storage for Enabling Integration of Distributed Solar Power Generation. *IEEE Trans. Smart Grid* **2012**, *3*, 850–857.
2. Carbone, R. PV plants with distributed MPPT founded on batteries. *Sol. Energy* **2015**, *122*, 910–923.
3. Carbone, R. Grid-connected photovoltaic systems with energy storage. In Proceedings of the 2009 International Conference on Clean Electrical Power, Capri, Italy, 9–11 June 2009.
4. Wang, G.; Konstantinou, G.; Townsend, C.D.; Pou, J.; Vazquez, S.; Demetriades, G.D.; Agelidis, V.G. A review of power electronics for grid connection of utility-scale battery energy storage systems. *IEEE Trans. Sustain. Energy* **2016**, *7*, 1778–1790.
5. Kouro, S.; Malinowski, M.; Gopakumar, K.; Pou, J.; Franquelo, L.G.; Wu, B.; Rodriguez, J.; Perez, M.A.; Leon, J.I. Recent advances and industrial applications of multilevel converters. *IEEE Trans. Ind. Electron.* **2010**, *57*, 2553–2580.
6. Akagi, H. Classification, terminology, and application of the modular multilevel cascade converter (MMCC). *IEEE Trans. Power Electron.* **2011**, *26*, 3119–3130.
7. Soong, T.; Lehn, P.W. Evaluation of emerging modular multilevel converters for BESS applications. *IEEE Trans. Power Deliv.* **2014**, *29*, 2086–2094.
8. Baruschka, L.; Mertens, A. Comparison of cascaded h-bridge and modular multilevel converters for BESS application. In Proceedings of the 2011 IEEE Energy Conversion Congress and Exposition, Phoenix, AZ, USA, 17–22 September 2011.

9. Hillers, A.; Stojadinovic, M.; Biela, J. Systematic comparison of modular multilevel converter topologies for battery energy storage systems based on split batteries. In Proceedings of the 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, Switzerland, 8–10 September 2015.
10. Kawakami, N.; Ota, S.; Kon, H.; Konno, S.; Akagi, H.; Kobayashi, H.; Okada, N. Development of a 500-kW modular multilevel cascade convertor for battery energy storage systems. In Proceedings of the 2013 IEEE Energy Conversion Congress and Exposition, Denver, CO, USA, 15–19 September 2013.
11. Ota, J.I.Y.; Sato, T.; Akagi, H. Enhancement of performance, availability, and flexibility of a battery energy storage system based on a modular multilevel cascaded converter (MMCC-SSBC). *IEEE Trans. Power Electron.* **2016**, *31*, 2791–2799.
12. Trintis, I.; Munk-Nielsen, S.; Teodorescu, R. A new modular multilevel converter with integrated energy storage. In Proceedings of the IECON 2011—37th Annual Conference on IEEE Industrial Electronics Society, Melbourne, Australia, 7–10 November 2011.
13. Schroeder, M.; Jaeger, J. The idea of a modular multilevel converter with integrated batteries. In Proceedings of the 2012 International Conference on Smart Grid Technology, Economics and Policies (SG-TEP), Nuremberg, Germany, 3–4 December 2012.
14. Coppola, M.; Pizzo, A.D.; Iannuzzi, D. A power traction converter based on modular multilevel architecture integrated with energy storage devices. In Proceedings of the 2012 Electrical Systems for Aircraft, Railway and Ship Propulsion (ESARS), Bologna, Italy, 16–18 October 2012.
15. Schroeder, M.; Henninger, S.; Jaeger, J.; Rasic, A.; Rubenbauer, H.; Leu, H. Integration of batteries into a modular multilevel converter. In Proceedings of the 2013 15th European Conference on Power Electronics and Applications (EPE), Lille, France, 2–6 September 2013.
16. Lachichi, A. Modular multilevel converters with integrated batteries energy storage. In Proceedings of the 2014 International Conference on Renewable Energy Research and Application (ICRERA), Milwaukee, WI, USA, 19–22 October 2014.
17. Lachichi, A. On modular multilevel converters-based batteries energy storage systems. In Proceedings of the 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney, Australia, 9–12 June 2015.
18. Gao, F.; Zhang, L.; Zhou, Q.; Chen, M.; Xu, T.; Hu, S. State-of-charge balancing control strategy of battery energy storage system based on modular multilevel converter. In Proceedings of the 2014 IEEE Energy Conversion Congress and Exposition (ECCE), Pittsburgh, PA, USA, 14–18 September 2014.
19. Vasiladiotis, M.; Rufer, A. Analysis and control of modular multilevel converters with integrated battery energy storage. *IEEE Trans. Power Electron.* **2015**, *30*, 163–175.
20. Hillers, A.; Biela, J. Low-voltage fault ride through of the modular multilevel converter in a battery energy storage system connected directly to the medium voltage grid. In Proceedings of the 2014 16th European Conference on Power Electronics and Applications (EPE'14-ECCE Europe), Lappeenranta, Finland, 26–28 August 2014.
21. Soong, T.; Lehn, P.W. Assessment of fault tolerance in modular multilevel converters with integrated energy storage. *IEEE Trans. Power Electron.* **2016**, *31*, 4085–4095.
22. Schroeder, M.; Schmitt, S.; Henninger, S.; Jaeger, J. Measurement results of a modular energy storage system unevenly equipped with lithium-ion batteries. In Proceedings of the 2015 17th European Conference on Power Electronics and Applications (EPE'15 ECCE-Europe), Geneva, Switzerland, 8–10 September 2015.
23. Konstantinou, G.; Zhang, J.; Ceballos, S.; Pou, J.; Agelidis, V.G. Comparison and evaluation of sub-module configurations in modular multilevel converters. In Proceedings of the 2015 IEEE 11th International Conference on Power Electronics and Drive Systems, Sydney, Australia, 9–12 June 2015; pp. 958–963.
24. Pou, J.; Ceballos, S.; Konstantinou, G.; Agelidis, V.G.; Picas, R.; Zaragoza, J. Circulating current injection methods based on instantaneous information for the modular multilevel converter. *IEEE Trans. Ind. Electron.* **2015**, *62*, 777–788.
25. Li, B.; Zhang, Y.; Wang, G.; Sun, W.; Xu, D.; Wang, W. A modified modular multilevel converter with reduced capacitor voltage fluctuation. *IEEE Trans. Ind. Electron.* **2015**, *62*, 6108–6119.
26. Konstantinou, G.; Ciobotaru, M.; Agelidis, V. Selective harmonic elimination pulse-width modulation of modular multilevel converters. *IET Power Electron.* **2013**, *6*, 96–107.

27. McGrath, B.P.; Holmes, D.G. Analytical determination of the capacitor voltage balancing dynamics for three-phase flying capacitor converters. *IEEE Trans. Ind. Appl.* **2009**, *45*, 1425–1433.
28. Darus, R.; Pou, J.; Konstantinou, G.; Ceballos, S.; Agelidis, V.G. Controllers for eliminating the ac components in the circulating current of modular multilevel converters. *IET Power Electron.* **2016**, *9*, 1–8.