Energies **2015**, *8*, 1273-1290; doi:10.3390/en8021273

OPEN ACCESS

energies

ISSN 1996-1073

www.mdpi.com/journal/energies

Article

Single DC-Sourced 9-level DC/AC Topology as Transformerless Power Interface for Renewable Sources

Juan R. Rodriguez-Rodríguez *, Vicente Venegas-Rebollar and Edgar L. Moreno-Goytia

Instituto Tecnológico de Morelia, Morelia 58120, Mexico;
E-Mails: vvenegasr@itmoreli.edu.mx (V.V.-R.); elmoreno@elec.itmorelia.edu.mx (E.L.M.-G.)

***** Author to whom correspondence should be addressed; E-Mail: jr_386@hotmail.com;
Tel.: +52-443-266-6101.

Academic Editor: Frede Blaabjerg

Received: 14 December 2014 / Accepted: 23 January 2015 / Published: 5 February 2015

Abstract: This paper introduces an advanced transformerless multilevel hybrid-conversion topology intended for the interconnection of renewable DC sources at small-scale. The most important contribution presented in this paper is the generation of two isolated DC sources from a single DC source without the use of any type of transformer. The DC sources feed a nine-level DC/AC hybrid cascade multilevel converter. This advanced topology is achieved by redesigning the conventional DC/DC Buck topology, attached to the multilevel converter, and embedding a suitable switching strategy along with a Field Programmable Gate Array (FPGA)-based control. The advantages of the proposed structure, when compared to other proposals in the literature, are higher efficiency, reduced number of power switches, and high power density derived of transformerless characteristic. As a way to highlight differences and advantages of this converter over other options recently available in the literature, this paper carries out a quantitative evaluation comparing the number of voltage levels and the number of elements involved in the structure of DC/AC multilevel converters. The mathematical model and control strategy of the converter are explained and analyzed by means of simulations. Finally experimental results, obtained from a laboratory-scale prototype, show the performance of the system and demonstrate its relative advantages.

Keywords: multilevel converters; buck converter; cascaded cells; transformerless; micro-grids; FPGA control

---

1. Introduction

Today, the power electronics converters are one of the essential elements for electrical energy transformation and interconnection of renewable DC power sources to today's electrical power grids.

On the pursuit of modernization of distribution networks, the participation of novel power-electronics technologies is required. These technologies, mainly based on DC/AC topologies, require continuous improvements in features, such as higher efficiency, higher power density, controllability and reduction of total voltage and current harmonic distortion [1]. These features can be met by the implementation of DC/AC multilevel converters.

The multilevel converters have gained widespread acceptance for medium and high voltage applications [2]. The main advantages of DC/AC multilevel converters are: (i) low harmonic distortion at the output voltage; (ii) low voltage stress on their switching devices; and (iii) operation at low switching frequencies [3]. The multilevel converters were initially engaged in high voltage grids and power train applications but afterwards these were included in renewable energy converters as part of utility-scale plants, in which they are still largely employed [4,5].

In small scale, or residential applications, there are several well-known disadvantages regarding the use of transformers for DC/AC converters such as: size, weight and frequency limitation. Due these limiting factors, there is a growing interest in developing cutting-edge efficient and flexible transformerless topologies. The high number of voltage levels of DC/AC converters greatly helps to minimize the total harmonic distortion of the current injected into the electrical grid and to reduce the size of Inductor-Capacitor (LC filters).

A comparison of characteristics among various recently proposed DC/AC multilevel converters—based on a single DC source—is shown in Table 1. These converters are mainly proposed for renewable power sources applications in which the power flows unidirectional from a DC source to the AC power grid [6–15].

It is noticeable in Table 1 that the elimination of the galvanic isolation is a relevant topic for new designs of DC/AC multilevel topologies. Therefore, the techniques presented in [8] and [15], are not considered as a viable option compared to transformerless techniques, such as the ones in [6,7,9–14].

Specifically, in [15], the voltage waveform is constructed with four H-Bridges, 16 Insulate-Gate bipolar transistor(IGBT), and four line-frequency transformers (50 or 60 Hz). The square-shaped voltage fed to all four transformers involves the presence of harmonics. This condition stresses the transformers and increases significantly losses due to the skin effect. Out of [8] and [15], most of the proposals analyzed in Table 1 have output voltage waveforms with fewer than nine levels [7–14].

From other point of view, the technique shown in [8] has some advantages over the one in [15]. For instance, the former uses only one transformer. However, this feature can be considered a disadvantage if compared to [7,11,12,14]. This is because the latter proposals have the same number of voltage levels (seven) than the one in [8] but without using any transformer. Moreover, it should be noted that proposals in [9–14] perform the balancing of DC voltages by means of its multilevel modulation scheme, in which the charge and discharge of its capacitors is defined by angles and switching tables.

The topologies shown in [16] and [17] need more than one DC source at input. These options are in disadvantage, compared to those presented in Table 1, because they need extra circuitry for the purpose of implementing multiple DC voltages from a single DC source.

Table 1. Comparison for recent proposal DC/AC multilevel converters based on single DC source.

Publications	Year	No. Levels	No. Transformers	No. IGBTs	No. Capacitors	No. Inductors	No. Diodes
Proposed Topology	2014	9	0	12	2	2	4
[6]	2014	9	0	11	3	1	4
[7]	2014	7	0	10	4	1	0
[8]	2014	7	1	8	3	2	5
[9]	2013	5	0	8	1	0	0
[10]	2012	5	0	8	2	0	0
[11]	2011	7	0	7	4	1	10
[12]	2011	7	0	14	3	1	11
[13]	2009	5	0	8	1	0	0
[14]	2009	7	0	8	1	0	0
[15]	2009	9	4	9	0	0	0

Moreover, the technique presented in [6] shows an acceptable performance in the task of generating a nine-level voltage waveform, free of transformers. It also requires only one power source and a floating capacitor, similar to [9]. However, this technique uses two cascaded cells and three extra semiconductor switches. In addition, this proposal implements a rather complex algorithm to support it operation, making it difficult for applications in grid-integrated renewable energies environments.

This paper introduces a novel hybrid multilevel conversion topology. This structure puts together two modified basic topologies, a DC/DC Buck converter and a DC/AC Multilevel hybrid cascaded cell, into a single nine-level DC/AC structure. The new single-phase, two-stage converter uses 12 power-switches only and a single DC input. Finally, this structure does not require switching tables or complex control algorithms to balance the capacitors. Significant advantages are obtained, based only on a single DC source at input, over all recent techniques of multilevel converters analyzed in Table 1. This research, in general, pursues to further improve the efficiency and power density of transformerless architectures as well as its reduction in complexity and costs.

2. Operation Principle of Proposed Converter

The main objective of this proposal is the generation of two isolated DC sources, named V_{C1} and V_{C2}, from a single power supply V_{DC}, without use of transformers. These isolated DC sources are required for the proper performance of 9-levels DC/AC cascaded cells topology.

To achieve this goal, this paper proposes a modification in the structure of conventional DC/DC Buck Converter, without changes in the operating principle.

The proposed modification consists on a time-lapse high impedance generation between each Buck converter and V_{DC} power supply, to achieve the continuous high impedance states between V_{C1} and V_{C2} voltages generated by the Buck converters. Using the converter $Buck_1$ shown in Figure 1, the proposed modification is described. It consists on adding a power switch ($T_{1,2}$) with the task of opening the ground path of the V_{DC} source. The diode $D_{1,2}$ is connected in series to $T_{1,2}$. This connection ensures the unidirectional current flow from the collector to the emitter of $T_{1,2}$.

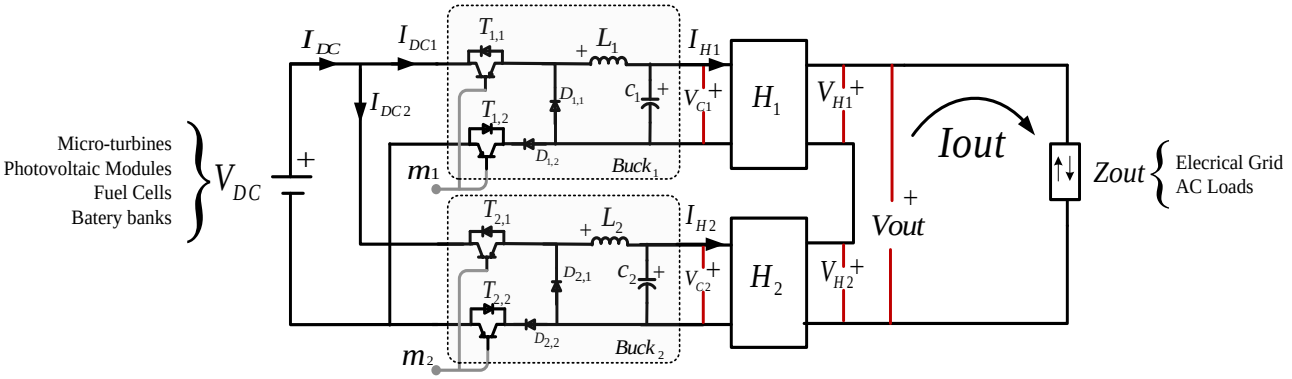


Figure 1. Single DC nine-level DC/AC hybrid proposed topology.

The power supply, V_{in}, is the input voltage of the proposed converter. V_{in} can be a renewable DC source, such as a solar PV array, a low-voltage wind, or a battery bank. It must be noted that the voltage DC source, V_{in}, must have a value greater than the peak value of the output voltage, V_{out}. The recommend range is $1.2 \times |V_{out}| < V_{in} < 1.5 \times |V_{out}|$.

The output voltage, V_{out}, can be connected to low–medium-voltage power grids or to off-grid AC loads. Since the proposed structure does not need a transformer for any conversions, process, or interconnection, it has advantages, such as higher power density, higher efficiency, lower cost and reduction of total harmonic distortion at output.

2.1. Isolated Bucks Converters

As shown in the *Buck₁* converter of Figure 1, the commutation states of the switches $T_{1,1}$ and $T_{1,2}$ are controlled in parallel by the control pulse m_1, while $T_{2,1}$ and $T_{2,2}$ are controlled by m_2, on *Buck*₂ converter. The PWM pulses, m_1 and m_2, are generated based on the magnitude comparison between D_1 and D_2 modulation signals and $carry_1$, and $carry_2$, ramp signals. The latter signals have a constant 180° phase shift and use the switching frequency, FC_{Buck}. Equations (1)and (2), shown the comparison rules for m_1 and m_2:

$$m_1 = \begin{cases} 1 & when \quad D_1 > Carry_1 \\ 0 & when \quad D_1 < Carry_1 \end{cases} \tag{1}$$

$$m_2 = \begin{cases} 1 & when \quad D_2 > Carry_2 \\ 0 & when \quad D_2 < Carry_2 \end{cases} \tag{2}$$

From Equations (1) and (2) it can be deduced a number of topological combinations between *Buck*₂ and *Buck*₁ converters, as shown in Table 2. These states are obtained considering that switching variables m_1 and m_2 do not take state 1 at the same time instant, which has been termed as a prohibited state for this application.

Table 2. Topological states for buck converters.

Topological State	m_1	m_2	I_{L1}	I_{L2}	$I_{D1,1}$	$I_{D1,2}$	$I_{D2,1}$	$I_{D2,2}$	I_{DC}
(i)	0	0	ΔI_{L1off}	ΔI_{L2off}	ΔI_{L1off}	0	ΔI_{L2off}	0	0
(ii)	1	0	ΔI_{L1on}	ΔI_{L2off}	0	ΔI_{L1on}	ΔI_{L2off}	0	ΔI_{L1on}
(iii)	0	1	ΔI_{L1off}	ΔI_{L2on}	ΔI_{L2off}	0	0	ΔI_{L2on}	ΔI_{L2on}
	1	1	Prohibited						

Figures 2 and 3 show the main topological states proposed for the Buck converters. Figure 2 shows specifically the topological state (ii) of Table 2, which meets the switching state $m_1 = 1$, and the *Buck*$_1$ converter takes the ΔI_{L1on} current state, which is dependent on the potential difference between V_{DC} and V_{C1} as shown in Equation (3):

$$\Delta I_{L1on} = \frac{1}{T}\int_0^{t_{1on}} \frac{V_{DC} - V_{C1}}{L_1} \cdot dt + I_{L1}^{\circ} = \frac{(V_{DC} - V_{C1})}{L_1} \cdot \frac{t_{1on}}{T} + I_{L1}^{\circ} \quad (3)$$

From Figure 2, it can be deduced that current I_{DC1} flows from the power supply V_{DC}, from collector-emitter of $T_{1,1}$ switch, followed by the inductor L_1 to the capacitor C_1, closing the circuit to ground by $D_{1,2}$ and the extra switch $T_{1,2}$. It is noted that for this current mesh, the diode $D_{1,1}$ is not polarized. Parallel to this process it is noted in *Buck*$_2$ converter, the current state ΔI_{L2off}, where this current is only dependent of voltage V_{C1}, and initial condition I_{L2}°, as described in Equation (4):

$$\Delta I_{L2off} = \frac{1}{T}\int_0^{t_{2off}} \frac{-V_{C2}}{L_2} \cdot dt + I_{L2}^{\circ} = -\frac{V_{C2}}{L_2} \cdot \frac{t_{2off}}{T} + I_{L2}^{\circ} \quad (4)$$

In Figure 2, referring to *Buck*$_2$ converter, it can be seen that the $T_{2,1}$ and $T_{2,2}$ switches are in open condition, due to $m_2 = 0$. In this way, a high impedance state is generated between the positive and negative source terminals V_{DC} and the level of voltage V_{C2}, where the current I_{L2} flows from the positive terminal of the inductance to the cathode of the diode $D_{1,1}$ to the negative terminal of the capacitor C_2.

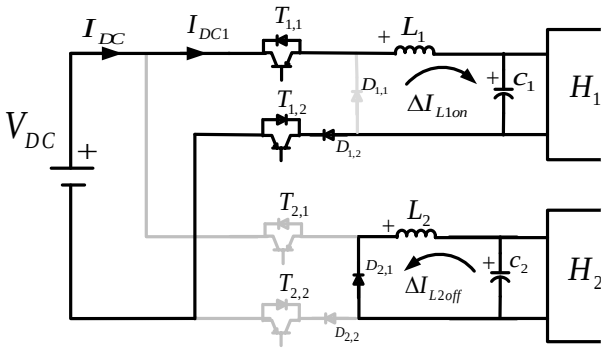


Figure 2. Topological state (ii), $m_1 = 1$, $m_2 = 0$.

Note that in this commutation state, the V_{DC} power supply is directly connected to the voltage V_{C1}, but in a high impedance state with V_{C2} voltage. We concluded that there is no direct connection between V_{C1} and V_{C2}.

Moreover, Figure 3 shows the next commutation stage (iii) of Table 2. It can be seen that the converter *Buck*$_1$ is in current state ΔI_{L1off}. This current depends only on voltage V_{C1}, and the initial condition I_{L1}°, as described in Equation (5):

$$\Delta I_{L1off} = \frac{1}{T}\int_0^{t_{1off}} \frac{-V_{C1}}{L_1}\cdot dt + I_{L1}^{\circ} = -\frac{Vc_1}{L_1}\cdot\frac{t_{1off}}{T} + I_{L1}^{\circ} \quad (5)$$

Parallel to this process, the current I_{DC2} in the *Buck*$_2$ converter flows from the power supply V_{DC} to the collector-emitter of $T_{2,1}$ switch, then to the L_2 inductance and afterward toward the capacitor C_2, closing the circuit to ground through $D_{2,2}$ and finally to emitter-collector of switch $T_{2,2}$:

$$\Delta I_{L2on} = \frac{1}{T}\int_0^{t_{2on}} \frac{V_{DC}-V_{C2}}{L_2}\cdot dt + I_{L2}^{\circ} = \frac{\left(V_{DC}-V_{C2}\right)}{L_2}\cdot\frac{t_{2on}}{T} + I_{L2}^{\circ} \quad (6)$$

It is observed that in this trajectory the diode $D_{2,1}$ is not polarized, so the topological state described (ΔI_{L2on}) is fulfilled by Equation (6).

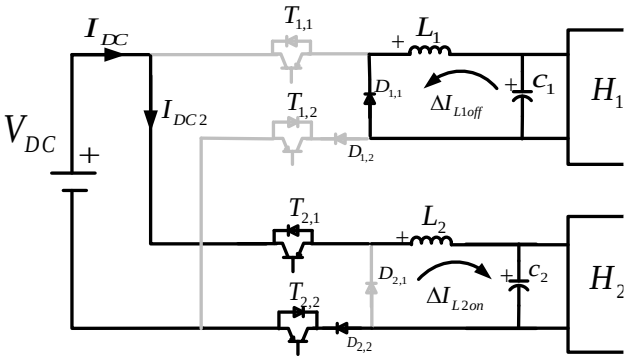


Figure 3. Topological state (iii), $m_1 = 1$, $m_2 = 0$.

Note that this switching state is complementary to state (ii) in Table 2. The V_{DC} power supply is directly connected to the voltage V_{C2}, but in a state of high impedance is connected to V_{C1}. It can be concluded again, that there is not direct connection between V_{C1} and V_{C2}.

Finally, the topological state (i), of the switching Table 2, can be considered as a dead time and there is no connection between the power supply V_{DC} with the V_{C1} and V_{C2} voltage, where the *Buck*$_1$ and *Buck*$_2$ converters acquired a complementary behavior (ΔI_{L1off} and ΔI_{L2off}), as Indicated in the Equations (4)–(6). Figure 4 shows the main waveforms involved in the process of DC/DC conversion, to generate two isolated voltage sources (V_{C1} and V_{C2}) based on single DC source at input.

The *carry*$_1$ and *carry*$_2$ variables are displayed in Figure 4a,d, respectively. In this figure it can be observed 180° of constant phase shift between the control pulses coming from the magnitude comparison between the *carry*$_1$ and *carry*$_2$ signals with D_1 and D_2. The variable modulation technique is shown in Figure 4b,e, in which it can be seen a complementary behavior and a dead time between the rising and falling edges. The generation of control pulses m_1 and m_2 is based on Equations (1) and (2). These pulses are applied directly to control circuit breakers, being $T_{1,1}$ and $T_{1,2}$ controlled by D_1 and $T_{2,1}$ and $T_{2,2}$ controlled by D_2, as previously indicated.

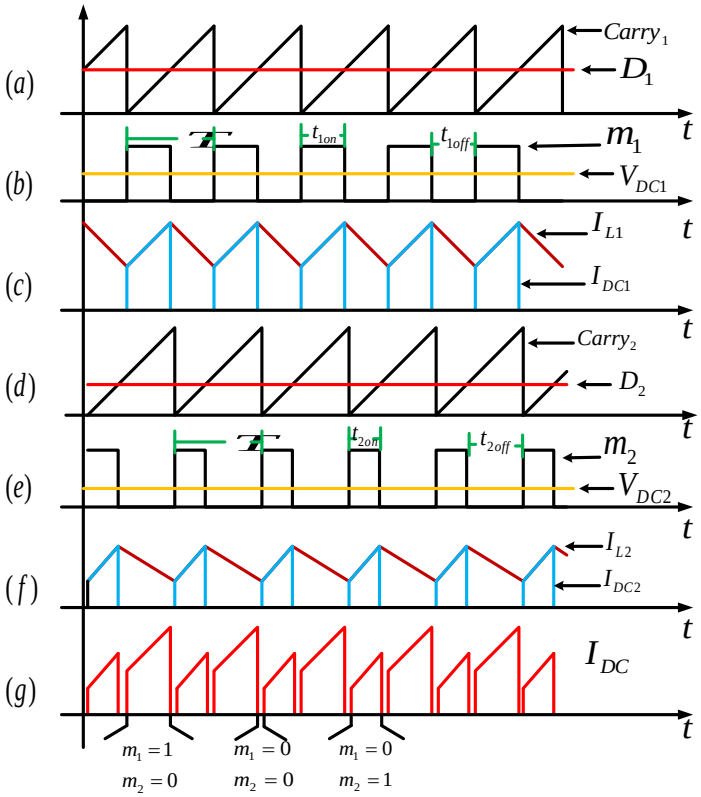


Figure 4. Main waveforms for buck$_1$ and buck$_2$ converters (**a**) *carry*$_1$ and D_1; (**b**) m_1; (**c**) I_{L1} and I_{DC1}; (**d**) *carry*$_2$ and D_2; (**e**) m_2; (**f**) I_{L2} and I_{DC2}; (**g**) I_{DC}.

Currents I_{L1} and I_{L2} in the inductances are shown in red in Figure 4c,f. In these, it can be observed a continuous conduction mode behavior. In the same figure, in blue color, there are shown the waveforms of currents I_{DC1} and I_{DC2} generated in each Buck converter, which are dependent of the product of the inductance current and the control drive variable m_1 and m_2, as is stated in the Equations (7)–(8):

$$I_{DC1} = I_{L1} \cdot m_1 \tag{7}$$

$$I_{DC2} = I_{L2} \cdot m_2 \tag{8}$$

Finally, the instantaneous sum of the I_{DC1} and I_{DC2} currents is shown through the I_{DC} variable in Figure 4g. This represents the total current supplied by the voltage source V_{DC}, and is calculated by means of Equation (9):

$$I_{DC} = I_{DC1} + I_{DC2} \tag{9}$$

The voltages V_{C1} and V_{C2} are depending of the inductors currents and the H-Bridges currents, defined as:

$$V_{C1} = \int (I_{L1} - I_{H1}) \cdot dt \tag{10}$$

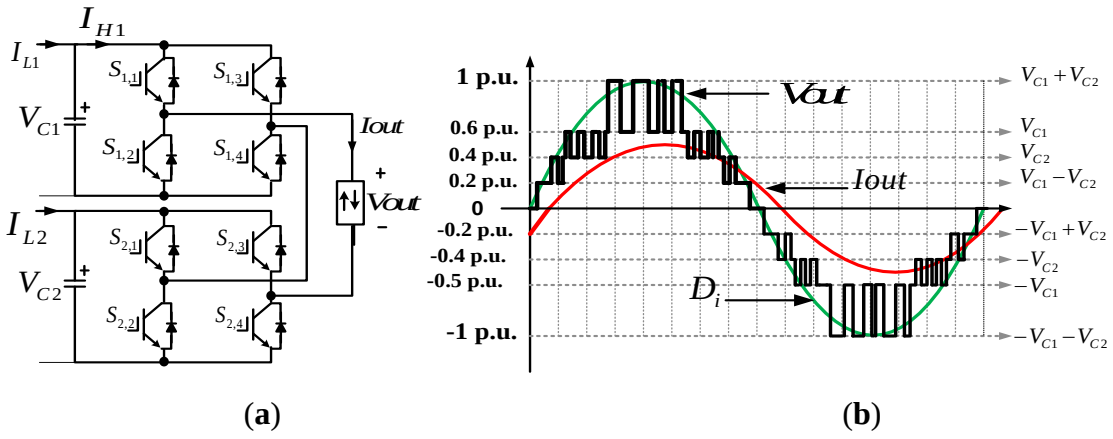
$$V_{C2} = \int (I_{L2} - I_{H2}) \cdot dt \tag{11}$$

Currents I_{H1} and I_{H2} are detailed in the next section. After analyzing the topological states of the Buck converters and by noting the connection and disconnection of alternating V_{DC} voltage source and also by noting a state of continuous high impedance between C_1 and C_2, we conclude that it is possible to feed the DC/AC multilevel cascaded hybrid cells from a single power supply.

2.2. DC/AC Nine Levels Cascaded Cell Topology

A hybrid, two-bridges, multilevel structure with asymmetrical sources has key advantages over the VSC-NPC and flying capacitor VSC. For instance, it can provide a higher number of voltage levels with fewer switches. In addition, the hybrid topology has no need of capacitors or transformers for its basic operation. As a consequence, using the latter configuration, a sine waveform can be reproduced with lower harmonic distortion than with other multilevel topologies.

The generation of different voltage levels in V_{out}, from the cascade cell converter, is shown in Figure 5. This voltages are obtained based on the algebraic sum of voltages V_{C1} and V_{C2} as shown in Table 3, where H_1 and H_2 bridges generate combinations independent of voltage *versus* time, being V_{H1} ϵ {+V_{C1}, 0, −V_{C1}}; and V_{H2}, ϵ {+V_{C2}, 0, −V_{C2}}; respectively.



(**a**) (**b**)

Figure 5. Nine levels DC/AC cascaded hybrid converter (**a**) topology; (**b**) V_{out} waveform.

Table 3. Switching states and respective voltage levels.

Vout Level	H_1				H_2			
	$S_{1,1}$	$S_{1,2}$	$S_{1,3}$	$S_{1,4}$	$S_{2,1}$	$S_{2,2}$	$S_{2,3}$	$S_{2,4}$
$V_{C1} + V_{C2}$	1	0	0	1	1	0	0	1
V_{C1}	1	0	0	1	1	0	1	0
V_{C2}	1	0	1	0	1	0	0	1
$V_{C1} - V_{C2}$	1	0	0	1	0	1	1	0
0	1	0	1	0	1	0	1	0
$-V_{C1} + V_{C2}$	0	1	1	0	1	0	0	1
$-V_{C2}$	1	0	1	0	0	1	1	0
$-V_{C1}$	0	1	1	0	1	0	1	0
$-V_{C1} - V_{C2}$	0	1	1	0	0	1	1	0

Finally, the magnitude and phase shift of I_{out} depend on the type of load connected to converter, which can be an independent load or a distribution electrical grid. The voltages of each H-bridge converter (V_{H1} and V_{H2}) can be defined by Equations (12) and (13) as:

$$V_{H1} = V_{C1} \cdot [S_{1,1} - S_{1,3}] \tag{12}$$

$$V_{H2} = V_{C2} \cdot [S_{2,1} - S_{2,3}] \tag{13}$$

The currents of each H-bridge converter (I_{H1} and I_{H2}) can be defined by Equations (14) and (15) as:

$$I_{H1} = I_{out} \cdot [S_{1,1} - S_{1,3}] \tag{14}$$

$$I_{H2} = I_{out} \cdot [S_{2,1} - S_{2,3}] \tag{15}$$

Figure 5 shows the nine levels DC/AC cascaded hybrid topology implemented in this research. It should be mentioned that for the topology employed specifically here, the voltage levels V_{C1} and V_{C2} have to satisfy the following ratio:

$$V_{C1} = \frac{3}{2} V_{C2} \tag{16}$$

where $V_{C1} \approx V_{in} \cdot D_1$ and $V_{C2} \approx V_{in} \cdot D_2$. Based on Equation (16) it is possible to calculate the duty cycle D_1 and D_2, applied in Buck$_1$ and Buck$_2$ converters, respectively. It is noteworthy to mention that if the voltage ratio between V_{C1} and V_{C2} is different from that stated in Equation (16), then V_{out} results with deformations and, as a pertinent consequence, some harmonics can be injected to the power grid. The harmonic distortion due to the imbalance of DC sources in DC/AC cascade-cell converter has been already studied [18]. As V_{C1} and V_{C2} depend of D_1 and D_2, a larger or shorter of the latter will deform V_{out}. The generation of voltage levels V_{out} is performed based on switching states in Table 3. To obtain the correct control pulses to be applied to inverter power switches connected in cascade is necessary to implement a multilevel modulation Sine-Pulse Width Modulation (SPWM) process, discussed in next section.

2.3. Nine-Level SPWM Modulation

The multilevel modulation process employed for the topology, and shown in Figure 6, is obtained from a magnitude comparison between eight modulating waves $carry^{-}_{j}$ and $carry^{+}_{j}$ where $j \in (1,2,3,4)$ and a sine modulating signal D_i.

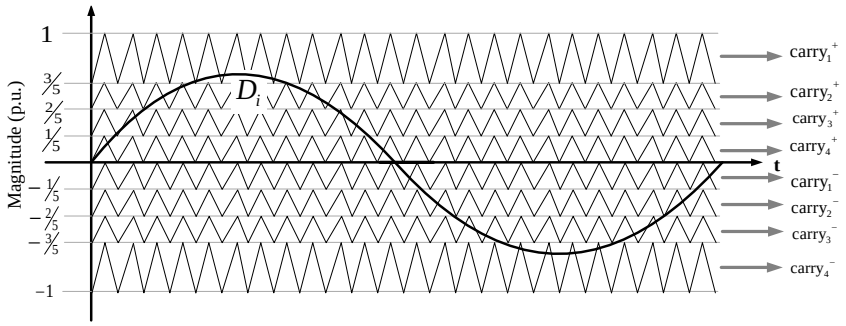


Figure 6. Nine levels SPWM scheme.

The control pulses are described by Equations (17) and (18):

$$C_i^+ = \begin{cases} 1 & when \quad carry_i^+ < D_i \\ 0 & when \quad carry_i^+ > D_i \end{cases} \tag{17}$$

$$C_i^- = \begin{cases} 1 & when \quad carry_i^- > D_i \\ 0 & when \quad carry_i^- < D_i \end{cases} \tag{18}$$

In order to obtain the necessary topological stages, described by Table 3, the combinational logic stage is necessary to obtain the required pulses for the cascaded multilevel converter. The logical diagram implemented is shown in the Figure 7.

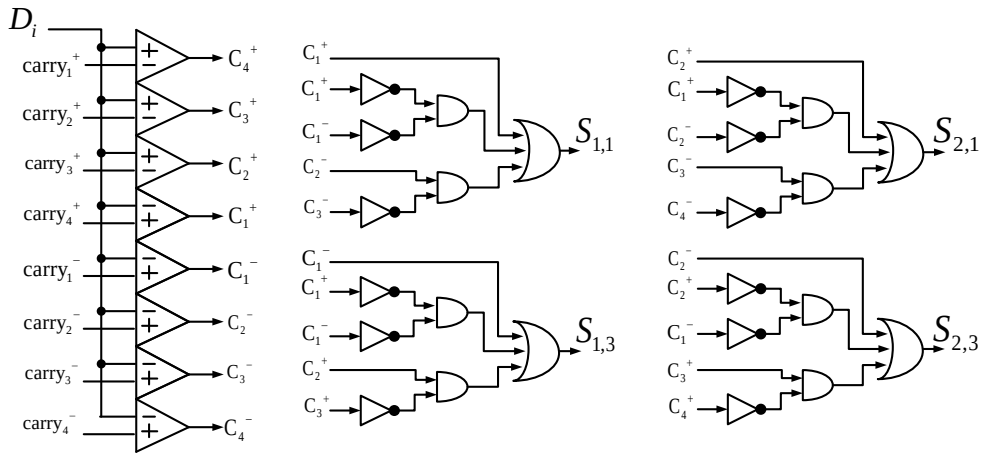


Figure 7. Combinational logic for IGBT pulses, on cascaded cell topology.

In order to verify the full operation of the converter stages, the Buck converters and the cascaded cells with their respective modulations, a number of simulations have been developed, which are presented in the next section.

3. Simulation

The proposed converter is analyzed through the Simulink—Matlab simulation platform, showing the main variables of voltage, current and control pulses involved in the conversion process of DC/DC through the Buck converters and DC/AC through hybrid cascaded cell converter.

Figure 8a,c shows the switching states of converters $Buck_1$ and $Buck_2$. The alternating duty cycles m_1 and m_2 ensures the effect of instant isolation between V_{C1} and V_{C2}. I_{L1} and I_{L2} current waveforms are shown in Figure 8b,d, respectively. The behavior of these variables has been verified on the basis of Equations (3)–(6).

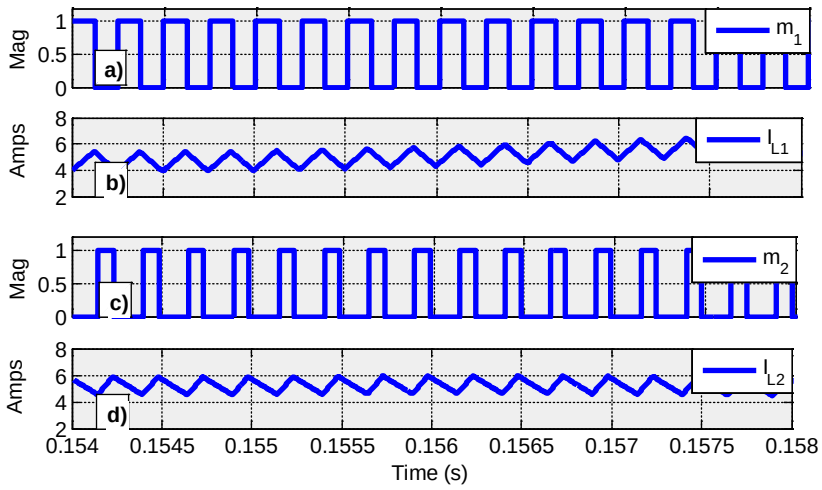


Figure 8. I_{L1} and I_{L2} currents for buck converters.

The waveforms of currents I_{DC1} and I_{DC2}, generated by each Buck converter, are shown in Figure 10a,b, respectively. Here, are clear again the alternating switching times between each converter.

Finally the total current I_{DC} supplied by the voltage source V_{DC}, is shown in Figure 9c, which is dependent on the instantaneous sum of I_{DC1} and I_{DC2}, fulfilling Equation (9).

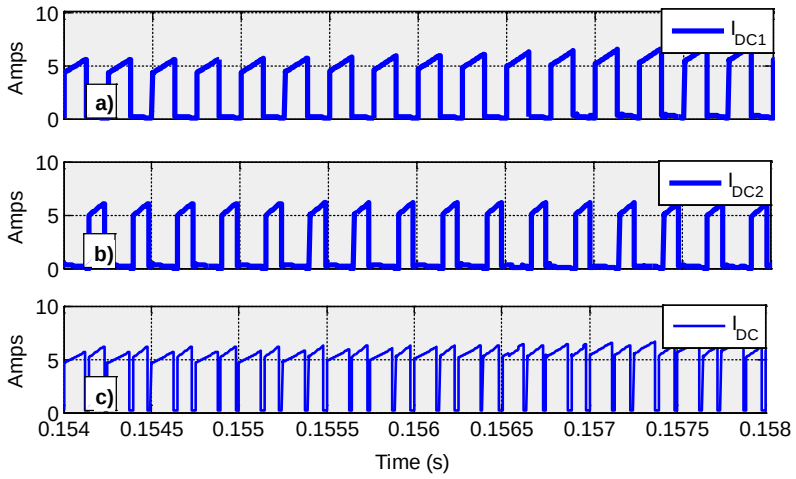


Figure 9. Current waveforms (**a**) I_{DC1}, (**b**) I_{DC2}, and (**c**) I_{DC}.

The steady-state output voltage of the Buck converters, V_{C1} and V_{C2}, are shown in Figure 10a. In this figure the relative voltage for proper operation of the hybrid cascaded cell converter is observed, as indicated by Equation (16).

The voltage waveforms generated by the H-Bridge converters, V_{H1} and V_{H2}, are shown in Figure 10b,c, respectively. From this, it can be seen the topological combinations *versus* time dependent modulation process, meeting the switching states, Table 2.

Finally, the stepped voltage waveform V_{out}, is shown by Figure 10d. V_{out} depends on the algebraic sum of the instantaneous V_{H1} and V_{H2} voltages.

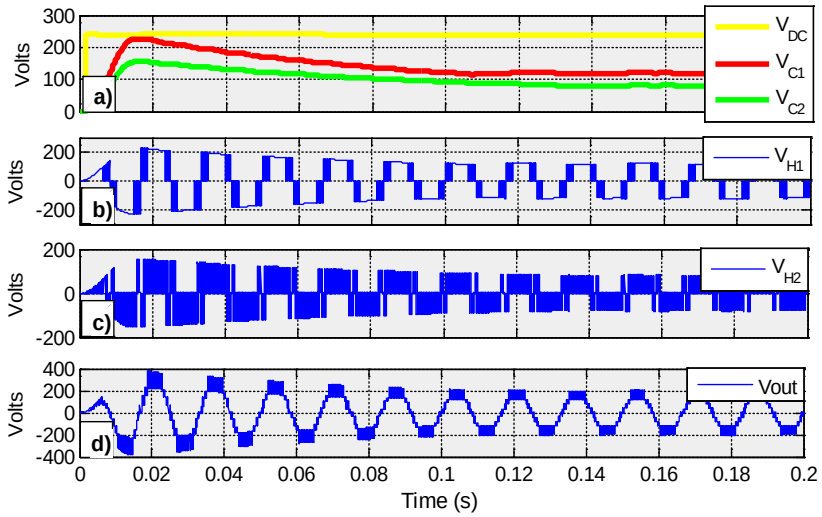


Figure 10. Main voltage waveforms (**a**) V_{DC}, V_{C1}, and V_{C2}; (**b**) V_{H1}; (**c**) V_{H2}; and (**d**) V_{out}.

Based on the performed simulations it is possible to verify compliance of the main goal of this research: to achieve nine voltage levels DC/AC from a single power supply with only 12 power switches and without transformers.

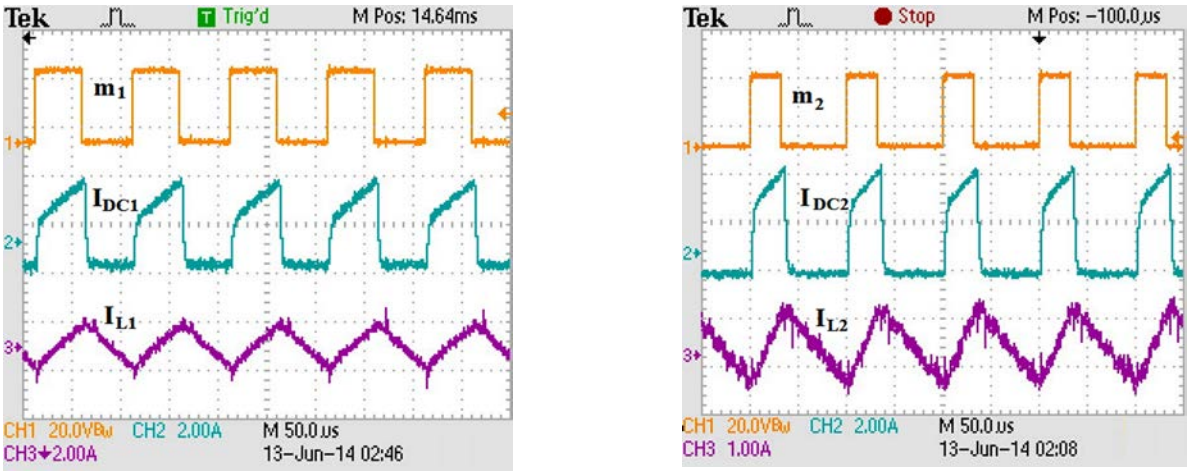
Additionally, it has been shown by means of circuit simulations that the waveforms satisfy the main equations obtained for the electrical conversion process.

4. Experimental Test

In order to experimentally verify the topology presented, a laboratory prototype has been built using the parameters shown in Table 4. These parameters are the same used in the simulations. In Figure 11a,b can be corroborated experimentally the modulation process of *Buck*$_1$ and *Buck*$_2$ converters, respectively, showing the variables modulation m_1 and m_2, compared to current inductance I_{L1} and I_{L2}, ending with the currents supplied by the source I_{DC1} and I_{DC2}.

Table 4. Parameter values for the simulation of the proposed converter.

Variable, Element	Value
Bucks Switching Frequency	16 kHz
Multilevel Modulation Frequency	6 kHz
$L_1 = L_2$	6 mH
$C_1 = C_2$	2200 uF
V_{DC}	240 V
D_1	0.5
D_2	0.33
D_i	0.95∗sin(ωt)



(**a**) (**b**)

Figure 11. Principal waveforms of the buck converters, (**a**) m_1, I_{L1} and I_{DC1} for buck$_1$ and (**b**) m_2, I_{L2} and I_{DC2} for buck$_2$.

Under the same case study, Figure 12 shows current I_{DC}, which corresponds to the sum of the currents I_{DC1} and I_{DC2} with respect to the control pulse m_1.

From these waveforms is possible to corroborate the different switching states of *Buck*$_1$ and *Buck*$_2$ converters, shown in Table 2 and analyzed with Equations (7)–(9). Finally, it can be observed that the waveforms exposed in Figure 12 are similar to those shown in Figure 4.

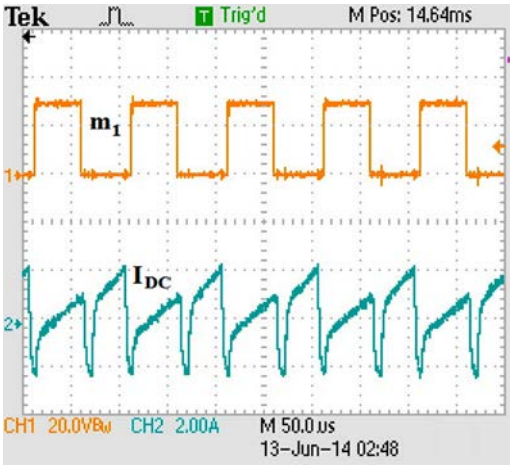
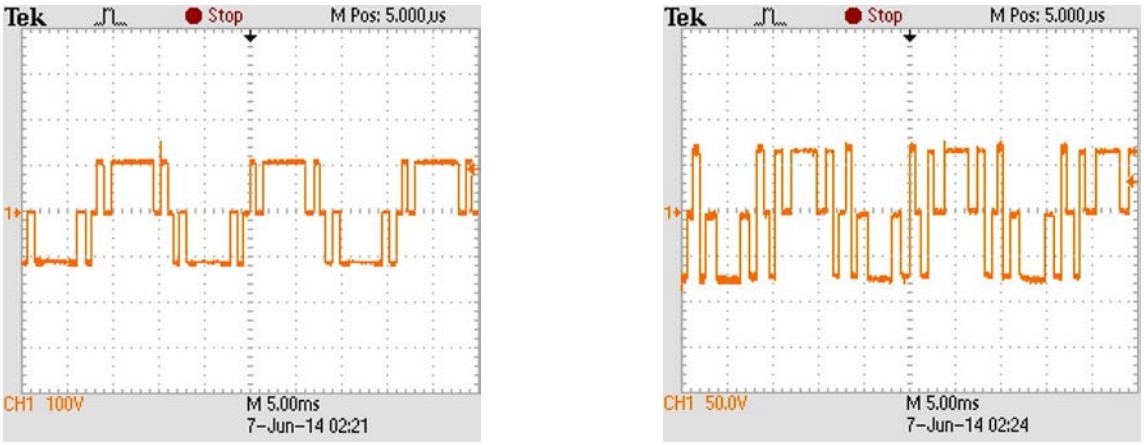


Figure 12. I_{DC} and m_1 waveforms.

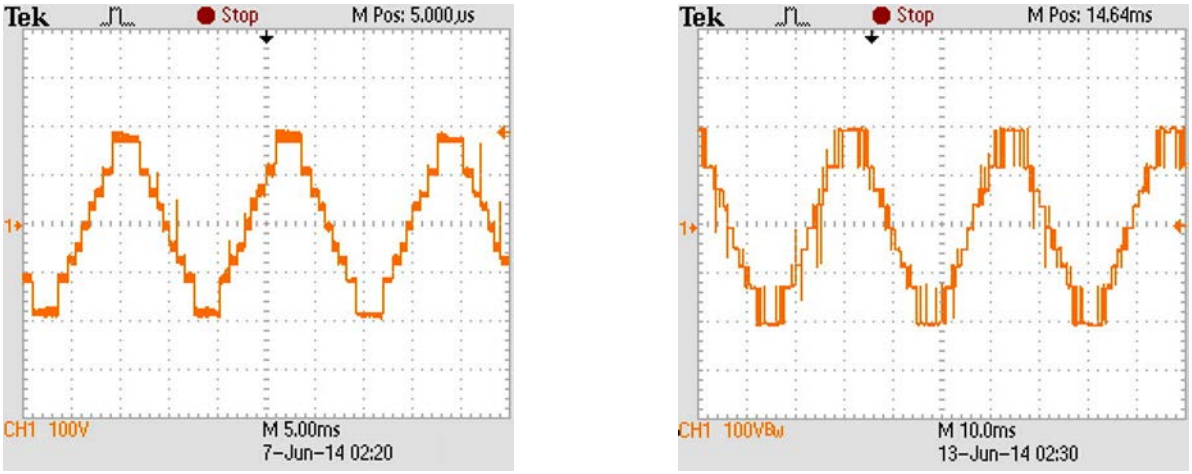
Under the principle of operation exposed previously, corresponding to the cascaded converter modulation, Figure 13a,b show the experimental voltages generated by each H bridge converter, where it can be seen that $V_{H1} \in \{+V_{C1}, 0, -V_{C1}\}$; and $V_{H2} \in \{+V_{C2}, 0, -V_{C2}\}$, respectively.



(**a**) (**b**)

Figure 13. Independent H-bridge voltages (**a**) V_{H1}; (**b**) V_{H2}.

Based on the voltages shown by Figures 13a,b, it is possible to corroborate the voltages ratio between V_{C1} and V_{C2} as 1:1.5, as stated in Equation (16). The algebraic sum of the V_{H1} and V_{H2}, corresponding to the output voltage V_{out}, is shown by Figure 14, where Figure 14a shows an experimental validation of the staggered signal and Figure 14b shows the same output signal with SPWM modulation applied.



(**a**) (**b**)

Figure 14. V_{out} (**a**) multilevel V_{out} (**b**) SPWM multilevel V_{out}.

The multilevel output voltage V_{out} needs filtering to reduce THD and bring the signal closer to the ideal sinusoidal waveform. As the frequency spectrum of the 3 and 5-level converter is wider than that of the nine-level, the filtering requirements of the latter are less demanding.

Figure 15 presents the scaled-down physical prototype of the nine levels converter with FPGA-based control, the principal auxiliary subsystems and the experimental setup, respectively. Figure 16 shows the efficiency curves against power, obtained from the prototype.

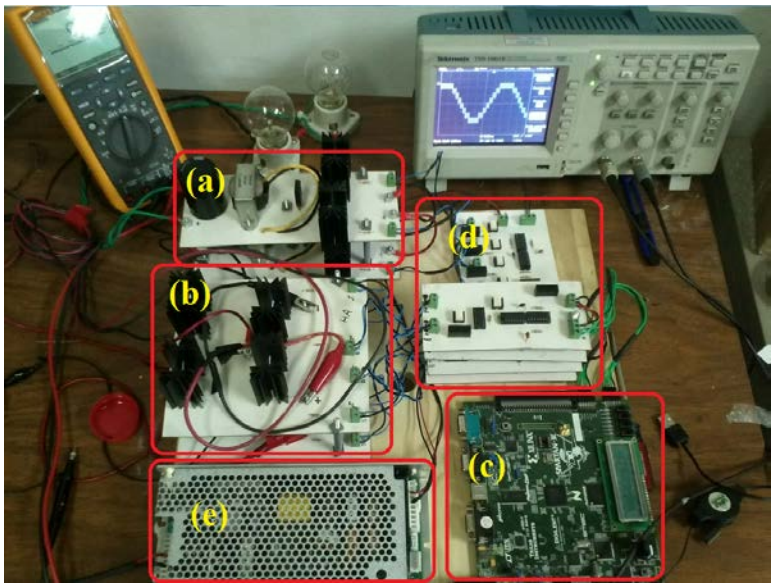


Figure 15. Laboratory prototype of the converter and experimental testing (**a**) Modified DC/DC buck converters; (**b**) H-bridges converters; (**c**) FPGA based control; (**d**) Drivers pulses for IGBTs; and (**e**) DC source circuitry.

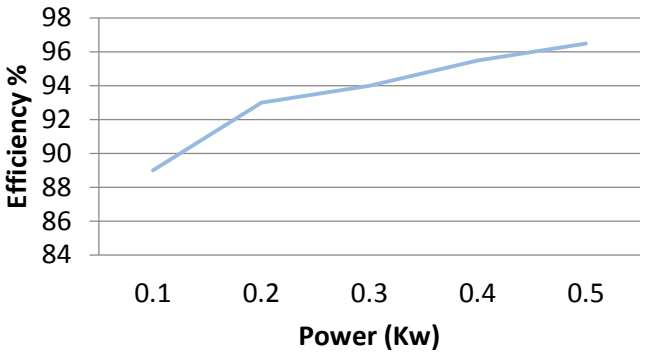


Figure 16. Efficiency tests.

Discussion

Table 5 shows a comparative analysis between basic DC/AC topologies and the proposed one. It should be remarked that the proposed topology is designed for unidirectional power flow applications only. Nevertheless, Table 5 also shows that the proposed topology has various relative advantages such as fewer power switches, diodes and capacitors compared to structures such as the clamped diode or the flying capacitor. Comparatively to the cascaded-cells topology, this novel nine-levels converter is lesser complex to build because it uses just one power source at input instead of two.

Table 5. Comparative analysis for nine levels DC/AC multilevel converters.

Multilevel Converter	No. IGBTs	No. Capacitors	No. Diodes	No. DC Sources
Proposed Topology	12	2	6	1
Clamped Diode	16	8	32	1
Flying Capacitor	16	32	0	1
Cascaded cells	8	0	0	2

A general advantage of the new nine-levels converter over the other configurations is its relative simple control algorithm, without the need of a transformer. These enhanced features make the nine-levels converter introduced in this paper very suitable to application in micro-grids.

The solutions and capabilities presented can be further enhanced. Additional future advances from this work focus on: (i) Minimizing the voltage and current harmonic distortion by means of a suitable modulation scheme; (ii) Obtaining a mathematical model of the dynamic behavior of the nine-level converter and its interaction with distribution grids and a microgrids; (iii) Evaluating the benefits of using various types of LC and LCL filter for the interconnection of the nine-level converter with the grid; (iv) Incorporating the converter to the Smart Grid concept; (v) Analyzing the transient behavior of the converter; and (vi) Evaluate the benefits and limitations of using various types of LC and LCL filter, located in between V_{in} and the Bucks converters, as a way for obtaining a continuous input current I_{DC}.

5. Conclusions

This work presents a new CD-CA nine-level topology, which combines a modified DC/DC Buck Converter and hybrid Cascade converter based on two H-bridge, in a single phase structure. The most important advantages of the proposed nine-level topology are: (i) Single DC source without need of transformer and (ii) Reduction of power switches.

This topology is a competitive option suitable for an efficient integration and controlling of renewable power sources (such as PV, fuel cells and low-voltage wind generator) into low and medium voltage power grids and microgrids. For instance, a household application is the interconnection of PV modules, while in isolated microgrids the applications may be PV and fuel cells. In other contexts, an ambitious goal is to explore the application possibilities related to the integration of large photovoltaic installations.

This work is a step forward in the direction of reducing the number of elements in a converter structure while improving overall efficiency and enhancing performance relative to other well-known converter configurations.

The authors expect that the step-up multi-level converter introduced in this paper will become a useful alternative for research and development in the area of DC/AC multilevel converters.

Acknowledgments

The authors would like to thank to the TNM (Tecnologico Nacional de Mexico) for the financial support to this project.

Author Contributions

All authors contributed equally to this work. J.R. Rodriguez-Rodríguez performed prototype experiments; Vicente Venegas-Rebollar wrote the manuscript; Edgar L. Moreno-Goytia gave technical support and conceptual advice; and all authors collected and analyzed the obtained data.

Conflicts of Interest

The authors declare no conflict of interest.

References

1. Arango, E.; Ramos-Paja, C.A.; Calvente, J.; Giral, R.; Serna, S. Asymmetrical interleaved DC/DC switching converters for photovoltaic and fuel cell applications—Part 1: Circuit generation, analysis and design. *Energies* **2012**, *5*, 4590–4623.
2. Rodriguez, J.; Lai, J.S.; Peng, F.Z. Multilevel inverters: A survey of topologies, controls, and applications. *IEEE Trans. Ind. Electron.* **2002**, *49*, 724–738.
3. Tolbert, L.M.; Peng, F.Z. Multilevel converters as a utility interface for renewable energy systems. In Proceedings of the Power Engineering Society Summer Meeting, Seattle, WA, USA, 16–20 July 2000; pp. 1271–1274.
4. Walker, G.R.; Sernia, P.C. Cascaded DC–DC converter connection of photovoltaic modules. In Proceedings of the 33rd Annual Power Electronics Specialists Conference, Cairns, Queensland, Australia, 22–27 June 2002; pp. 24–29.
5. Gonzalez, R.; Gubia, E.; Lopez, J.; Marroyo, L. Transformerless single-phase multilevel-based photovoltaic inverter. *IEEE Trans. Ind. Electron.* **2008**, *55*, 2694–2702.
6. Buticchi, G.; Barater, D.; Lorenzani, E.; Concari, C.; Franceschini, G. A nine-level grid-connected converter topology for single-phase transformerless PV systems. *IEEE Trans. Ind. Electron*. **2014**, *61*, 3951–3960.
7. Tsunoda, A.; Hinago, Y.; Koizumi, H. Level- and phase-shifted PWM for seven-level switched-capacitor inverter using series/parallel conversion. *IEEE Trans. Ind. Electron*. **2014**, *61*, 1411–1421.
8. Wu, J.C.; Chou, C. A solar power generation system with a seven-level inverter. *IEEE Trans. Power Electron*. **2014**, *29*, 3454–3452.
9. Sepahvand, H.; Liao, J.; Ferdowsi, M.; Corzine, K.A. Capacitor voltage regulation in single-DC-source cascaded H-bridge multilevel converters using phase-shift modulation. *IEEE Trans. Ind. Electron*. **2013**, *9*, 3619–3626.
10. Roshankumar, P.; Rajeevan, P.P.; Mathew, K.; Gopakumar, K.; Leon, J.I.; Franquelo, L.G. A five-level inverter topology with single-DC supply by cascading a flying capacitor inverter and an H-bridge. *IEEE Tran. Power Electron*. **2012**, *27*, 3505–3512.
11. Rahim, N.A.; Chaniago, K.; Selvaraj, J. Single-phase seven-level grid-connected inverter for photovoltaic system. *IEEE Trans. Ind. Electron*. **2011**, *58*, 2435–2443.
12. Nami, A.; Zare, F.; Ghosh, A.; Blaabjerg, F. A hybrid cascade converter topology with series-connected symmetrical and asymmetrical diode-clamped H-bridge cells. *IEEE Trans. Power Electron*. **2011**, *26*, 51–65.
13. Vazquez, S.; Leon, J.I.; Franquelo, L.G.; Padilla, J.J.; Carrasco, J.M. DC-voltage-ratio control strategy for multilevel cascaded converters fed with a single DC source. *IEEE Trans. Ind. Electron*. **2009**, *56*, 2513–2521.
14. Du, Z.; Tolbert, L.M.; Ozpineci, B.; Chiasson, J.N. Fundamental frequency switching strategies of a seven-level hybrid cascaded H-bridge multilevel inverter. *IEEE Trans. Power Electron*. **2009**, *24*, 25–33.
15. Song, S.G.; Kang, F.S.; Park, S.J. Cascaded multilevel inverter employing three-phase transformers and single DC input. *IEEE Trans. Ind. Electron*. **2009**, *56*, 2005–2014.

16. Ruiz-Caballero, D.A.; Ramos-Astudillo, R.M.; Mussa, S.A.; Heldwein, M.L. Symmetrical hybrid multilevel DC–AC converters with reduced number of insulated DC supplies. *IEEE Trans. Ind. Electron*. **2010**, *57*, 2307–2314.
17. Liu, J.; Cheng, K.; Ye, Y. A cascaded multilevel inverter based on switched-capacitor for high-frequency AC power distribution system. *IEEE Trans. Power Electron.* **2014**, *29*, 4219–4230.
18. Jimenez, O.L.; Vargas, R.A.; Aguayo, J.; Arau, J.E.; Vela, G.; Claudio, A. THD in cascade multilevel inverter symmetric and asymmetric. In Proceedings of the IEEE, Electronics, Robotics and Automotive Mechanics Conference (CERMA), Cuernavaca, Morelos, Mexico, 15–18 November 2011; pp. 289–295.