energies

MDPI

Article

Improved LADRC-Based DC-Bus Voltage Control Strategy for Bidirectional Converters in AC/DC Hybrid Microgrids

Jiamian Wang, Yi Zhang * and Baojiang Wu

Hebei Wind-Photovoltaic-Hydrogen-Storage System Security Monitoring, Intelligent Operation Center of Technology Innovation, North China University of Science and Technology, Tangshan 063210, China; wjm@stu.ncst.edu.cn (J.W.); spring@ncst.edu.cn (B.W.)

* Correspondence: zhangyi@ncst.edu.cn; Tel.: +86-151-2755-0087

Abstract

Bidirectional AC/DC converters in hybrid microgrids are prone to DC-bus voltage instability caused by source-side, grid-side, and load-side disturbances. Conventional linear active disturbance rejection control (LADRC) suffers from a trade-off between transient overshoot suppression and disturbance rejection capability, which limits its practical application. To address this issue, an improved LADRC strategy for bidirectional AC/DC converters is proposed in this paper. First, a linear tracking differentiator (LTD) is introduced to smooth the DC-bus voltage reference and suppress overshoot caused by abrupt command changes. Second, a proportional-derivative (PD) term is embedded into the linear extended state observer (LESO) to introduce phase lead compensation, thereby improving the observer phase characteristics without excessively increasing the observation bandwidth or amplifying high-frequency noise. Frequency domain analysis, MATLAB/Simulink simulations, and full-hardware prototype experiments are carried out to validate the proposed method. The simulation study covers grid voltage sag, photovoltaic-side source fluctuation, and DC-side load disturbance conditions. To further strengthen the experimental verification, hardware tests are conducted under grid voltage dip, PV-side voltage reduction, and DC-side load-switching conditions. The results consistently show that the proposed strategy can effectively reduce DC-bus voltage fluctuation and improve transient recovery performance compared with conventional LADRC. Therefore, the improved LADRC provides a practical and robust control solution for stabilizing bidirectional converters in AC/DC hybrid microgrids.

Keywords: hybrid microgrid; bidirectional AC/DC converter; active disturbance rejection control (ADRC); linear tracking differentiator (LTD)

Check for updates

Received: 17 March 2026
Revised: 12 April 2026
Accepted: 16 April 2026
Published: 20 April 2026

Copyright: © 2026 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license.

1. Introduction

The integration of distributed generation, such as wind and photovoltaic power, with energy storage technologies forms a microgrid system [1–3]. Due to its flexibility, low-carbon nature, and control ability, it has become an effective form of renewable energy utilization [4–6]. However, the increasing penetration rate of renewable energy and the integration of numerous electronic devices present new challenges to the power quality of the distribution network. The bidirectional AC/DC converter, acting as the key equipment linking AC and DC microgrids, provides crucial support for achieving bidirectional power flow between sub-microgrids and improving power quality [7].

Although advanced voltage control algorithms exhibit satisfactory performance in standalone AC/DC conversion systems, formidable challenges are posed in regulating DC-bus voltage within AC/DC hybrid microgrids. During microgrid operation, the renewable energy output on the DC side is highly susceptible to meteorological disturbances, and load switching on both the AC and DC sides is frequent and unpredictable. The strong coupling and multi-source disturbances within the system make it difficult for traditional PI control and conventional linear active disturbance rejection control (LADRC) to balance disturbance rejection and stability. Therefore, under the background of AC/DC hybrid microgrids, the effectiveness of the improved LADRC algorithm in dealing with strong nonlinear disturbances is investigated in this paper through theoretical analysis, multi-condition simulations, and hardware experiments under representative source-side, grid-side, and load-side disturbances [8]. In a grid-connected AC/DC microgrid scenario, the voltage and frequency of the AC microgrid are supported by the public grid, while the DC sub-microgrid is indirectly connected to the main grid through a bidirectional AC/DC converter [9]. Within the DC sub-microgrid, distributed generation units are easily affected by external environmental factors, and the bus is directly connected to the load, leading to significant voltage fluctuations [10]. To summarize, references [8–10] lay a foundational understanding of the necessity of improved LADRC algorithms in hybrid microgrids, the topological connection of grid-connected AC/DC microgrids, and the key factors causing DC-bus voltage fluctuations. However, these existing studies still fall short in addressing practical engineering challenges such as balancing control stability and response speed, as well as avoiding noise amplification while ensuring control accuracy, which provides a direction for further disturbance rejection performance of the control strategy.

Thus, various strategies have been proposed for the stable control of DC-bus voltage in AC/DC hybrid microgrids [11]. Reference [12] proposed an improved virtual DC generator control strategy, which enhanced dynamic response and current sharing performance by co-operating with an average current controller; however, this strategy only addressed voltage fluctuations caused by sudden changes in loads and distributed generation units, neglecting input-side mutations. Reference [13] introduced a dynamic compensation control strategy based on a residual generator, utilizing model matching theory to reversely compensate for current disturbances, but it lacked in-depth exploration regarding controller optimization, such as improving response speed, reducing overshoot, and synergistically enhancing stability and control accuracy. Reference [14] proposed a sliding-mode active disturbance rejection control strategy, leveraging a linear extended state observer to provide state variables for the sliding-mode controller, effectively solving chattering and demonstrating good disturbance rejection; nevertheless, when increasing the observer bandwidth parameter w_0 to improve tracking accuracy, actual system noise was also amplified, negatively impacting the control effect. Despite theoretical progress, traditional LADRC faces obvious engineering bottlenecks in practical industrial microgrids when dealing with severe source–load fluctuations and transient grid faults [15]. Blindly increasing the observation bandwidth to pursue high disturbance rejection inevitably amplifies high-frequency sampling noise and causes system phase lag. Simultaneously, during large-scale power step changes, the traditional framework struggles to achieve both fast tracking of the bus voltage and zero overshoot, restricting its deep application in bidirectional converters. To break through these bottlenecks, this paper proposes an improved LADRC strategy that balances dynamic flexibility and strong disturbance rejection.

Although existing ADRC-based studies have demonstrated improvements in DC-bus voltage regulation, several practical issues remain insufficiently addressed. First, many methods enhance disturbance rejection mainly by increasing the observer bandwidth, which may accelerate disturbance estimation but also tends to amplify measurement

noise in practical digital-control systems [16,17]. Second, the contradiction between rapid voltage recovery and overshoot suppression during operating-condition transitions is often not explicitly resolved. Third, the validation of many existing methods is limited to either simulation or a single disturbance scenario, which makes it difficult to assess their applicability under coupled source-side, grid-side, and load-side disturbances in AC/DC hybrid microgrids. In contrast, the present work combines LTD-based reference shaping with a PD-enhanced LESO so as to improve transient response and disturbance estimation simultaneously without relying solely on bandwidth enlargement. Moreover, the proposed method is evaluated under representative source-side, grid-side, and load-side disturbances through both simulation and hardware experiments, which strengthens its practical relevance.

The main contributions of this paper are summarized as follows:

(1) A linear tracking differentiator (LTD) is introduced into the outer voltage loop to smooth the reference signal and suppress voltage overshoot during start-up and operating-condition transitions.

(2) A proportional-derivative (PD) term is incorporated into the linear extended state observer (LESO) to compensate for observer phase lag without significantly increasing noise sensitivity, thereby enhancing disturbance estimation and rejection capability.

(3) The proposed strategy is validated under representative source-side, grid-side, and load-side disturbances by combining frequency domain analysis, MATLAB 2020a/Simulink simulations, and full-hardware experiments.

2. Topology and Mathematical Model of the Microgrid

2.1. Topology of the AC/DC Hybrid Microgrid

The topology of the hybrid microgrid is shown in Figure 1. AC-side links to the main grid via a point of common coupling (PCC), which enables seamless switching between grid-connected and islanded modes. In grid-connected mode, the public grid maintains the operational stability of the AC sub-microgrid. The hybrid microgrid incorporates separate AC and DC buses for connecting AC and DC loads, respectively, with bidirectional energy exchange between the two sub-microgrids realized by a bidirectional AC/DC converter. Specifically, disconnection of the converter isolates the AC and DC sub-microgrids for independent operation, while its connection facilitates bidirectional power flow between AC and DC buses [18].

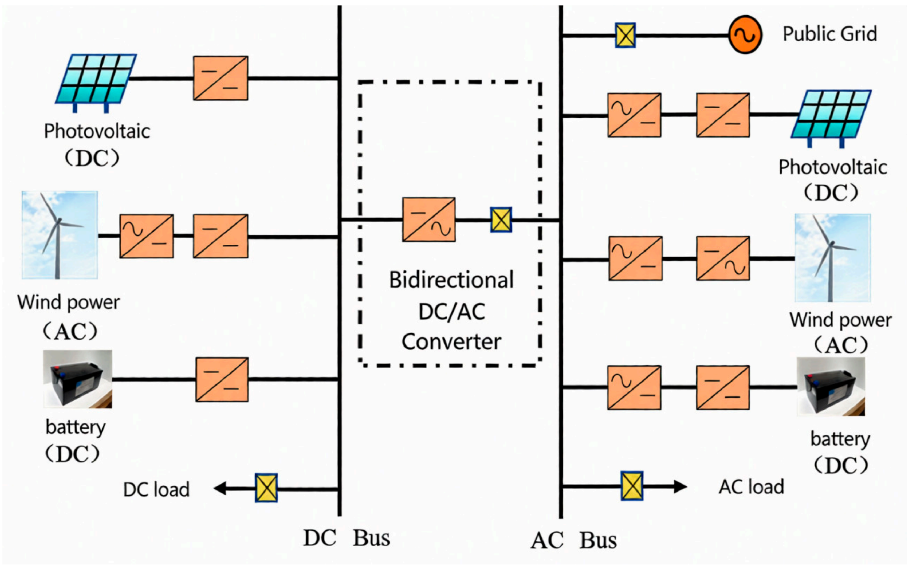


Figure 1. Typical topology of a microgrid.

The bidirectional AC/DC converter adopts a three-phase voltage-source two-level topology, as shown in Figure 2. Here, L_1 and L_2 represent filter inductors, R_1 and R_2 are the equivalent internal resistances of the inductors, and C is the AC-side filter capacitor. C_{dc} represents the DC filter capacitor, u_{dc} is the DC-side bus voltage, i_L is the DC-side load current, and i_{dc} represents the DC-side input/output current. u_a, u_b, and u_c are the three-phase voltages on the AC side of the converter, i_k is the AC-side current, and i_{gk} is the grid-side current. u_{ga}, u_{gb}, and u_{gc} denote the three-phase voltages of the AC grid. S1–S6 are insulated-gate bipolar transistors (IGBT), controlling their on/off states facilitates bidirectional power flow between the AC and DC sides.

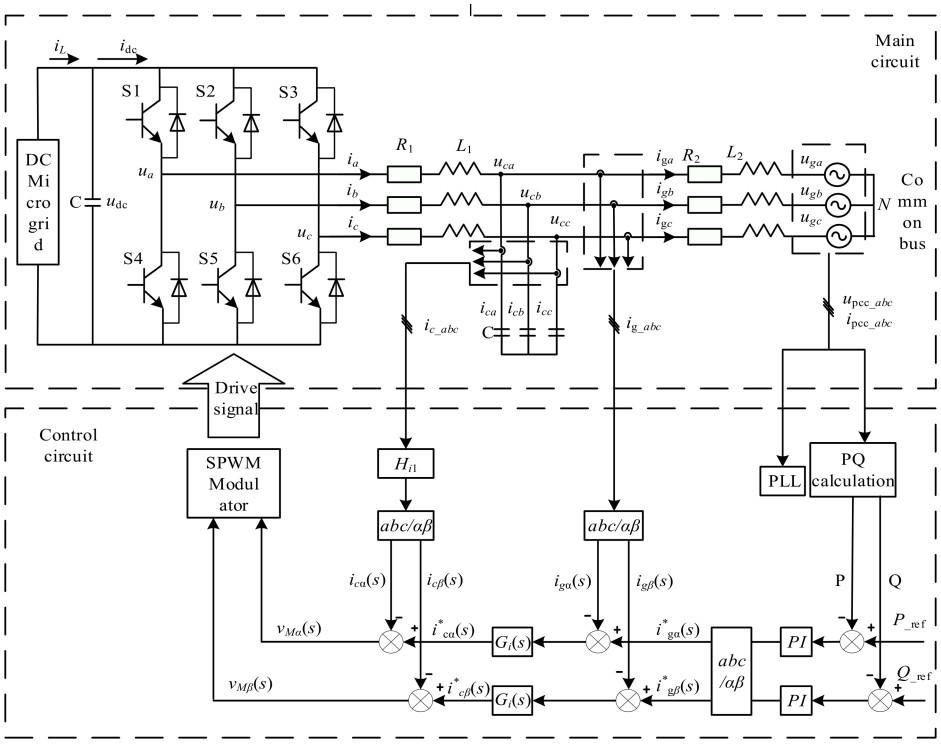


Figure 2. Main circuit and control circuit diagram of a bidirectional AC/DC converter.

2.2. Mathematical Model of the AC/DC Converter in the dq Coordinate System

According to Kirchhoff's Voltage Law (KVL), the basic voltage and current dynamic equations of the bidirectional AC/DC converter are first established in the three-phase stationary *abc* coordinate system. By applying the Clark transformation, the variables are converted into the two-phase stationary $\alpha\beta$ framework. Subsequently, the Park transformation is utilized to project these variables into the two-phase rotating *dq* coordinate system. In this frame, the *d*-axis and *q*-axis are defined as the active and reactive power axes, respectively. The resulting mathematical model in the *dq* frame is expressed as:

$$\begin{cases} L\frac{di_d}{dt} = u_d - Ri_d - u_{cd} + \omega Li_q \\ L\frac{di_q}{dt} = u_q - Ri_q - u_{cq} - \omega Li_d \\ C\frac{du_{dc}}{dt} = i_L - \frac{3}{2}\sum\limits_{k=d,q} S_k i_k \end{cases} \quad (1)$$

As shown in the equations above, the bidirectional AC/DC converter in the *dq* frame is a complex, strongly coupled nonlinear system. To effectively apply the second-order LADRC strategy for the outer voltage loop, the plant model must be decoupled and reconstructed into a standard second-order form. By taking the derivative of the DC-bus

voltage equation with respect to time (t) and substituting the current derivatives (di_d/dt and di_q/dt) into it, the dynamic model is rewritten as a second-order differential equation:

$$\begin{aligned}\frac{d^2u_{dc}}{dt^2} &= \frac{3}{2LC}\sum_{k=d,q} S_k u_{ck} + \frac{3R}{2LC}\sum_{k=d,q} S_k i_k \\ &-\frac{3}{2LC}\sum_{k=d,q} S_k u_k - \frac{3\omega}{2C}(S_d i_q - S_q i_d) + \frac{1}{C}\dot{i}_L\end{aligned} \tag{2}$$

By redefining all internal coupling dynamics and external load variations as a generalized total disturbance f, the system is simplified into a unified second-order structure $\ddot{y} = f + b_0 u$. This transformation establishes the direct mathematical foundation for the LADRC voltage controller. It should be noted that the above reduced-order second-order model is established under the commonly used bandwidth-separation assumption of cascaded control. Specifically, the inner current loop is designed to be sufficiently faster than the outer voltage loop, so that within the effective design bandwidth of the voltage controller, the current loop can be approximated as an ideal controlled channel. Therefore, Equation (2) is intended for outer-loop controller synthesis and analysis, rather than as an exact full-order representation of all converter dynamics.

3. Bus Voltage Control System Based on Improved LADRC

Based on traditional linear active disturbance rejection control (LADRC), an improved LADRC technique is proposed for the DC-bus voltage control problem, with the overall control framework shown in Figure 3. The LADRC mainly consists of three parts: a linear tracking differentiator (LTD), a linear extended state observer (LESO), and a linear state error feedback (LSEF) law.

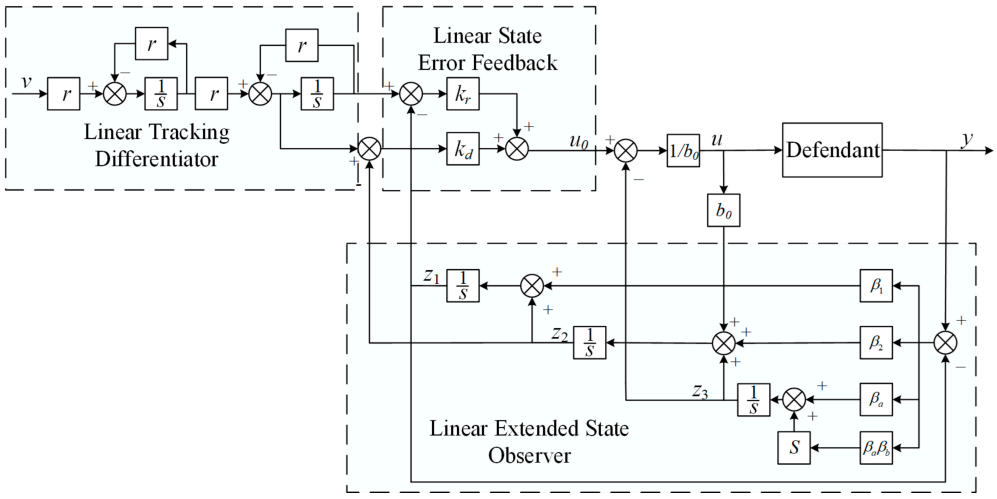


Figure 3. Improved second-order LADRC architecture.

To apply the abstract LADRC theory to an actual physical AC/DC converter system, the mapping between the variables in Figure 3 and the physical converter variables must be clarified. In this voltage control framework, the system input is the DC-bus voltage reference, and the system output is the actual sampled DC-bus voltage. The controller output acts on the "Plant," which is equivalent to the d-axis active current command in the inner current loop. The "Plant" represents the equivalent generalized controlled model comprising the closed-loop transfer function of the inner current loop, converter losses, and the DC-side filter capacitor.

3.1. Design of the Second-Order Linear Tracking Differentiator (LTD)

In traditional control frameworks, a sudden step change in the DC-bus voltage reference introduces a massive initial error, forcing the system to face a severe contradiction between fast dynamic response and large voltage overshoot. To resolve this inherent contradiction, a linear tracking differentiator (LTD) is introduced at the input stage of the controller.

The LTD aims to smooth the rigid step reference signal into a trackable, continuous trajectory. Based on standard tracking differential theory, the expression of the bus voltage reference $v(t)$ after being processed by a second-order LTD in the complex frequency (s) domain is defined as:

$$v_1(s) = \frac{1}{(\tau s + 1)^2} v(s) \tag{3}$$

where τ represents the time constant. By introducing a bandwidth parameter $r = 1/\tau$, this transfer function can be converted into a state-space form. This design enables the controller to smoothly extract the reference signal and its derivative, thereby fundamentally eliminating the step overshoot without sacrificing dynamic tracking speed.

$$\begin{cases} R_1(\mathrm{s}) = \frac{r^2}{(s+r)^2} v(s) \\ R_2(\mathrm{s}) = s\frac{r^2}{(s+r)^2} v(s) \end{cases} \tag{4}$$

Then, the linear error feedback rate designed by the above formula is shown as follows:

$$u_0 = k_p(r_1 - z_1) + k_d(r_2 - z_2) \tag{5}$$

The closed-loop transfer function of the converter is obtained as follows:

$$G(s) = \frac{k_d r^2 s + k_p r^2}{s^4 + (k_d + 2r)s^3 + (2rk_p + k_d r^2)s + k_p r^2} \tag{6}$$

Based on the design idea of pole placement, to simplify the analysis process, the influence of zeros is not considered for the time being. Combined with the above formula, it can be further derived that:

$$\begin{aligned} &s^4 + (k_d + 2r)s^3 + (2rk_p + k_d r^2)s + k_p r^2 \\ &= (s + r)^2(s^2 + k_d s + k_p) \\ &= (s + \omega_c)^4 \end{aligned} \tag{7}$$

The parameters of LTD and LSEF are calculated as shown in the following formula:

$$\begin{cases} r = \omega_c \\ k_p = \omega_c^2 \\ k_d = 2\omega_c \end{cases} \tag{8}$$

Among them, k_p and k_d denote the proportional gain and derivative gain of the controller, respectively. The controller bandwidth is characterized by the parameter $r = \omega_c$, and the controller parameters are determined according to the pole-placement principle. By properly selecting ω_c, a desirable balance between response speed and system robustness can be achieved.

3.2. Improvement of the Design of Linear Extended State Observer (LESO)

By improving the linear extended state observer (LESO), the selection of the controller gain ω_c is linked to the stability of the controller, and the transfer functions of the state variables Z_1, Z_2, and Z_3 are constructed in the frequency domain:

$$\begin{cases} Z_1 = \frac{3\omega_0 s^2 + 3\omega_0^2 s + \omega_0^3}{(s+\omega_0)^3} y + \frac{b_0 s}{(s+\omega_0)^3} u \\ Z_2 = \frac{3\omega_0^2 s^2 + \omega_0^3 s}{(s+\omega_0)^3} y + \frac{b_0 (s+3\omega_0) s}{(s+\omega_0)^3} u \\ Z_3 = \frac{\omega_0^3 s^2}{(s+\omega_0)^3} y - \frac{b_0 \omega_0^3}{(s+\omega_0)^3} u \end{cases} \tag{9}$$

where ω_0—observation gain of the observer, and y:

$$\begin{aligned} \ddot{y} &= -a_1 \dot{y} - a_2 y + w + (b - b_0) u + b_0 u \\ &= f + b_0 u \end{aligned} \tag{10}$$

In the formula: $b_0 = 3/(2LC)$

f-disturbance, $f = -a_1 \dot{y} - a_2 y + w + (b - b_0) u$.

According to Equations (7) and (8), the disturbance-observation transfer function of LESO is obtained as:

$$\phi_a(s) = \frac{z_1}{f(y, \dot{y}, w)} = \frac{\beta_3}{\beta_1 s^2 + \beta_2 s + \beta_3} \tag{11}$$

The observation effect of the linear extended state observer on disturbances is determined by the characteristics of $\phi_a(s)$. As a second-order system, Equation (9) shows that $\phi_a(s)$ has a contradiction between response speed and overshoot, and exhibits a phase-lag phenomenon in frequency domain analysis. These issues reflect the inherent defects of the traditional LESO. Therefore, an improved design is carried out for the observation gain coefficient β_3, and the improved expression is as follows:

$$\beta_3(s) = \beta_a(1 + \beta_b s) \tag{12}$$

In the formula:

β_a—Proportional coefficient;

β_b—Differential coefficient.

This design can effectively improve the phase-lag problem in the observation process, and the disturbance-observation transfer function can be expressed as follows:

$$\phi_a(s) = \frac{\beta_a(1 + \beta_b s)}{\beta_1 s^2 + (\beta_2 + \beta_a \beta_b) s + \beta_a} \tag{13}$$

Among them, β_a and β_b need to be coordinated with the observer bandwidth ω_0 and the controller bandwidth ω_c. β_a can inherit the dominant role of the traditional β_3, and its initial value can be set as $\beta_a \approx {\omega_0}^3$ to ensure the observation capability in the mid-low frequency range. Due to the introduction of the zero point $s = -1/\beta_b$, the phase characteristics in the high-frequency range are improved, and the phase lag of disturbance observation is reduced. Therefore, the zero frequency $\omega = 1/\beta_b$. The main frequencies of grid voltage fluctuations include the fundamental frequency of 50 Hz (314 rad/s), the 2nd harmonic of 100 Hz (628 rad/s), etc. To cover the above frequency bands, the zero frequency is initially set to 500 rad/s to calculate the value of β_b.

Compared with Equation (9), Equation (11) adds a zero point. In the time domain, the role of the zero point can improve the response speed of the system; from a frequency domain perspective, a series lead network is added, which can reduce the problem of phase lag. It should be emphasized that the introduced PD term does not suppress noise

directly. Instead, its main role is to improve the phase characteristics of the observer by introducing a compensating zero, so that the disturbance-estimation performance can be enhanced without relying solely on a further increase in observer bandwidth. In this sense, the proposed design helps mitigate the noise-amplification problem that would otherwise arise from excessively large observer gains in conventional LESO tuning.

4. Performance Analysis of Improved LADRC

4.1. Improve the Tracking and Anti-Disturbance Analysis of LTD

According to Equation (2), the tracking characteristic analysis of the DC-bus voltage and the influence of disturbances on LTD are carried out, that is, the frequency Bode analysis of r is performed, as shown in Figure 4.

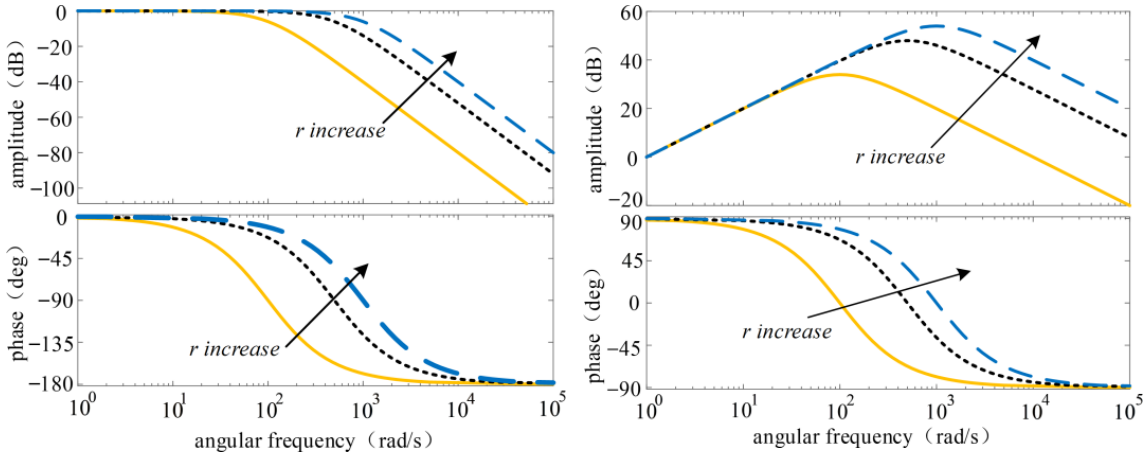


Figure 4. Bode plot of the frequency domain characteristics of the improved LTD under different bandwidth parameters r. (**a**) Traceability frequency analysis; (**b**) analysis of anti-disturbance capability against disturbances.

It can be seen from Figure 4 that as r (ω_c) increases, its bandwidth and gain range also expand, and the system's tracking performance, response speed, and robustness are improved. At the same time, as the bandwidth increases, the system's tracking performance for differential signals improves. However, it should be noted that when the value of r is too high, it may cause system instability. Therefore, it is necessary to determine the optimal value of r through a comprehensive evaluation.

4.2. Analysis of Improving the Tracking Anti-Disturbance Performance of LESO

According to Equations (7) and (10), the improved transfer functions of Z_1, Z_2, and Z_3 can be obtained as follows:

$$\begin{cases} Z_1 = \frac{3\omega_0 s^2+3\omega_0^2 s+\omega_0^3}{(s+\omega_0)^3} y + \frac{b_0 s}{(s+\omega_0)^3} u \\ Z_2 = \frac{3\omega_0^2 s^2+\omega_0^3 s}{(s+\omega_0)^3} y + \frac{b_0 s(s+3\omega_0)}{(s+\omega_0)^3} u \\ Z_3 = \frac{\omega_0^3 s^2+\omega_0^3 \beta_b s^3}{(s+\omega_0)^3} y - \frac{b_0 \omega_0^3 (1+\beta_b)}{(s+\omega_0)^3} u \end{cases} \tag{14}$$

Similar to the traditional second-order LADRC, let the tracking error be $e_1 = z_1 - y$, $e_2 = z_2 - \dot{y}$, $e_3 = z_3 - f$ and we can obtain:

$$\begin{cases} e_1 = -\frac{s^3}{(s+\omega_0)^3}y + \frac{b_0 s}{(s+\omega_0)^3}u \\ e_2 = -\frac{(s+3\omega_0)s^3}{(s+\omega_0)^3}y + \frac{b_0 s}{(s+\omega_0)^3}u \\ e_3 = -\left(s^2 - \frac{\omega_0^3 s^2 + \omega_0^3 \beta_b s^3}{(s+\omega_0)^3}\right)y + \left(b_0 - \frac{b_0 \omega_0^3 (1+\beta_b)}{(s+\omega_0)^3}\right)u \end{cases} \quad (15)$$

It can also be concluded that:

$$\begin{cases} e_{1s} = \lim\limits_{s\to 0} s e_1 = 0 \\ e_{2s} = \lim\limits_{s\to 0} s e_2 = 0 \\ e_{3s} = \lim\limits_{s\to 0} s e_3 = 0 \end{cases} \quad (16)$$

It is shown that the improved second-order LADRC also has good error estimation ability, verifying that the tracking performance has been improved.

For enhancing anti-interference ability, after improving the proportional-derivative link in LESO implementation, its anti-disturbance-observation transfer function is in Equation (11). Frequency domain analysis (Figure 5) shows that the improved LESO has a significantly increased gain, enhancing the system's anti-interference ability and effectively optimizing the phase-lag problem.

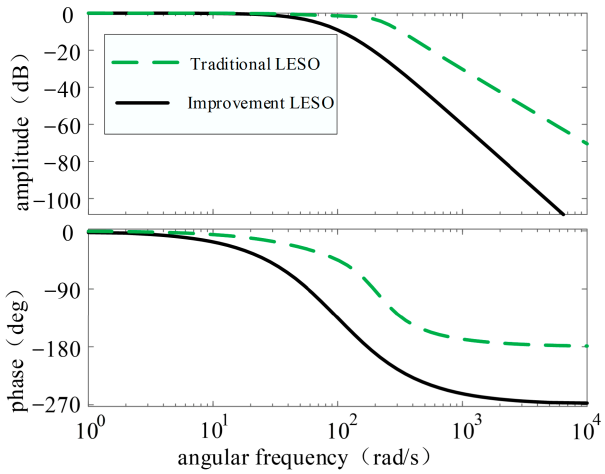


Figure 5. Frequency analysis of disturbance transfer functions for traditional LESO and improved LESO.

Improving the independent contribution analysis of LESO: Traditional LESO often needs to increase the observation gain when pursuing high anti-disturbance performance, which will inevitably amplify the high-frequency noise of the sensor and bring about severe phase lag. In this paper, by introducing a proportional-derivative link (i.e., adding a high-frequency zero point) into LESO, it can be intuitively seen from the frequency domain analysis in Figure 5 that under the same observation bandwidth, the amplitude–frequency gain of the improved LESO is enhanced, and the phase lag is effectively compensated in the medium and high-frequency bands. This means that when the microgrid faces load mutations (external disturbances) or model parameter drifts (internal disturbances), the improved LESO can estimate the total disturbance f at a faster speed and with lower noise sensitivity, thereby generating the compensation control quantity in a timely manner, which greatly enhances the anti-disturbance recovery capability of the system. From the practical control perspective, the main advantage of the proposed PD-enhanced LESO lies in the fact that it improves disturbance estimation and phase compensation under the same or similar observer bandwidth, instead of pursuing performance only through bandwidth

enlargement. Therefore, compared with the conventional approach of simply increasing ω_0, the proposed observer structure is less likely to aggravate high-frequency noise sensitivity.

4.3. Performance Analysis of Improved LADRC in Bus Voltage Control System

To demonstrate the improvement in control performance of the improved LADRC in DC-bus voltage control, this section will prove the stability of the control system using the Liénard–Chipart stability criterion [19]. According to Equation (12), the system output consists of two parts: the tracking term and the disturbance term. When disturbances are not considered for the time being, the tracking of the reference signal can be achieved by adjusting ω_c and ω_0 [20]. For the bidirectional power converter, its disturbances mainly come from the grid-side current, and based on this, the control structure of the bidirectional power converter can be determined as shown in Figure 6.

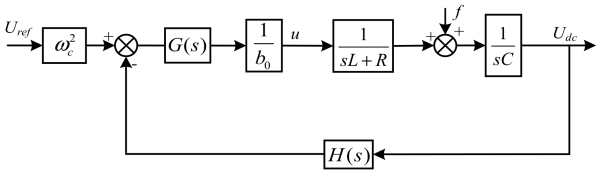


Figure 6. Overall system structure of the improved LADRC bidirectional power converter.

As analyzed from Figure 6, the transfer function of the DC-bus voltage can be expressed as:

$$U_{dc} = G_1(s)\omega_c^2 U_{ref} + G_2(s)f \tag{17}$$

In the formula:
U_{dc}—Actual value of bus voltage;
U_{ref}—Reference setting value of bus voltage;
f—Interference in the system;
$G_1(s)$—Transfer function following the DC-bus voltage;
$G_2(s)$—Transfer function of external interference.

Figure 7 compares the practical disturbance rejection performance of two complete control strategies, namely the conventional LADRC with the traditional LESO and the improved LADRC with the PD-enhanced LESO. The previous description only highlighted the observer difference, which may have caused ambiguity between the controller level and observer level. As shown in the figure, the improved LADRC exhibits a smaller disturbance-induced fluctuation amplitude under the same operating condition, indicating that the proposed observer improvement effectively enhances the disturbance-estimation accuracy and improves the anti-disturbance capability of the overall controller.

When external disturbances and other interferences are not considered, the closed-loop transfer function of the system can be obtained as:

$$y = \frac{(s+\omega_0^3)\omega_c^2}{a_5 s^5 + a_4 s^4 + a_3 s^3 + a_2 s^2 + a_1 s^1 + a_0} \tag{18}$$

In the formula:

$$\begin{aligned}
a_5 &= b_0 LC \\
a_4 &= b_0 LC(3\omega_0 + 2\omega_c) + b_0 RC \\
a_3 &= b_0 LC(3\omega_0^2 + \omega_c^2 + 6\omega_0\omega_c - \omega_0^3\beta_b) \\
&\quad +3b_0 RC\omega_0 + 2b_0 RC\omega_c + (\omega_0^3\beta_b - 2\omega_c) \\
a_2 &= b_0 RC(3\omega_0^2 + \omega_c^2 + 6\omega_0\omega_c - \omega_0^3\beta_b) \\
&\quad +(3\omega_c^2\omega_0 + 6\omega_c(\omega_0^2 - \omega_0) + \omega_0^3) \\
a_1 &= 3\omega_0^2\omega_c^2 + 2\omega_0^3\omega_c - 6\omega_0^2\omega_c \\
a_0 &= 2\omega_0^3\omega_c - \omega_0^3\omega_c^2
\end{aligned}$$

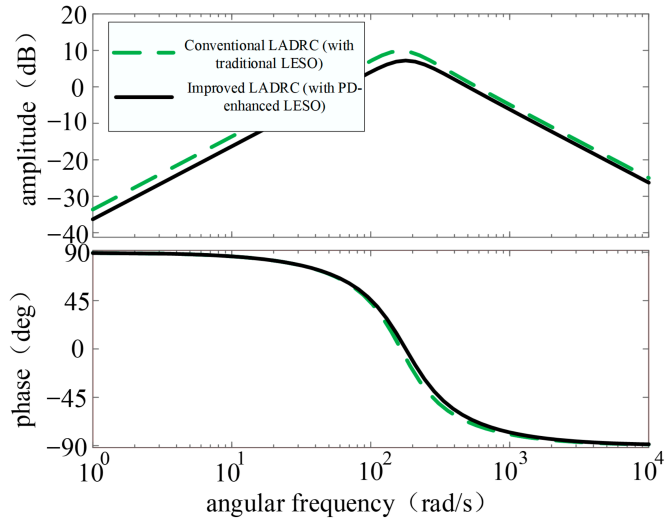


Figure 7. Comparison of disturbance rejection performance between conventional LADRC with traditional LESO and improved LADRC with PD-enhanced LESO in the practical system.

It can be known from the parameters of this design (i = 0, 1, 2, 3, 4, 5) that, according to the Liénard–Chipart stability criterion, the sufficient and necessary condition for the system to remain stable is that its odd-order Hurwitz determinants are positive. Combined with the parameters in Table 1, it can be seen that:

$$\Delta_5 = \begin{vmatrix} a_1 & a_0 & 0 & 0 & 0 \\ a_3 & a_2 & a_1 & a_0 & 0 \\ a_5 & a_4 & a_3 & a_2 & a_1 \\ 0 & 0 & a_5 & a_4 & a_3 \\ 0 & 0 & 0 & 0 & a_5 \end{vmatrix} > 0, \Delta_3 = \begin{vmatrix} a_1 & a_0 & 0 \\ a_3 & a_2 & a_1 \\ a_5 & a_4 & a_3 \end{vmatrix} > 0 \quad (19)$$

Table 1. LADRC controller parameters.

Controller Parameters	Numerical Value
Controller Bandwidth/Hz	3000
Observer bandwidth/Hz	500
b_0	2.5×10^5
Proportionality coefficient	1000
Derivative coefficient	0.04

It can be known from the above results that the system is stable.

5. Simulation Verification

To evaluate the performance of the improved LADRC under representative disturbances in AC/DC hybrid microgrids, the simulation study considers source-side, grid-side, and load-side operating scenarios. In the simulation model, photovoltaic source fluctuation is directly represented by irradiance variation in the PV array, whereas in the hardware platform, the same class of source-side disturbance is equivalently emulated by PV-side voltage reduction. In this way, the simulation and experimental studies remain physically consistent while being suitable for their respective implementation conditions.

To evaluate the performance of the improved LADRC strategy under multiple operating conditions, a microgrid simulation model was built based on Matlab/Simulink, with specific simulation parameters listed in Table 1. To compare and analyze the performance differences between the improved and traditional LADRC, a comparative analysis of multi-

condition simulations was conducted. Figure 8 shows the simulation waveforms of the bus voltage under different operating conditions, covering the following typical conditions: (1) the grid-side voltage experiences a 15% symmetric drop and a 40% asymmetric drop respectively; (2) the light intensity of the photovoltaic array increases; (3) the experiment of switching between light load and heavy load on the DC side.

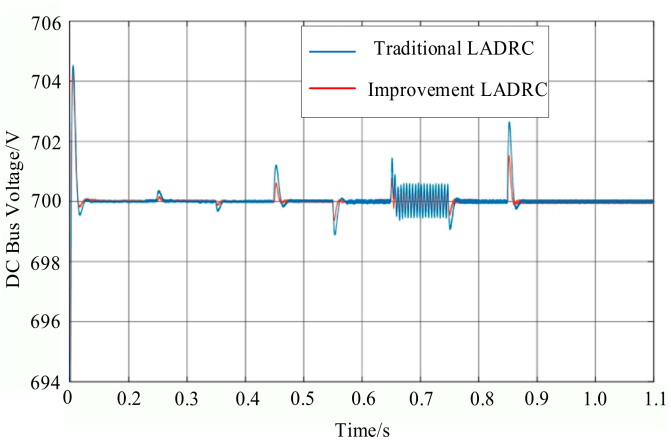


Figure 8. Global simulation operation waveforms of the AC/DC hybrid microgrid system.

The parameters listed in Table 1 were selected by considering the trade-off among dynamic response speed, disturbance-estimation capability, and noise sensitivity. Specifically, the controller bandwidth mainly determines the transient response of the outer voltage loop, while the observer bandwidth affects the convergence rate and accuracy of disturbance estimation. In practical tuning, the controller bandwidth should be chosen to ensure sufficiently fast voltage regulation without introducing excessive overshoot, whereas the observer bandwidth should be high enough to capture the dominant disturbance dynamics but should not be increased excessively, in order to avoid unnecessary amplification of high-frequency measurement noise. In addition, β_a is selected to preserve the dominant low- and mid-frequency disturbance-observation capability of the conventional LESO, whereas β_b is determined according to the desired zero location for phase compensation in the disturbance frequency range of interest. Therefore, the final parameter values were obtained according to the combined consideration of theoretical design requirements and practical closed-loop performance.

(1) Symmetrical and asymmetrical dips of grid voltage

Grid faults or disturbances can cause grid voltage dips. Therefore, this phenomenon is simulated. In the simulation, a symmetrical grid voltage dip of 15% is set at [specific time], and it recovers at [specific time], as shown in Figure 9a. The grid-side voltage has an asymmetrical dip of 40% at [specific time] and recovers after 40 ms, with the simulation results shown in Figure 9b.

Analysis of Figure 9a shows that when the grid voltage experiences a 15% symmetrical drop, the traditional LADRC takes 10 ms to reach 1.0 p.u., with small-range steady-state error fluctuations of 0.0001 p.u. during this period; in contrast, the improved LADRC reaches 1.0 p.u. in only 7 ms with a smaller fluctuation range. During the grid voltage recovery phase, the improved LADRC has a faster response speed than the traditional LADRC. The maximum voltage fluctuation of the former is 0.0002 p.u., while that of the latter is 0.00045 p.u., indicating that this design effectively resolves the contradiction between overshoot and rapidity. Figure 9b shows that after an asymmetric drop in grid voltage, the improved LADRC can achieve stability in approximately 5 ms, with voltage fluctuations of about 0.0006 p.u., and can quickly restabilize when the grid voltage recovers at 40 ms. However, for the traditional LADRC during an asymmetric drop, the voltage

fluctuation reaches 0.0009 p.u., and it takes 10 ms to stabilize, with its rapidity significantly weaker than that of the improved scheme. Overall, the improved LADRC performs better in terms of dynamic response speed, steady-state accuracy, and ability to resist grid voltage disturbances.

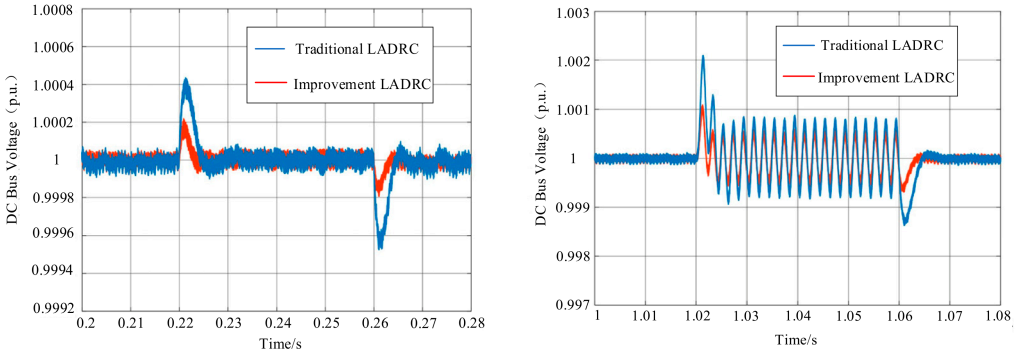


Figure 9. Grid voltage sag. (**a**) The grid voltage drops symmetrically by 15%; (**b**) the grid voltage drops asymmetrically by 40%.

(2) Simulation of increased light intensity

When the light intensity suddenly increases, the output voltage of the photovoltaic cell suddenly rises, which in turn causes fluctuations in the DC-bus voltage. When it recovers, the output voltage of the photovoltaic cell array decreases, and the simulation waveform is shown in Figure 10.

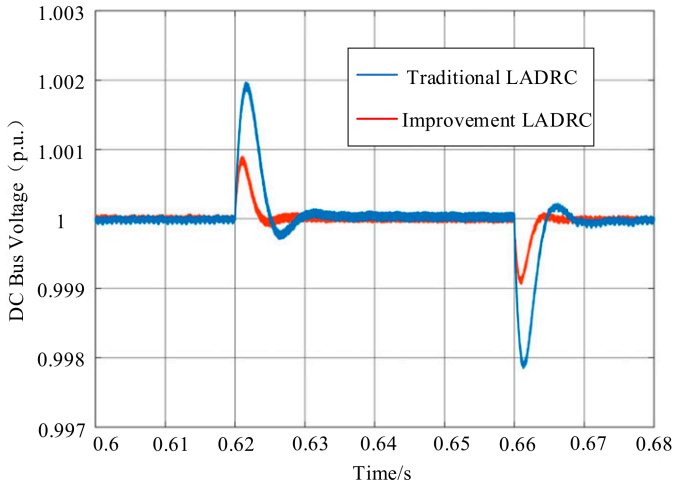


Figure 10. Enhanced light intensity.

It can be seen from Figure 10 that $t = 0.62$ s when the light intensity increases, the bus voltage of the traditional LADRC takes 10 ms to reach 1.0 p.u., with a steady-state error fluctuation of 0.0001 p.u., while the improved LADRC reaches 1.0 p.u. in only 7 ms, showing better stability. During the grid voltage recovery process, the improved LADRC stabilizes in only 5 ms, while the traditional LADRC takes about 10 ms, indicating that the response speed of the improved scheme is significantly faster.

In the simulation study, photovoltaic source fluctuation is directly represented by irradiance variation in the PV array model, whereas in the hardware platform, the same class of source-side disturbance is equivalently emulated by PV-side voltage reduction.

(3) DC-side load shedding simulation

An increase in DC load often leads to a rise in DC-bus voltage. Figure 11 shows the simulation comparison results between 1.5 s of the traditional LADRC and the improved LADRC under the condition of simulating the DC load with a time-multiplying operation. It can be seen that after the load increases, the traditional LADRC takes 10 ms to restore the bus voltage to 1.0 p.u., with a maximum overshoot of 0.005 p.u., while the improved LADRC reaches 1.0 p.u. in only 6 ms, with a maximum overshoot of only 0.002 p.u., indicating that the improved control strategy has better performance.

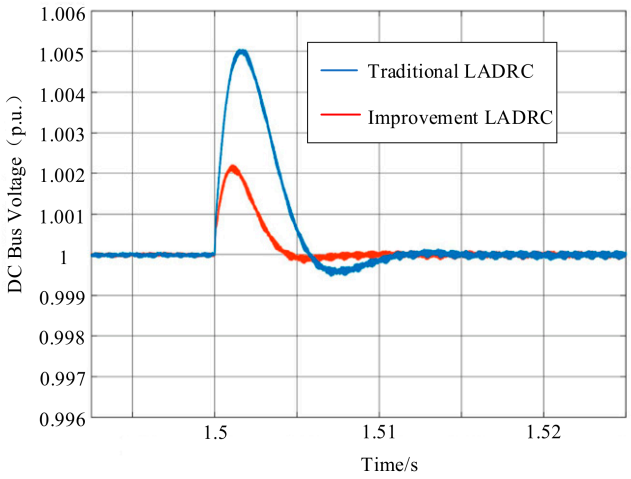


Figure 11. The DC-side load increases.

6. Experimental Verification

6.1. Introduction to the Experimental Platform

To further verify the feasibility of the proposed improved LADRC strategy in a practical system, a full-hardware prototype platform was built instead of a simple hardware-in-the-loop (HIL) test. In order to maintain consistency with the disturbance scenarios analyzed in the simulation section, the experimental study is expanded from only DC-side load switching to representative source-side, grid-side, and load-side disturbances. Specifically, a grid voltage dip is introduced on the AC side by a programmable AC power supply, PV-side voltage reduction is applied to emulate source-side photovoltaic fluctuation, and DC-side load switching is realized by a programmable electronic load.

As shown in Figure 12, the main circuit of the converter experimental platform consists of the converter platform itself, a photovoltaic simulator, an electronic load, a programmable AC power supply, an oscilloscope, and the associated voltage and current probes. On the DC side, a photovoltaic simulator is connected to provide a stable DC input source, while an electronic load is utilized to perform precise power switching and load variation tests. On the AC side, a programmable AC power supply is employed to emulate grid voltage disturbance conditions. The control core adopts a digital control board based on the TI TMS320F28335 DSP, in which the proposed improved LADRC algorithm is discretized and implemented in C language, with the control cycle set to 10 kHz. During the experiments, voltage and current waveforms are sampled in real time by Tektronix high-voltage differential probes and current probes, and ultimately recorded by a Tektronix oscilloscope for comparative analysis.

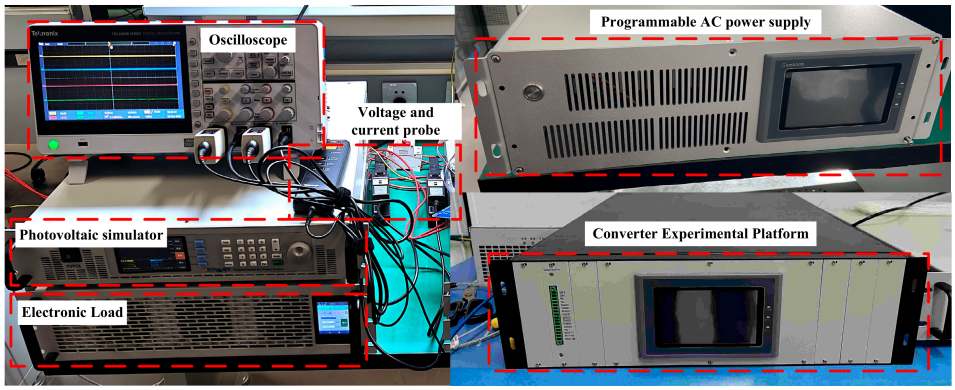
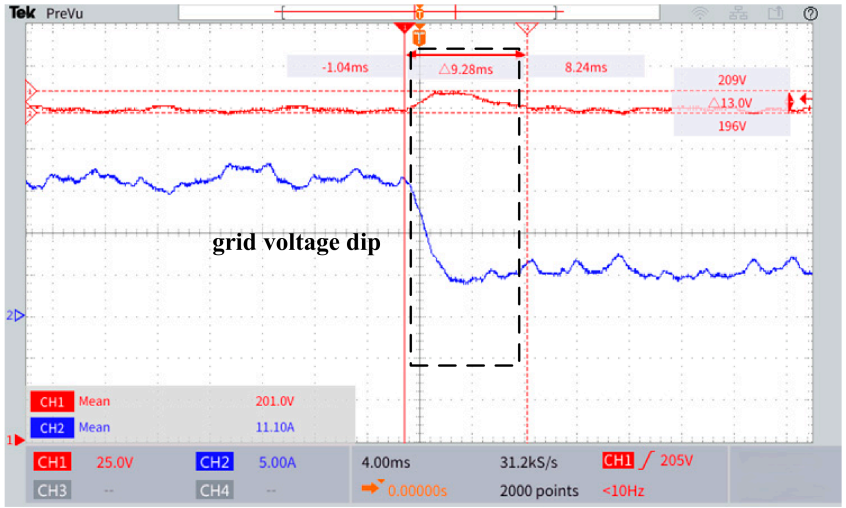


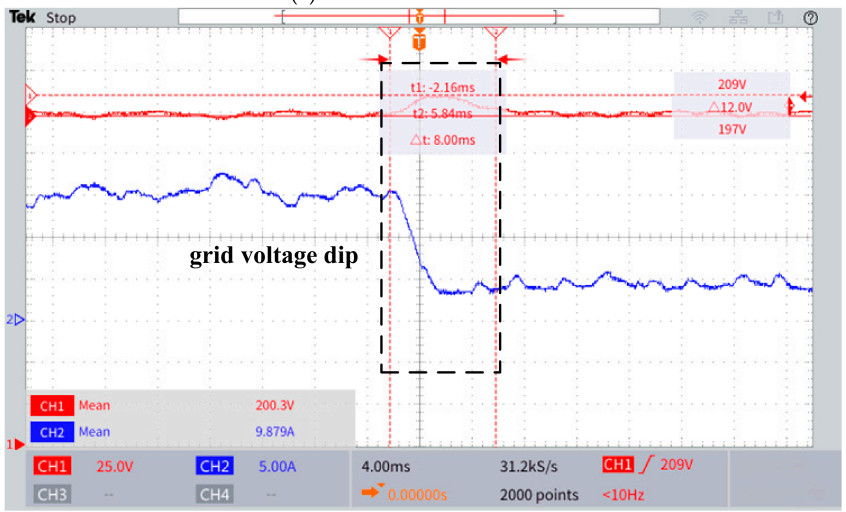
Figure 12. Experimental platform.

6.2. Experimental Verification Under Grid Voltage Dip

To verify the disturbance rejection capability of the proposed controller under grid-side disturbance, a grid voltage dip experiment was conducted on the hardware platform. The comparative waveforms before and after the improvement are shown in Figure 13.



(**a**) Conventional LADRC



(**b**) Improved LADRC

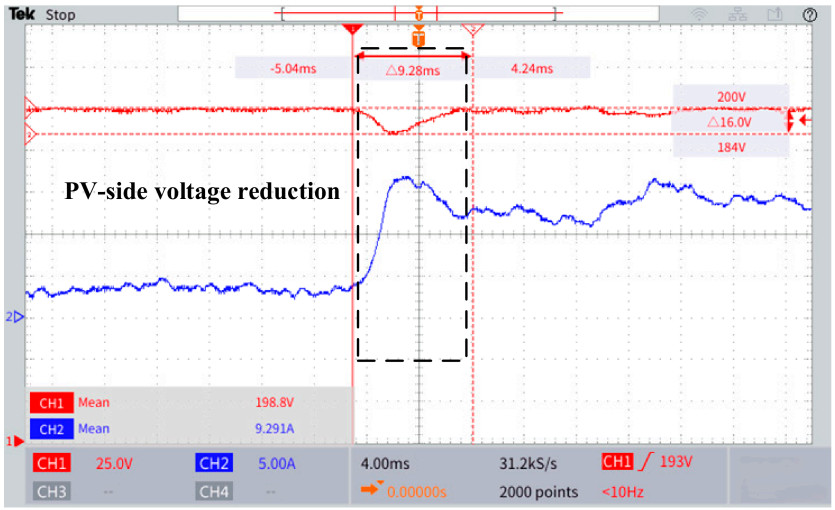
Figure 13. Hardware experimental waveforms under grid−voltage dip.

As can be observed, when the grid voltage suddenly dips, both control strategies can maintain the DC-bus voltage within a limited fluctuation range; however, the improved

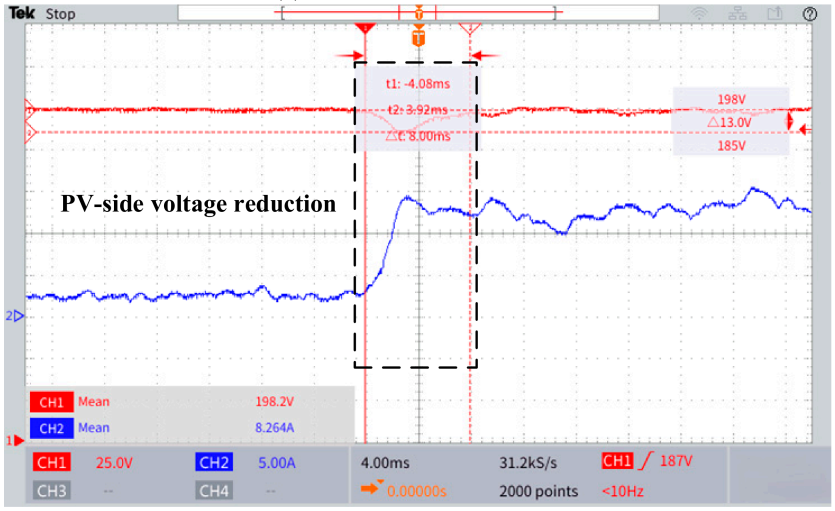
LADRC exhibits a faster recovery and a smaller transient deviation. According to the oscilloscope cursor measurements, the DC-bus voltage fluctuation amplitude decreases from 13.0 V under the conventional LADRC to 12.0 V under the improved LADRC, while the recovery interval is shortened from 9.28 ms to 8.00 ms. This indicates that the proposed PD-enhanced LESO improves the disturbance estimation and compensation capability under grid-side voltage disturbance, thereby enhancing the transient regulation performance of the DC bus.

6.3. Experimental Verification Under PV-Side Voltage Reduction

To experimentally evaluate the controller performance under source-side disturbance, a PV-side voltage reduction test was further carried out on the hardware platform. The corresponding waveforms before and after the controller improvement are shown in Figure 14.



(**a**) Conventional LADRC



(**b**) Improved LADRC

Figure 14. Hardware experimental waveforms under PV−side voltage reduction.

It can be seen that the sudden reduction in PV-side voltage causes a transient disturbance to the DC bus. Compared with the conventional LADRC, the improved LADRC suppresses the DC-bus voltage fluctuation more effectively and restores the steady-state condition faster. Based on the oscilloscope measurements, the transient voltage deviation is reduced from 16.0 V to 13.0 V, and the recovery interval is shortened from 9.28 ms to 8.00 ms

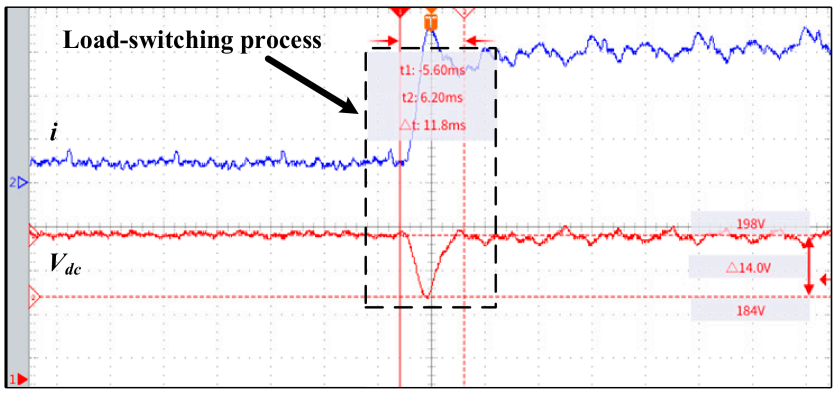
after the proposed improvement is applied. These results verify that the proposed control strategy can effectively enhance the DC-bus voltage stability under source-side fluctuation.

6.4. Experimental Verification Under DC-Side Load Switching

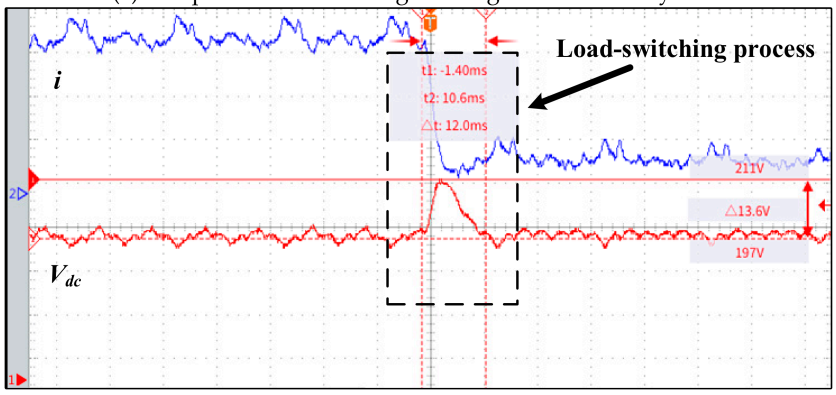
In addition to the grid-side and source-side disturbance tests, comparative hardware experiments were also conducted under DC-side load-switching conditions, including light-load to heavy-load switching and heavy-load to light-load switching. The corresponding waveforms are shown in Figures 15 and 16.

To make the dynamic-performance comparison more explicit, the transient behaviors in Figures 15 and 16 were further evaluated using two quantitative indices, namely the peak-to-peak DC-bus voltage deviation and the settling time under the same measurement criterion.

For the light-load-to-heavy-load transition, the improved LADRC reduces the peak-to-peak voltage deviation by 3.2 V and shortens the settling time by 1.8 ms compared with the conventional LADRC. For the heavy-load-to-light-load transition, the peak-to-peak voltage deviation is reduced by 3.6 V, and the settling time is shortened by 2.0 ms. These quantitative results demonstrate that the improved LADRC not only suppresses transient voltage fluctuation more effectively, but also accelerates the recovery of the DC-bus voltage after load switching. Therefore, the conclusion that the improved strategy enhances the transient response speed is supported not only by the waveform trend but also by explicit experimental indices. Quantitative comparison of hardware transient performance under DC-side load-switching conditions is shown in Table 2.

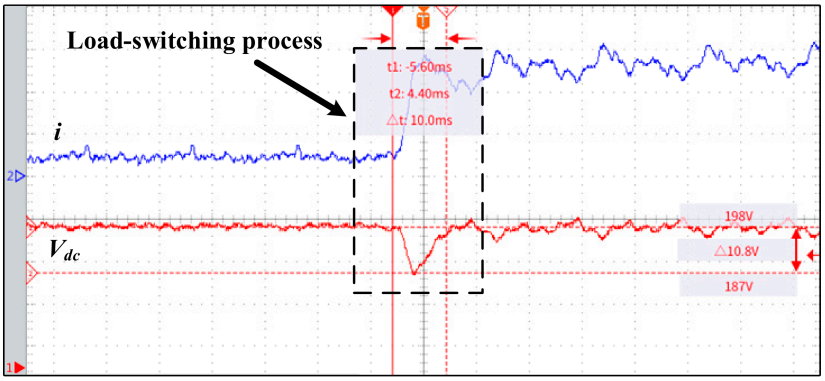


(**a**) The process of switching from light load to heavy load

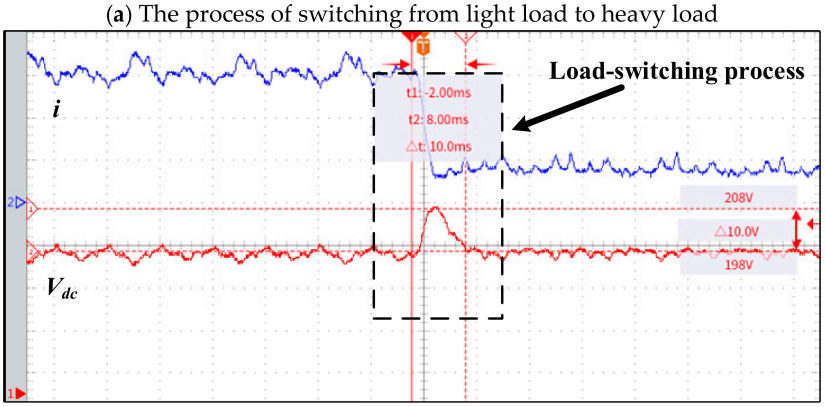


(**b**) Process of switching from heavy load to light load

Figure 15. Traditional LADRC waveform.



(**a**) The process of switching from light load to heavy load



(**b**) Process of switching from heavy load to light load

Figure 16. Improve the LADRC waveform.

Table 2. Quantitative comparison of hardware transient performance under DC-side load-switching conditions.

Operating Condition	Improvement in Peak-to-Peak Voltage Deviation	Improvement in Settling Time
Light load → heavy load	3.2 V reduction	1.8 ms shorter
Heavy load → light load	3.6 V reduction	2.0 ms shorter

Together with the PV-side voltage reduction and grid voltage dip experiments, the load-switching results demonstrate that the proposed controller achieves improved DC-bus voltage regulation under representative source-side, grid-side, and load-side disturbances.

7. Conclusions

This paper proposes an improved LADRC strategy for DC-bus voltage control of bidirectional converters in AC/DC hybrid microgrids. To address the phase lag and noise-sensitivity problems of the conventional LESO, a proportional-derivative (PD) term is introduced into the observer structure, which improves the disturbance-estimation capability without excessively increasing the observer bandwidth. Meanwhile, to alleviate the contradiction between fast response and overshoot suppression, a linear tracking differentiator (LTD) is incorporated into the outer voltage loop to smooth the reference signal and improve the dynamic tracking performance of the system. To validate the proposed control strategy, this paper combines theoretical analysis, multi-condition MATLAB/Simulink simulations, and full-hardware prototype experiments. The simulation study evaluates the controller under grid voltage sag, photovoltaic-side source fluctuation, and DC-side load disturbance conditions, while the hardware study further verifies its performance under

grid voltage dip, PV-side voltage reduction, and DC-side load-switching disturbances. The results consistently demonstrate that the improved LADRC achieves smaller DC-bus voltage fluctuation and better transient recovery performance than the conventional LADRC. In the hardware tests, the recovery interval is shortened from 9.28 ms to 8.00 ms in both the grid voltage dip and PV-side voltage reduction experiments. In addition, under DC-side load-switching conditions, the improved LADRC reduces the peak-to-peak DC-bus voltage deviation by 3.2 V and 3.6 V for the light-load-to-heavy-load and heavy-load-to-light-load transitions, respectively, while the corresponding settling times are shortened by 1.8 ms and 2.0 ms. Therefore, the proposed method offers an effective and practically applicable solution for enhancing the DC-bus voltage stability of bidirectional converters in AC/DC hybrid microgrids.

Author Contributions: Conceptualization: B.W. and Y.Z.; methodology: J.W.; software: B.W.; validation: J.W., Y.Z. and B.W.; formal analysis: Y.Z. and B.W.; investigation: B.W.; resources: Y.Z.; data curation: J.W.; writing—original draft preparation: J.W.; writing—review and editing: Y.Z.; visualization: Y.Z.; supervision: Y.Z.; project administration: Y.Z.; funding acquisition: Y.Z. All authors have read and agreed to the published version of the manuscript.

Funding: This work was supported by the National Natural Science Foundation of Hebei Province (Grant No. E2025209038).

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Gadanayak, D.A. Protection algorithms of microgrids with inverter interfaced distributed generation units—A review. *Electr. Power Syst. Res.* **2021**, *192*, 106986. [CrossRef]
2. Wang, X.; Yao, G.; Li, Y. Improved WAC Control Strategy for LCL Grid-Connected Inverters Considering Digital Control Delay in Weak Grids. *Mod. Electron. Tech.* **2024**, *47*, 108–116.
3. Wang, C.; Wu, Z.; Li, P. Research on key technologies of microgrid. *Trans. China Electrotech. Soc.* **2014**, *29*, 59–68.
4. Dagar, A.; Gupta, P.; Niranjan, V. Microgrid protection: A comprehensive review. *Renew. Sustain. Energy Rev.* **2021**, *149*, 111401. [CrossRef]
5. Jia, L.; Zhu, Y.; Du, S.; Wang, Y. Control strategy of interlinked converter for AC/DC microgrid. *Autom. Electr. Power Syst.* **2016**, *40*, 98–104.
6. Sarangi, S.; Sahu, B.K.; Rout, P.K. Review of distributed generator integrated AC microgrid protection: Issues, strategies, and future trends. *Int. J. Energy Res.* **2021**, *45*, 14117–14144. [CrossRef]
7. Jiao, J.; Meng, R.; Ren, C.; Du, Y. Control Strategy of AC/DC Bidirectional Power Converter in AC/DC Microgrid. *Power Syst. Prot. Control* **2020**, *48*, 84–92.
8. Wang, Y.; Zhao, X.; Lai, J.; Gao, L.; Song, L.; Li, G. Energy Storage Control Strategy for Photovoltaic Microgrid Based on Active Disturbance Rejection Control. *J. Electr. Eng.* **2024**, *19*, 120–129.
9. Cai, X.; Zhang, Q. A Review of Topologies and Reconfiguration of AC-DC Hybrid Microgrids. *Autom. Appl.* **2018**, *9*, 79–82.
10. Hong, Y.; Chen, B.; Dai, D.; Wu, J. Design of Synchronous Rectification BUCK DC-DC Regulated Switching Power Supply. *Mod. Electron. Tech.* **2022**, *45*, 94–100.
11. Huang, Y.; Yuan, X.; Hu, J.; Zhou, P.; Wang, D. DC-bus voltage control stability affected by AC-bus voltage control in VSCs connected to weak AC grids. *IEEE J. Emerg. Sel. Top. Power Electron.* **2015**, *4*, 445–458. [CrossRef]
12. Zhang, H.W.; Zhang, Q.J.; Liu, Y.C.; Wang, H.L.; Hu, W.B. A modified virtual generator control for dc microgrid with improved dynamic characteristics of dc bus voltage and enhanced current sharing effect. *J. Electr. Eng. Technol.* **2022**, *17*, 3445–3456. [CrossRef]
13. Hu, C.; Lu, H.; Wang, H.; Zhou, J.; Luo, S.; Ma, R.; Meng, L. Dynamic compensation control strategy of DC bus voltage based on residual generator. *Sci. Prog.* **2021**, *104*, 6886–6896. [CrossRef] [PubMed]
14. Ma, Y.; Yang, L.; Zhou, X.; Yang, X.; Zhou, Y.; Zhang, B. Linear Active Disturbance Rejection Control for DC Bus Voltage Under Low-Voltage Ride-Through at the Grid-Side of Energy Storage System. *Energies* **2020**, *13*, 1207. [CrossRef]

15. Li, H.; Xiao, S.; Yu, J. Feedforward Active Disturbance Rejection Control of Microgrid Bidirectional DC-DC Converter Based on Adaptive PSO. *Electr. Mach. Control Appl.* **2023**, *50*, 73–81.
16. Smadi, A.A.; Khoucha, F.; Amirat, Y.; Benrabah, A.; Benbouzid, M. Active Disturbance Rejection Control of an Interleaved High Gain DC-DC Boost Converter for Fuel Cell Applications. *Energies* **2023**, *16*, 1019. [CrossRef]
17. Li, B.; Ye, H.; Jia, Y.; Liu, J.; Pu, M.; Ye, Z.; Li, S.; Wang, C.; Gu, Z.J.; Sea, J.L. Improvement of Active Disturbance Rejection Control for DC Side Voltage of Photovoltaic Grid-Connected Inverters. *Adhesion* **2025**, *52*, 179–182.
18. Li, Z.; Luan, Y.; Zhang, F.; Xu, F. Optimal Scheduling of AC-DC Hybrid Microgrid Considering Interconnected Converters. *Sci. Technol. Eng.* **2024**, *24*, 14690–14698.
19. Zhang, K.; Ren, Y.; Zhao, J.; Kang, R. Fixed-Time Active Disturbance Rejection Control Scheme for Hybrid Energy Storage System Based on Cascaded Extended State Observer. *Energies* **2023**, *18*, 5917. [CrossRef]
20. Zhou, X.; Wang, J.; Ma, Y. Linear Active Disturbance Rejection Control of Grid-Connected Photovoltaic Inverter Based on Deviation Control Principle. *Energies* **2020**, *13*, 3790. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.