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A Mutual Inductance–Capacitance IPOS-Type Self-Balancing LLC Resonant Converter

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Abstract

In low-voltage-input, high-voltage-output applications, the input-parallel output-series (IPOS) LLC resonant converter experiences voltage and current imbalances due to parameter mismatches in resonant tank components. To address this issue, a self-balancing IPOS LLC resonant converter based on a shared inductance–capacitance (shared L-C) network is proposed. This topology achieves passive voltage and current self-equalization with an interconnection network of resonant inductors and capacitors between modules that does not need additional active components or complex control strategies. An analytical model based on the fundamental harmonic approximation (FHA) is developed to quantitatively assess the balancing performance, and a comparison is made with traditional structures and IPOS structures with only shared inductance. A 1.25 kW two-phase LLC resonant converter prototype is built for experimental validation. The results demonstrate that the balancing errors of the traditional structure and the shared inductance structure reach up to 25.43% and 17.63%, respectively, whereas the proposed structure significantly reduces the balancing error to only 0.43%. This study confirms that this structure provides a simple and reliable solution for voltage and current equalization in high-gain DC–DC conversion systems.

Keywords: input-parallel output-series (IPOS); LLC resonant converter; self-balancing; shared inductance–capacitance; passive balancing

1. Introduction

Many high-output-voltage applications, such as large-capacity photovoltaic power generation for DC transmission and offshore wind power delivery, require the conversion of low-voltage input to high-voltage output [1,2]. In these scenarios, the higher input current and output voltage exacerbate the current and voltage stress on devices [3].

The input-parallel output-series (IPOS) LLC resonant converter with multiple modules is an effective solution to the aforementioned issues [4–7]. This topology not only significantly reduces the voltage and current stress on power devices but also enhances the system's output voltage level and power capacity. However, in practical applications, the LLC converter based on the IPOS topology is prone to imbalances in output voltage and input current due to unavoidable manufacturing discrepancies in the resonant tank components of each module. These imbalances can adversely affect the device's heat dissipation, shorten its lifespan, and, in severe cases, lead to module damage due to overvoltage and overcurrent stress, threatening the overall stability of the power conversion system [8].

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Consequently, the issue of output voltage equalization and input current sharing in IPOS-based LLC resonant converters has become a focal point of attention in both academia and industry.

A substantial amount of research has been conducted on the issue of voltage equalization and current sharing in IPOS-based LLC resonant converters. The core idea is to achieve impedance matching between phases. These research approaches can be broadly classified into two categories: active and passive methods [9].

In active voltage equalization and current-sharing schemes, reference [10] proposes a maximum voltage equalization method that adjusts the voltage of each module by regulating the maximum output voltage, but this requires additional signal cascading and isolation. Researchers [11] employed droop control to ensure power balance, though the control is complex, and voltage fluctuations may occur in the event of a failure in the main module. Authors [12] implemented dual-loop control to achieve output voltage equalization at the series output of the IPOS converter, but it increases the number of components and sampling circuits, thereby raising costs and complexity. Others [13,14] regulated voltage gain using methods such as phase-shift control by sampling current to achieve voltage equalization and current sharing.

In passive voltage equalization and current-sharing schemes, Reference [15] proposes a coupled transformer scheme that reduces the magnetic core size and achieves output voltage balance through flux cancellation. However, the transformer design is complex, and it places high demands on core materials and flux control, which increase the system's cost and design difficulty. Reference [16] proposes paralleling two-phase resonant inductors to achieve automatic voltage equalization, but, under multi-resonant parameter mismatches, the effectiveness remains suboptimal.

To address the aforementioned issues, this paper proposes a shared inductance–capacitance LLC resonant IPOS converter. This method connects the resonant inductors and resonant capacitors of each phase of the LLC resonant converter in parallel through interconnection lines, achieving precise voltage equalization across all phases and input current sharing over the entire load range.

The sections of this paper are arranged as follows:

Section 2 reviews and analyzes the limitations of the traditional IPOS-type LLC resonant converter and the shared inductance structure. Section 3 introduces in detail the voltage and current equalization principles and advantages of the proposed shared inductance–capacitance structure in the IPOS-type LLC converter and discusses the module expansion capabilities. Section 4 analyzes the voltage and current equalization performance of the proposed method considering parasitic parameter mismatches. Section 5 validates the effectiveness of the proposed method through simulations. Section 6 develops a 1.25 kW two-phase experimental prototype and builds a testing platform, comparing it with traditional structures and the shared inductance structure to verify the effectiveness and superiority of the proposed topology. Section 7 summarizes this research and describes future research directions.

2. Analysis of Traditional IPOS and Shared Inductance Issues

2.1. Analysis of Traditional IPOS Topology and Voltage–Current Equalization Performance

The IPOS LLC resonant converter topology is shown in Figure 1. This topology employs an input-parallel, output-series configuration to achieve higher voltage gain. In the diagram, Q_{11}–Q_{14} and Q_{21}–Q_{24} are the primary-side switching devices of the two-phase LLC converter, while L_{r1}, C_{r1}, and L_{m1} are the resonant inductance, resonant capacitance, and magnetizing inductance of the first phase. Similarly, L_{r2}, C_{r2}, and L_{m2} are the resonant inductance, resonant capacitance, and magnetizing inductance of the second phase. In this

topology, the two modules share the input current on the primary side and equally divide the output voltage on the secondary side, thereby achieving high power and high gain DC/DC conversion.

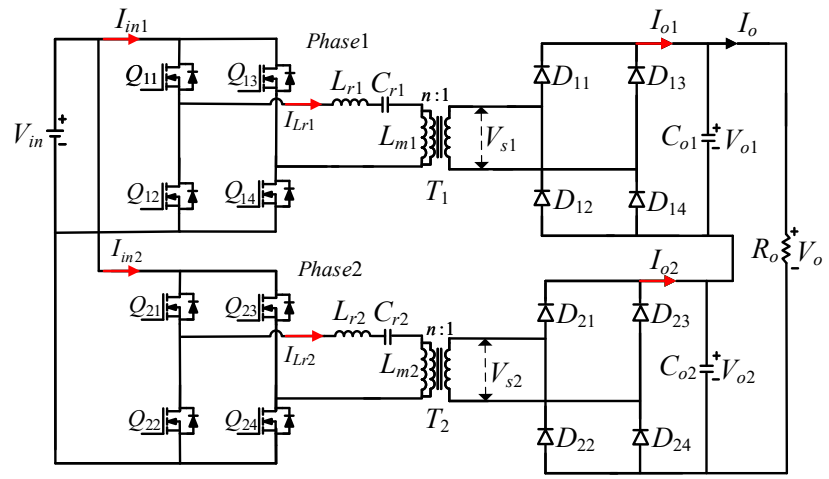


Figure 1. Traditional IPOS-type LLC converter topology.

When there are deviations in the resonant tank parameters of the two modules, it causes a shift in the resonant frequency, leading to imbalances in the output voltage and input current. This results in excessive voltage and current stress on power devices, which affects the converter's performance and reliability.

2.2. Analysis of Voltage and Current Equalization Performance in Interconnection-Line Shared Inductance Structure

In reference [16], a passive equalization scheme based on the interconnection-line shared inductance structure is proposed. This scheme achieves voltage and current equalization by paralleling resonant inductors between the two modules. The interconnection-line shared inductance topology is shown in Figure 2.

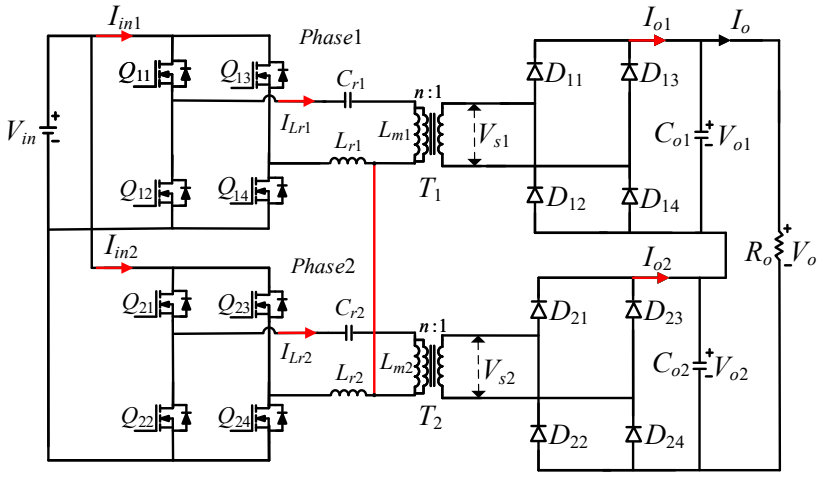


Figure 2. Interconnection-line shared inductance IPOS-type LLC resonant converter.

To avoid lengthy derivations, this section briefly presents key equations for the shared inductance structure in reference [16].

Figure 3 shows the equivalent circuit diagram of the interconnection-line shared inductance structure under the fundamental harmonic approximation. The coefficient μ is defined as the voltage imbalance factor between the modules, and V_{in}(s) and V_{Ls}(s) represent the AC input voltage and inductor voltage in the fundamental harmonic equivalent

circuit, respectively. The resonant currents for the two phases are denoted i_{Lr1} and i_{Lr2}. R_{ac1} and R_{ac2} are the equivalent loads for the two phases, while $V_1(s)$ and $V_2(s)$ represent the equivalent fundamental wave voltages for the first and second phases, as expressed in Equation (1).

$$\begin{cases} \dfrac{V_1(s)}{V_2(s)} = \dfrac{\mu}{1-\mu} \end{cases} \tag{1}$$

Based on the resonant tank voltage divider relationship, $V_1(s)$ and $V_2(s)$ can be expressed as:

$$\begin{cases} V_1(s) = \dfrac{R_{ac1}//sL_{m1}}{\frac{1}{sC_{r1}}+R_{ac1}//sL_{m1}}(V_{in}(s)+V_{Ls}(s)) \\ V_2(s) = \dfrac{R_{ac2}//sL_{m2}}{\frac{1}{sC_{r2}}+R_{ac2}//sL_{m2}}(V_{in}(s)+V_{Ls}(s)) \end{cases} \tag{2}$$

By solving Equations (1) and (2) simultaneously, the voltage equalization error μ can be obtained.

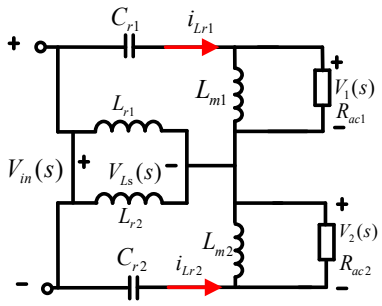


Figure 3. Fundamental equivalent circuit of the interconnection-line shared inductance structure.

Although the parallel inductors eliminate the imbalance in output voltage between the two phases caused by resonant inductance errors, the resonant capacitors and magnetizing inductance still affect the voltage equalization performance.

The relative relationship between the resonant currents of the two modules is:

$$\frac{i_{Lr1}}{i_{Lr2}} = \frac{V_{in}(s)-V_1(s)}{1/sC_{r1}+sL_{r1}//sL_{r2}} \frac{1/sC_{r2}+sL_{r1}//sL_{r2}}{V_{in}(s)-V_2(s)} \tag{3}$$

According to Equation (3), when using the shared inductance structure, both phases share the same inductor. However, when there are still parameter differences in the resonant capacitors and magnetizing inductors of each module, the current-sharing characteristics of this scheme are limited. The currents are no longer independent, resulting in some degree of difference in the resonant currents between the modules, which affects the overall current-sharing performance.

Therefore, although the interconnection-line shared inductance structure can improve voltage and current equalization under certain conditions, the system's balancing performance still has limitations when there are significant differences in the parameters of the resonant components, affecting the reliability and efficiency of the converter.

3. Proposed Shared Inductance–Capacitance Structure for Voltage and Current Equalization Characteristics

3.1. Proposed IPOS Shared Inductance–Capacitance Converter Topology

This section presents a topology for the interconnection-line shared inductance–capacitance self-balancing voltage and current equalization IPOS-type LLC resonant converter, shown in Figure 4.

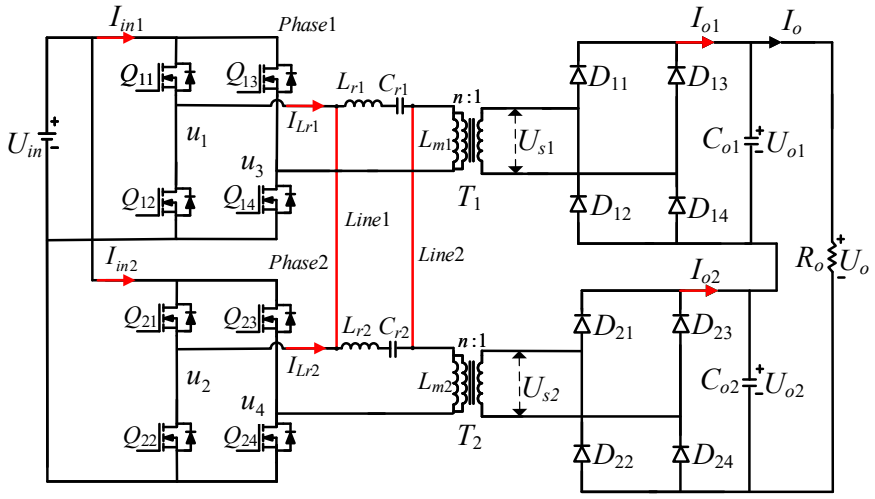


Figure 4. Interconnection-line shared inductance and capacitance IPOS LLC resonant converter.

In Figure 4, Line 1 and Line 2 represent the interconnection lines in the proposed topology. Line 1 and Line 2 connect the resonant inductors and resonant capacitors of Phase 1 and Phase 2 in parallel on the primary side, achieving mutual coupling between the two modules and forming a shared inductance–capacitance branch, thereby effectively balancing the input impedance between different modules.

During operation, the driving signals for the primary-side switches Q_{11}, Q_{14}, Q_{21}, and Q_{24} are the same, while the driving signals for Q_{12}, Q_{13}, $Q_{22,}$ and Q_{23} are identical. L_{r1}, C_{r1}, and L_{m1} represent the resonant inductance, resonant capacitance, and magnetizing inductance of phase 1, respectively. L_{r2}, C_{r2}, and L_{m2} represent the resonant inductance, resonant capacitance, and magnetizing inductance of phase 2. *Uo* is the output voltage, and U_{o1} and U_{o2} are the output voltages of the two phases. u_1 to u_4 represent the bridge arm voltages of the two phases. n is the transformer turn ratio.

3.2. Fundamental Harmonic Approximation (FHA) Assumptions and Validity Limits

To analyze the voltage and current equalization system, this paper introduces the fundamental harmonic approximation (FHA). Before applying the FHA model, its assumptions, applicability, and limitations must be clarified.

(a) Basic Assumptions of FHA Model

FHA assumes the system's voltage and current are dominated by the fundamental harmonic, ignoring higher-order harmonics. The voltage waveform is approximated as:

$$V(t) = V_0 \sin(\omega t + \phi) \tag{4}$$

Here, V_0 is the amplitude of the fundamental harmonic, ω is the resonance frequency, and ϕ is the phase. This assumption holds near the ideal resonance frequency, where it is assumed that the responses of the inductors and capacitors are linear, allowing the fundamental harmonic component to dominate.

(b) Validity Limits of the FHA Model

While the FHA model is accurate under resonant conditions, it may fail under the following circumstances:

Non-resonant conditions: when deviating from resonance, higher-order harmonics significantly affect the balance, invalidating the model.

Partial load operation: nonlinearities and increased harmonics cause analysis deviations.

Significant harmonics: harmonics generated by operating condition fluctuations affect energy transfer and impedance matching, reducing model validity.

3.3. Voltage Equalization Analysis of the Proposed Structure

To quantitatively analyze the impact of parameter differences on the output voltage, the resonant tank parameter relationship is defined as shown in Equation (4). Using the parameters of the first phase of the resonant tank as the reference, error coefficients a, b, and c are introduced to represent the proportional relationships between the resonant inductance L_{r2}, resonant capacitance C_{r2}, and magnetizing inductance L_{m2} of the second phase and the corresponding parameters of the first phase of the resonant tank.

$$\begin{cases} L_{\mathrm{r1}} = L_r, L_{\mathrm{r2}} = aL_r \\ C_{\mathrm{r1}} = C_r, C_{\mathrm{r2}} = bC_r \\ L_{m1} = L_m, L_{\mathrm{m2}} = cL_m \end{cases} \tag{5}$$

In the steady state, the total output voltage U_o is composed of the output voltage of phase 1, U_{o1}, and the output voltage of phase 2, U_{o2}:

$$U_o = U_{o1} + U_{o2} \tag{6}$$

Since the output is a series configuration, it can be expressed as:

$$I_o = I_{o1} = I_{o2} \tag{7}$$

The equivalent load resistances for each phase, R_{o1} and R_{o2}, as well as the total equivalent load R_o, can be expressed as:

$$R_o = \frac{V_o}{I_o}, R_{o1} = \frac{V_{o1}}{I_{o1}}, R_{o2} = \frac{V_{o2}}{I_{o2}} \tag{8}$$

The coefficient k is defined as the proportion of the total output voltage carried by the first phase's output voltage. When k = 0 or 1, it indicates that the voltage is handled by only one module, and when k = 0.5, the voltage is evenly distributed between the two modules. Therefore, the output voltages U_{o1} and U_{o2} can be expressed as:

$$U_{o1} = k \cdot U_o, U_{o2} = (1-k) \cdot U_o \tag{9}$$

Figure 5 shows the equivalent circuit of the structure under the fundamental harmonic approximation.

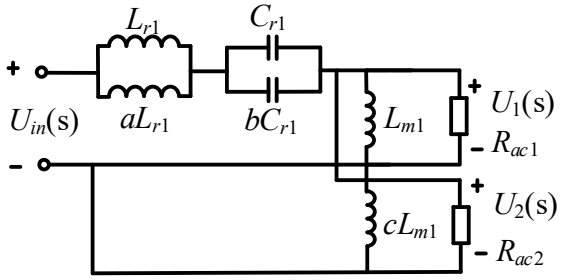


Figure 5. The fundamental equivalent circuit of the mutual inductance and capacitance structure of interconnect lines.

$U_{in}(s)$ represents the AC input voltage in the fundamental harmonic equivalent circuit. $U_1(s)$ and $U_2(s)$ denote the equivalent fundamental wave voltages of the two phases, which can be expressed using coefficient k.

$$\begin{cases} \dfrac{U_1(s)}{U_2(s)} = \dfrac{k}{1-k} \end{cases} \tag{10}$$

R_{ac1} and R_{ac2} are the equivalent loads for the two phases, and they are expressed in Equation (11).

$$R_{ac1} = \frac{8n^2}{\pi^2} R_{o1}, R_{ac2} = \frac{8n^2}{\pi^2} R_{o2} \tag{11}$$

The simplified fundamental harmonic equivalent circuit of the shared inductance–capacitance structure is shown in Figure 6. In this circuit, L_{r_total} and C_{r_total} represent the total resonant inductance and total resonant capacitance, respectively, and their expressions are given in Equation (12).

$$\begin{cases} L_{r_total} = \frac{a}{1+a} L_r \\ C_{r_total} = (1+b) C_r \end{cases} \tag{12}$$

Unlike the shared inductance structure, in this case, the impedance divider relationship of $U_1(s)$ and $U_2(s)$ in the resonant tank changes. The expression for this relationship is given in Equation (13).

$$U_1(s) = U_2(s) = (U_{in}(s) - U_{L_{r_total}} - U_{C_{r_total}}) \tag{13}$$

By solving Equations (10) and (13) simultaneously, the value of k can be determined. Additionally, to evaluate the voltage equalization performance of the proposed structure, the load voltage equalization error δ_v is defined, and its expression is:

$$\delta_v = abs(\frac{U_1(s) - U_2(s)}{U_1(s) + U_2(s)}) = abs(2k-1) k \in [0, 1] \tag{14}$$

According to Equation (13), when $U_1(s)$ equals $U_2(s)$, the voltage equalization error δ_v is 0, indicating that the output voltages of the two modules are equal.

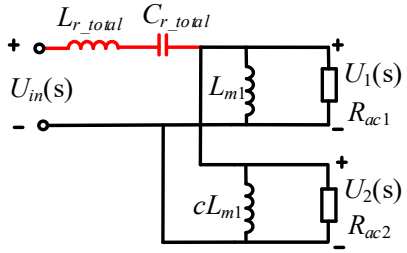


Figure 6. Simplified fundamental harmonic equivalent circuit.

3.4. Current-Sharing Analysis of the Proposed Structure

To simplify the analysis, it is assumed that the power devices of the two modules in Figure 4 have the same driving signals and no delay:

$$\begin{cases} u_1 = u_2 \\ u_3 = u_4 \end{cases} \tag{15}$$

The equivalent circuit model of the shared inductance–capacitance structure is shown in Figure 7.

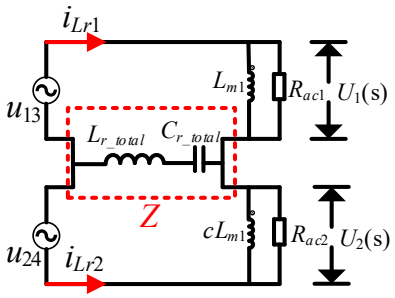


Figure 7. Equivalent circuit model of the mutual inductance and capacitance structure.

The input voltage is given in Equation (16).

$$\begin{cases} u_{13} = i_{Lr1}.Z + U_1(s) \\ u_{24} = i_{Lr2}.Z + U_2(s) \end{cases} \tag{16}$$

where

$$Z = j\omega L_{r_total} + \frac{1}{j\omega C_{r_total}} \tag{17}$$

Due to the parallel output, $u_{13} = u_{24}$. Combining Equations (16) and (17), it can be concluded that i_{Lr1} and i_{Lr2} are equal.

The current-sharing error δ_i is defined as follows, where rms(i_{Lr1}) and rms(i_{Lr2}) represent the root mean square values of the resonant currents i_{Lr1} and i_{Lr2}, respectively:

$$\delta_i = abs(\frac{rms(i_{Lr1}) - rms(i_{Lr2})}{rms(i_{Lr1}) + rms(i_{Lr2})}) \tag{18}$$

After the shared inductance–capacitance, the current-sharing error δ_i is 0, indicating that the input current is perfectly shared between the modules.

3.5. Comparison with Traditional Structure and Interconnection-Line Shared Inductance Structure

This section explores the quantitative sensitivity analysis of component tolerances for L_r, C_r, and L_m. It investigates the impact of different combinations of error coefficients a, b, and c on the voltage equalization error δ_v, considering the parameter variations in the actual manufacturing process. The resonant tank parameters are set with a ±10% tolerance, and thus the values of a, b and c range from {0.9, 1, 1.1}. Due to the symmetry of the different values, the combination (a = 0.9 b = 0.9 c = 0.9) has the same impact on the voltage equalization error δ_v as the combination (a = 1.1 b = 1.1 c = 1.1). Therefore, there are 13 effective combinations covering all possible parameter variations within the ±10% tolerance range. The specific error combinations are shown in Table 1, and the converter parameter indicators are shown in Table 2.

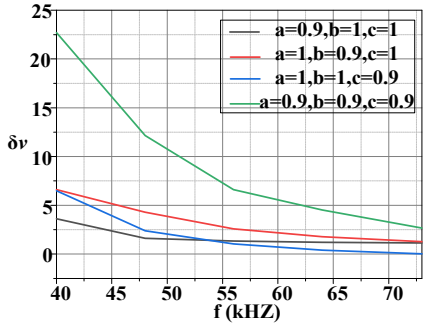
Table 1. Resonant tank parameter error combinations.

Variable	Value												
a	0.9	1	1	0.9	0.9	0.9	0.9	0.9	0.9	0.9	0.9	1	1
b	1	0.9	1	0.9	0.9	1	0.9	1	1.1	1.1	1.1	0.9	0.9
c	1	1	0.9	0.9	1	0.9	1.1	1.1	0.9	1	1.1	0.9	1.1

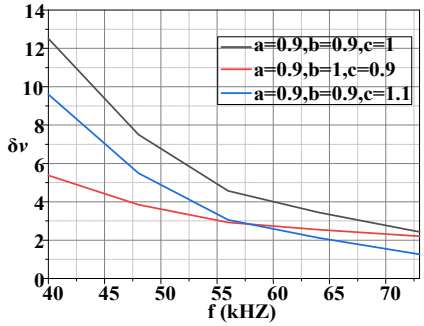
The relationship between the output voltage equalization error δ_v and switching frequencies for the traditional structure for all 13 error combinations in Table 1 and the parameter indicators in Table 2 are shown in Figure 8.

Table 2. Converter parameter indicators.

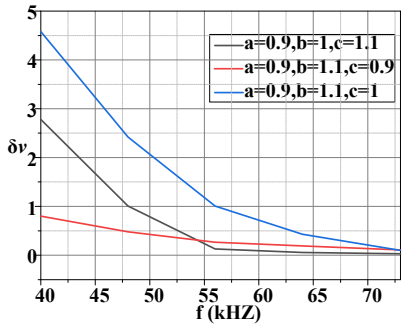
Converter Parameters	Value	Unit
Input voltage	100	V
Switching frequency	40–73	kHz
Rated power	1.25	kW
Transformer turn ratio	1.25:1	
Resonant inductor L_{r1}	36	μH
Resonant inductor L_{r2}	a * 36	μH
Resonant capacitor C_{r1}	132	nF
Resonant capacitor C_{r2}	b * 132	nF
Magnetizing inductance L_{m1}	160	μH
Magnetizing inductance L_{m2}	c * 160	μH



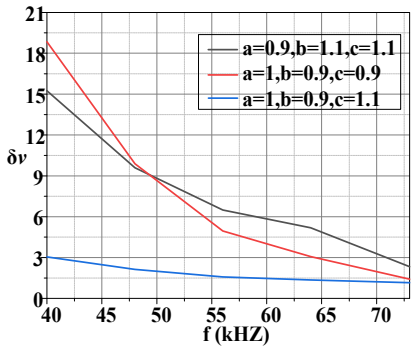
(**a**) The first group of error curves



(**b**) The second group of error curves



(**c**) The third group of error curves



(**d**) The fourth group of error curves

Figure 8. Relationship between voltage equalization error δ_v and switching frequency for the traditional structure under all parameter error combinations.

As shown in Figure 8, the output voltage error of the traditional structure significantly increases as the frequency decreases, with the maximum error occurring at 40 kHz. Its voltage equalization performance is sensitive to operating condition variations, exhibiting poor robustness.

To demonstrate the advantages of the proposed interconnection-line shared inductance–capacitance structure in voltage equalization performance and its practical robustness to parameter tolerances, this section compares it with the traditional structure and the interconnection-line shared inductance structure. The four typical error combinations with the largest output voltage equalization errors from the 13 combinations in Figure 8 are selected for comparison: Case 1 (a = 0.9, b = 0.9, c = 0.9), Case 2 (a = 0.9, b = 0.9, c = 1), Case 3 (a = 0.9, b = 1.1, c = 1.1), and Case 4 (a = 1, b = 0.9, c = 0.9). These four cases represent the most extreme parameter variation conditions and effectively validate the stability of the structure's performance under extreme deviations.

Figure 9 shows the calculated output voltage equalization error δ_v for the three structures under the parameters in Table 2.

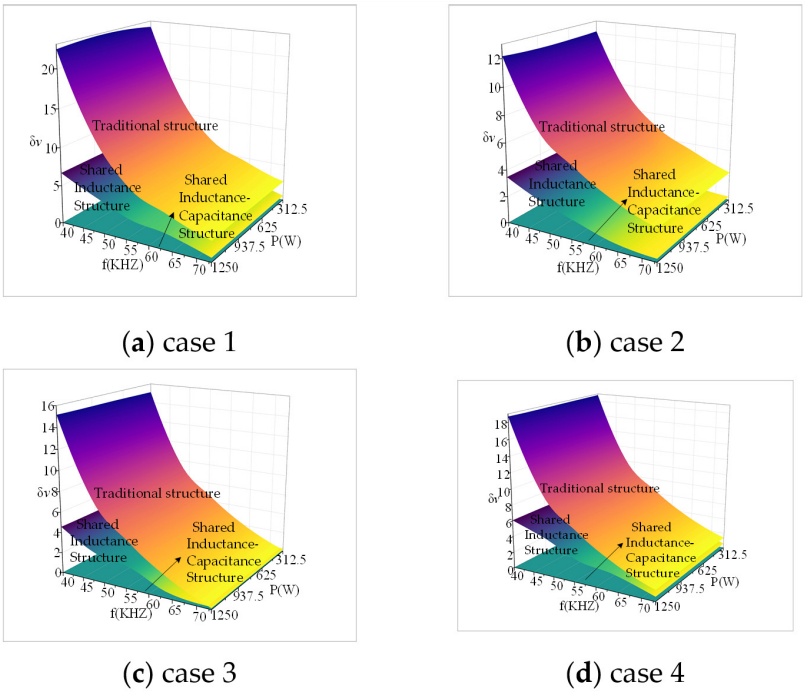


Figure 9. Output voltage balancing error under different errors of the mutual inductance and capacitance structure and common inductance structure and traditional structure.

In Case 1 (a), with a switching frequency of 40 kHz and under half-load conditions, the voltage equalization error of the existing converter reaches 23%. The interconnection-line shared inductance structure has a voltage equalization error of 6.69%, while the proposed interconnection-line shared inductance–capacitance structure achieves complete voltage equalization between the phases. The above results show that the proposed passive voltage equalization structure not only significantly improves voltage equalization performance under harsh operating conditions across all error combinations but also maintains excellent voltage equalization in other conditions. This fully demonstrates the structure's strong tolerance to the manufacturing tolerances of L_r, C_r and L_m, with robustness far superior to the traditional structure and the shared inductance structure. It greatly enhances the reliability of the converter in practical engineering applications.

3.6. Extension of the Proposed Shared Inductance–Capacitance Structure

Building on the previous analysis of the two-phase voltage and current equalization characteristics, the extension of the proposed shared inductance–capacitance structure to multi-phase systems is further explored. The topology is shown in Figure 10.

The fundamental harmonic equivalent circuit of the shared inductance–capacitance structure in an N-phase system is shown in Figure 11.

The dashed lines in the figure represent the extended connections between modules. The resonant tank parameter error coefficients, a_N, b_N and c_N, reflect the differences in resonant inductance, resonant capacitance, and magnetizing inductance between modules. Specifically, a_N, b_N and c_N are within the range [0.9, 1.1]. In this way, the two-phase system can be extended to any number of modules.

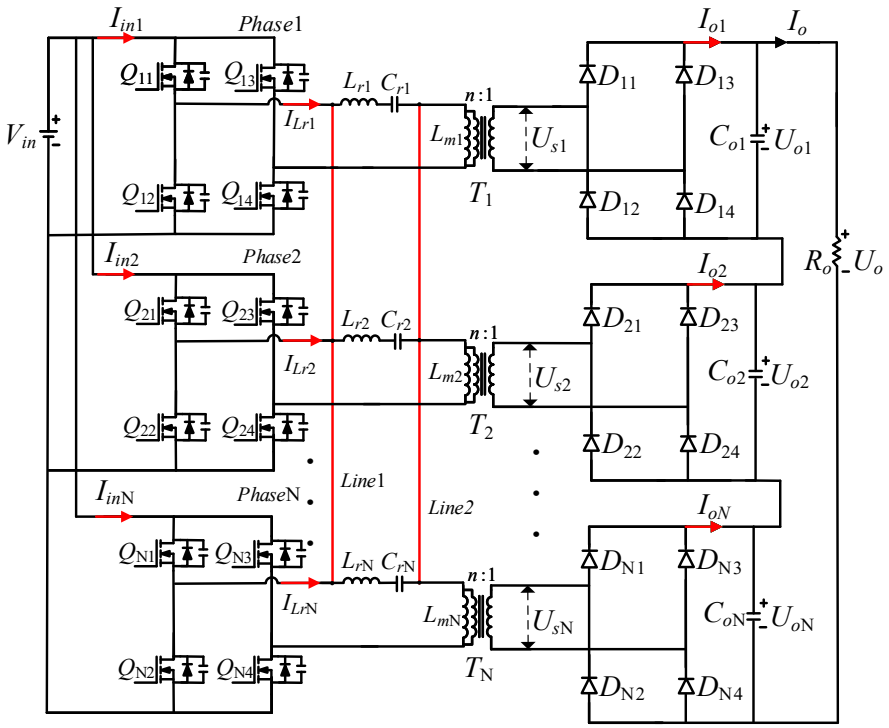


Figure 10. Application of the shared inductance–capacitance structure in N-phase systems.

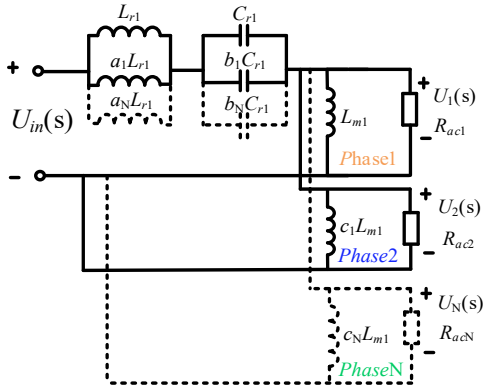


Figure 11. Fundamental harmonic equivalent model of the shared inductance–capacitance structure in an N-phase system.

As shown in Figure 11, in the N-phase system, the resonant inductors and resonant capacitors of each phase are connected in parallel, forming a unified shared inductance–capacitance branch. The equivalent loads are connected in parallel, and the output voltage of each module is equal, improving current sharing and reducing circulating currents caused by one module bearing excessive power. This enhances the system's efficiency and stability, reduces the interaction between resonant tanks, and prevents energy imbalance. A detailed simulation analysis will be provided in Section 5.2 below.

4. Voltage and Current Equalization Performance of Proposed Structure Considering Parasitic Parameter Mismatches

4.1. Voltage Equalization Analysis of Proposed Structure

In practical applications, for multi-phase series-parallel LLC resonant converters, in addition to mismatches in resonant inductance, resonant capacitance, and magnetizing inductance, there are also mismatches in other parasitic parameters. These mismatches mainly include leakage inductance and the on-resistance of the power switches. Regarding

the selection of parasitic parameters, reference is made to [17]. Nevertheless, a distinct topological configuration was adopted in this study compared to the aforementioned literature, specifically an IPOS-type full-bridge topology, whose detailed circuit schematic is illustrated in Figure 12.

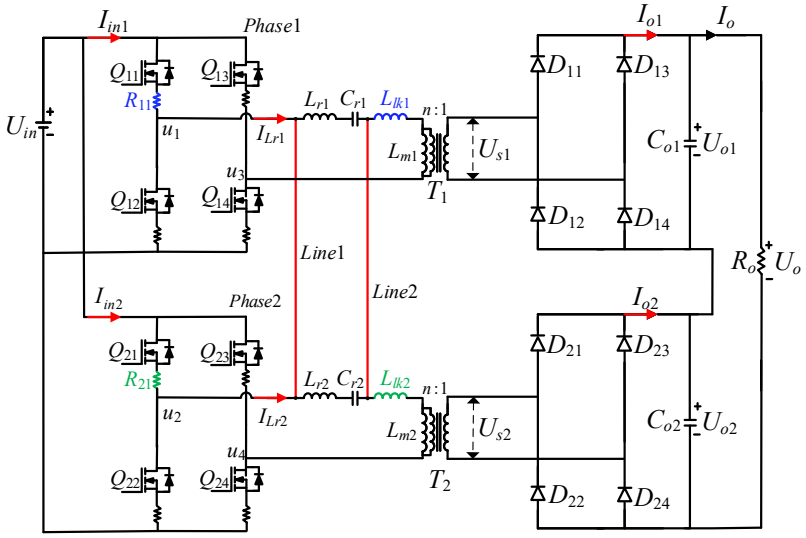


Figure 12. Detailed circuit of the proposed method considering parasitic parameters. Modified from [17].

L_{lk1} and L_{lk2} represent the leakage inductances of phase 1 and phase 2, respectively; R_{11} and R_{21} are the on-resistance of the upper switch of the two-phase modules. The parameter mismatches of the two-phase modules in Figure 12 are defined in (19), where a, b, c, d and e are used to indicate the parameter mismatches of the two-phase LLC converter.

$$\begin{cases} L_{r2} = aL_{r1}, C_{r2} = bC_{r1} \\ L_{m2} = cL_{m1}, L_{lk2} = dL_{lk1}, R_{21} = eR_{11} \end{cases} \tag{19}$$

The equivalent circuit of the proposed structure based on FHA with parasitic parameters is shown in Figure 13.

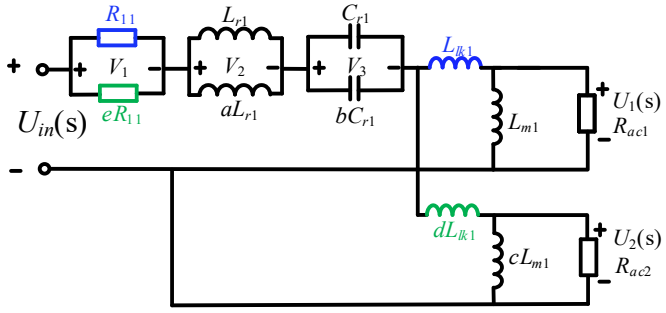


Figure 13. Fundamental harmonic equivalent circuit considering parasitic parameters.

As shown in Figure 13, due to the interconnection lines, the on-resistance, resonant inductance, and resonant capacitance of the two modules are connected in parallel. The impedance divider relationship between $U_1(s)$ and $U_2(s)$ is expressed in Equation (20).

$$\begin{cases} U_1(s) = (U_{in}(s) - V_1 - V_2 - V_3)\frac{sL_{m1}//R_{ac1}}{sL_{lk1}+(sL_{m1}//R_{ac1})} \\ U_2(s) = (U_{in}(s) - V_1 - V_2 - V_3)\frac{scL_{m1}//R_{ac2}}{sdL_{lk1}+(scL_{m1}//R_{ac2})} \end{cases} \tag{20}$$

At this point, the relationship between U_1(s) and U_2(s) can still be expressed using k. Based on the analysis in Section 3.3, and combining Equations (10), (14) and (20), the voltage equalization error δ_v can be determined. The related simulations will be discussed in detail in Section 5.3.

4.2. Current-Sharing Analysis of the Proposed Structure

The equivalent circuit model of the proposed structure considering parasitic parameter mismatches is shown in Figure 14.

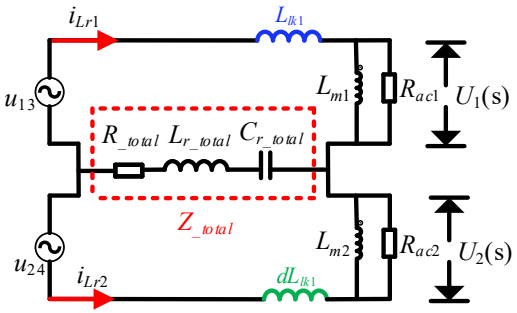


Figure 14. Equivalent circuit model considering parasitic parameters.

L_{r_total} and C_{r_total} are the total resonant inductance and total resonant capacitance, and their expression is still represented in Equation (12). R_total is the total on-resistance of the switches, and it is expressed in Equation (21).

$$R_total = \frac{e}{1+e} R_{11} \tag{21}$$

where

$$Z_total = R_total + j\omega L_{r_total} + \frac{1}{j\omega C_{r_total}} \tag{22}$$

The input voltage relationship can be expressed as:

$$\begin{cases} u_{13} = i_{Lr1}.(Z_total + sL_{lk1}) + U_1(s) \\ u_{24} = i_{Lr2}.(Z_total + seL_{lk1}) + U_2(s) \end{cases} \tag{23}$$

Due to the parallel output, $u_{13} = u_{24}$, the relationship between U_1(s) and U_2(s) can be expressed using k. By combining Equations (10) and (23), the values of i_{Lr1} and i_{Lr2} can be determined. Substituting them into Equation (18), the current-sharing error δ_i can be calculated. The related simulations will be discussed in detail in Section 5.3.

5. Simulation Validation

5.1. Simulation Results Without Considering Parasitic Parameter Mismatches

To verify the effectiveness of the proposed method, simulation validation was performed. The parameters of the two-phase LLC converter are shown in Table 2. According to theoretical analysis, the switching frequency was selected for the most adverse condition, 40 kHz. The maximum voltage equalization error occurs when the parameter errors are set to −10%. Therefore, the most unfavorable parameter mismatch combination was used: (a = 0.9, b = 0.9, c = 0.9). Figure 15 shows the PSIM simulation waveforms of the two-phase output voltage and resonant current for the three structures under full-load and operating conditions.

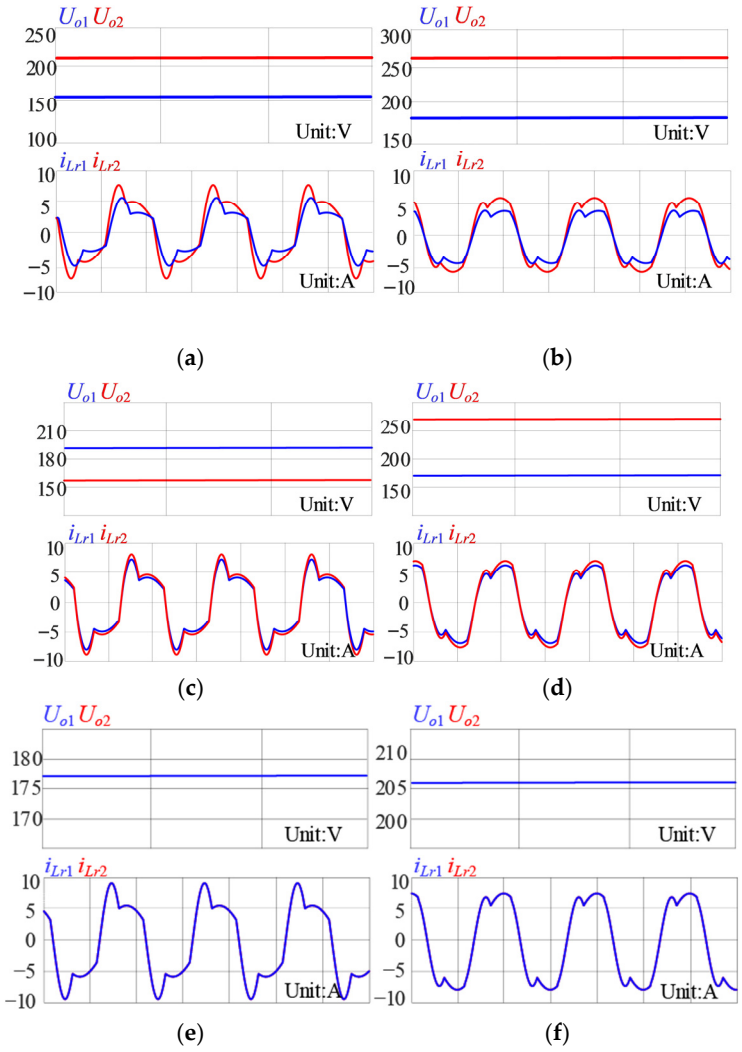


Figure 15. Simulation waveforms of load voltage and resonant current for each structure. Traditional structure: (**a**) full load, (**b**) half load. Shared inductance structure: (**c**) full load, (**d**) half load. Proposed structure: (**e**) full load, (**f**) half load.

Under the above errors, whether the system is under full-load or half-load conditions, the traditional structure LLC converter exhibits significant voltage and current imbalances. Under half-load conditions, the output voltage and input current error between the phases reaches 21.12%. Even with the shared inductance structure, the output voltage error remains at 14.2%, and the resonant current error is 5.29%. However, as shown in Figure 15e,f, regardless of full-load or half-load conditions, the proposed shared inductance–capacitance structure achieves balanced two-phase output voltage and resonant currents.

Table 3 presents the load voltages and output voltage-sharing errors obtained from PSIM simulations and FHA calculations.

As shown in Table 3, the deviation calculated by the FHA is significantly larger than the simulation results. The reason for this is that the FHA method neglects the influence of higher-order harmonics, leading to a discrepancy between its calculations and the actual simulation results. Since FHA only considers the fundamental harmonic component, the calculated voltage gain is lower. Therefore, to achieve the same output voltage, the switching frequency predicted by FHA is always lower than the actual simulation frequency. In other words, the actual switching frequency is higher than the FHA-predicted value. Overall, the simulation results are more reliable than the FHA method in all cases.

Table 3. Simulation data and FHA data for each structure.

Case	PSIM Simulation			FHA
	***Uo*1 (V)**	***Uo*2 (V)**	**δv**	**δv_FHA**
(a)	152.9	211.6	16.10%	22.69%
(c)	154.5	187.5	9.65%	6.69%
(e)	176.5	176.5	0%	0%
(b)	170.7	262.1	21.12%	22.61%
(d)	177	235.6	14.2%	6.65%
(f)	206.1	206.1	0%	0%

5.2. Simulation Results of the Proposed Method in Multi-Module Systems

To verify the effectiveness of the proposed method in multi-module systems, a simulation was conducted using a three-module system as an example. The converter parameters are shown in Table 2. Based on the analysis above, the most adverse conditions were chosen: half-load operation with a switching frequency of 40 kHz and parameter mismatches using the two error combinations with the worst output voltage mismatch levels as defined in Section 3.5, specifically Case 1 (a = 0.9, b = 0.9, c = 0.9) and Case 4 (a = 1, b = 0.9, c = 0.9), ensuring distinct errors across the three modules. Figure 16 shows the PSIM simulation waveforms of the output voltage and resonant current for each module under these conditions.

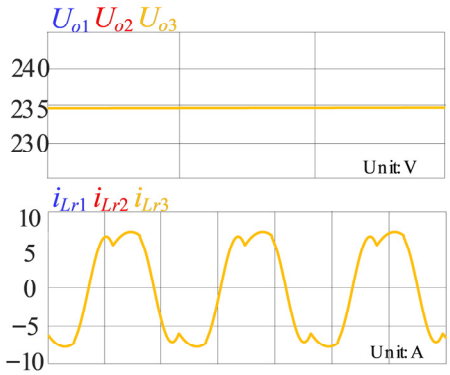


Figure 16. Simulation waveforms of load voltage and resonant current for the three-module system of the proposed structure.

As shown in Figure 16, the proposed structure effectively achieves voltage equalization and current sharing across phases in the N-phase system. This ensures that the voltage equalization and current-sharing characteristics of the output voltage and input current in the multi-phase system are not affected by resonant component parameter differences, significantly improving the system's stability and reliability.

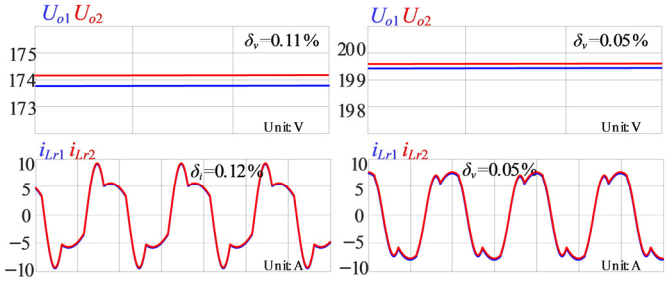
5.3. Simulation Results Considering Parasitic Parameter Mismatches

To verify the effectiveness of the proposed method under parasitic parameter mismatches, a simulation was conducted. The parameters of the two-phase LLC converter are shown in Table 4. Based on the theoretical analysis, the switching frequency was selected for the most adverse condition, 40 kHz, and the parameter errors were set to −10%, i.e., (a = 0.9, b = 0.9, c = 0.9, d = 0.9, e = 0.9). Figure 17 shows the PSIM simulation waveforms of the two-phase output voltage and resonant current for the proposed structure under full-load and half-load conditions with these errors.

Table 4. Converter parameter indicators.

Converter Parameters	Value	Unit
Input voltage	100	V
Switching frequency	40	kHz
Rated power	1.25	kW
Transformer turn ratio	1.25:1	
Resonant inductor L_{r1}/L_{r2}	36/32.4	μH
Resonant capacitor C_{r1}/C_{r2}	132/118.8	nF
Magnetizing inductance L_{m1}/L_{m2}	160/144	μH
Leakage inductance L_{lk1}/L_{lk2}	2/1.8	μH
On-resistance R_{11}/R_{21}	100/90	mΩ

Under the maximum error of parasitic parameters, the voltage and current equalization errors at full load are only 0.11% and 0.12%. Therefore, the proposed shared inductance–capacitance structure can achieve balanced two-phase output voltage and resonant currents.



(**a**) Full Load (**b**) Half Load

Figure 17. Simulation waveforms of load voltage and resonant current for the proposed structure.

6. Experimental Verification

6.1. Steady-State Experimental Result Validation

To verify the voltage and current equalization performance of the proposed structure, a 1.25 kW two-phase LLC resonant converter prototype was built, as shown in Figure 18. The two-module LLC resonant converter shared the same control board, and the consistent timing of the power devices was ensured by sending unified driving signals. The actual parameters of the experimental platform prototype are shown in Table 5.

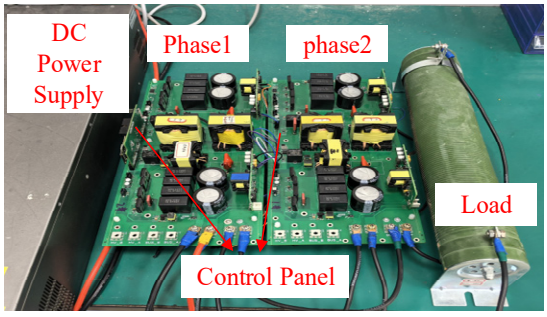


Figure 18. The proposed experimental platform for the common inductance capacitor LLC converter.

With an input voltage of 100 V, rated power of 1.25 kW, and switching frequency of 40 kHz, Figure 19a–c present the output voltage waveforms of the traditional structure under full-load, half-load, and 25% load conditions, respectively. Figure 19d–f show the corresponding input current waveforms. Figure 20a–c illustrate the output voltage waveforms of the interconnected shared-inductor structure under the same three load

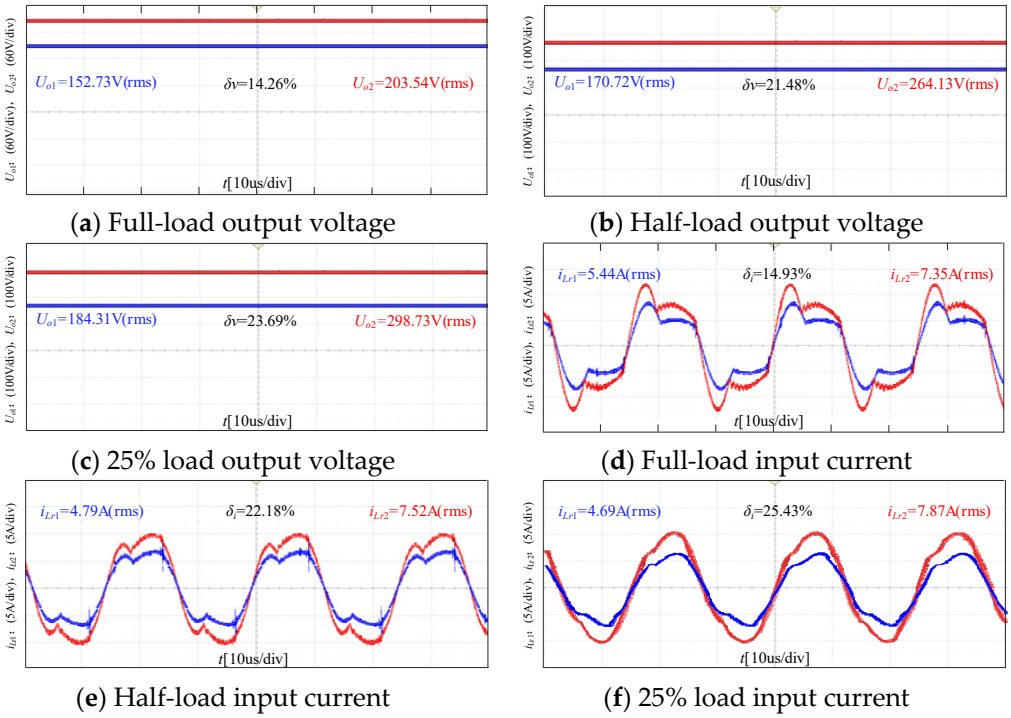
conditions, while Figure 20d–f display the associated input current waveforms. Likewise, Figure 21a–c plot the output voltage waveforms of the proposed shared-inductor–capacitor structure under full-load, half-load, and 25% load conditions, and Figure 21d–f show the corresponding input current waveforms.

Table 5. Experiment parameters.

Parameter	Value	Unit
Input voltage	100	V
Rated power	1.25	kW
Transformer turn ratio	1.25:1	
Resonant Inductor L_{r1}/L_{r2}	36/32.4	μH
Resonant capacitor C_{r1}/C_{r2}	132/118.8	nF
Magnetizing inductance L_{m1}/L_{m2}	160/144	μH

From the experimental waveforms, the traditional structure exhibits two-phase output voltage errors of 14.26%, 21.48%, and 23.69% at full-load, half-load, and 25% load conditions, accompanied by input current errors of 14.93%, 22.18%, and 25.43%. For the interconnected shared inductor structure, the corresponding voltage errors are 9.45%, 14.19%, and 17.33%, while the current errors are 9.53%, 14.15%, and 17.63% under the same loading conditions. Strikingly, the proposed shared inductance–capacitance structure achieves ultra-low errors: only 0.33%, 0.34%, and 0.43% for both output voltage and input current throughout the entire load range. These results validate that the proposed structure realizes superior voltage and current balancing over the full operating range of the converter.

It is important to highlight that the proposed shared inductance–capacitance structure mitigates the issue of resonant current imbalance by establishing a unified shared inductance–capacitance network. This approach significantly reduces the resonant tank stress induced by current imbalance and prevents the additional losses associated with resonant current misbalance.

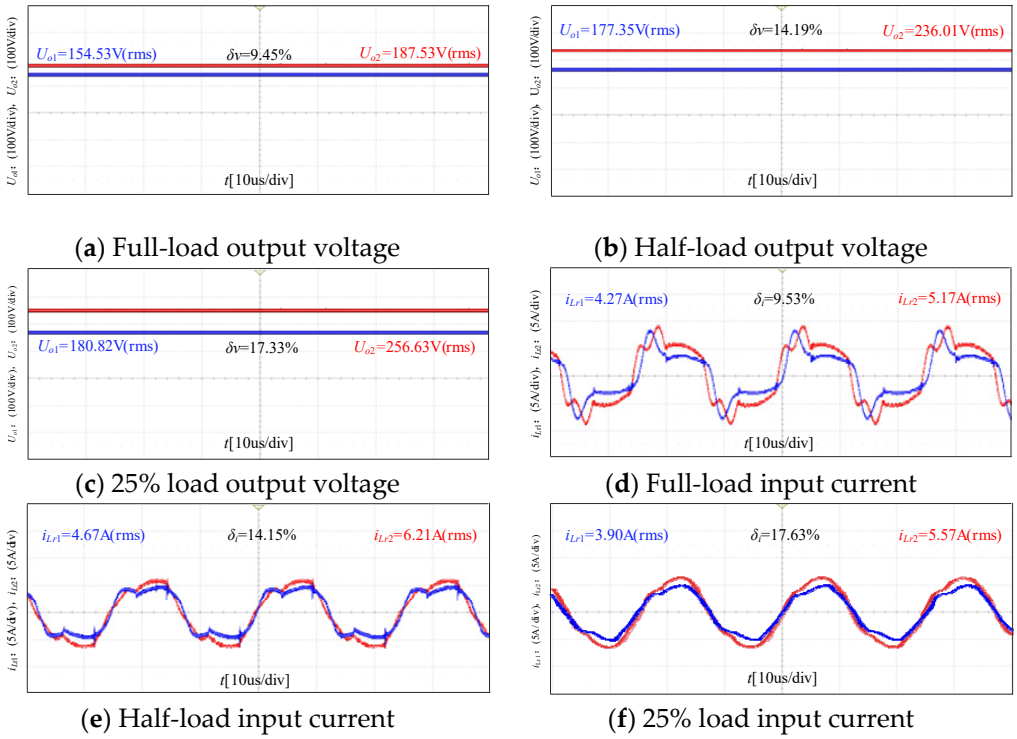


(**a**) Full-load output voltage (**b**) Half-load output voltage

(**c**) 25% load output voltage (**d**) Full-load input current

(**e**) Half-load input current (**f**) 25% load input current

Figure 19. Experimental waveform of the traditional structure.

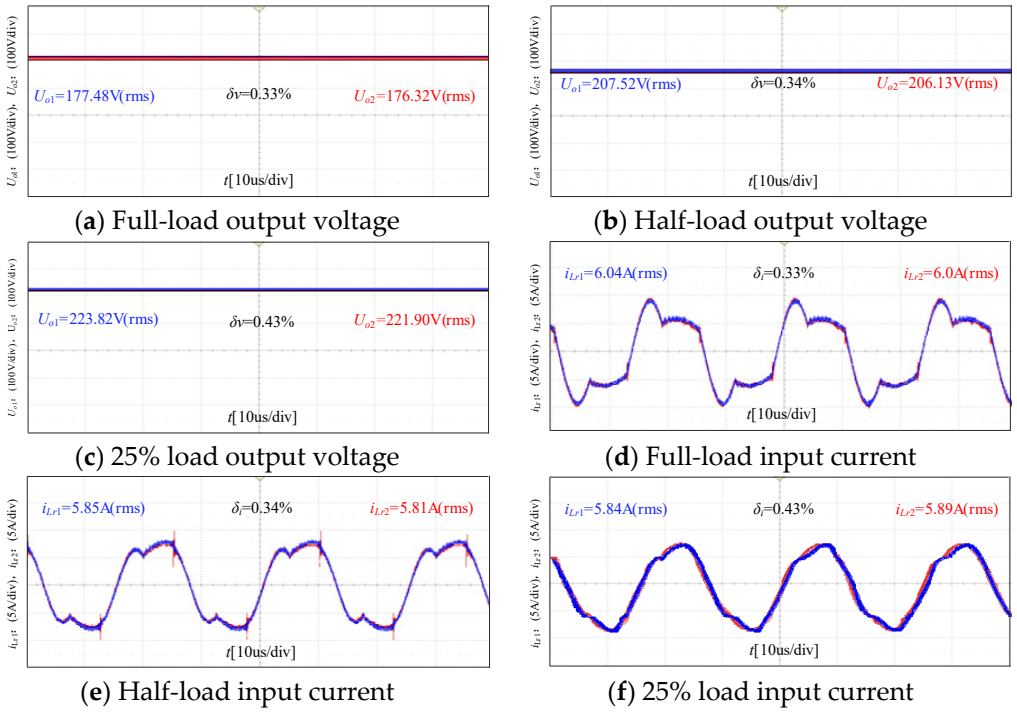


(**a**) Full-load output voltage (**b**) Half-load output voltage

(**c**) 25% load output voltage (**d**) Full-load input current

(**e**) Half-load input current (**f**) 25% load input current

Figure 20. Experimental waveform of the interconnection-line shared inductance structure.



(**a**) Full-load output voltage (**b**) Half-load output voltage

(**c**) 25% load output voltage (**d**) Full-load input current

(**e**) Half-load input current (**f**) 25% load input current

Figure 21. Experimental waveform of the interconnection-line shared. inductance and capacitance structure.

6.2. Dynamic Experimental Results

Figure 22 shows the experimental waveforms of the output voltage and resonant current for the two modules, corresponding to the full-load and half-load conditions of the proposed method.

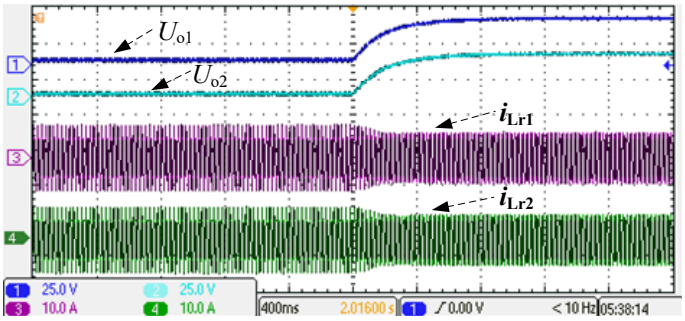


Figure 22. Output voltage and resonant current of the two modules during the transition from full load to half load.

As shown in Figure 22, during the transition from full load to half load, the system is able to maintain stable output voltages U_{o1} and U_{o2}, which fully demonstrates the excellent voltage-balancing capability of the proposed scheme during load switching. Meanwhile, during the switching process, the resonant currents i_{Lr1} and i_{Lr2} of the two modules remain highly synchronized, and the current distribution between the modules stays balanced, further proving that the system can maintain outstanding current-sharing characteristics under different load conditions. The system quickly stabilizes to the new operating state, indicating that the proposed solution has excellent responsiveness and stability under dynamic load variations, showcasing its voltage and current equalization ability in dynamic processes.

6.3. Comparison with Existing Solutions

The method proposed in this paper includes a unified shared inductance–capacitance branch using interconnection lines to achieve voltage and current equalization. The significant advantage or distinction of this method lies in its avoidance of complex control strategies and its modular characteristics. The comparison with existing active/passive equalization solutions is shown in Table 6.

Table 6. Comparative Analysis of Existing Equalization Solutions.

Literature Solution	Additional Components	Equalization Method	Dynamic Performance	Modularity Ability	Complexity	Pros and Cons
Reference [10] Distributed Autonomous Voltage Control	2 current sensors, sampling circuit	Active control	Poor	low	Complex	Complex hardware, poor balancing performance
Reference [11] Droop Control	4 current sensors, sampling circuit	Active control	Poor	Medium	Very complex	Complex control strategy, poor dynamic performance
Reference [15] Magnetically Integrated Transformer	2 current sensors, magnetically integrated transformer	Passive equalization	Medium	Low	Complex	High hardware cost, poor module expandability
Reference [16] Coupled Inductance	None added	Passive equalization	Medium	Medium	simple	Incomplete equalization capability, limited dynamic performance
Proposed Solution	None added	Passive equalization	Good	High	Very simple	Simple, reliable, low cost, best equalization performance, easy to expand

By comparison, the specific advantages of this solution are as follows:

(1) The ease of implementation and reliability of this method are superior to active balancing methods. For instance, droop control requires four current sensors and a complex control strategy, resulting in poor dynamic performance.

(2) Compared to other passive equalization methods, the proposed solution has lower complexity and features modularity, making it easier to scale to multi-phase systems as the system's power capacity increases. This approach shortens the development cycle and reduces development costs.

7. Conclusions

To address the imbalances in output voltage and input current caused by parameter differences in the resonant tank components of input-parallel output-series LLC resonant converters, a new interconnection-line shared inductance–capacitance IPOS-type LLC resonant converter is proposed. This method achieves output voltage equalization and input current sharing between modules without the need for additional components or control strategies, significantly reducing system costs.

Furthermore, a new fundamental harmonic equivalent mathematical model is established for the proposed structure. Based on this model, the voltage and current equalization performance of the proposed converter is analyzed and compared with the voltage and current equalization characteristics of the traditional structure and interconnection-line shared inductance structure. Finally, the performance of a two-phase LLC resonant converter prototype is experimentally validated. The experimental results demonstrate that the proposed structure significantly reduces the output voltage and input current errors between the two phases under different resonant tank parameter variations. Additionally, this structure can be effectively extended to N-phase systems, providing an efficient voltage and current equalization solution for multi-module IPOS-type LLC resonant converters, with broad application prospects.

Future work will focus on in-depth investigations into the proposed shared inductance–capacitance structure, further evaluating its overall performance under non-ideal operating conditions. The planned tests and analysis include quantitatively assessing resonant tank voltage and current stress, system efficiency, and loss distribution tests. These endeavors will elucidate the impact of the proposed structure on voltage and current equalization accuracy, operational stability, and overall system performance.

Author Contributions: Methodology, A.L.; Software, A.L.; Validation, A.L.; Formal analysis, W.T.; Investigation, A.L.; Resources, J.L.; Writing—original draft, A.L.; Supervision, J.L. and W.T.; Project administration, J.L. and W.T. All authors have read and agreed to the published version of the manuscript.

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