

Article

A Comparative Study of SiC Power Module with Reduced Footprint for High Power Density Applications

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Abstract

Driven by the increasing demand for high power density in modern power electronic converters, this paper proposes two novel packaging designs based on the concept of an overlaying chip placement structure, including the design with a two-layer substrate (designated as M2) and the one with a three-layer substrate overlaying structure (designated as M3). Electrical and thermal simulations demonstrate that M2 achieves a 32.78% volume reduction while incurring a 12.70% increase in average thermal resistance, and a 5.72% reduction in power loop parasitic inductance compared to the conventional packaging design (designated as M1), representing a balance between compact packaging and electrothermal performance. Meanwhile, M3 achieves an ultra-low loop inductance of 2.02 nH thanks to the mutual inductance cancellation effect; however, the physical volume is increased by 38.17%, and the thermal resistance is reduced by 1.59% compared to the M1 design. The prototype of the M1 power module has been fabricated for experimental validation. Double-pulse testing and steady-state thermal resistance measurements are conducted based on the M1 prototype to confirm the accuracy of the simulation model.

Keywords: SiC power module; packaging; power density; thermal management; parasitic inductance

1. Introduction

With the growing demand for high power density in modern power electronic converters, wide-bandgap (WBG) semiconductors, i.e., Silicon Carbide (SiC) and Gallium Nitride (GaN), have attracted much attention thanks to their premium electrical and thermal properties [1–3]. SiC devices exhibit superior characteristics over conventional silicon (Si) devices, including a higher operating switching frequency, a higher breakdown voltage and the capability to work at an elevated temperature [4–6]. Meanwhile, the continuous demand for higher power density places increasingly stringent requirements on module packaging design and the fabrication process. Such demand places special requirements on reducing the module footprint, which typically involves a trade-off with the thermal management capability of the power module. In addition, the fast-switching transients of SiC MOSFETs exacerbate sensitivity to parasitic parameters, causing significant voltage overshoots [7,8]. Consequently, it is quite challenging to achieve a power module design with balanced electrothermal performance [9].



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To overcome the electrothermal bottlenecks of conventional packaging, a variety of three-dimensional (3D) packaging techniques have been developed to shorten the commutation path, improve thermal management, and increase power scalability.

One category of designs focuses on compact structures that integrate double-side cooling or embedded dies within a minimized footprint. Chang et al. [10] presented a sandwiched press-pack module where laminated busbars and double-side heatsinks are directly packaged together, achieving low stray inductance and a balanced thermal distribution among paralleled chips. However, reliable pressure contacts for small SiC dies and gate connections remain challenging. The variation in die thickness needs to be strictly controlled. Special tooling with independent contact control is required to minimize the pressure difference applied to each die. Hoene et al. [11] employed PCB-embedded technology to realise sub-nanohenry inductance, yet they explicitly noted that the poor thermal conductivity of PCB materials severely limits heat dissipation in high-power applications. Yao et al. [12] proposed a wire-free PCB plus DBC hybrid module where microtube liquid cooling was used to improve the thermal capability. However, the microtubes embedded in the PCB substrate cannot be easily realised through standard PCB fabrication. Liang [13] and Huang and Chen [14] pursued wire-bondless double-side cooling through novel interconnect techniques—Planar-Bond-All and low-temperature co-fired ceramic (LTCC) interposers with copper balls, respectively—but neither has demonstrated proven long-term reliability or quantified performance under high-power conditions. Yang et al. [15] introduced an interleaved planar layout that places the phase-output electrode at the centre surrounded by power busbars, reducing inductance through mutual cancellation while ensuring symmetrical commutation and uniform temperature. Despite high power density and low inductance, compact structures remain limited by pressure-contact reliability, PCB thermal bottlenecks, and inter-chip thermal coupling.

A second group of studies consists of multi-layer hybrid structures that utilise multiple substrates to shorten the commutation path vertically, further lowering the parasitic inductance. Huang et al. [16] proposed a DBC-stacked hybrid structure that achieves low parasitic inductance through a 3D commutation path formed by two stacked DBC substrates. However, the dual ceramic layers increase thermal resistance, requiring SiC chips to be embedded in the bottom DBC to offset this penalty, which demands extremely high alignment accuracy. Ke et al. [17] proposed a 3D prismatic packaging method, and Hui et al. [18] introduced a multiple DBC-stacked units (MDSU) structure; both rely on multi-layer commutation paths to achieve mutual inductance cancellation and an enlarged heat dissipation area. Bruyere et al. [19] further proposed a modular 3D packaging concept assembling two DBC-sandwiched SiC prepackages with PCB motherboards via compressed copper foam to achieve a 2.7 nH stray inductance. These multi-layer hybrid structures increase process complexity, require careful optimisation of thermal coupling, and pose challenges to manufacturing yield, though they reduce parasitic inductance effectively.

The third category encompasses vertical-chip structures that fundamentally reorient the chips by stacking them vertically or placing them upright to achieve the shortest possible current paths and exploit 3D heat flow. Vagnon et al. [20] first demonstrated the power-chip-on-chip (PCoC) concept, stacking chips vertically and integrating them directly between busbars with pressure contacts for double-side cooling. This approach dramatically reduced parasitic inductance and electromagnetic interference (EMI) coupling, but the initial prototype was limited to a single-chip configuration. Regnat et al. [21] extended the PCoC idea to multi-chip paralleling by embedding four SiC MOSFETs in a PCB, achieving an ultra-low inductance of 0.25 nH with a balanced impedance layout. However, the thermal bottleneck of the PCB substrate remained unsolved. Liang et al. [22] constructed a vertical half-bridge by stacking copper core PCBs and

VDMOS transistors, achieving a thermal resistance of $1.9\text{ }^{\circ}\text{C}/\text{W}$. However, the middle PCB still reached $110\text{ }^{\circ}\text{C}$ at full power with severe inter-chip thermal coupling. Ribeiro et al. [23] stacked two SiC dies face-to-face with integrated ceramic decoupling capacitors, achieving a low loop inductance of 0.48 nH ; however, no assessment was conducted on thermal management.

In summary, 3D concepts targeting at low thermal resistance or low packaging parasitics often rely on the development of new packaging materials, e.g., interconnection and encapsulation materials, or the maturity of certain packaging processes, e.g., through-hole copper plating for the embedded power packaging concept. The introduction of these new packaging materials and processes requires thorough evaluation from electrical, mechanical, chemical, and economic aspects. Research and engineering optimisation needs to be completed before any novel 3D packaging concepts can be applied to mass production.

This paper proposes two packaging structures based on overlaying chip placement: a dual-DBC structure (M2) and a three-layer DBC stacked structure (M3). Detailed comparisons of the electrical and thermal characteristics of the proposed designs and the conventional packaging structure (M1) have been carefully conducted. An M1 prototype has been fabricated and validated through double-pulse testing and steady-state thermal testing, establishing an experimental baseline for subsequent comparison.

2. Module Design

To achieve a more compact SiC power module package, the upper-switch devices and the lower-switch devices of the power module are placed separately on the DBC substrate with only half of the dies used in conventional power modules. To complete the current commutation loop while adopting different thermal management technologies, two individual designs are proposed. The conventional module and the two proposed designs are designated as M1, M2, and M3, respectively. Detailed module designs are shown below.

2.1. Conventional Packaging Structure (M1)

The schematic of the M1 design is shown in Figure 1, representing the conventional half-bridge package. Both the upper-switch and the lower-switch devices are soldered on the DBC substrate, with a pin-fin liquid-cooled heatsink connected to the bottom of the ceramic substrate. For ease of demonstration, only the main power section of the DBC and the overall layer structure are shown in Figure 1, omitting details such as the control leads and the NTC sensors that are used for temperature measurement. Specifically, the footprint of the DBC in the M1 design is $44.34\text{ mm} \times 63.36\text{ mm}$. A commercially available heatsink made of copper is used for thermal dissipation, with a total thickness of 8.8 mm , and the overall module height (including the heatsink) is 10.11 mm .

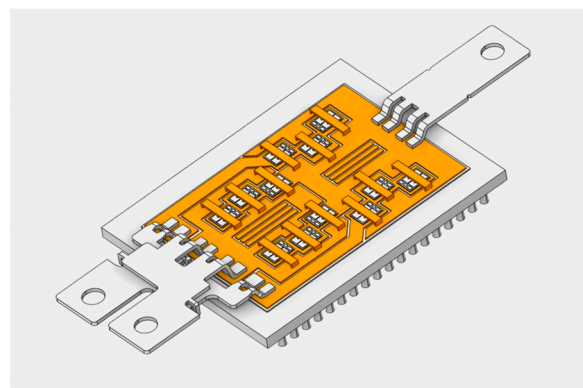


Figure 1. Structure of the conventional half-bridge power module (M1).

2.2. Dual-DBC Vertical Structure (M2)

The schematic of the M2 design is shown in Figure 2, which employs a two-layer DBC stacked structure. The upper-switch and the lower-switch devices are placed on two separate DBC substrates of half the size of the ones used in the M1 design. These two substrates are then placed on the front and the back sides of the same heatsink, allowing for only half the packaging footprint compared to the M1 design. Electrical interconnections between the upper-switch and the lower-switch are achieved through additional power terminals. The heatsink, which is sandwiched between two DBCs, is slightly different from the one used in the M1 design such that two flat surfaces are used to enclose the pin-fins in the cooling path. The total thickness of the heatsink is 10.0 mm, with a central pin-fin height of 4 mm and 3 mm copper plates on each side. Figure 2a,b show the module structural views as observed from the upper-switch and the lower-switch, respectively, while Figure 2c represents the overall cross-sectional view of the arrangement of the DBCs, heatsink, and connection terminals. The footprint of M2 is 44.34 mm × 34.12 mm, representing a 46.15% reduction compared to that of M1. Despite the slight increase in total height, this substantial area saving yields a total volume of only 19,092.56 mm³, a 32.78% reduction compared to that of the M1 design.

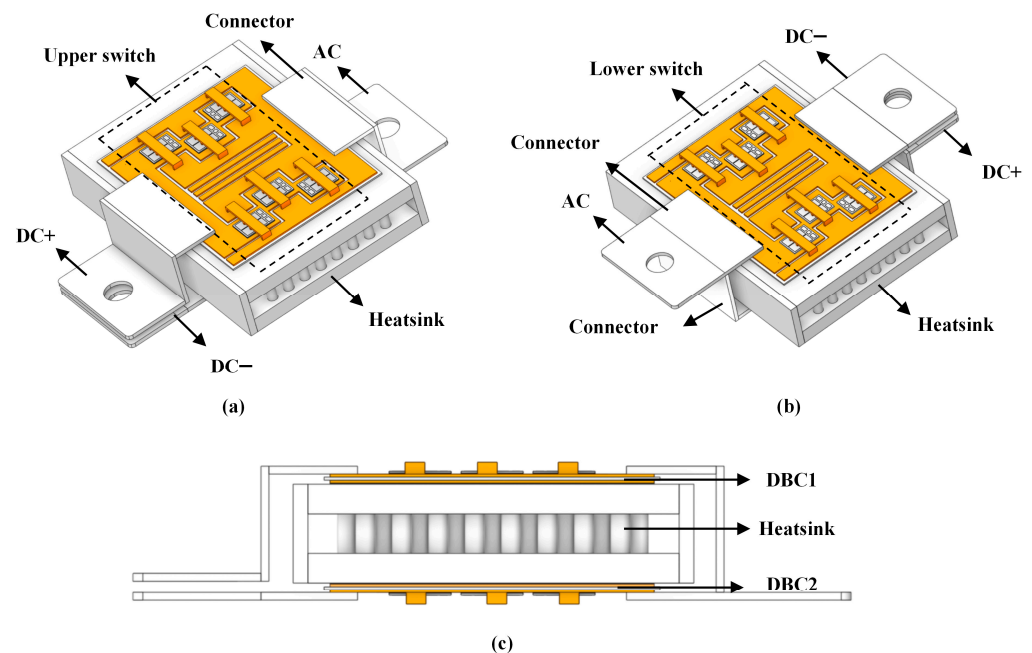


Figure 2. Structure of the proposed vertical-chip dual-DBC module (M2). (a) View from the high-side switch. (b) View from the low-side switch. (c) Cross-sectional view.

2.3. Three-Layer DBC Stacked Structure (M3)

The schematic of M3 is shown in Figure 3. This design employs a three-layer DBC overlaying structure, designated as DBC1, DBC2, and DBC3 from top to bottom. The upper-switch and the lower-switch devices are attached to the top and the bottom copper layers of DBC2, respectively. These devices are then connected to DBC1 and DBC3 through copper spacers by silver sintering. Electrical interconnections between the upper-switch and the lower-switch are achieved through power terminals between the upper and the lower copper layers of DBC2. DBC1 and DBC3 not only serve as circuit interconnections but also connect to pin-fin heatsinks on their outer sides, forming a dual-channel heat dissipation path. Figure 3a,b show the device layout views as observed from the upper-switch and the lower-switch, respectively. The heatsinks, as well as DBC1 and DBC3, are removed to better show the internal structure close to DBC2. Figure 3c presents the overall

cross-sectional view. The heatsinks employed on both sides are identical to those in M1, each with a total thickness of 8.8 mm. The footprint of M3 is the same as M2 for ease of comparison. However, due to the introduction of two heatsinks, three DBC layers, and the copper spacers, M3 reaches a total height of 25.94 mm, an increase of 156.58% over M1. The total volume of the M3 design also reaches 39,244.13 mm³, an increase of 38.17% compared to the M1 design.

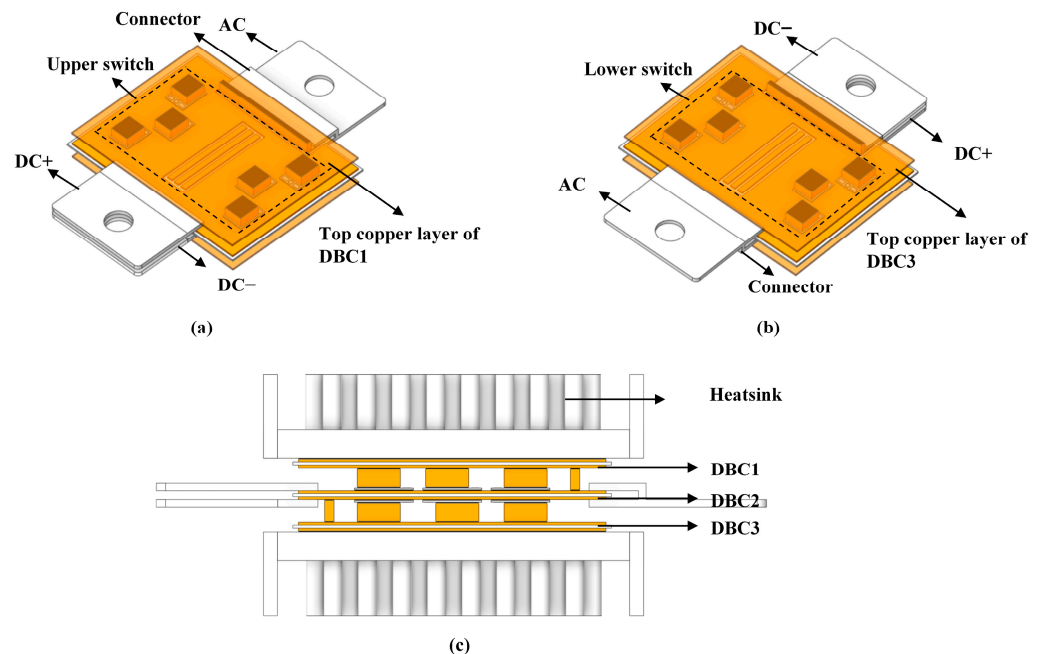


Figure 3. Structure of the proposed stacked three-layer DBC module (M3). (a) High-side view with the heatsink, backside copper, and ceramic of DBC1 removed, showing the circuit copper layer and chip layout. (b) Low-side view with the heatsink, backside copper, and ceramic of DBC3 removed, showing the circuit copper layer and chip layout. (c) Cross-sectional view.

Table 1 summarises the detailed dimensional comparison for the three above-mentioned module designs. M2 and M3 exhibit a significant advantage in substrate area, providing greater layout design freedom that allows further optimisation of electrical performance. However, it is challenging to mass-produce M2 and M3 power modules due to their overlaying structures; special jigs and tools are needed to protect the dies or the ceramic substrate on one side while attaching the dies and substrates to the other side. Compared to the M3 design, the assembly process for M2 is relatively straightforward. Silver sintering die-attach and wire-bonding of SiC devices on each ceramic substrate can be performed independently. Two ceramic substrates are then attached to the opposite sides of the heatsink by silver sintering to allow for low interfacial thermal resistance. Since the sintered silver remains in the solid phase even at high-temperatures, the substrate-attachment process can be performed in series. On the contrary, the fabrication process for the M3 design is slightly more complicated since additional heatsinks and spacers are required, which may cause a lower fabrication yield. In addition, for the M2 design, splitting a large ceramic substrate into two smaller pieces may be beneficial for the die-attach process since low warpage of the substrate is expected and only half of the dies are involved when preparing one of the substrates. Such concerns will be addressed in the following research based on module prototypes.

Table 1. Dimensional comparison of the three modules.

Module	Height (mm)	Height vs. M1	Footprint (mm × mm)	Footprint (mm ²)	Footprint vs. M1	Volume (mm ³)	Volume vs. M1
M1	10.11	—	44.34 × 63.36	2809.38	—	28,402.86	—
M2	12.62	+24.83%	44.34 × 34.12	1512.88	−46.15%	19,092.56	−32.78%
M3	25.94	+156.58%	44.34 × 34.12	1512.88	−46.15%	39,244.13	+38.17%

3. Electrothermal Performance Comparative Analysis

3.1. Power Loop Parasitic Inductance Analysis

The parasitic inductance introduced by packaging has a critical impact on the switching performance of SiC devices [24]. High power loop parasitic inductance induces severe voltage overshoot during the turn-off period and strong oscillation during the switching transients, thereby constraining the inherent high-speed switching advantage of SiC devices [25]. The geometric dimensions and configurations of conductors within the package directly influence the parasitic inductance.

The fundamental principles for reducing conductor parasitic inductance can be understood from two perspectives. For a single-layer planar conductor, the self-inductance is primarily determined by the current path length and the cross-sectional area of the conductor; thus, inductance can be reduced by shortening the current path or enlarging the conductor cross-section. For dual-layer parallel conductors, when the current in the upper and the lower layers flows in opposite directions, the mutual inductance cancellation principle dictates that the magnetic fluxes generated by the two conductors are anti-parallel, yielding a negative mutual inductance that effectively reduces the net parasitic inductance. This principle has been widely applied in stacked busbar designs and multi-layer DBC power module configurations.

Figure 4 illustrates the power loop current commutation paths of M2 and M3, where electrical interconnection between the high-side and low-side switches is achieved through connection terminals. ANSYS Q3D Extractor is used to conduct finite element extraction of the power loop parasitic inductance for the three modules. The simulation frequency range is set from 0 to 1 GHz. Due to the skin effect, the parasitic inductance decreases gradually with increasing frequency and stabilises above 10 MHz. The simulation results are presented in Figure 5.

The power loop parasitic inductance of M2 at 100 MHz is 9.07 nH, 5.72% lower than that of M1 (9.62 nH). The analysis reveals that although M2 utilises only approximately half the DBC area of M1, resulting in a proportionally shortened current path on the DBC, the power terminals between the upper-switch and the lower-switch introduce additional current path length, partially offsetting the inductance reduction achieved by the DBC area reduction. Further optimisation of the connection terminal width and geometry could yield additional reductions in parasitic inductance for M2.

The power loop parasitic inductance of M3 at 100 MHz is only 2.02 nH, representing a 79.00% reduction compared to M1. This significant reduction is attributed to the unique three-layer DBC stacked structure of M3, such that the DC+ and the DC− currents flow through the upper and lower copper layers of the same DBC (DBC2) in opposite directions. This configuration fully exploits the mutual inductance cancellation effect, dramatically reducing the net parasitic inductance. However, special attention is needed when building the M3 power module since the DC+ and DC− currents are only separated by a thin ceramic substrate. An encapsulant, such as silicone gel or epoxy moulding compound, with high dielectric strength is required to fill all the gaps among power paths before the power module can be used for any electrical characterisation. Fortunately, such a method

has already been employed in commercial power modules, e.g., eMPack from Semikron, for automotive applications. The isolation between the DC+ and DC− current paths of the M3 prototype will be verified by a HiPot tester.

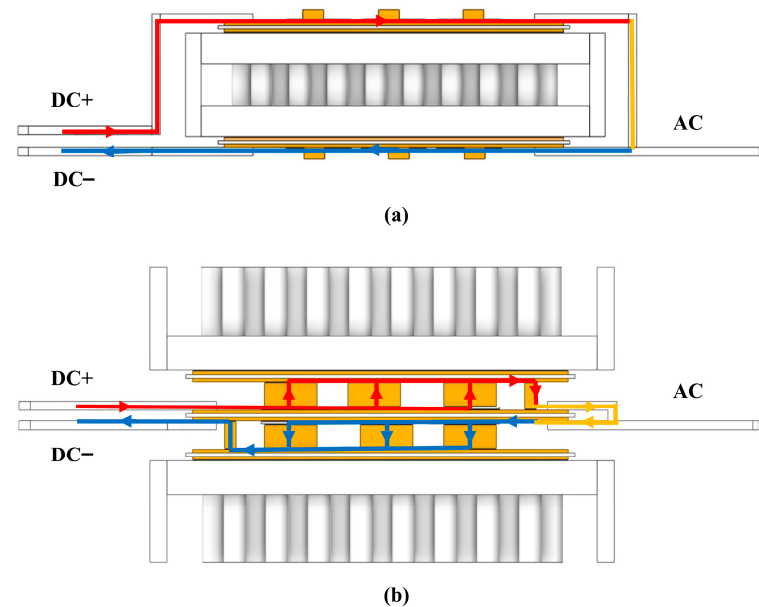


Figure 4. Power loop current commutation paths of the proposed modules. (a) M2. (b) M3.

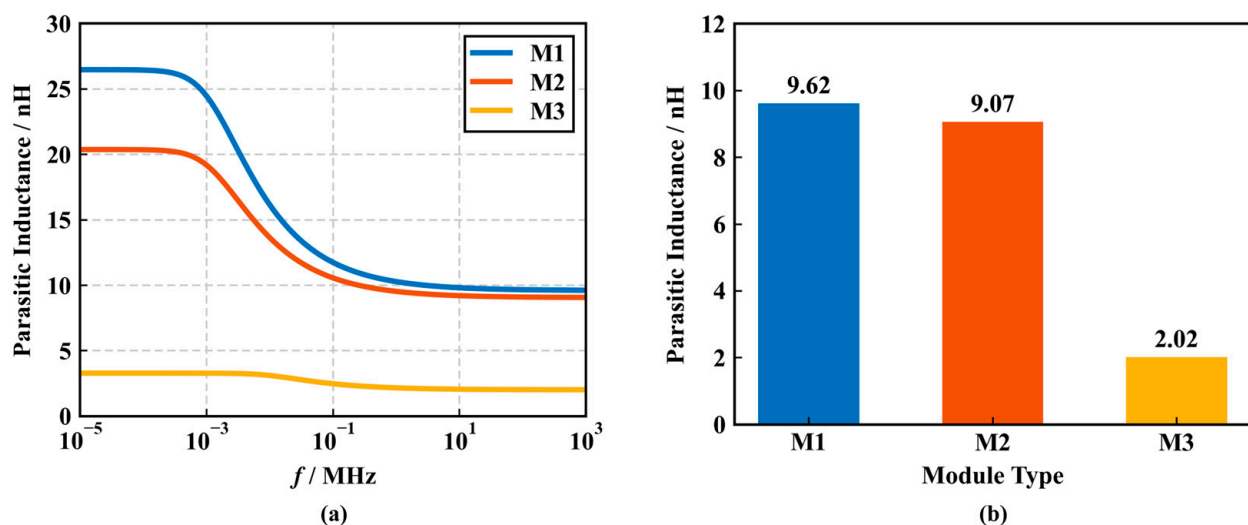


Figure 5. Power loop parasitic inductance simulation results extracted by ANSYS Q3D. (a) Simulation results of parasitic inductance. (b) Comparison of parasitic inductance at 100 MHz.

3.2. Thermal Management Performance Comparison

Power losses under both static and switching conditions cause the junction temperature to rise, thereby limiting the output current capability of the power devices [26,27]. Optimising the module thermal management technology is of paramount importance for enhancing power density. In addition, inter-chip thermal coupling is crucial in determining the thermal resistance of each device, which needs to be mitigated at all costs. For power modules with any given footprint, the key to minimizing the thermal coupling among devices is to create the shortest thermal dissipation path between the device and the coolant, such that most of the heat can be dissipated to the coolant directly along the vertical direction, rather than forming a large spreading angle between neighbouring dies

that causes a high thermal coupling effect. In this regard, Ansys Icepak is used to conduct a comparative thermal performance analysis of the three modules [28].

A mixture of 50%/50% ethylene glycol-water is used as a coolant, with an inlet temperature of 50 °C and a flow rate of 1 m/s. In each simulation, power is applied only to the devices in the same switch, with each chip dissipating 50 W (300 W in total), reflecting the operating characteristic of half-bridge topologies wherein the upper-switch and the lower-switch do not conduct current simultaneously. Detailed material properties and layer thicknesses are listed in Table 2. The DBC substrate employs a Cu/Si₃N₄/Cu sandwich structure with a total thickness of 0.92 mm. The junction-to-coolant average thermal resistance is defined by equation:

$$R_{th,j-f} = \frac{T_{j,avg} - T_f}{P_{loss}}, \quad (1)$$

where $T_{j,avg}$ is the average junction temperature of the chips, T_f is the coolant inlet temperature, and P_{loss} is the dissipation power per chip.

Table 2. Material properties and thickness of module structure.

Component	Material	Thickness (mm)	Thermal Conductivity (W/m·K)
Chip	SiC	0.19	340
Solder	SAC305	0.10	56.9
DBC	Cu/Si ₃ N ₄ /Cu	0.92 (total)	395/90/395
Heatsink	Cu	8.8/10.0 *	395
Spacer	Cu	2.00	395

* 8.8 mm for M1 and M3; 10.0 mm for M2.

Figure 6 presents the thermal simulation results of M1, where Figure 6a shows the overall temperature distribution contour of the module, Figure 6b displays the junction temperature distribution of the active chips on one side, and Figure 6c shows the cross-sectional temperature distribution, illustrating the heat dissipation path from the chips through the die-attach layer and the DBC substrate to the pin-fin heatsink. The average junction temperature of M1 is 81.42 °C, corresponding to an average thermal resistance of 0.63 °C/W.

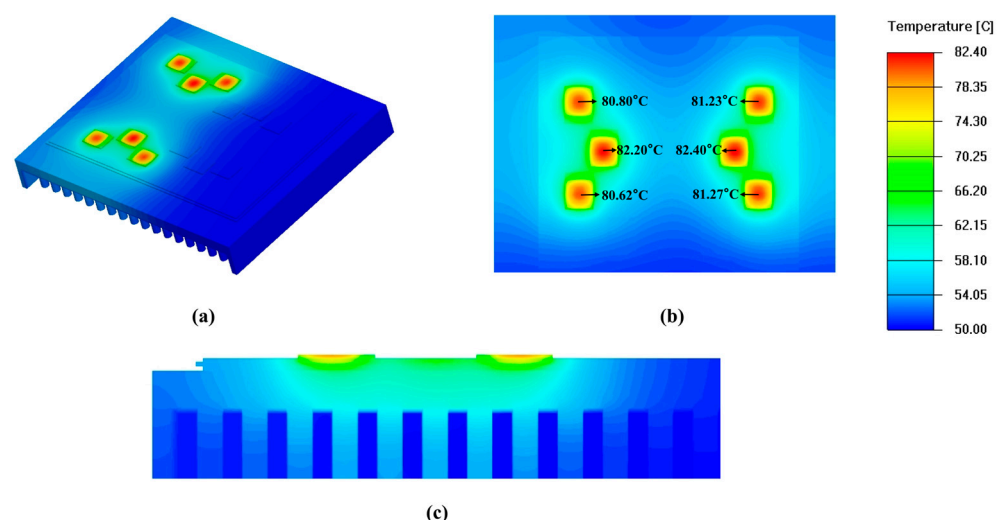


Figure 6. Thermal simulation results of M1. (a) Overall temperature distribution. (b) Junction temperature distribution of the active chips. (c) Cross-sectional temperature distribution.

Figure 7 presents the thermal simulation results of M2. Figure 7a shows the overall temperature distribution contour, Figure 7b displays the junction temperature distribution of the chips, and Figure 7c shows the cross-sectional temperature distribution. The average junction temperature of M2 is 85.72 °C, with an average thermal resistance of 0.71 °C/W, representing a 12.70% increase compared to that of M1. The increased thermal resistance is primarily due to the reduction in the pin-fin height, which was 4 mm compared to the 5.8 mm height of the ones used in M1.

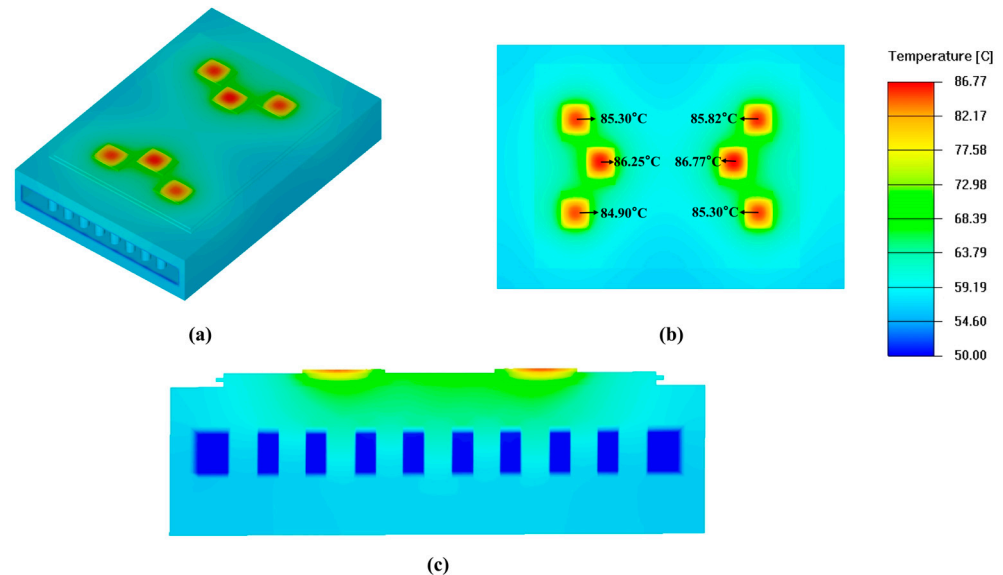


Figure 7. Thermal simulation results of M2. (a) Overall temperature distribution. (b) Junction temperature distribution of the active chips. (c) Cross-sectional temperature distribution.

Figure 8 presents the thermal simulation results of M3. Figure 8a shows the overall temperature distribution of the thermal dissipation structure above the chips, illustrating the top-side heat dissipation path unique to M3, where heat is conducted from above the chips through the copper spacers and DBC1 (or DBC3) to the outer heatsinks. Figure 8b and Figure 8c display the top-view junction temperature distribution and the cross-sectional view, respectively. The average junction temperature of M3 is 80.75 °C, with an average thermal resistance of 0.62 °C/W, representing a 1.59% reduction compared to that of M1. M3 features a dual-channel heat dissipation path. Although the cooling capacity beneath the chips is limited, the top-side dissipation channel bears most of the heat load, resulting in a modest overall reduction in thermal resistance.

As illustrated in Figure 9, M2 exhibits the highest thermal resistance of 0.71 °C/W, primarily attributed to the reduced pin-fin height in the sandwiched heatsink structure, while M3 achieves the lowest value of 0.62 °C/W, as the additional top-side heat dissipation path provides limited thermal improvement relative to the conventional single-side cooling approach.

To further evaluate the trade-off between thermal performance and volumetric efficiency, Table 3 summarises the comparative relationship between volume and thermal resistance across the three designs. M2 allows significant power density improvement, while M3 achieves the lowest thermal resistance due to the dual-side cooling design.

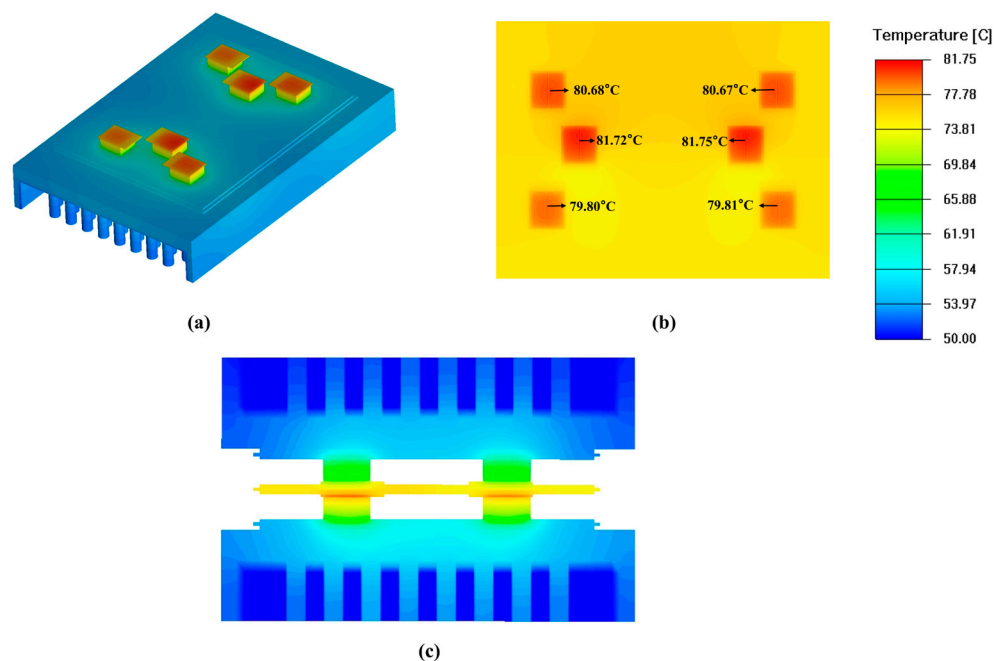


Figure 8. Thermal simulation results of M3. (a) Temperature distribution of the top-side heat dissipation structure (heatsink and DBC above the chips). (b) Junction temperature distribution of the active chips. (c) Cross-sectional temperature distribution.

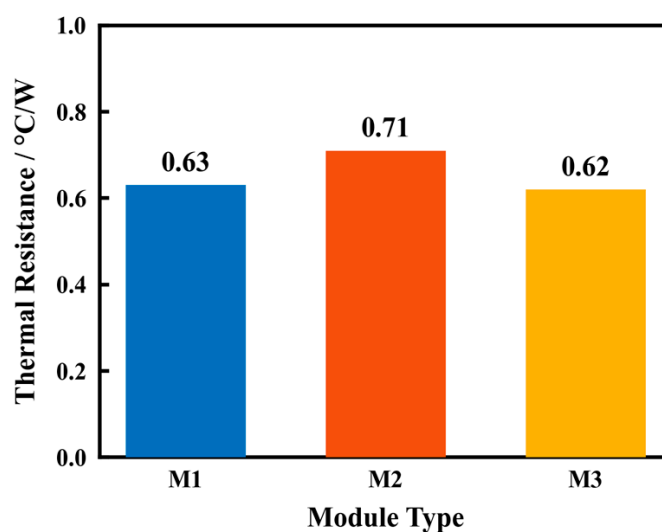


Figure 9. Comparison of thermal resistance.

Table 3. Comprehensive comparison of volume and thermal resistance.

Module	Volume (mm ³)	Volume vs. M1	$R_{th,j-f}$ (°C/W)	$R_{th,j-f}$ vs. M1
M1	28,402.86	—	0.63	—
M2	19,092.56	−32.78%	0.71	+12.70%
M3	39,244.13	+38.17%	0.62	−1.59%

4. Experimental Verification

To validate the accuracy of the simulation analysis and establish an experimental baseline for the subsequent M2 and M3 comparison, an M1 prototype has been fabricated, as shown in Figure 10. SiC MOSFET bare dies (model SG2M014120BJ) from SiChain

Semiconductors (Ningbo) Co., Ltd. (Ningbo, China) were used to construct the three-phase half-bridge power module, with each bridge arm comprising six paralleled chips. The double-pulse test (DPT) was employed for the extraction of the power loop parasitic inductance, and the steady-state thermal test was conducted for validating the thermal resistance of M1.

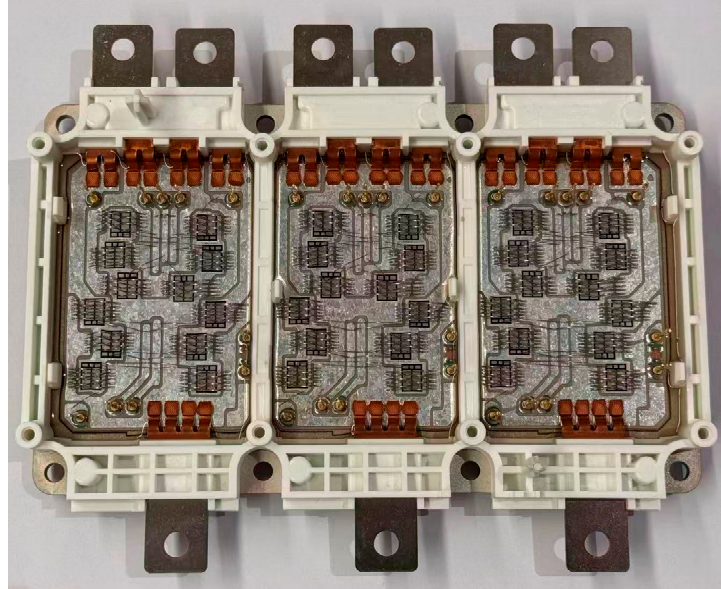


Figure 10. M1 prototype.

4.1. Double-Pulse Test

The DPT bench is shown in Figure 11, with the detailed testing conditions listed in Table 4. The bus voltage was set to 550 V, the load inductance to 20 μH , the turn-on gate resistor $R_{g,on}$ to 9.1 Ω , and the turn-off gate resistor $R_{g,off}$ to 7.4 Ω . The switching current during the first pulse was 600 A.

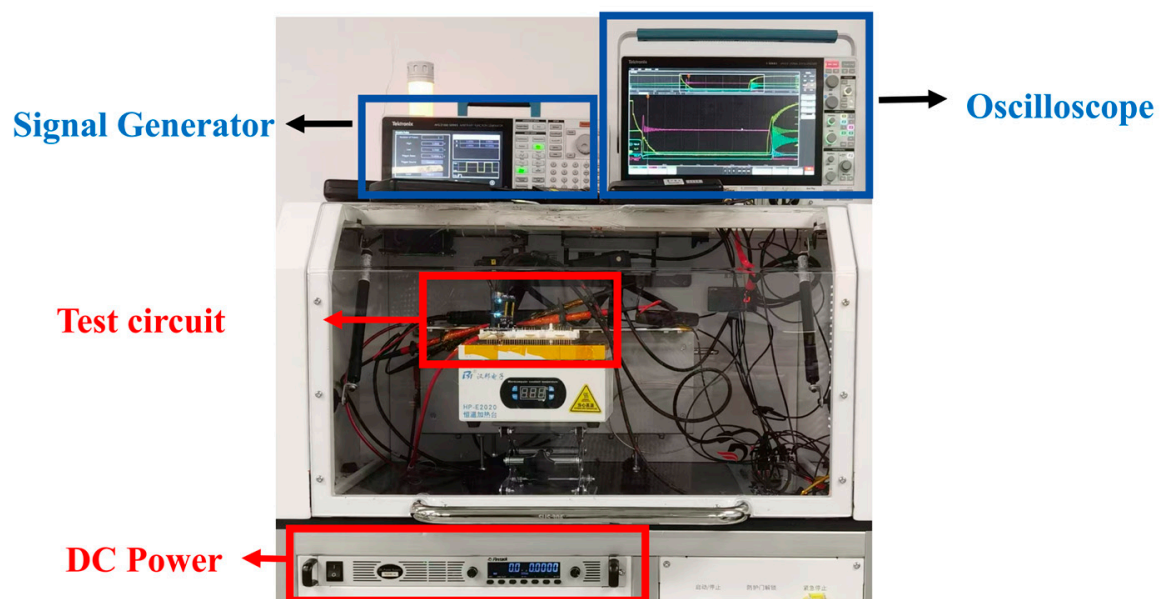


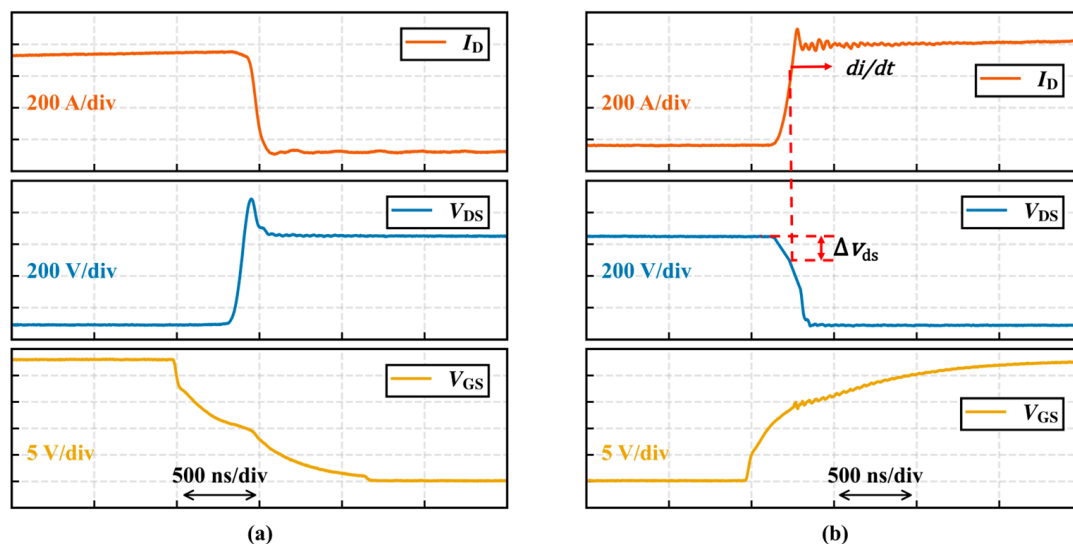
Figure 11. DPT experimental setup.

Table 4. Double pulse test conditions.

Parameter	Value	Unit
Ambient temperature	25	°C
Bus voltage (V_{dc})	550	V
Load inductance (L_{load})	20	μ H
Gate resistance, turn-on ($R_{g,on}$)	9.1	Ω
Gate resistance, turn-off ($R_{g,off}$)	7.4	Ω
External gate capacitance ($C_{gs,ext}$)	10	nF
Switching current (I_{sw})	600	A

Figure 12 presents the DPT switching waveforms of the upper-switch at 550 V/600 A, including the turn-on and the turn-off transients. The module exhibited well-behaved switching characteristics under these test conditions, with no abnormal gate oscillation observed. The power loop parasitic inductance was calculated from the drain-source voltage drop and the drain current rate of change during the second turn-on event:

$$L_{loop} = \frac{\Delta v_{ds}}{di/dt}. \quad (2)$$

**Figure 12.** DPT switching waveforms of M1 at 550 V/600 A. (a) Turn-off transient. (b) Turn-on transient.

Using the waveforms shown in Figure 12b as an example, the measured turn-on transient voltage drop, Δv_{ds} , was 190 V, and the current slew rate, di/dt , was 7.5 A/ns, yielding a total loop inductance of 25.33 nH for this measurement, including the parasitic inductance of the external capacitor and connectors. Across multiple measurements under varying operating conditions and different bridge arms, the average total loop inductance was 26.11 nH. The parasitic inductance introduced by the decoupling capacitor and external connectors in the loop was separately measured as 16.16 nH. Subtracting the external parasitic inductance from the total yielded a module-level power loop parasitic inductance of 9.95 nH for M1. The experimental result of 9.95 nH deviated by only 0.33 nH from the ANSYS Q3D (2024 R1) simulation of 9.62 nH, demonstrating excellent agreement and validating the accuracy of the simulation model.

4.2. Steady-State Thermal Characterisation

To validate the thermal performance of M1, a steady-state thermal test was conducted using the Simcenter Power Tester, with the experimental setup shown in Figure 13. The testing conditions were consistent with the simulation boundary conditions described in Section 3.2, with a coolant flow rate of 1 m/s and a target dissipation power of 50 W per chip. Based on the on-state resistance $R_{ds(on)} = 13 \text{ m}\Omega$ of the chips, the required current per chip was calculated as approximately 62 A from the power dissipation relationship:

$$I = \sqrt{\frac{P}{R_{ds(on)}}}. \quad (3)$$

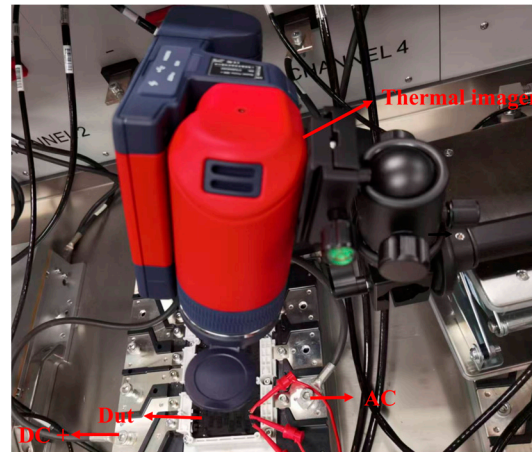


Figure 13. Setup of steady-state thermal testing.

With six chips connected in parallel on one side of the module, the total applied current was approximately 372 A. The module surface was coated with black paint to enhance surface emissivity, and an infrared thermal imager was used to record the temperature distribution contour after the chip temperature reached a thermal steady state.

The experimental results from Figure 14 showed that the maximum chip junction temperature was 83.20 °C, and the average junction temperature across the six chips was 82.30 °C. Accordingly, the average thermal resistance $R_{th,j-f}$ was determined to be 0.65 °C/W. The experimental thermal resistance, 0.65 °C/W, differed from the Ansys Icepak simulation value, 0.63 °C/W, in Section 3.2 by only 0.02 °C/W, a deviation of approximately 3.17%.



Figure 14. Thermal distribution of M1 under steady-state test. Captions on the upper-left corner shows the highest temperature of 83.2 °C and the lowest temperature of 34.8 °C.

5. Conclusions

This paper proposes two SiC power module packaging structures based on the concept of overlaying chip placement: a dual-DBC vertical structure (M2) and a three-layer DBC stacked structure (M3), to address the trade-off between footprint and electrothermal performance in high power density applications. Through systematic finite element analysis and comparison with the conventional half-bridge packaging structure (M1), the following conclusions are drawn.

An M1 prototype power module was fabricated for experimental validation. However, due to limited packaging resources, studies on the M2 and M3 module designs were only conducted based on finite-element analysis. It was found that both M2 and M3 achieved a 46.15% footprint reduction by placing the upper-switch and lower-switch devices on separate DBC substrates. M2 achieved a 32.78% volume reduction with only a 12.70% increase in average thermal resistance, primarily due to the reduced pin-fin height in the sandwiched heatsink. M3 achieved an ultra-low parasitic inductance of 2.02 nH by exploiting the mutual inductance cancellation effect between opposite direction currents on the upper and lower copper layers of DBC2; however, the introduction of dual heatsinks and three DBC layers resulted in a 38.17% volume increase with only a 1.59% thermal resistance improvement, rendering it less favourable from a power density optimisation standpoint.

Overall, M2 demonstrates a well-balanced trade-off among volume, thermal resistance, and parasitic inductance, along with favourable manufacturability, making it a promising packaging solution for high power density SiC modules. Both module-level parasitic inductance and the steady-state thermal resistance showed high consistency with the simulation values. These results confirm the accuracy of the simulation model and establish a reliable baseline for subsequent fabrication and comparative validation of the M2 and the M3 designs.

In addition to the electrical and thermal validation of the M2 and M3 designs, the thermomechanical reliability of the proposed designs will be evaluated once the samples are completed. Due to the symmetrical structure of M1 and M2, the thermomechanical stress will be balanced from the upper and the lower sides of the power module, similar to the construction of any direct-bond-copper ceramic substrate such that two copper layers with identical thickness are bonded to each side of the ceramic plate. It is likely that both structures will result in similar or even longer lifetimes than conventional power modules in thermal shock and power cycling testing.

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Abbreviations

The following abbreviations are used in this manuscript:

SiC	Silicon Carbide
GaN	Gallium Nitride
Si	Silicon
WBG	Wide-Bandgap
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
3D	Three-Dimensional
DBC	Direct Bonded Copper
PCB	Printed Circuit Board
LTCC	Low-Temperature Co-fired Ceramic
PCoC	Power-Chip-on-Chip
VDMOS	Vertical Double-Diffused Metal-Oxide-Semiconductor
MDSU	Multiple DBC-Stacked Units
EMI	Electromagnetic Interference
NTC	Negative Temperature Coefficient
DPT	Double-Pulse Test
SAC305	Sn96.5Ag3.0Cu0.5 Solder Alloy

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