

Article

Dual-Output, Hybrid-Clamped, Quasi-Five-Level Inverter and Its Modulation Strategy

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Abstract

This paper proposes a novel, dual-output, hybrid-clamped, quasi-five-level inverter (DO-HC-FLI) topology, capable of providing two independent AC voltage outputs with adjustable frequency and amplitude. Derived from a dual-output, active, neutral-point-clamped, three-level inverter, the proposed topology introduces three additional switches per phase to create dynamic switching paths. This expands the available range of DC-side voltage outputs and significantly improves the utilization rate of the DC-link voltage. Additionally, by adopting an asymmetric DC-link voltage configuration, the output line voltage levels of the conventional four-level inverter are increased to a number comparable to that of a five-level inverter. The front-end stage employs a hybrid series-parallel architecture, integrating dual Buck circuits with DC power sources. This configuration supplies the subsequent inverter stage with DC voltage levels at an optimal asymmetric ratio. In conjunction with a dual-output space vector pulse width modulation (SVPWM) strategy, the proposed system can collaboratively optimize the output voltage level characteristics of the inverter stage. Furthermore, a comprehensive analysis and comparison with other multilevel inverters are presented to demonstrate the superiority of the proposed topology. Finally, simulations and experiments are conducted to validate the effectiveness and feasibility of the proposed topology and modulation strategy.

Keywords: dual-output inverter; quasi-five-level; dual-output space vector modulation

1. Introduction

Driven by the global energy transition towards cleaner and low-carbon sources, the integration of renewable energy generation (such as photovoltaic (PV) and wind power) and the high penetration of distributed energy resources have become increasingly imperative. This trend imposes stricter requirements on power electronic inverters in terms of multilevel output capability, waveform quality, and multi-port control flexibility. Multilevel inverters have been widely adopted in medium- and high-voltage applications [1], such as motor drives [2,3] and grid-connected PV systems [4–6], owing to their distinct advantages, including excellent harmonic performance, low switching stress, reduced electromagnetic interference (EMI), and superior system efficiency [7,8].

As the foundational architecture of multilevel inverter technology, the three-level topology is the most widely applied. Currently, the mainstream three-level inverter topologies include the diode-clamped (neutral-point-clamped, NPC) inverter [9,10], the T-type inverter [11], the cascaded H-bridge (HB) [12,13], and the flying capacitor (FC) variant [14,15]. Furthermore, by employing advanced modulation strategies (e.g., SVPWM, VSVPWM),



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these inverters can optimize switching sequences, lower device switching frequency, and enhance overall efficiency [16]. Moreover, their inherent structural compactness renders them highly suitable for high-power-density designs.

Currently, although large-capacity inverters are technologically mature and widely deployed, they are typically restricted to a single operating mode—either grid-tied or standalone load supply. In complex scenarios requiring simultaneous grid connection and local load support, conventional single-port architectures suffer from hardware duplication and increased costs. Consequently, research attention is shifting towards integrated solutions, particularly dual-output inverters. These topologies enable simultaneous power delivery to both the grid and local loads via a single unit, effectively reducing the switch count and enhancing system power density.

Existing dual-output topologies can be broadly categorized into vertically stacked (series-type), parallel-configured, and switched-capacitor (SC)-based structures, each with inherent structural limitations.

The quasi-five-level inverter in [17] and the dual-output NPC in [18] represent the series-type approach, where output ports share the DC-link voltage vertically. Although [17] achieves a compact structure with reduced switch count, its vertically stacked configuration creates a strong coupling between the upper and lower ports. This forces the adoption of a time-sharing modulation strategy, leading to a significant penalty in DC-link voltage utilization. Similarly, while [18] reduces voltage stress on individual components, it is fundamentally constrained by the series architecture: the maximum modulation index for each port is rigorously capped at 0.5. This theoretical limit severely restricts their application in scenarios requiring the full-range independent operation of dual loads. Another category involves switched-capacitor (SC)-based topologies, which utilize the charging and discharging cycles of flying capacitors to synthesize multilevel outputs. As highlighted in a recent comprehensive review [19–21], while SC topologies can effectively reduce the number of DC sources, they inherently suffer from high inrush currents during the capacitor parallel charging states. This phenomenon imposes significant current stress on the switching devices, necessitating oversized components and reducing system reliability.

To break the modulation index barrier, the dual-output ANPC topology in [22] shifts to a parallel configuration. By structurally decoupling the two output groups, it successfully allows both AC outputs to reach the maximum modulation index, regardless of frequency differences. However, this architectural improvement comes at the cost of waveform quality. Being a three-level topology, it inherently produces line voltages with significantly higher harmonic content compared to five-level structures. Furthermore, the reliance on a split DC-link introduces complex neutral-point balancing challenges.

Consequently, a critical gap remains in the literature: there is a lack of a unified topology that simultaneously achieves full DC-link utilization (decoupling), high-resolution output (multilevel quality), and structural simplicity. The proposed topology is specifically designed to bridge this gap. Unlike [17,18], it adopts a specific switch-multiplexing architecture that eliminates the 0.5 modulation index limit. Unlike [19], it synthesizes a nine-level line voltage (pseudo-five-level performance) rather than a three-level one, significantly improving THD without the excessive component count of full dual-five-level inverters. This places the proposed solution in a unique position that balances control flexibility, waveform quality, and hardware cost.

In light of the escalating complexity of grid and load demands, architectural innovation in inverters has become imperative. To address the hardware redundancy and functional limitations of traditional single-port inverters, while simultaneously resolving the critical bottlenecks inherent in existing dual-output topologies—specifically restricted modulation indices and low DC-link voltage utilization—this paper proposes a novel dual-output

hybrid-clamped quasi-five-level inverter (DO-HC-FLI). The main contributions of this paper are summarized as follows:

- (1) A novel dual-output hybrid-clamped topology is proposed. By utilizing a hybrid clamping structure that introduces intermediate voltage levels (specifically $0.25 V_{dc}$ and $0.75 V_{dc}$), the proposed topology not only realizes high-performance dual-output operation but also eliminates the rigid sequential constraints of traditional architectures. This structural flexibility enables the selection of optimal switching paths within a single cycle, thereby significantly enhancing waveform quality.
- (2) In conjunction with the proposed modulation strategy, the configuration achieves full control decoupling between the two ports. This addresses the inherent flaw of traditional time-sharing schemes, where dynamic variations in voltage amplitude or phase at one port inevitably compress the available modulation space of the other, forcing a performance trade-off under complex asymmetric loading conditions (e.g., mixed heavy/light or high/low voltage loads). Consequently, the proposed approach overcomes the limitation of low DC-link voltage utilization, ensuring that the modulation index ranges of both outputs remain unconstrained and mutually non-interfering.
- (3) An optimized line voltage synthesis method is realized by strategically aligning phase voltage levels and utilizing their differential superposition to track sinusoidal reference trajectories. This establishes an efficient mapping mechanism where a simplified phase structure yields a nine-level line voltage output comparable to conventional five-level inverters. Consequently, the output waveform achieves a high degree of sinusoidal approximation, maximizing waveform quality and significantly reducing harmonic distortion.

In essence, this topology distinguishes itself from existing solutions by effectively bridging the gap between hardware simplicity and performance. It replicates the superior spectral quality of traditional five-level inverters using significantly fewer switches, and critically, it eliminates the voltage utilization constraints of conventional dual-output designs, thereby maximizing DC-link usage.

2. Topology and Working Principle of DO-HC-FLI

2.1. Topology of DO-HC-FLI

The structure of the proposed dual-output, hybrid-clamped, quasi-five-level inverter is illustrated in Figure 1.

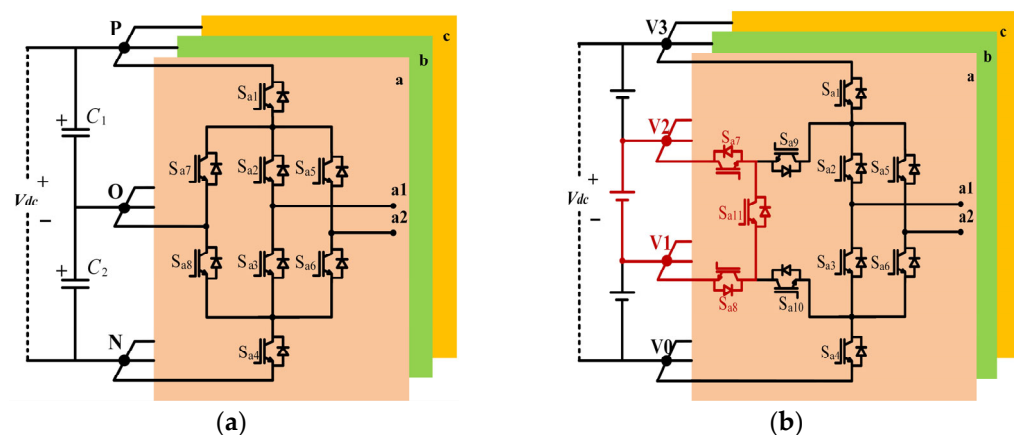


Figure 1. Topology structure of inverter: (a) topology of dual-output, active, neutral-point-clamped, three-level inverter; (b) topology of dual-output, hybrid-clamped, quasi-five-level inverter.

The three bridge arms of the proposed inverter topology share an identical structure, with each phase comprising 11 switches, denoted as S_{x1} – S_{x11} (where x represents the phase index from the set $\{a, b, c\}$). Taking phase a as an example, the external switches S_{a1} and S_{a4} are responsible for introducing the two outermost DC voltage levels to the internal output branches. Switches S_{a2} and S_{a3} constitute the first output branch, leading to the first output port $a1$; meanwhile, switches S_{a5} and S_{a6} form the second output branch, which is arranged in parallel with the first, leading to the second output port $a2$. Regarding the clamping mechanism, the upper clamping switches S_{a7} and S_{a9} introduce the $0.75 V_{dc}$ level, while the lower clamping switches S_{a8} and S_{a10} introduce the $0.25 V_{dc}$ level. Crucially, switch S_{a11} acts as a selective link for the intermediate levels. By coordinating the conduction states of the output bridges (S_{a2}/S_{a3} and S_{a5}/S_{a6}), it allows the two output ports to independently select and generate the desired voltage levels.

In contrast to conventional five-level inverters, the proposed topology significantly reduces the switch count while offering dual-output capability, allowing the upper and lower ports to operate independently.

2.2. Working Principle

Taking phase a as an example, the four phase voltage levels available at the circuit's output terminals are denoted as $V3$, $V2$, $V1$, and $V0$.

When one output terminal delivers the $V3$ level, the conduction of switches S_{a7} , S_{a10} , and S_{a11} enables the $V2$ level to be output to another terminal via the lower bridge arm. When one output terminal produces $V0$, switches S_{a8} , S_{a9} , and S_{a11} conduct, allowing the $V1$ voltage level to be output to another terminal via the upper bridge arm. From these switch states, it can be observed that this topology provides non-unique output paths for the intermediate voltage level, thereby enabling the independent control of each set of output terminals, enhancing the modulation index, and increasing control flexibility. All valid switch states are illustrated in Figure 2. Due to effective switch multiplexing, the switch states of the upper and lower ports are completely symmetrical. Therefore, eight independent switch states are detailed, and all valid switch states are presented in Table 1.

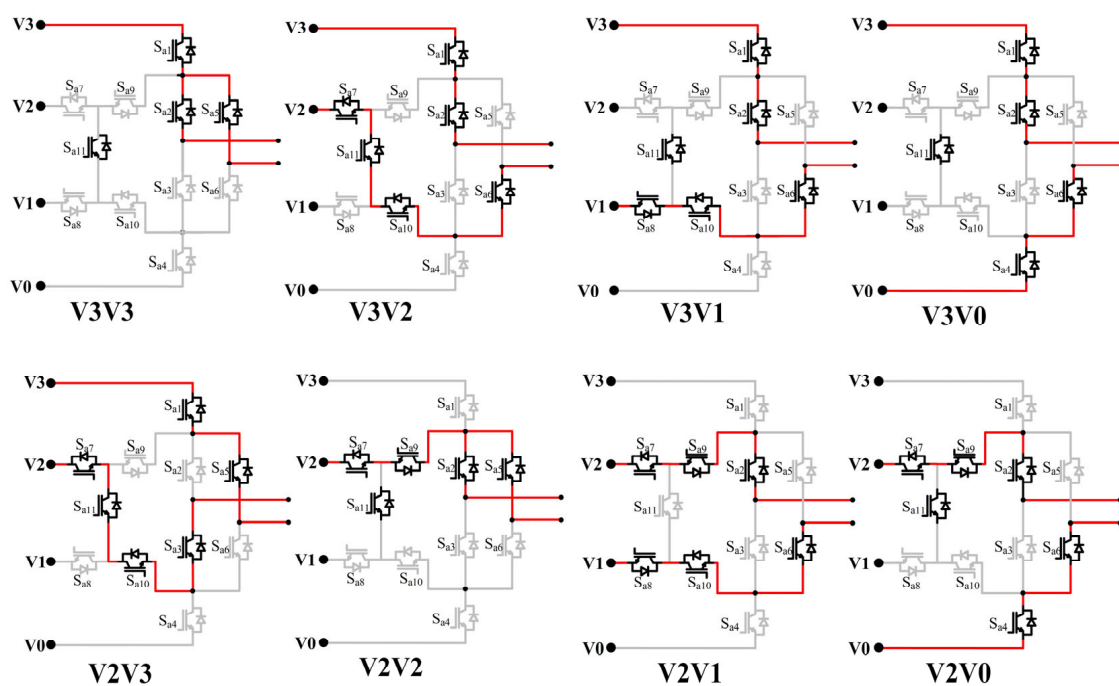


Figure 2. Effective working states of DO-HC-FLI.

Table 1. Effective operational status of the topological structure.

Group	Mode	On-State Switches	Up	Down
$V_{up} = V3$	1	$S_1S_2S_5S_{11}$	V3	V3
	2	$S_1S_2S_6S_7S_{10}S_{11}$	V3	V2
	3	$S_1S_2S_6S_8S_{10}S_{11}$	V3	V1
	4	$S_1S_2S_4S_6S_{11}$	V3	V0
$V_{up} = V2$	5	$S_1S_3S_5S_7S_{10}S_{11}$	V2	V3
	6	$S_2S_5S_7S_9S_{11}$	V2	V2
	7	$S_2S_6S_7S_8S_9S_{10}$	V2	V1
	8	$S_2S_4S_6S_7S_9S_{11}$	V2	V0
$V_{up} = V1$	9	$S_1S_3S_5S_8S_{10}S_{11}$	V1	V3
	10	$S_3S_5S_7S_8S_9S_{10}$	V1	V2
	11	$S_3S_6S_8S_{10}S_{11}$	V1	V1
	12	$S_2S_4S_6S_8S_9S_{11}$	V1	V0
$V_{up} = V0$	13	$S_1S_3S_4S_5S_{11}$	V0	V3
	14	$S_3S_4S_5S_7S_9S_{11}$	V0	V2
	15	$S_3S_4S_5S_8S_9S_{11}$	V0	V1
	16	$S_3S_4S_6S_{11}$	V0	V0

While the switching logic defines the available output paths, the specific voltage values assigned to these levels depend on the DC-link configuration. The operation of a multilevel inverter does not solely rely on a specific DC-side voltage distribution ratio. In principle, as long as the DC-side provides unequal voltage levels, a multilevel step wave can be synthesized through various switch combinations. In this context, the set of phase voltage levels ($0, 0.25 V_{dc}, 0.75 V_{dc}, V_{dc}$) adopted in this work represents an optimal solution derived from specific optimization criteria, rather than a unique feasible solution for system operation.

The gap between the chosen phase levels ($0.75 V_{dc} - 0.25 V_{dc}$) is exactly $0.5 V_{dc}$. This differential property allows the system to synthesize the “missing” intermediate level $0.5 V_{dc}$ in the line voltage output naturally. By selecting this specific asymmetric ratio, the resulting line-to-line voltage levels ($V_{AB} = V_A - V_B$) are expanded to $0, 0.25 V_{dc}, 0.5 V_{dc}, 0.75 V_{dc}$, and V_{dc} . This distribution ensures that the voltage steps are densely distributed in regions of rapid sinusoidal change (e.g., zero-crossing points), thereby maximizing the sampling resolution where it matters most. Consequently, this approach generates a refined nine-level staircase waveform with significantly lower harmonic content, achieving an output performance comparable to that of a standard five-level inverter.

It is worth noting that, while the output voltage levels are logically asymmetric, the underlying DC-link structure remains physically symmetric. Specifically, level V3 is generated by superimposing the voltage of V_{C1} onto the base potential E2. Numerically, the physical voltages across the two capacitors V_{C1} and V_{C2} are identical. Consequently, the negative impact on voltage balancing typically associated with asymmetric structures—where a high-voltage capacitor undergoes more frequent charge/discharge cycles than a low-voltage one—does not exist in this topology. The virtual vector V_{S1} , constructed via time-averaging, ensures that the switching sequence adheres to the single-step switching principle, maintaining state continuity during critical sector transitions. By refining the granularity of the voltage synthesis in these irregular sub-sectors, the virtual vector minimizes the deviation between the reference and applied vectors, thereby reducing current ripple and improving THD performance.

To stabilize the DC-link voltage of the preceding stage, this paper employs the DC-side power supply section depicted in Figure 3, which comprises two DC power sources and two Buck chopper circuits. The first Buck converter, Buck-1, consists of switch T_1 , inductor L_1 , diode D_1 , and capacitor C_1 , and is configured as a reverse-mode Buck converter. The

second Buck converter comprises switch T_2 , inductor L_2 , diode D_2 , and capacitor C_2 , and operates as a forward-mode Buck chopper circuit. The operation of two Buck converters enables the front-end DC-link to supply four distinct DC voltage levels (V_3 , V_2 , V_1 , V_0) to the subsequent three-phase inverter circuit.

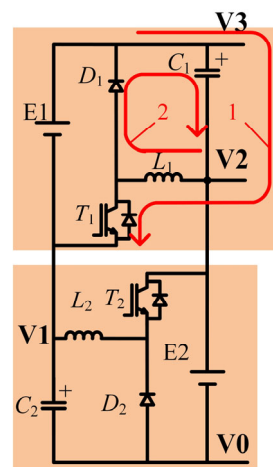


Figure 3. Working principle of Buck-1.

The operating principle is illustrated using the first Buck converter, Buck-1, as an example, as shown in Figure 3. When the DC-side voltage V_3 falls below the required voltage, since V_3 is equal to the voltage of the DC power supply, E_2 , plus the voltage across capacitor C_1 (i.e., $V_3 = E_2 + V_{C1}$), to increase the value of V_3 , it is necessary to increase the voltage across capacitor C_1 , V_{C1} . Consequently, the first Buck converter, Buck-1, operates. The operation of the Buck-1 converter is as follows: When switch T_1 is closed, inductor L_1 stores energy. The current path is from the positive terminal of DC source E_1 , through capacitor C_1 , inductor L_1 , and switch T_1 , to the negative terminal of DC source E_1 , as illustrated by loop 1 in Figure 3. Conversely, when switch T_1 is open, due to the inability of the voltage across inductor L_1 to change instantaneously, inductor L_1 discharges, thereby charging capacitor C_1 . In this state, the current flows from inductor L_1 , through diode D_1 , to capacitor C_1 , as illustrated by loop 2 in Figure 3.

When the DC-side voltage V_1 falls below the required level, since V_1 is equivalent to the voltage across capacitor C_2 (i.e., $V_1 = V_{C2}$) and simultaneously serves as the output voltage of the second Buck converter, Buck-2, an increase in V_1 necessitates raising the voltage across capacitor C_2 (V_{C2}). The second Buck converter, Buck-2, then activates. Its operational principle mirrors that of the first Buck converter and will not be reiterated. The DC-side power provision stage of the preceding section is capable of supplying four stable DC voltage levels to the subsequent three-phase inverter topology.

2.3. Voltage and Current Stresses on the Power Switch

By analyzing the effective switching states, the blocking voltage stress across each non-conducting switch is derived.

The voltage stress distribution for the non-conducting switches in phase a is detailed as follows:

Outer switches (S_{a1} , S_{a4}): The stress varies among $0.25 V_{dc}$, $0.375 V_{dc}$, $0.5 V_{dc}$, and $0.75 V_{dc}$. Notably, 56% of the operating states correspond to the lowest stress level of $0.25 V_{dc}$.

Hybrid clamping switches (S_{a7} , S_{a8}): These switches withstand discrete levels of 0, $0.25 V_{dc}$, and $0.5 V_{dc}$, with 67% of the states clamping at $0.5 V_{dc}$.

Central switch (S_{a11}): This component is subjected to a fixed peak stress limit of $0.5 V_{dc}$.

Clamping switches (S_{a9} , S_{a10}): The stress levels include $0.25 V_{dc}$, $0.375 V_{dc}$, $0.5 V_{dc}$, and $0.75 V_{dc}$, with 44% of instances at $0.25 V_{dc}$.

Inner switches (S_{a2} , S_{a3} , S_{a5} , and S_{a6}): These switches experience the broadest range of stress, covering $0.25 V_{dc}$, $0.375 V_{dc}$, $0.5 V_{dc}$, $0.75 V_{dc}$, and V_{dc} .

To obtain a comprehensive assessment of the switch's actual operating conditions, it is necessary to look beyond peak voltage and consider both the magnitude of the voltage stress and the duration of each operating state. Therefore, this paper adopts the time-average voltage stress (TAVS) as a key metric. A lower time-average voltage stress signifies that the switch experiences reduced voltage across the majority of its switching states, which in turn can mitigate switching losses (particularly turn-off losses). The hybrid clamping switches ensure that the switching states of this topology are complete and symmetrically distributed, making it highly suitable for calculating the time-average voltage stress. This metric quantifies the time-weighted operating voltage of the switch, thus enabling a more accurate assessment of the overall voltage stress level.

Calculations reveal that the time-averaged voltage stress on S_{a1} and S_{a4} is $0.403 V_{dc}$, on S_{a2} , S_{a3} , S_{a5} , and S_{a6} is $0.547 V_{dc}$, on S_{a7} and S_{a8} is $0.4375 V_{dc}$, and on S_{a9} and S_{a10} is $0.484 V_{dc}$. S_{a11} remains in the ON state for most of the time, experiencing $0.5 V_{dc}$ for only a very short duration.

In three-level NPC inverters, switching devices typically withstand voltage stress of $0.5 V_{dc}$ or higher. For five-level, diode-clamped inverters, the peak voltage across switching devices often reaches $0.5 V_{dc}$ or more, with the average voltage stress potentially approaching $0.5\text{--}0.6 V_{dc}$. Therefore, the TAVS across all switching devices in the proposed topology is significantly lower than the typical levels found in conventional five-level topologies. This reduced voltage stress allows for the consideration of power devices with slightly lower voltage ratings or superior on-resistance, while still satisfying safety margins, which helps to reduce system costs and decrease heat sink size.

The current flowing through the switching devices is a critical factor in determining inverter losses, junction temperature, and efficiency, which in turn dictates the overall performance of the power electronic equipment. Therefore, it is necessary to investigate the current carried by the switching devices within the topology.

Due to the inherent symmetry of the topological structure, the analysis of current paths is confined to the switching devices in the upper half. For a detailed illustration, the switching devices of the phase a bridge arm are selected. Let the current flowing out from the upper output terminal be i_1 and the current flowing out from the lower output terminal be i_2 , with the outward direction defined as positive. By formulating Kirchhoff's Current Law (KCL) equations within the circuit, the currents flowing through each switching device can be derived, as presented in Table 2.

Table 2. Instantaneous current of the switch tube corresponding to different switch states.

Switching State	i_{Sa1}	i_{Sa2}	i_{Sa5}	i_{Sa7}	i_{Sa9}
33	$i_1 + i_2$	i_1	i_2	0	0
32	i_1	i_1	0	i_2	0
31	i_1	i_1	0	0	0
30	i_1	i_1	0	0	0
23	i_2	0	i_2	i_1	0
22	0	i_1	i_2	$i_1 + i_2$	$i_1 + i_2$
21	0	i_1	0	i_1	i_1
20	0	i_1	0	i_1	i_1

2.4. Comparative Analysis and Scalability Discussion

The proposed topology is benchmarked against existing dual-output converters in Table 3, focusing on component count, voltage levels, and modulation flexibility.

Table 3. Comparison between the previous topologies and the proposed topology.

	Back-to-Back, 5-Level Inverter [23]	Dual-Output, Neutral-Point-Clamped, Three-Level Inverter [18]	Dual-Output, Quasi-Five-Level Inverter [17]	Proposed Topology
Power Switches	48	20	21	33
Clamping Diodes	72	12	6	0
Line-to-Line Voltage	9	7	9	9
Dual Outputs	Yes	Yes	Yes	Yes
Modulation	Yes	No	No	Yes
Index Independence				

It can be observed that, similar to the conventional independent NPC five-level inverter, the proposed structure supports unrestricted dual outputs and generates 9-level line voltages. However, by leveraging switch multiplexing, it achieves this with a reduced number of switches. Furthermore, compared to other switch-sharing counterparts, this topology successfully realizes mutually independent modulation ranges for both output ports while ensuring high output quality.

3. Modulation Strategy and Loss Analysis

Following the analysis of the topology and operating principles of the DO-HC-FLC presented in the previous chapter, this chapter focuses on its core modulation strategy and system losses. In existing research, time-sharing modulation has been commonly employed in dual-output topologies; however, it presents significant challenges in multi-port multilevel inverters, including limited degrees of freedom, degraded waveform quality, and uneven thermal distribution. Leveraging the unique hybrid clamping mechanism of the quasi-five-level topology, this chapter proposes a fully decoupled dual-output SVPWM strategy. This strategy achieves independent control of the dual-output ports in terms of frequency, amplitude, and modulation index by reconfiguring the clamping paths.

Furthermore, to comprehensively evaluate the efficiency performance of the proposed system, a detailed analysis of power loss characteristics is presented. Based on the calculated loss distribution, the overall system efficiency is further investigated across a wide range of modulation indices.

3.1. Analysis of Modulation Strategy

Given the asymmetric DC source configuration and the dual-output characteristics of this topology, traditional standard SVPWM algorithms are not directly applicable. Consequently, this chapter establishes a hierarchical modulation framework, the overall control block diagram of which is illustrated in Figure 4. The core concept of this strategy is to decompose the complex dual-output modulation task into two independent single-output modulation processes, which are then synthesized through a subsequent logic decision stage. As shown in the figure, the control flow consists of three main phases:

Major Sector Determination is first performed for the two sets of reference voltages (V_{ref1} and V_{ref2}). This is followed by precise Sub-sector Determination within the asymmetric vector space to address the mapping challenges caused by the non-uniform voltage-level distribution. Upon determining the sub-sector, the Duty Cycle Calculation is executed. Subsequently, the Switching Sequence and Dwell Time Calculations are performed. Adhering

to the principle of minimum switching transitions, the algorithm arranges the switching states and determines their dwell times for each basic voltage vector to ensure efficient operation. The switching states generated from both parallel channels are ultimately input into the Decision Block. This module is responsible for managing the coupling relationship between the two channels and synthesizing the final PWM driving signals, ensuring that the inverter can drive both loads (Load 1 and Load 2) simultaneously and independently. The subsequent sections will provide a detailed analysis of the implementation principles and logic design for the Major Sector Determination, Sub-sector Determination algorithms, Dwell Time Calculations under asymmetric conditions, and the Decision Block, respectively.

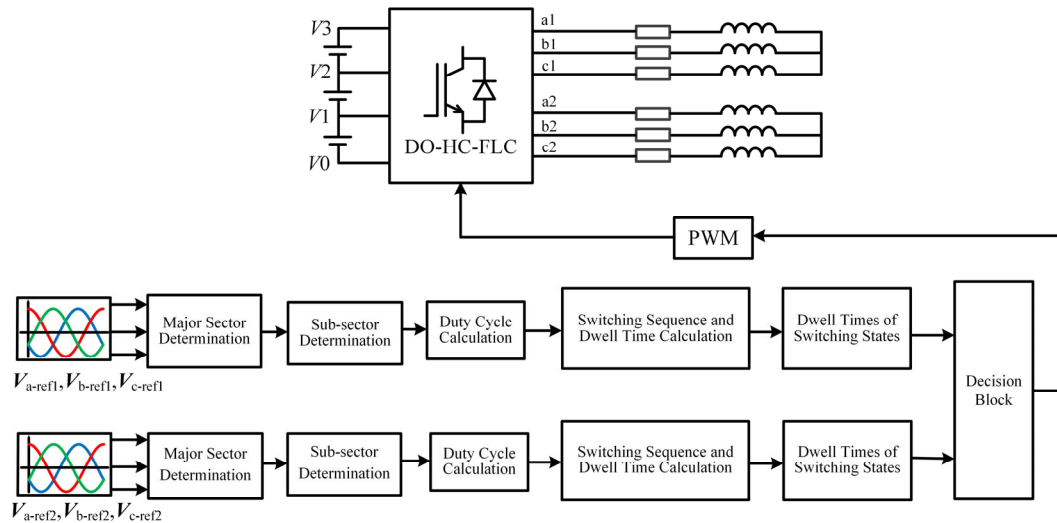


Figure 4. Implementation flowchart of dual-output SVPWM.

Assume that the three-phase reference voltage for the n -th output group is:

$$\begin{bmatrix} V_{a-refn} \\ V_{b-refn} \\ V_{c-refn} \end{bmatrix} = V_m \begin{bmatrix} \sin(\omega_n t + \varphi_n) \\ \sin(\omega_n t + \varphi_n - 2\pi/3) \\ \sin(\omega_n t + \varphi_n + 2\pi/3) \end{bmatrix} \quad (1)$$

In the equation, V_m , ω_n , and φ_n denote the amplitude, angular frequency, and initial phase of the three-phase reference voltage, respectively. Thus, the reference voltage vector V_{refn} for the n -th output group is given by:

$$V_{refn} = \frac{2}{3} \left(V_{a-refn} + V_{b-refn} e^{j\frac{2\pi}{3}} + V_{c-refn} e^{j\frac{4\pi}{3}} \right) \quad (2)$$

Let V_1 , V_2 , and V_3 be the three fundamental vectors involved in synthesizing the reference vector V_r . Their respective active durations are T_1 , T_2 , and T_3 , and the sampling period is T_s . Substituting these into the volt-second balance equation yields:

$$\begin{cases} V_1 T_1 + V_2 T_2 + V_3 T_3 = V_r T_s \\ T_1 + T_2 + T_3 = T_s \end{cases} \quad (3)$$

The space vector diagram for the first major sector under the SVPWM modulation scheme is illustrated in Figure 5a. Considering the reference vector V_{refn} located within the fourth sub-sector of the first major sector, as illustrated in Figure 5b.

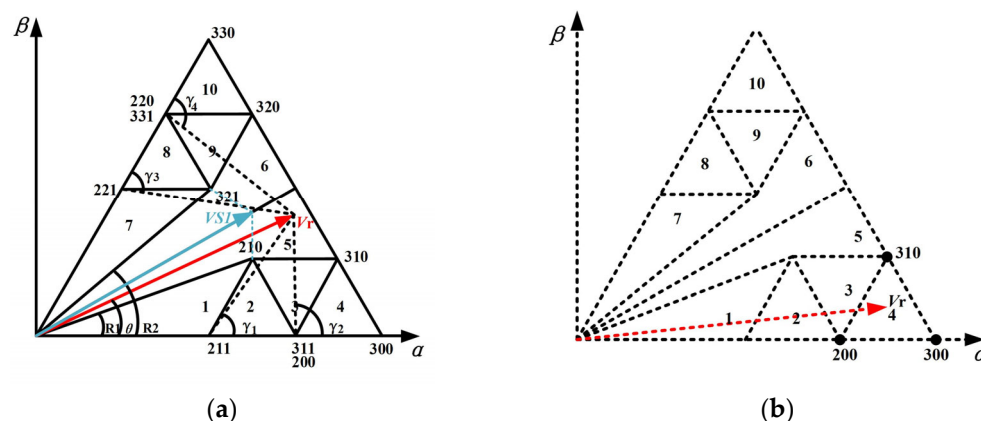


Figure 5. Sub-sector distribution and synthesis principle: (a) sub-sector division of Sector I; (b) vector synthesis in the fourth sub-sector of Sector I.

Referring to the position of V_{ref} in Figure 5a, the partition of minor sectors is determined by the angles formed by connecting V_{ref} to specific points. Consequently, the identification logic relies on the angular orientation of the lines linking V_{ref} to these key nodes. The mathematical definitions of these parameters are as follows:

The angle between the reference voltage vector V_r and the α -axis is θ , the angle with vector V_{210} is $R1$, and the angle with vector V_{321} is $R2$. V_r connects to $(2(V_2 - V_1)/3, 0)$ with an angle of γ_1 to the α -axis; to $(2V_2/3, 0)$ with an angle of γ_2 to the α -axis; to $(V_2/3, \sqrt{3}V_2/3)$ with an angle of γ_3 to the $\pi/3$ direction; and to $((V_2 - V_1)/3, \sqrt{3}(V_2 - V_1)/3)$ with an angle of γ_4 to the $\pi/3$ direction.

Initially, based on the angles of $R1$ and $R2$, the reference vector is located within one of the constituent sub-sectors (labeled 1, 5, 6, or 7) that comprise the 60° sector. $R1$ and $R2$ are calculated as follows:

$$R1 = \arctan \frac{\sqrt{3}V_1}{2V_2 - V_1} \quad (4)$$

$$R2 = \arctan \frac{\sqrt{3}(V_2 - V_1)}{2V_3 - V_2 - V_1} \quad (5)$$

The specific sub-sector among 2, 3, and 4 is identified using the angles γ_1 and γ_2 , whereas the location among sub-sectors 8, 9, and 10 is derived from γ_3 and γ_4 . γ_1 , γ_2 , γ_3 , and γ_4 are calculated as follows:

$$\gamma_1 = \arctan \frac{V_r \sin \theta}{V_r \cos \theta - 2(V_2 - V_1)/3} \quad (6)$$

$$\gamma_2 = \arctan \frac{V_r \sin \theta}{V_r \cos \theta - 2V_2/3} \quad (7)$$

$$\gamma_3 = \pi/3 - \arctan \frac{V_r \sin \theta - \sqrt{3}(V_2 - V_1)/3}{V_r \cos \theta - (V_2 - V_1)/3} \quad (8)$$

$$\gamma_4 = \pi/3 - \arctan \frac{V_r \sin \theta - \sqrt{3}V_2/3}{V_r \cos \theta - V_2/3} \quad (9)$$

After identifying the sector of V_{ref} , the vectors V_{200} , V_{300} , and V_{310} are selected for synthesis based on the nearest three-vector principle. Applying the volt-second balance principle allows for the calculation of the dwell times and duty cycles of each basic vector, thereby determining the specific switching sequence. The calculation equations are as follows:

$$\begin{cases} V_{200} \cos \theta T_1 + V_{300} \cos \theta T_2 + V_{310} \cos \theta T_3 = V_r \cos \theta T_s \\ V_{200} \sin \theta T_1 + V_{300} \sin \theta T_2 + V_{310} \sin \theta T_3 = V_r \sin \theta T_s \\ T_1 + T_2 + T_3 = T_s \end{cases} \quad (10)$$

The corresponding action times T_1 , T_2 , and T_3 for the three fundamental vectors are obtained. The three fundamental vectors contributing to the synthesis in region I4 are V_{200} , V_{300} , and V_{310} , with their respective action times being:

$$\begin{cases} T_1 = \frac{T_s (3V_r \cos \theta - 2V_3 + \sqrt{3}V_r \sin \theta)}{2(V_2 - V_3)} \\ T_2 = \frac{-T_s (3V_r V_1 \cos \theta - 2V_1 V_2 + \sqrt{3}V_r V_1 \sin \theta)}{2V_1(V_2 - V_3)} \\ \quad + \frac{2\sqrt{3}V_r V_2 \sin \theta - 2\sqrt{3}V_r V_3 \sin \theta}{2V_1(V_2 - V_3)} \\ T_3 = \frac{\sqrt{3}T_s V_r \sin \theta}{V_1} \end{cases} \quad (11)$$

The switching sequence of SVPWM is not unique. To prevent voltage transient issues, the switching sequence adopted in this paper is presented in Table 4 (switching sequence for the A1 major sector). Once the switching sequence and the active times of the synthesized vectors are determined, the active times for each switch can be obtained. By combining the vector active times with the vector states, a symmetrical five-segment SVPWM waveform can be derived, as shown in Figure 6.

Table 4. Vector order of the first sub-sector in Sector I.

Sub-Sector			Vector Order		
I1	210	211	111	211	210
I2	200	210	211	210	200
I3	200	210	310	210	200
I4	200	300	310	300	200
I5	210	310	320	310	210
I6	310	320	321	320	310
I7	222	221	321	221	222
I8	220	221	321	221	220
I9	320	321	331	321	320
I10	320	330	331	330	320

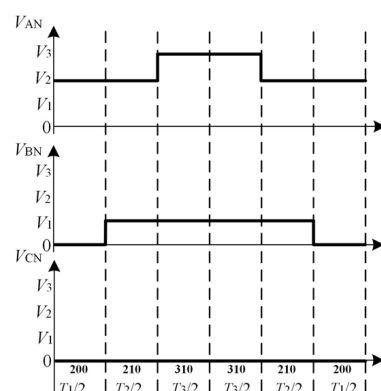


Figure 6. The switching time of the inverter.

The final pulse-width modulation pulses are then derived based on the active time of each switch during its respective switching state. As depicted in the figure, Sectors I, III, and V share an identical calculation method, while Sectors II, IV, and VI are calculated identically (and symmetrically to Sector I). This characteristic effectively reduces the complexity of the space vector pulse width modulation algorithm.

Figure 7a and Figure 7b respectively present the space vector distribution diagrams for the first major sector of the quasi-five-level inverter and the conventional five-level inverter. Due to the differing DC-link voltage values of the quasi-five-level inverter, this characteristic offers a significant advantage for its sector division scheme: its first major sector only requires partitioning into a smaller number of sub-sectors with simpler structures.

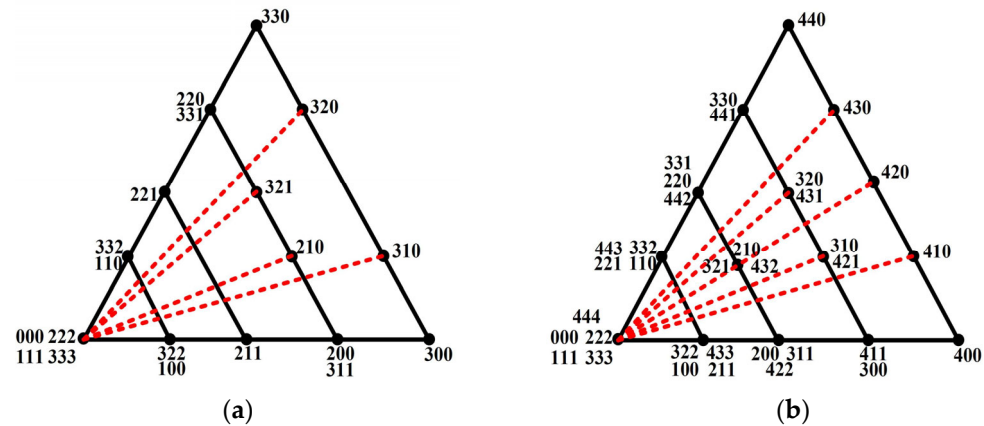


Figure 7. Space voltage vector distribution diagram: (a) vector distribution in the first major sector of the quasi-five-level inverter; (b) vector distribution in the first major sector of the five-level inverter.

The space vector distribution for each major sector of the quasi-five-level inverter is shown in Figure 8. Each three-phase voltage level state of the two output groups corresponds to a space vector. The space vector diagram for each output group is divided into six major sectors, defined as A_n to F_n , respectively, where $n \in \{1, 2\}$ represents the first and second output groups. Following the simplification of active vectors, each major sector can be divided into 10 sub-sectors.

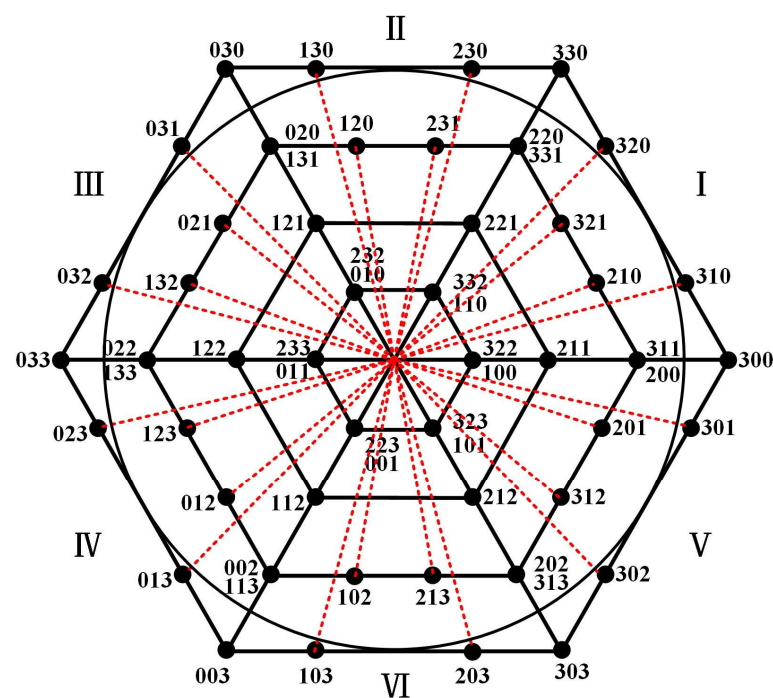


Figure 8. Quasi-five-level voltage space vector distribution diagram.

To address the discontinuities inherent in the unique level structure, virtual vectors are introduced in the fifth and sixth sub-sectors to optimize the switching transient performance during sector transitions. By constructing the virtual vector $V_{S1} = 5(V_{221} + V_{211})/6$, spatial

vector modulation is performed using differentiated basic vector combinations based on the specific positions within the fifth and sixth sub-sectors. Specifically, within the lower half of the fifth sub-sector, the vector required for voltage synthesis is V_{210} , $V_{S1}(V_{211}, V_{221})$, V_{222} . In the upper half of the same sector, synthesis is performed using vectors V_{210} , V_{310} , and V_{320} . This modulation strategy ensures that all voltage vectors can be effectively and continuously synthesized throughout the entire vector space, particularly in critical sector transition region. This achieves seamless coverage and smooth switching across all sub-sectors.

From an implementation perspective, the active synthesis of virtual vectors using existing switching states, rather than increasing the system burden, effectively reduces both control complexity and sensor requirements. This is because the method relies entirely on a software-based time-averaging algorithm that achieves precise waveform construction without the need for any additional hardware balancing circuits or an increased number of sensing components. Simultaneously, this synthesis logic is based on deterministic algebraic operations, avoiding the complex redundant state optimization or computations common in conventional methods, thereby significantly simplifying the implementation of the control system. The deployment of the virtual vector fundamentally optimizes the commutation trajectory. By inserting this intermediate state, the modulation enforces a strict nearest-level transition principle. This effectively mitigates long-distance vector jumps (e.g., sudden transitions across $0.5 V_{dc}$) and constrains the voltage step magnitude of each commutation to the minimum unit ($0.25 V_{dc}$). Such a mechanism not only prevents uncontrolled transients caused by simultaneous multi-device transitions but also significantly reduces the voltage stress (dv/dt) across the switches during commutation. Consequently, this leads to a direct reduction in the cumulative switching energy dissipation (E_{on}/E_{off}) and an improvement in electromagnetic interference (EMI) performance.

The vector distributions of other major sectors are similar to that of A1. Given the four output voltage level states: V_3 , V_2 , V_1 , and V_0 , and after simplification, there are 52 fundamental output voltage space vectors, as detailed in Table 5.

Table 5. Output voltage space vector of dual-output hybrid-clamped quasi-five-level inverter. ($X = 2V_3/3$, $Y = 2V_2/3$, $Z = X - Y = 2V_1/3$, $W = Y - Z$, $k = e^{j\pi/3}$).

Long Vector		Positive Central Vector		Negative Central Vector		Non-Zero Zero Vector		Zero Vector
300	X	320	$X + Yk^2$	310	$X + Zk^2$	211	W	333
330	Xk	230	$Y + Xk^2$	130	$Z + Xk^2$	221	Wk	000
030	Xk^2	032	$Xk^2 + Yk^4$	031	$Xk^2 + Zk^4$	121	Wk^2	222
033	Xk^3	023	$Yk^2 + Xk^4$	013	$Zk^2 + Xk^4$	122	Wk^3	111
003	Xk^4	203	$Y + Xk^4$	103	$Z + Xk^4$	112	Wk^4	
303	Xk^5	302	$X + Yk^4$	301	$X + Zk^4$	212	Wk^5	
2V2/3 Positive Short Vector		2V2/3 Negative Short Vector		Non-standard Positive Short Vector		Non-standard Negative Short Vector		
311	Y	200	Y	321	$X + Yk^2 + Zk^4$	210	$Y + Zk^2$	
331	Yk	220	Yk	231	$Y + Xk^2 + Zk^4$	120	$X + Yk^2$	
131	Yk^2	020	Yk^2	132	$Z + Xk^2 + Yk^4$	021	$Yk^2 + Zk^4$	
133	Yk^3	022	Yk^3	123	$Z + Yk^2 + Xk^4$	012	$Xk^2 + Yk^4$	
113	Yk^4	002	Yk^4	213	$Y + Zk^2 + Xk^4$	102	$Z + Yk^4$	
313	Yk^5	202	Yk^5	312	$X + Zk^2 + Yk^4$	201	$Y + Zk^4$	

3.2. Inverter Loss Analysis

During operation, power device losses are primarily categorized into three types: conduction loss, off-state loss, and switching loss. Specifically, due to the small leakage

current of the switching device in its off-state, off-state losses are typically considered negligible in engineering calculations. This paper proceeds to analyze the calculation methods for the conduction loss and switching loss of the switching device.

Given that the initial saturation voltage drop and on-resistance of the switching device vary approximately linearly with temperature, the initial saturation voltage drop $v_{0,T}$ and on-resistance r_T of the switching device are expressed as:

$$v_{0,T} = v_{0,T,25} + K_{v0,T}(T_{j,T} - 25^{\circ}\text{C}) \quad (12)$$

$$r_T = r_{T,25} + K_{r,T}(T_{j,T} - 25^{\circ}\text{C}) \quad (13)$$

where $v_{0,T,25^{\circ}\text{C}}$ and $r_{T,25^{\circ}\text{C}}$ are the initial saturated voltage drop and on resistance of the switch at junction temperature of 25°C , respectively; $K_{v0,T}$ and $K_{r,T}$ are the temperature correction coefficients of the initial saturation voltage drop and on resistance, respectively; $T_{j,T}$ is the junction temperature of the switch tube. Therefore, the conduction loss $P_{\text{cond},T}$ of the switch tube is calculated as

$$P_{\text{cond},T} = v_{0,T}I_T + r_T I_T^2 \quad (14)$$

where I_T is the instantaneous current value flowing through the switch tube.

The switching loss of the switch tube is composed of on loss and off loss, and the calculation formula is

$$E_{\text{sw},T}(I) = E_{\text{on},T}(I) + E_{\text{off},T}(I) = (A_{\text{sw},T}I_T^2 + B_{\text{sw},T}I_T + C_{\text{sw},T})\left(\frac{U_{\text{ce}}}{U_{\text{base}}}\right)^{D_{\text{sw},T}}\left(\frac{T}{T_{\text{base}}}\right)^{k_{\text{sw},T}} \quad (15)$$

where $A_{\text{sw},T}$, $B_{\text{sw},T}$, $C_{\text{sw},T}$ are the quadratic fitting curve coefficients of the switching loss of the switch tube with respect to the current; U_{ce} is the actual withstand voltage of the switch tube; U_{base} is the test voltage; T is the actual temperature of the switch tube; T_{base} is the test temperature; $D_{\text{sw},T}$, $k_{\text{sw},T}$ are the voltage correction factor and temperature correction factor of switching loss of switch tube, respectively.

In a switching cycle, the average switching loss of the switch is

$$P_{\text{sw},T} = f_{\text{sw}}E_{\text{sw},T}(I) \quad (16)$$

where f_{sw} is the switching frequency. The loss of anti-parallel diode in the process of turning on is very small and can be ignored.

The thermal model of DO-HC-FLI was established when $f_1 = 50\text{ Hz}$, $f_2 = 100\text{ Hz}$, $m_1 = 0.95$, $m_2 = 0.95$, $f_s = 10\text{ kHz}$, $V_{\text{dc}} = 48\text{ V}$, $R_{1,2} = 10\ \Omega$, $L_{1,2} = 10\text{ mH}$. Figure 9 shows the total loss distribution of each switching device of phase a under four commutation modes.

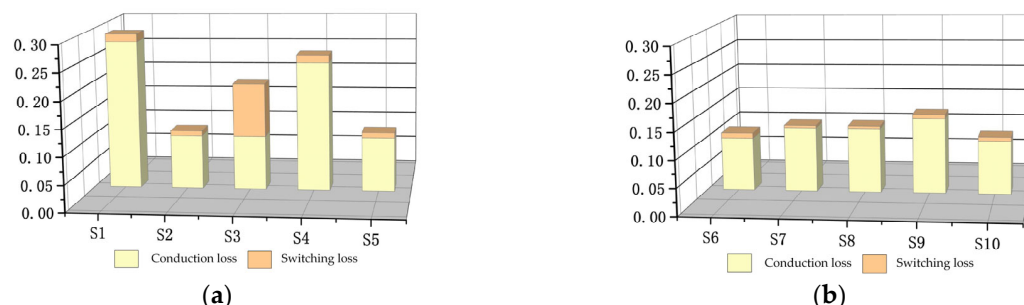


Figure 9. Switch loss distribution: (a) S1–S5 loss distribution; (b) S6–S10 loss distribution.

4. Simulation Results and Analysis

4.1. Output Waveform Analysis

To verify the feasibility of the dual-output, hybrid-clamped, quasi-five-level inverter, a simulation model will be established in the Matlab (R2021a)/Simulink environment. The

simulation parameters are as follows: the DC power supply voltage is 450 V, the capacitance of capacitors C_1 and C_2 is 75F, and the resistive–inductive (RL) load is configured with $R = 10 \Omega$ and $L = 10 \text{ mH}$. By adjusting the two Buck step-down circuits at the front end, the four output levels can be controlled as follows: $V_3 = 600 \text{ V}$, $V_2 = 450 \text{ V}$, $V_1 = 150 \text{ V}$, $V_0 = 0$.

The proposed inverter is tested in both same-frequency and different-frequency modes. Furthermore, to verify the independence of the two AC output ports under load variations, two identical sets of three-phase loads are connected in parallel to one port. At $t = 0.1 \text{ s}$, one set of loads is disconnected, and the three-phase output currents of the other port are observed to check for any cross-interference.

The experimental line voltage waveforms V_{ab1} and V_{ab2} for Mode a operation are depicted in Figure 10a,b. Both output sets exhibit a clear nine-level staircase structure, with voltage levels at $\pm 600 \text{ V}$, $\pm 450 \text{ V}$, $\pm 300 \text{ V}$, $\pm 150 \text{ V}$, and 0 V . The measured fundamental amplitude for both groups is 599 V, which closely matches the theoretical value of 597.6 V. Further spectral analysis is presented in the FFT results shown in Figure 10c,d. The measured total harmonic distortion (THD) is 20.37%. Crucially, the spectral distribution demonstrates that low-order harmonics (e.g., 5th and 7th orders) are effectively suppressed, verifying the efficacy of the proposed modulation strategy. Instead, the harmonic energy is predominantly concentrated in high-frequency bands near the switching frequency. This characteristic is highly advantageous for practical applications, as these high-frequency components are easily attenuated by the inductive nature of the load.

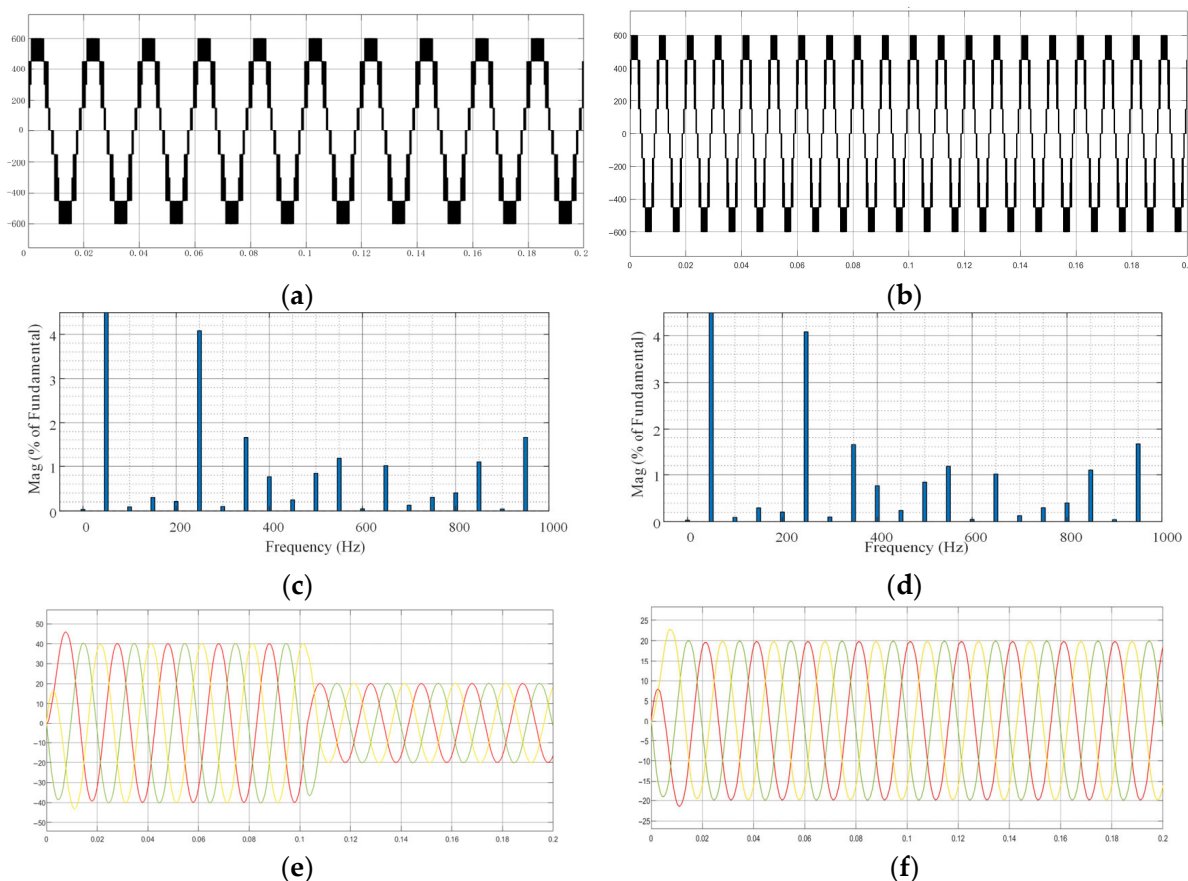


Figure 10. Simulation waveforms with $f_1 = f_2 = 50 \text{ Hz}$ and $m_1 = m_2 = 1.15$: (a) line voltage V_{ab1} ; (b) line voltage V_{ab2} ; (c) harmonic spectrum of V_{ab1} ; (d) harmonic spectrum of V_{ab2} ; (e) three-phase current i_{abc1} ; (f) three-phase current i_{abc2} .

When these voltages are applied to the load, balanced three-phase sinusoidal currents are obtained, as illustrated in Figure 10e,f. To evaluate the dynamic performance, a sudden

load change test was conducted. It can be observed that the output current amplitude responds instantly to the step change. The current decreases immediately to approximately half of its initial value with a smooth transition, exhibiting no noticeable overshoot or oscillation, while the other port remains unaffected. This stable and rapid transient behavior validates the excellent dynamic response capability of the controller.

The simulation waveforms of the two output line voltages, V_{ab1} and V_{ab2} , are shown in Figure 11a,b for mode a operation. As the modulation index decreases, the line voltage in Figure 10b changes to seven levels. In each basic cycle, the duration of the ± 600 V levels decreases, while the duration of the ± 450 V, ± 300 V, and ± 150 V levels increases. Figure 11c,d display the FFT analysis results for the two output line voltages.

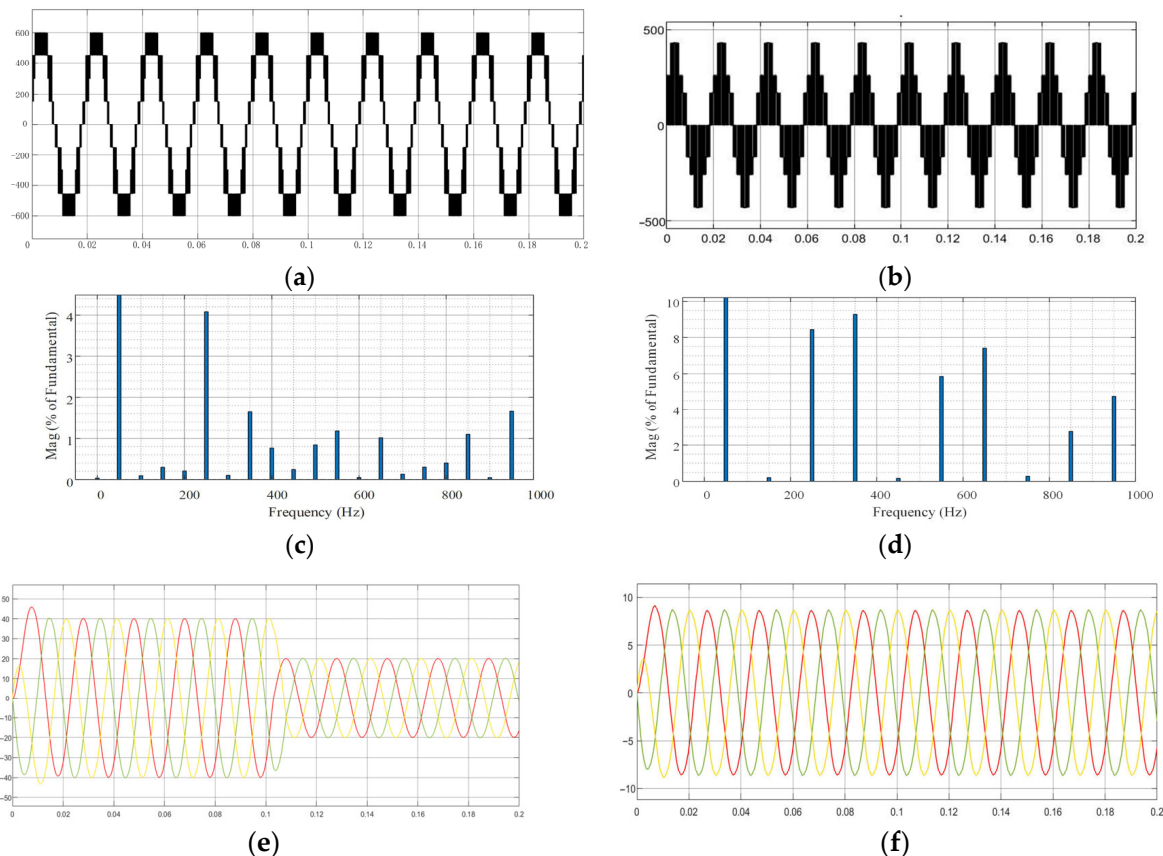


Figure 11. Simulation waveforms with $f_1 = f_2 = 50$ Hz, $m_1 = 1.15$, $m_2 = 0.566$: (a) line voltage V_{ab1} ; (b) line voltage V_{ab2} ; (c) harmonic spectrum of V_{ab1} ; (d) harmonic spectrum of V_{ab2} ; (e) three-phase current i_{abc1} ; (f) three-phase current i_{abc2} .

In mode c, the two sets of outputs are in different frequency modes. Figure 12a,b present the measured waveforms of the two output line voltages, V_{ab1} and V_{ab2} . It can be seen that the output line voltages of both groups can still maintain nine levels and can operate at maximum modulation. The FFT results for line voltages V_{ab1} and V_{ab2} are shown in Figure 12c,d. It can be seen that the fundamental wave amplitudes of the two sets of output line voltages are 601.2 V and 599.2 V, respectively, while the theoretical value is 597.6 V. The output voltage amplitudes closely match the theoretical values. Most harmonic components in V_{ab1} and V_{ab2} appear around the switching frequency and its integer multiples. Figure 12e,f confirm that the load currents remain highly sinusoidal throughout the dynamic process.

In mode d, the simulation waveforms of the output line voltages V_{ab1} and V_{ab2} are shown in Figure 13a,b. Figure 13c,d analyze the FFT of two sets of output line voltages.

The experimental waveforms show that the first set of outputs has seven levels, and as the modulation index decreases, the fundamental amplitude decreases, while the second set of outputs still has nine levels. As shown in Figure 13e,f, the dynamic response to the load step remains effective even at an output frequency of 100 Hz, while maintaining a symmetrical sinusoidal waveform.

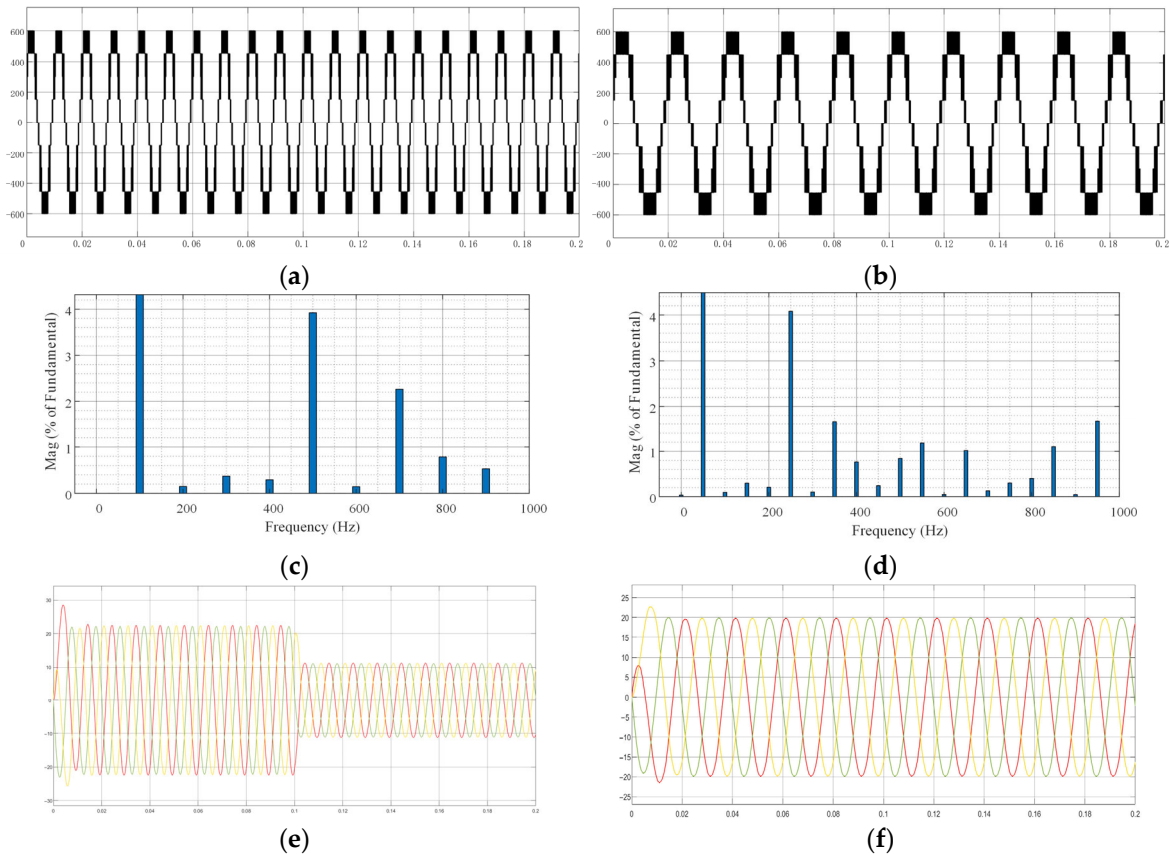


Figure 12. Simulation waveforms with $f_1 = 100$ Hz, $f_2 = 50$ Hz, $m_1 = m_2 = 1.15$: (a) line voltage V_{ab1} ; (b) line voltage V_{ab2} ; (c) harmonic spectrum of V_{ab1} ; (d) harmonic spectrum of V_{ab2} ; (e) three-phase current i_{abc1} ; (f) three-phase current i_{abc2} .

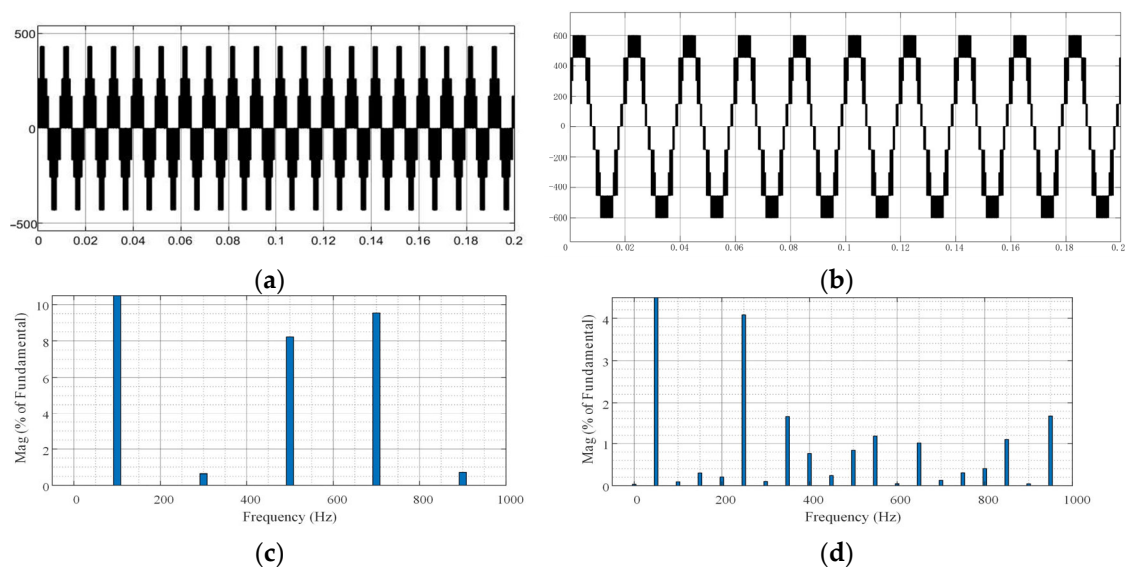


Figure 13. Cont.

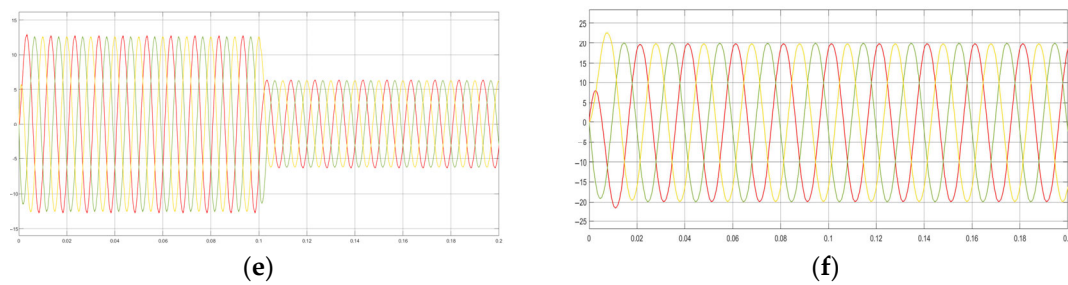


Figure 13. Simulation waveforms with $f_1 = 100$ Hz, $f_2 = 50$ Hz, $m_1 = 0.566$, $m_2 = 1.15$: (a) line voltage V_{ab1} ; (b) line voltage V_{ab2} ; (c) harmonic spectrum of V_{ab1} ; (d) harmonic spectrum of V_{ab2} ; (e) three-phase current i_{abc1} ; (f) three-phase current i_{abc2} .

4.2. Harmonic Performance and Efficiency Analysis

Total harmonic distortion (THD) is quantified as the root mean square (RMS) magnitude of the harmonic components divided by the RMS magnitude of the fundamental component in the inverter's output waveform.

$$THD = \frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + \dots + V_n^2}}{V_1} \quad (17)$$

where V_1 is the RMS value of the fundamental component, and V_n is the RMS value of the n th harmonic component ($n = 1, 2, \dots$).

To simultaneously account for the effects of both low-order harmonics and harmonics near the switching frequency, the maximum frequency for THD calculation is set to the Nyquist frequency (2500 kHz), with an output frequency of 50 Hz. Since changes in one set of outputs do not affect the THD value of the other set, the modulation index of the other set is fixed at 0.8 during THD measurement. The relationship between the two sets of output currents and the output line voltage THD values as a function of modulation indices m_1 and m_2 ($m_1, m_2 \in [0, 1]$) is shown in Figure 14. The figure reveals that, as modulation increases, the THD of the output line voltage gradually decreases. When modulation exceeds 0.5, the THD stabilizes around 25%, significantly lower than that of the ANPC.

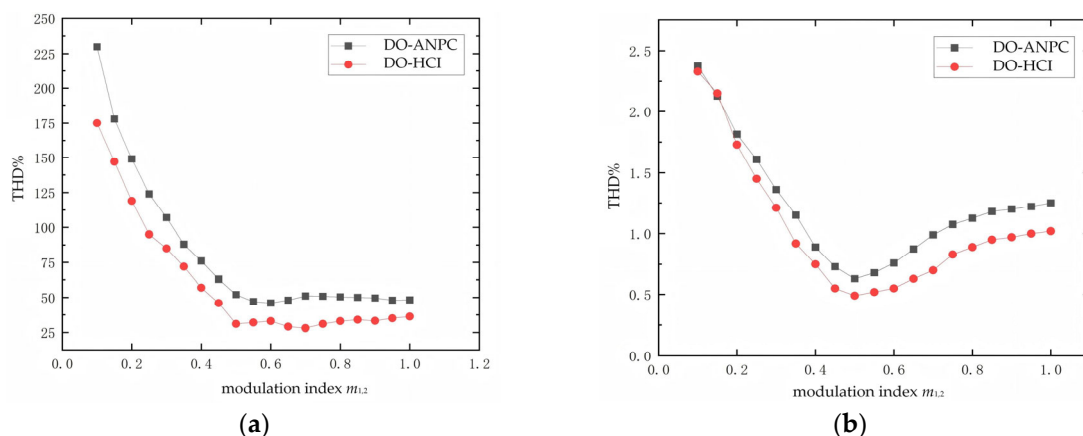


Figure 14. Comparison of THD test results: (a) total harmonic distortion of the output current; (b) total harmonic distortion of the output line voltage.

While this value is slightly higher than that of fully populated five-level inverters, it represents a highly favorable trade-off for space-constrained and cost-sensitive applications. Unlike conventional topologies that require massive hardware redundancy to achieve minimal THD, the proposed structure utilizes a minimal component count to realize dual-port independent control and nine-level voltage synthesis. This unique feature makes it

exceptionally suitable for compact dual-drive systems (e.g., dual-motor electric vehicles or conveyor belts), where reducing system volume and weight is prioritized over achieving marginally lower voltage THD. Furthermore, the spectral distribution confirms the design's practicality: the harmonics are primarily concentrated at high frequencies. When applied to inductive loads, these high-order harmonics are naturally filtered, resulting in a high-quality sinusoidal current. Thus, the topology successfully bridges the gap between the simplicity of three-level inverters and the performance of multilevel inverters, offering an optimal solution for scenarios demanding high power density.

To further evaluate the power conversion capability of the proposed topology, the system efficiency under different modulation indices is investigated. Figure 15 illustrates the efficiency curve where both ports operate symmetrically with the same modulation index. As observed, the efficiency exhibits a positive correlation with the modulation index. In the low-modulation region ($m < 0.4$), the efficiency is relatively low. This is primarily because the effective output voltage and power are small, while the constant losses account for a significant proportion of the total energy. In the high modulation region ($m > 0.8$), the efficiency improves significantly and stabilizes. Since the output power increases quadratically with the voltage, the growth in effective output power dominates over the increase in conduction and switching losses. Consequently, the inverter achieves its optimal performance in the linear modulation range near unity, reaching a peak efficiency of 97.2% at the rated output power of 32.6 kW.

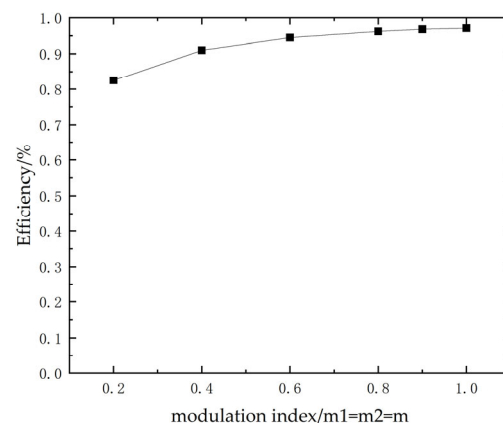


Figure 15. Simulated efficiency and total output power versus modulation index under symmetrical operation ($m_1 = m_2$).

5. Experimental Results

To validate the effectiveness of the proposed topology and modulation scheme, an experimental prototype of the DO-HC-FLI was built, as shown in Figure 16. The prototype includes a controller board, driver circuits, a main circuit, and two sets of three-phase loads. The control functions are jointly implemented by an FPGA-based PWM driving signal generation unit. The FPGA used is an Altera Cyclone IV series EP4CE115F23I7N, and the power devices are model IPW60R060P7.

In order to validate the independent control capability and the high DC voltage utilization of the proposed topology, the experimental verification was performed under asymmetrical conditions (i.e., distinct frequencies and amplitudes). This setup presents a more rigorous test than the symmetrical scenario, thereby confirming that the two outputs function independently without mutual coupling. The parameters of the experimental platform are shown in Table 6.

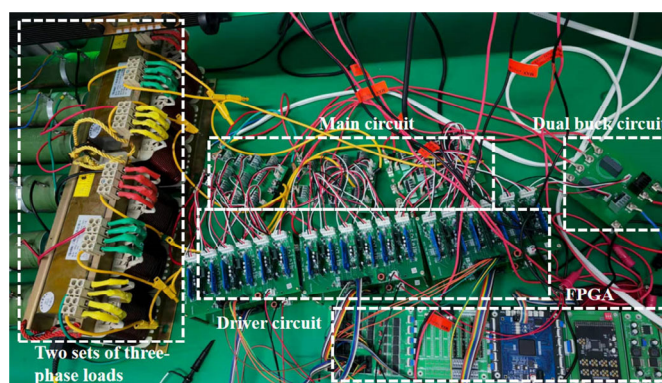


Figure 16. Experimental platform.

Table 6. System parameters and testing parameters.

Component	Parameters
DC-side four-level parameters/V	12, 36, 48
Modulation index	0.96/1.15
Carrier frequency f_s /kHz	10
Fundamental frequency f_s /Hz	50/100
Load resistance R/Ω	10
Load inductance L /mH	10
Capacitors $C_{1,2}/\mu\text{F}$	75

To verify the uniqueness of the topology, experimental parameters were set with different modulation indices for the upper and lower output ports and at different frequencies. Figure 17 shows the three DC voltage levels V3, V2, and V1 output by the Buck converters. Figure 18a,b show, respectively, the line voltage waveforms between phases a1 and b1, and between phases a2 and b2, at reference voltage frequencies of 50 Hz and 100 Hz.

As illustrated in Figure 18a,b, the proposed inverter generates a clear nine-level staircase line voltage waveform. The distinct voltage levels demonstrate the correct synthesis of the voltage vectors. Crucially, despite the distinct modulation indices and frequencies applied to the upper and lower ports, the voltage waveforms remain stable and undistorted. This experimental result strongly corroborates the decoupling capability of the proposed topology, verifying that the operation of one port does not impose interference on the other, even under asymmetrical conditions.

Furthermore, it can be observed from Figure 19a,b that, after simple filtering of the DO-HC-FLI output, good sinusoidal output voltage and current can be obtained. This is attributed to the multilevel characteristic of the DO-HC-FLI, which significantly reduces the voltage stress (dv/dt) and the harmonic content compared to traditional inverters. The smooth current waveforms further indicate the high tracking accuracy of the control strategy and the low current distortion.

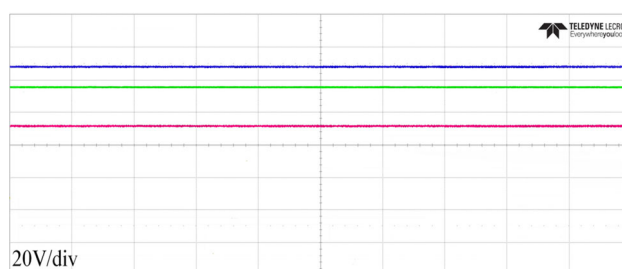


Figure 17. Four DC levels output by the front end.

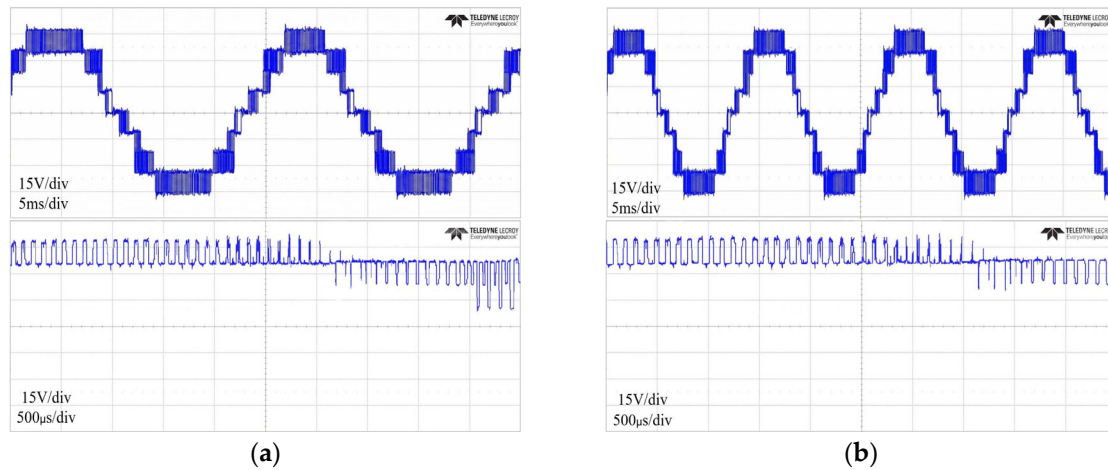


Figure 18. Line voltage waveforms: (a) upper output port; (b) lower output port.

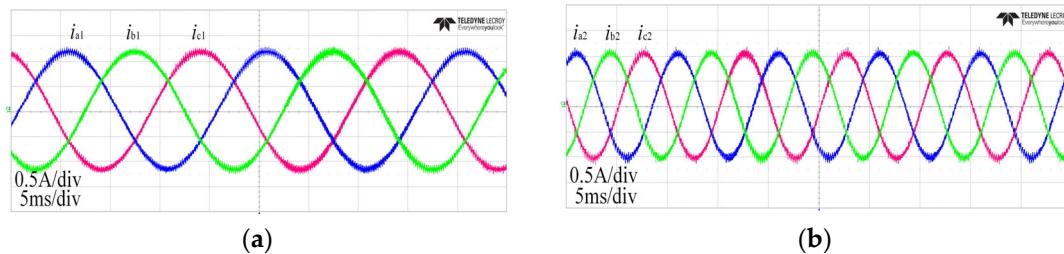


Figure 19. Three-phase output current waveforms: (a) upper output; (b) lower output.

Figure 20a,b present the FFT analysis of the line voltages V_{ab1} and V_{ab2} . It is evident that the low-order harmonics are effectively suppressed, and the harmonic energy is primarily distributed around the switching frequency and its multiples. This high-frequency distribution implies that the harmonics can be easily filtered out by small-sized passive components. Consequently, the measured total harmonic distortion (THD) is maintained at a low level, which satisfies the standard requirements and verifies the effectiveness of the proposed modulation scheme.

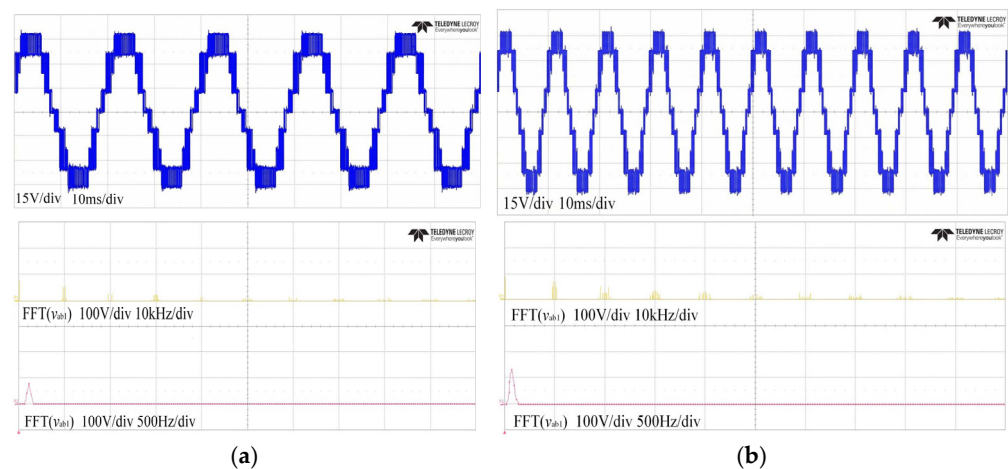


Figure 20. Experimental FFT spectrum of line voltage: (a) upper output V_{ab1} ; (b) lower output V_{ab2} .

6. Conclusions

In this paper, a novel dual-output hybrid-clamped quasi-five-level inverter topology is proposed to address the limitations of existing dual-output architectures, specifically the

constraints on modulation indices and low DC-link voltage utilization. By integrating a hybrid clamping mechanism with an optimized control strategy, the proposed topology successfully combines the advantages of multi-port integration and high-quality multilevel waveform output. The specific conclusions are drawn as follows:

- (1) **Innovative topology structure and flexibility:** The topology of the proposed inverter allows for adjacent voltage level outputs at the dual ports. This design not only realizes a quasi-five-level output with reduced component redundancy but also eliminates the rigid sequential constraints found in traditional vertically stacked topologies. The structural flexibility allows for the selection of optimal switching paths within a single cycle, establishing a solid foundation for high-performance power conversion.
- (2) **Decoupled control and enhanced voltage utilization:** A coordinated modulation strategy is developed to effectively decouple the control of the two output ports. Unlike traditional time-sharing schemes where the operation of one port restricts the other, the proposed method ensures that the modulation index ranges of both outputs remain unconstrained and mutually non-interfering. This breakthrough significantly improves DC-link voltage utilization, allowing the system to adapt to complex asymmetric loading conditions and diverse frequency requirements without performance degradation.
- (3) **Superior waveform quality via line voltage synthesis:** Through the strategic alignment of phase voltage levels and their differential superposition, the proposed topology achieves a nine-level line voltage output. This optimized synthesis method enables the inverter to track sinusoidal reference trajectories with high precision using a simplified phase structure. Consequently, the output waveform exhibits a high degree of sinusoidal approximation with significantly reduced total harmonic distortion (THD), making it highly suitable for grid-connected renewable energy systems and sensitive motor drive applications.

Future work will investigate active balancing circuits or advanced redundant-state selection algorithms to address this stability issue. In parallel with voltage control, although the current spectral performance is satisfactory, implementing advanced control strategies, such as Model Predictive Control (MPC), could further optimize THD and dynamic response beyond the capabilities of the current SVPWM scheme. From a reliability perspective, given the reduced component count, the impact of a single switch failure on the dual-output functionality warrants detailed investigation. By leveraging structural integration and control decoupling, the proposed topology achieves exceptional power density in dual-motor electric vehicle (EV) powertrains and cost-effective multi-functional integration in microgrid applications. Furthermore, through a modular cascaded configuration, it possesses the scalability to smoothly transition toward medium-voltage and high-power scenarios. Ultimately, these targeted advancements will bridge the gap between theoretical innovation and industrial deployment, establishing the proposed topology as a competitive solution for next-generation power conversion systems.

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Abbreviations

DO-HC-FLI	dual-output, hybrid-clamped, quasi-five-level inverter
NPC	neutral-point-clamped
ANPC	active neutral-point-clamped
SVPWM	space vector pulse width modulation
VSVPWM	virtual space vector pulse width modulation
PV	photovoltaic
EMI	electromagnetic interference
HB	H-bridge
FC	flying capacitor
MVS	maximum voltage stress
TAVS	time-average voltage stress
THD	total harmonic distortion
RMS	root mean square
SC	switched capacitor
RL	resistive–inductive
MPC	Model Predictive Control
EV	electric vehicle

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