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Design Optimization and Control System of a 3-Phase T-Type Active Front End for Bi-Directional Charging Technologies for Electric Vehicles

Hakan Polat [1,2], Thomas Geury [1,2], Mohamed El Baghdadi [1,2] and Omar Hegazy [1,2,*]

[1] MOBI-EPOWERS Research Group, Electrical Engineering and Energy Technology Department, Vrije Universiteit Brussel (VUB), Pleinlaan 2, 1050 Brussels, Belgium; hakan.polat@vub.be (H.P.); thomas.geury@vub.be (T.G.); mohamed.el.baghdadi@vub.be (M.E.B.)
[2] Flanders Make, Gaston Geenslaan 8, 3001 Heverlee, Belgium
* Correspondence: omar.hegazy@vub.be

Abstract

Most electric vehicles use 400 V batteries, while some companies are moving to 800 V to reduce current in electric drives. More cars are expected to adopt 800 V at the DC terminals of the batteries, but 400 V will remain common for the duration of this transition, so future off-board chargers must support a wide voltage output range. Silicon carbide switches are used to keep the power–electronics interface compact and scalable. The AC/DC stage of a modular silicon carbide-based interface is designed using a T-type active front end and a dual active bridge. The T-type front end is optimized with a genetic algorithm. The resulting model is used to tune the inner current and outer voltage controllers. Bode analysis shows an inner current loop bandwidth of 4.25 kHz with a phase margin of 53° and a gain margin of 30 dB. The outer voltage loop reaches 50 Hz with a phase margin of 108° and a gain margin of 33 dB. The controller is implemented on a dSPACE MicroLabBox. Tests show peak efficiency of 98.5% in G2V mode and 98.3% V2G mode. THD stays under 5% above 4 kW and reaches 3% at peak power.

Keywords: T-type AFE; Charging systems; component optimization; control tuning; V2G; G2V; EV charging

1. Introduction

The adoption of electric vehicles (EVs) is being encouraged worldwide as a substitute for conventional internal combustion engine vehicles (ICEVs) [1]. This transition toward EVs is motivated by the limited supply of fossil fuels and the growing investment in renewable energy sources such as solar and wind power. The shortage of fossil fuels has pushed many countries to focus on alternative energy solutions, and a similar trend is now evident in the promotion of EVs [2]. The EV industry nowadays uses three DC voltages for the batteries: 48 V [3], 400 V, and 800 V [4]. While 48 V is the new standard for hybrid vehicles and small vehicles like golf carts, forklifts, etc., 400 and 800 V are used in fully electric battery EVs (BEVs). Until recently, 400 V was the standard in the industry; however, to reduce the overall losses due to high currents during charging, 800 V batteries emerged and are expected to take over the industry over the years. This transition is expected to take time, and therefore, the EV-charging industry should adapt itself to provide charging to both voltage levels. According to [5], the industry is already adapting to the transition period. Major EV charger manufacturers already support both 400 and 800 V charging.

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Moreover, the power levels are flexible. Therefore, it can be stated that they are using modular structures. This allows not only changing the power level but also increases the scalability and reliability, which is especially problematic in remote areas like rural zones.

Regardless of the voltage level, the first step is the AC/DC conversion followed by a DC/DC converter to achieve a wide output voltage range. According to IEC 61851-25:2020, the EV battery has to be isolated from the grid. This can be achieved either with a low-frequency transformer, or high-frequency isolation is often realized in the DC/DC stage. According to [5], T-type active front end (AFE) and conventional dual active bridge (DAB) converters are suitable for AC/DC AFE and isolated DC/DC stages, respectively. In [6,7], 3-phase AC/DC AFE topologies are compared for EV charging applications, focusing on SiC. The T-type AFE has a smaller input filter due to the fact that it is a 3-level topology. Compared to other 3-level topologies, such as neutral point clamped (NPC) topology, it has a lower number of switches, and it is bidirectional. While the line switches are subject to a voltage stress (V_{stress}) of V_{dc}, the neutral switches are subject to $V_{dc}/2$. The comparison of the 3-phase AC/DC topologies is presented in Table 1. So far in the literature, different control methods [8–10], PCB design [11], and testing are presented. However, an overall design procedure starting from component-level optimization to experimental verification for T-type AFE is yet missing in the literature.

Table 1. Comparison of AC/DC topologies. (AS = active switch, D = diode).

Feature	2-Level AFE	3-Level NPC AFE [12]	T-Type AFE [13]	Vienna Rectifier [14]
Number of Semiconductors	6 AS + 0 D	12 AS + 6 D	12 AS + 0 D	6 AS + 6 D
Power Direction	Bi-directional	Bi-directional	Bi-directional	Uni-directional
V_{stress}	V_{dc}	$V_{dc}/2$	V_{dc}, $V_{dc}/2$	V_{dc}, $V_{dc}/2$
Filter Size	Large	Small	Small	Small

In this paper, first, the studied T-type converter topology and fundamentals are presented. Then, in Section 3, the overall component level optimization is presented to size the T-type AFE converter by reducing power loss and volume. The lifetime analysis and power loop optimizations were previously performed in [15,16]. After the validation of the optimization results using PLECS, the plant is modeled in Section 4, and the controller tuning is detailed, including implementation in the dSPACE Microlabbox FPGA environment. Finally, prototyping and experimental validation are presented in Section 5.

2. Fundamentals of T-Type AFE

The T-type AFE converter consists of six lines and six neutral switches. While the theoretical voltage rating of the line switches is V_{DC}, the neutral switches are subject to $V_{DC}/2$. Unlike 2-level conventional inverter topologies, the T-type converter has three voltage levels. Compared to other 3-level topologies, the T-type converter has a lower number of switches, and the generation of the modulation signals is quite straightforward. When connecting the T-type converter to the grid, an L/LC/LCL filter is often used to filter the harmonics and comply with the grid standards. A benefit of using a 3-level over a 2-level is that the inverter-side voltage inherently has lower harmonics. This is due to the additional voltage level.

A single phase T-type AFE converter is presented in Figure 1. The MOSFET junctions and body diodes are denoted as $A_{x,j}$ and $A_{x,D}$, respectively. The switching states are presented in Table 2. To better illustrate the voltage levels, the DC-link voltage is denoted as V_{DC}.

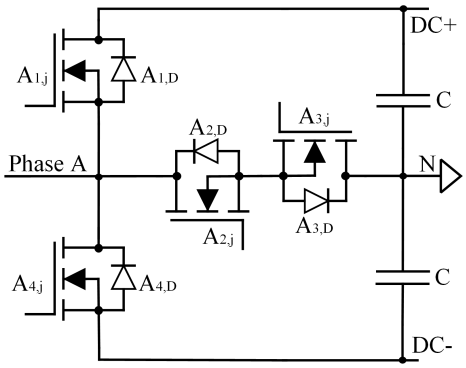


Figure 1. Single-phase illustration of the T-type AFE converter. The junction and body diodes are also marked to better illustrate the current paths.

Table 2. Single-phase T-type AFE switching states.

State	V_{out}	A_1	A_2	A_3	A_4
1	$+V_{DC}/2$	ON	OFF	ON	OFF
2	0	OFF	ON	ON	OFF
3	$-V_{DC}/2$	OFF	ON	OFF	ON

When the current is positive, to achieve "State-1", the A_3 switch is always kept on. A_1 and A_2 work complementarily, and hence the voltage at the switching node oscillates between "State-1" and "State-2". During the transition, a small dead-time is implemented so that the upper DC-link capacitance is not short-circuited. Throughout "State-1" and "State-2", A_4 is always OFF, and hence the possibility of a shoot-through between A_1 and A_4 is avoided. When the current is negative, A_2 is always kept ON, and A_4 and A_3 are operated in complement with a small dead-time. The voltage at the switching node oscillates between "State-2" and "State-3".

3. Multi-Objective Optimization and Simulation of T-Type AFE Converter

In this section, the T-type converter component-level optimization is performed. Firstly, the overall framework of T-Type AFE optimization is presented. Each part of the optimization, LCL filter design (Section 3.2), semiconductor loss modeling (Section 3.3), inductor design (Section 3.4), and DC-link capacitor design (Section 3.5), is explained in detail. Finally, the fully optimized T-type AFE is modeled in the PLECS environment, and the results are compared to the simulation results.

3.1. Component-Level Optimization Flowchart of T-Type AFE

The T-type AFE optimization flowchart is presented in Figure 2. The input parameters are switching frequency, DC-link voltage, K, and AFE-side inductor ripple. K is the ratio of the resonant frequency of the LCL filter (ω_r) to the switching frequency (ω_{sw}), as shown in Equation (1). The optimization is performed for the rated power of 30 kW for a constant 400 V_{l-l} and 50 Hz grid. The input parameters are randomly generated within the selected solution space. Initially, the LCL filter is designed. Depending on the LCL filter design, the semiconductor voltage and current waveforms can be analytically created, and the semiconductor losses can be calculated using an iterative approach with the thermal model to compensate for temperature-dependent switch parameters. In parallel, a genetic algorithm is used for inductor and capacitor optimization. This is performed to reduce the number of input parameters and hence reduce the size of the solution space. The optimal LCL filter inductor designs are used to calculate the volume and the loss of the magnetics.

For the capacitor optimization, the aim is to achieve a DC voltage oscillation smaller than the pre-determined limit and have a high lifetime. Finally, the total losses and volume are plotted on the Pareto graph, and all solutions are ranked, and the optimal solution is selected.

$$K = \frac{\omega_r}{\omega_{sw}} = \frac{1}{\omega_{sw}} \sqrt{\frac{L_{AFE} + L_{grid}}{L_{AFE}\, L_{grid}\, C_f}} \tag{1}$$

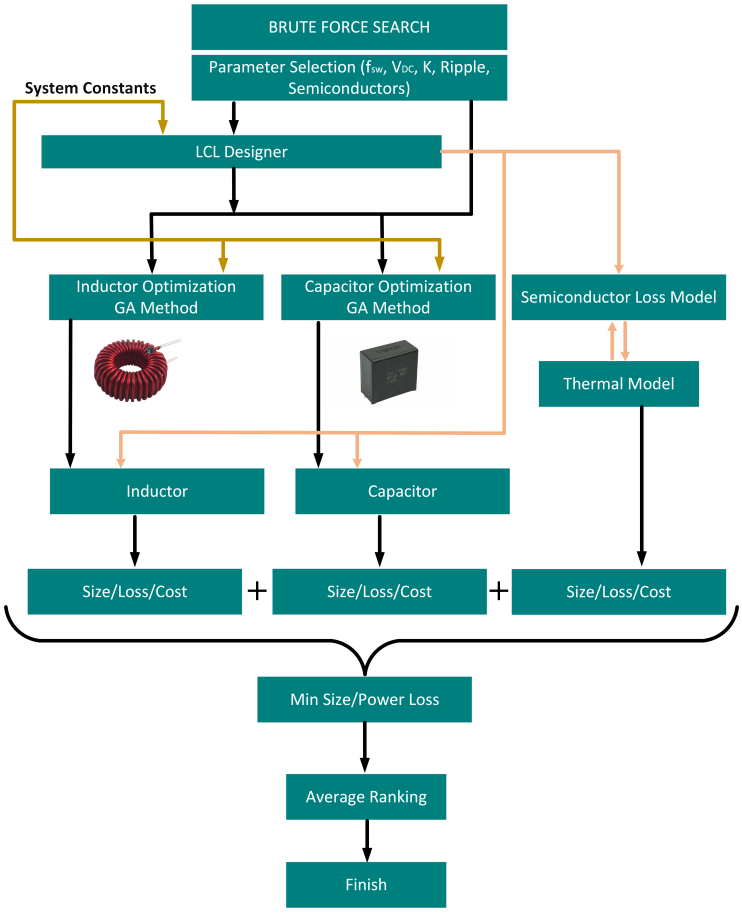


Figure 2. T-type AFE component level optimization flowchart.

3.2. LCL Filter Design

The LCL filter design is performed according to the methodology in [17]. Firstly, the grid-side ($I_{ripple,g}$) and inverter-side ($I_{ripple,i}$) inductor current ripples are calculated.

$$I_{ripple,g} = I_{peak} I_{ripple,g}(\%) \tag{2}$$

$$I_{ripple,i} = I_{peak} I_{ripple,i}(\%) \tag{3}$$

The attenuation factor of the grid side current (H_g) ripple to the converter side voltage (V_{fsw} is 38 V for 3 level) at f_{sw} is calculated as

$$H_g = \frac{I_{ripple,g}}{V_{fsw}} \tag{4}$$

The ratio of $I_{ripple,i}$ to $I_{ripple,g}$ is denoted by N is calculated as

$$N = \frac{I_{ripple,i}}{I_{ripple,g}} \tag{5}$$

The total inductance ($L_{total} = L_i + L_g$) can be calculated as

$$L_{total} = \frac{K^2}{(1-K^2)H_g\omega_s} \tag{6}$$

The filter capacitance (C_f) can be calculated as

$$C_f = \frac{\frac{(1+N^2)(1-K^2)}{(1+N)K^2-1}H_g}{\omega_s} \tag{7}$$

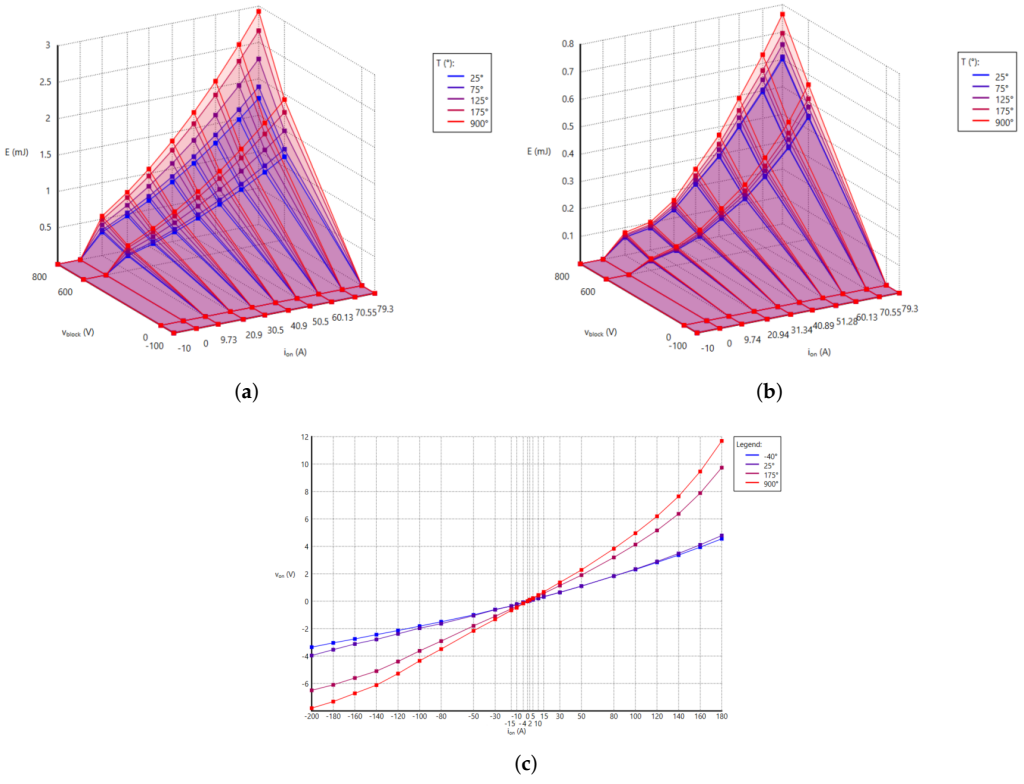
Inverter side inductance ratio to total inductance (λ) is calculated as

$$\lambda = \frac{1}{(1+N)K^2} = \frac{L_i}{L_{total}} \tag{8}$$

In this design, the grid side ripple percentage is taken as 0.15. and I_{peak}, f_{sw}, K and $I_{ripple,i}$ are provided as input. Therefore, it is possible to calculate all unknown parameters.

3.3. Semiconductor Loss Model

In this optimization study, the losses are calculated using look-up tables (LUT). The turn-on and turn-off losses are calculated using the instantaneous voltage and current across the junction. The values are used to interpolate on the curves given in Figure 3. A similar approach is used to calculate the voltage across the junction during conduction in the first and third quadrants.



(**a**) (**b**)

(**c**)

Figure 3. (**a**) Turn-on losses, (**b**) Turn-off losses, and (**c**) conduction losses and voltage across the junction for different junction currents for different junction temperatures for the 1200 V 100 A SiC "C3M0021120K" switch.

The semiconductor losses can be divided into three parts, namely, turn-on, turn-off, and switching losses, as given in the equation below:

$$P_{loss} = P_{turn-on} + P_{turn-off} + P_{conduction} \tag{9}$$

The conduction losses are calculated as in the equation below, where T_j is the junction temperature. For each time step, the V_{ds} is estimated using the look-up table as presented in Figure 3.

$$P_{conduction} = f_{sw} V_{ds}(I_{ds}, T_j) I_{ds}(t) \tag{10}$$

From the system constants and optimization parameters, the rated power, current, and switching frequency are known. The frequency of the inverter side current is 50 Hz, and the current magnitude changes over one period, where the ripple frequency is the same as the switching frequency. Therefore, an average model is necessary to accurately calculate the semiconductor loss for both the line and neutral switches.

The first step to calculating the semiconductor loss is to model the AFE side inductor current (I_{AFE}). The AFE current ripple (I_{ripple}) is determined by the optimization. A basic modeling of the current can be performed as

$$I_{AFE}(t) = I_{peak} sin(100\pi t) + I_{ripple} sin(100\pi t) sin(2 f_{sw} \pi t) \tag{11}$$

where I_{peak} is the peak of I_{grid}. An example current waveform is presented in Figure 4.

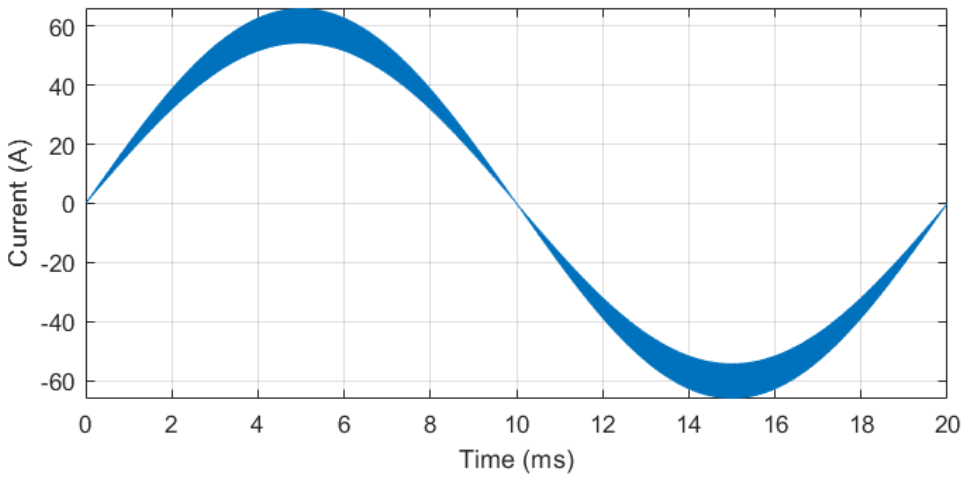


Figure 4. The waveform of the AFE side inductor current. The low frequency (50 Hz) component is a sine wave with an RMS of 43 A. The ripple changes and is maximum at the peak of the 50 Hz component. The current ripple changes depending on the parameters in the optimization.

The line switches block V_{DC}; however, the voltage across drain-source is $V_{DC}/2$ while it goes into conduction. The turn-on/off loss can be calculated as

$$P_{turn,on-off} = f_{grid} \sum_{n=2k}^{f_{sw}/f_{grid}} LUT(T_j, \frac{V_{dc}}{2}, I_{AFE}(n)) \tag{12}$$

For the conduction loss, the $V_{ds,on}$ should be calculated. At any given time, the $V_{ds,on}$ can be calculated using the LUT.

$$V_{ds,on} = LUT(T_j, I_{AFE}) \tag{13}$$

Thereby the average conduction loss can be calculated as

$$P_{conduction} = \frac{V_{ds,on} I_{AFE} d}{2} \tag{14}$$

where d is the duty cycle and can be calculated as

$$d = sin(100\pi t) V_{l-l} \sqrt{\frac{2}{3}} (\frac{V_{dc}}{2}) \tag{15}$$

The reason for the division by 2 on $P_{conduction}$ is that half of the time the switches are not under conduction.

The same methodology can be applied to the neutral switches as well, and finally, the total semiconductor loss can be calculated as

$$P_{total} = 6(P_{line} + P_{neutral}) \tag{16}$$

In order to estimate the junction temperature, a loop is created. Initially, the junction temperature is assumed to be 25 °C, and the semiconductor losses are estimated. Then, the steady-state junction temperature is calculated as in Equation (17) and iterated until $\frac{T_j(n) - T_j(n-1)}{T_j(n)} = 1\%$. $R_{heatsink}$ is heatsink-ambient thermal resistance, and R_{case} is the junction to case thermal resistance.

$$T_j(n) = T_{amb} + (R_{heatsink} + R_{case}) P_{loss}(T_j(n-1)) \tag{17}$$

3.4. Inductor Design

For the inductor design, a dedicated genetic algorithm is used. This is performed to reduce the number of inputs and reduce the solution space of the overall optimization. The optimization parameters are core shape, core material, and core relative permeability. For this optimization, a LUT is created using the different toroidal core shapes by the manufacturer "Magnetics" (Magnetics® headquarters, located in Pittsburgh, PA, USA). As for material, Edge, Xflux, Kool Mu, and Kool Mu Max materials are selected. For the relative permeability, "14, 19, 26, 40, 60, 75, 90, 125" are selected. Since at any given point during the optimization, the core shape, material, and relative permeability are known, the design is relatively simple. The initial step is the calculation of the reluctance (R), inductance factor (A_L), and window area (W_A) in mm^2.

$$R = \frac{L_{effective}}{\mu_0 \mu_r Core_{area}} \tag{18}$$

$$A_L = \frac{1}{R} \tag{19}$$

$$W_A = \pi (\frac{ID}{2})^2 \tag{20}$$

$L_{effective}$ is the effective length, $core_{area}$ is the core area, and ID is the inner diameter of the toroidal core. The next step is to calculate the number of turns to achieve the desired auxiliary inductance. The number of turns is rounded to the closest integer:

$$\#_{turns} = round(\sqrt{\frac{L_{desired}}{A_L}}) \tag{21}$$

Peak current density can be calculated as

$$B_{peak} = \frac{\#_{turns} I_{max}}{Core_{area} R} \tag{22}$$

I_{max} is the peak of the inverter side inductor current that can be calculated as $I_{max} = I_{peak} + I_{ripple}$. The current density is assumed to be 5 A/mm^2. The cable area can be calculated as

$$Cable_{area} = \frac{I_{rms}}{5} \tag{23}$$

The total copper area is calculated as (fill factor (k_u) is taken as 0.3)

$$Copper_{area} = \frac{1}{k_u} Cable_{area} N_{turns} \tag{24}$$

The total cable length (L_{cable}) is calculated using the mean length turn (MLT) and number of turns (N_{turns}):

$$L_{cable} = \#_{turns} MLT \tag{25}$$

The cable resistance (R_{cable}) and copper loss (P_{loss}) are calculated as

$$R_{cable} = \frac{\rho_{cu}(@100\ ^\circ\mathrm{C}) L_{cable}}{Cable_{area}} \tag{26}$$

$$P_{loss} = 1.5 R_{cable} I_{rms}^2 \tag{27}$$

The factor to calculate R_{ac} from R_{dc} for litz wire is 1.5. It is assumed that the litz strand diameters are much smaller than the skin depth. The core loss is calculated using the improved generalized Steinmetz equation (iGSE):

$$P = \frac{1}{T} \int_0^T k_1 \left| \frac{dB(t)}{dt} \right|^\alpha |B(t)|^{\beta-\alpha}\, dt, \tag{28}$$

where α and β are Steinmetz parameters of the selected material [18]. The parameter k_1 is also calculated using conventional Steinmetz parameters. The trapezoidal magnetic flux density is calculated using the equation:

$$B = \frac{V_{in}}{4 f_{sw} N_1 \#_{stack} A_l 10^{-6}} \tag{29}$$

$$P_{total} = P_{core} + P_{copper} \tag{30}$$

The core temperature is calculated using an empirical equation presented in [19]:

$$R_{core} = 5 (V_{total})^{-0.54} \tag{31}$$

$$T_{core} = T_{amb} + P_{total} R_{core} \tag{32}$$

Finally, peak magnetic flux density (B_{peak}), temperature (T), and copper area are compared with rated conditions to create the penalties for the cost function. The overall optimization aims to minimize the volume and loss at the same time.

3.5. Capacitor Optimization

Knowing ΔQ, the output capacitance can be calculated as

$$C_{out} = \frac{\Delta Q}{\%_{Ripple} V_{DC}} \tag{33}$$

The $\%_{Ripple}$ is the voltage peak-to-peak ripple in percentage and is assumed to be 2% for the optimization. Knowing the desired capacitance (C_{out}), f_{sw}, and capacitor current, it is possible to create a dedicated DC-link optimization using genetic algorithms. For the optimization, the parameters are the number of parallel connected capacitors ($N_{parallel}$) and

different capacitors. The capacitors are taken from 1200 V film capacitors from Vishay's "MKP1848C DC-Link" series [20].

From the selected capacitor and the $\#_{parallel}$, the capacitor loss can be calculated as

$$P_{loss} = \Omega_{esr}\left(\frac{I_{rms,cap}}{N_{parallel}}\right)^2 \tag{34}$$

The volume of each capacitor is known from the LUT. The thermal resistance of capacitors is known from another LUT. The lifetime of the capacitor can be calculated as

$$LT = L_f e^{\frac{E_a}{k_b}\left(\frac{1}{T_N}-\frac{1}{T_A}\right)}\left(\frac{V_A}{V_N}\right)^n \tag{35}$$

3.6. T-Type AFE Optimization Results

The T-type optimization parameters are presented in Table 3. The optimization is run for five intervals each. Each point is run, and the volume and power loss are noted. Later, it is ranked by the "average ranking method" [21], as summarized in Table 4. In Figure 5, all solutions are plotted on the graph, and the optimal solution is presented in red.

Table 3. T-Type AFE optimization parameters and their boundaries.

Parameters	Value Range
Input Voltage (V_{in})	400 V
Output Voltage (V_{out})	650–800 V
Rated power (P_{rated})	30 kW
Semiconductor Devices	1200/650 SiC-MOSFET
Switching frequency	10–200 kHz
$I_{AFE,ripple}$	5–20%
K	0.25–0.5

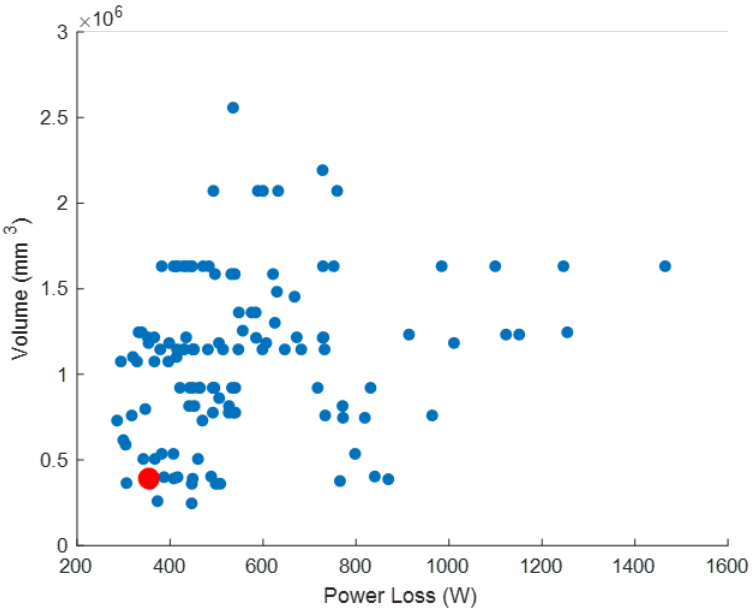


Figure 5. Pareto front plot of T-type AFE optimization. The selected solution is presented in red.

Table 4. T-type AFE top 10 according to the average ranking method.

Rank	$I_{AFE,ripple}$ (%)	K	f_{sw} (kHz)	V_{DC} (V)	P_{loss} (W)	Volume (mm^3)
1	11.17	0.26	108.00	754.00	386.74	399,750
2	12.27	0.25	59.40	795.00	367.11	506,125
3	10.70	0.25	31.20	717.00	317.35	760,075
4	8.49	0.28	65.45	768.00	342.22	506,125
5	5.42	0.28	56.50	710.00	304.27	589,375
6	6.82	0.26	50.60	702.00	299.17	616,075
7	6.26	0.32	72.60	742.00	354.31	391,825
8	6.89	0.27	25.60	710.00	285.97	730,375
9	5.83	0.32	99.90	772.00	372.84	259,575
10	8.77	0.27	88.10	787.00	357.99	360,937

3.7. Simulation Model and Results

The output of the optimization model is inserted into a simulation model developed in PLECS. The PLECS model consists of the T-type AFE circuit, thermal circuit, and the control block. For control, a decoupled current control method is used with space vector modulation (details of the control method will be explained in the upcoming chapters). The active and reactive power from the grid is controlled by i_d and i_q currents, respectively. In the simulation, a unity power factor is desired. Therefore, i_q is set to zero. The PLECS model is presented in Figure 6.

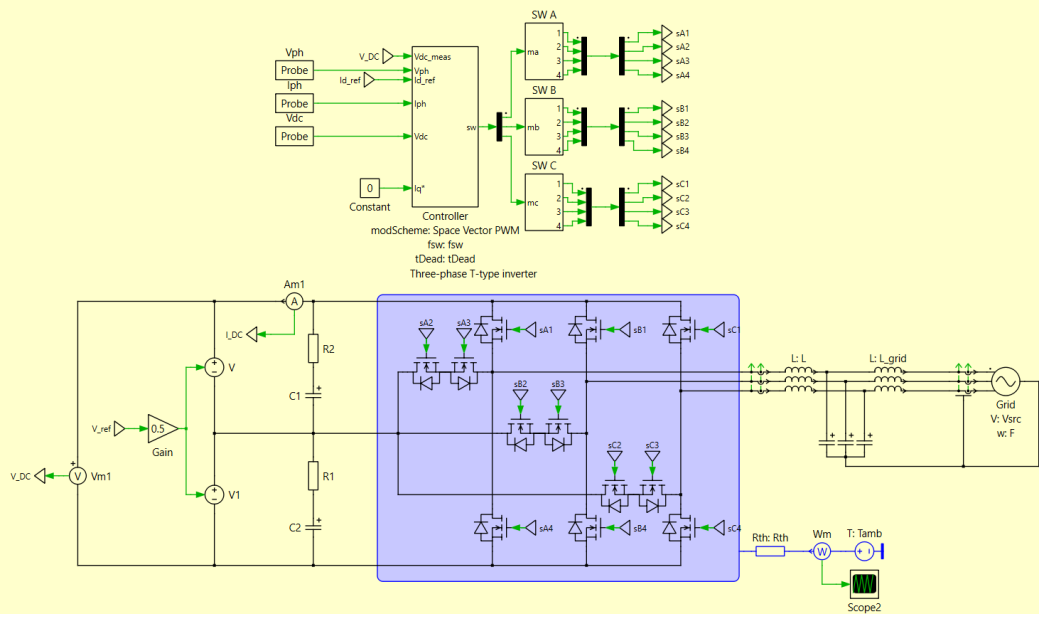


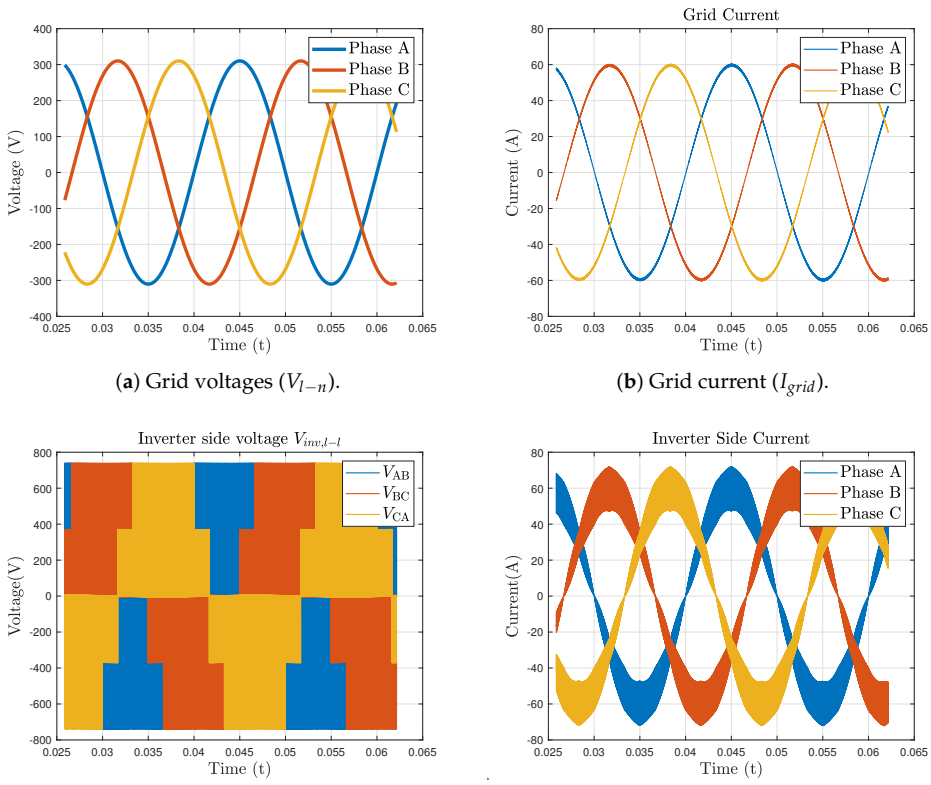
Figure 6. T-type AFE simulation model in PLECS. The circuit is coupled with a single heatsink thermal model shown in blue.

The PLECS model takes the same look-up tables (LUT) as input to calculate the power loss on each semiconductor. At each switching instant, the model uses the LUT to estimate the turn-on/off loss. The switch and gate driver dynamics are omitted, and hence less computation is made. Moreover, in the simulation model, parasitics are ignored, which also reduces the overall complexity and decreases the non-linearity and further decreases the computation time without a major change in the results. The simulation parameters are presented in Table 5.

Table 5. T-type AFE PLECS simulation parameters.

Parameter	Value
Line switch	C3M0021120K (1200 V, 21 mΩ, TO-247)
Neutral Switch	C3M0025065K (650 V, 25 mΩ, TO-247)
L_i	45 µH (906, Edge-19 µ, 41 turns)
L_g	15 µH (906, Edge-19 µ, 25 turns)
C_f	7 µF
V_{DC}	742 V
V_{grid}	400 V_{l-l}, 50 Hz
f_{sw}	70 kHz
Deadtime	200 ns
DC-link Capacitor	MKP1848C66012JY5
Equivalent DC-link Capacitance	60 µF

The simulation results are presented in Figure 7. The circuit parameters are taken directly from the optimization results (solution number 7). Solution number 7 is selected instead of the first solution with the highest ranking due to practical laboratory implementation. In the laboratory, 45 and 15 µH inductors were already present, which almost overlapped with the 7th solution. The switching frequency is rounded down to 70 kHz. The THD is calculated as 2%, which is below the 5% limit as stated in IEC 61851-1:2017. The total semiconductor loss settles at 310 W. The optimization showed a total semiconductor loss of 295 W, which results in around 5% error in loss calculation.



(**a**) Grid voltages (V_{l-n}).

(**b**) Grid current (I_{grid}).

(**c**) Inverter side voltage (V_{inv}).

(**d**) Inverter side current (I_{inv}).

Figure 7. (**a**) Three-phase grid voltages, (**b**) grid side inductor current, (**c**) inverter side voltage, and (**d**) inverter side current waveforms for the optimal solution for the T-type AFE. The simulation is for the rated condition of 30 kW, 400 V_{l-l}, 50 Hz grid and 742 V_{out}.

4. Control Design For Bi-Directional T-Type AFE

The T-type AFE is controlled using a decoupled current controller. The overall system, including voltage and current measurement, is shown in Figure 8. To suppress harmonics, an LCL filter is employed, where the inverter-side inductor, grid-side inductor, and their corresponding resistances are denoted as L_i, L_g, R_i, and R_g, respectively. The filter capacitor is represented as C_f.

$$\begin{bmatrix} V, I_d \\ V, I_q \\ V, I_0 \end{bmatrix} = \frac{2}{3} \begin{bmatrix} \cos\theta & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ -\sin\theta & -\sin\left(\theta - \frac{2\pi}{3}\right) & -\sin\left(\theta + \frac{2\pi}{3}\right) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix} \begin{bmatrix} V, I_a \\ V, I_b \\ V, I_c \end{bmatrix} \tag{36}$$

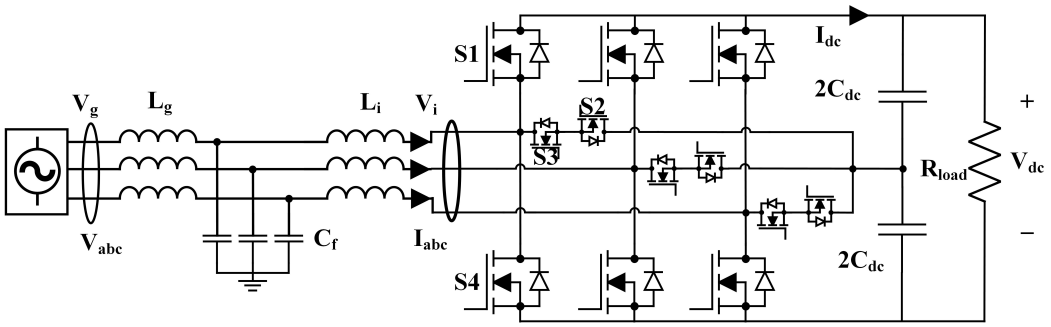


Figure 8. T-type AFE with voltage and current measurement.

Using Clarke-Park transformation in Equation (36), V_{abc} and I_{abc} are converted into V_{dq0} and I_{dq0}. Assuming the 3-phase is symmetrical, the zero components are calculated as zero. Inverter-side voltage $V_{dq,i}$ can be written as

$$v_{d,i} = -R_i i_d - L_i \frac{di_d}{dt} + \omega L_i i_q + v_{d,g} \tag{37}$$

$$v_{d,i} = -R_i i_q - L_i \frac{di_q}{dt} - \omega L_i i_d + v_{g,q} \tag{38}$$

Equations (37) and (38) show that it is possible to control the inverter-side voltage $V_{dq,i}$ using I_{dq}. By controlling the voltage drop across the inverter-side inductor in the dq frame using conventional PI controllers, and with the additional feed forward terms $\omega L_i i_d$ and $\omega L_i i_q$, $V_{d,i}$ and $V_{q,i}$ can be controlled independently. The control scheme is presented in Figure 9.

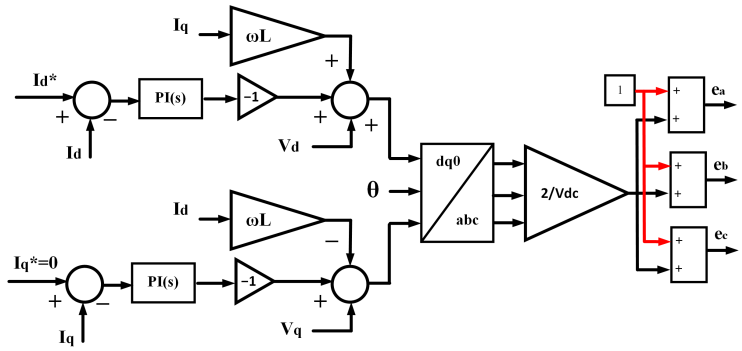


Figure 9. Decoupled current controller structure for T-Type AFE.

I_d^* is often generated by another PI controller controlling the DC-link voltage. I_q^* is 0 when no reactive power is required to be absorbed/supplied to the grid. The output of the current PI controllers is multiplied by -1. This is necessary due to the direction of the

current measurement. The output of the inverse Clarke-Park transform is later multiplied by $2/V_{dc}$ such that the reference voltage is always within the range $[-1, 1]$. Later, 1 is added such that the reference voltages e_a, e_b, e_c are between [0, 2].

The pulse width modulation (PWM) for the 3-level strategy is presented in Figure 10. Two carrier waves are used. The higher carrier triangle wave is limited to [1, 2] while the lower triangle carrier is limited to [0, 1]. The voltage reference signal e_x is compared with both carriers, and the PWMs are created, ensuring all five voltage levels are applied $[V_{dc}, V_{dc}/2, 0, -V_{dc}/2, -V_{dc}]$. The PWM generation is presented in Figure 10.

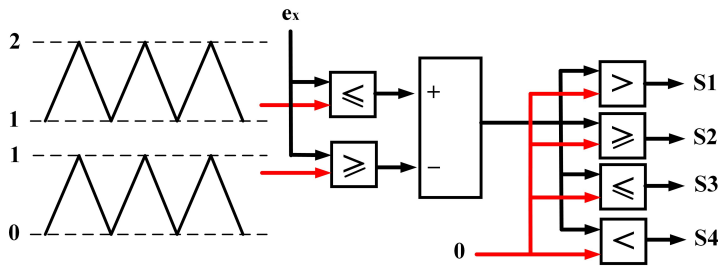


Figure 10. Decoupled current control PWM generation.

The overall control methodology is shown in Figure 11. The fast inner loop controls the D-axis current (I_d) (the same is true for Q-axis current). The current reference I_d^* is created by the slow voltage control loop.

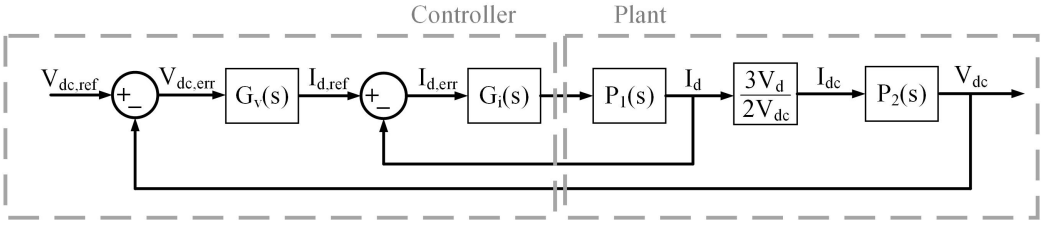


Figure 11. Cascaded control methodology for T-type AFE. $P_1(s)$ = Plant LCL, $P_2(s)$ = id to Vdc $G_i(s)$ = PID control current $G_v(s)$ = PID voltage.

In Figure 11, $P_1(s)$ and $P_2(s)$ are plant transfer functions, $G_i(s)$ and $G_v(s)$ are the current and voltage PID controllers, respectively. $P_1(s)$ can be written as in Equation (39).The plant model of the system can be derived using Equation (39), where X_i is the impedance of the inverter side inductor, X_{Cf} is the impedance of the filter capacitor, and X_g is the impedance of the grid-side inductor. Alternatively, a state space approach can be followed as presented in [22,23].

$$\frac{I_i(s)}{V_i(s)} = \frac{1}{X_i + X_{Cf}||X_g} P_4(s)P_5(s) = \frac{L_g C_f s^2 + R_g C_f s + 1}{L_i L_g C_f s^3 + (L_i R_g + L_g R_i) C_f s^2 + (L_i + L_g)s + (R_i + R_g)} P_4(s)P_5(s) \quad (39)$$

In Equation (39), $P_4(s)$ is the single-pole approximation of the current sensor. The sensor used in the T-type is AMC1302 from Texas Instruments. The input to output delay is around 3 µs. Moreover, an RC low pass filter is also present with a cut-off frequency of 7 kHz = 142 µs. 142 µs >> 3 µs and hence the $P_4(s)$ can be written as in Equation (40).

$$P_4(s) = \frac{1}{\frac{1}{2\pi f_{cutoff}} s + 1} \quad (40)$$

$P_5(s)$ is the transfer function of the sampling time. In this paper, the sampling is performed at $\tau = 1$ µs, and the first-order Pade approximation is presented in Equation (41).

$$P_5(s) = \frac{1 - (\tau/2)s}{1 + (\tau/2)s} \tag{41}$$

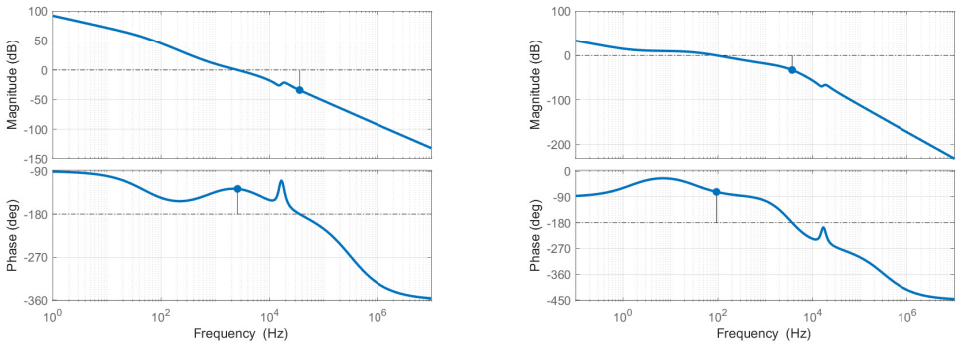
In the decoupled current control, the D-axis is aligned with the grid voltage. The DC current (I_{dc}) and d-axis current (I_d) relation is presented in Equation (42). In the equation, it is assumed 100% efficiency.

$$\frac{3}{2}V_d I_d \approx V_{dc} I_{dc} \rightarrow \frac{I_{dc}}{I_d} = \frac{3V_d}{2V_{dc}} \tag{42}$$

The plant transfer function $P_2(s) = V_{dc}/I_{dc}$ can be written as in Equation (43).

$$P_2(s) = \frac{R_{load}}{1 + sC_{dc}R_{load}} \tag{43}$$

$G_i(s)$ is tuned to ensure stability. PI control is selected where P = 1 and I = 5000. The open-loop transfer function Bode plot is presented in Figure 12. With these parameters, a phase margin of 53° at 2.7 kHz is achieved. The controller bandwidth (−3 dB) is calculated as 4.25 kHz. The gain margin is calculated as 30 dB. It is advised to have a controller bandwidth that is smaller than $f_s/10$, where f_s is the switching frequency, which is chosen as 70 kHz. Hence, 4.2 kHz < 7 kHz, ensuring this condition. Similarly, for $G_v(s)$, PI parameters are set as P = 3 and I = 30, ensuring a controller bandwidth of 314 rad/s (50 Hz) with a phase margin of 108 degrees and a gain margin of 33 dB as presented in Figure 12. The calculated continuous time PI parameters are converted to discrete time using the forward Euler method as in [24].



(**a**) Bode plot for inner current controller. (**b**) Bode plot outer voltage controller.

Figure 12. Open-loop transfer function Bode plot for inner current and outer voltage controller.

Real Time Control Implementation

In order to control the T-type AFE and DAB converter, the proposed control algorithms need to be implemented in a real-time controller. In the industry, this is often performed using DSPs like TI C-2000Ware microcontrollers or using FPGAs. Although it is the industry standard, both DSP and FPGA require extensive time during development and code testing. Whereas companies like PLECS, OPAL-RT, dSPACE, and TyphoonHIL aim to combine the best of both worlds, where DSP/FPGA programming is performed using conventional blocks as in Simulink 2020b/PLECS 4.9.4 or other programs that are often used in simulation. In this paper, the control is performed using the dSPACE MicroLabBox environment using the Xilinx FPGA blockset.

In order to implement the proposed control algorithm presented in Figure 10, the grid voltages, inverter side currents, and the DC-link voltage need to be measured. The measurement block of the dSPACE in the FPGA domain is presented in Figure 13.

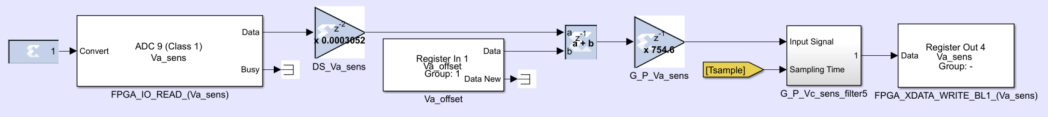


Figure 13. Measurement of signals and digital moving average filtering.

The measurement in dSPACE is performed using a 16-bit analog-to-digital converter (ADC). It is capable of measuring 0–10 V. Therefore, voltage across the ADC is converted into a digital number between 0–$2^{16} - 1$ or 0–65,535 (for unsigned integer). In order to convert it back, the ADC signal is fed into a gain equal to 10/32,767. Therefore, the output of the gain block is the exact voltage across the ADC port. Later, an offset block and a gain block are added. The values are taken from the DSP domain, and hence they can be adjusted easily during actual control operation. A pre-set gain is also placed on each voltage and current measurement, depending on the gain of the voltage/current sensor. Although the current and voltage sensors have analog RC low-pass filters that are capable of filtering any undesired noise, a digital moving average filter is also implemented as in Figure 14. It has a window of 10 with a time step of 1 µs. It results in −3 dB around 44 kHz.

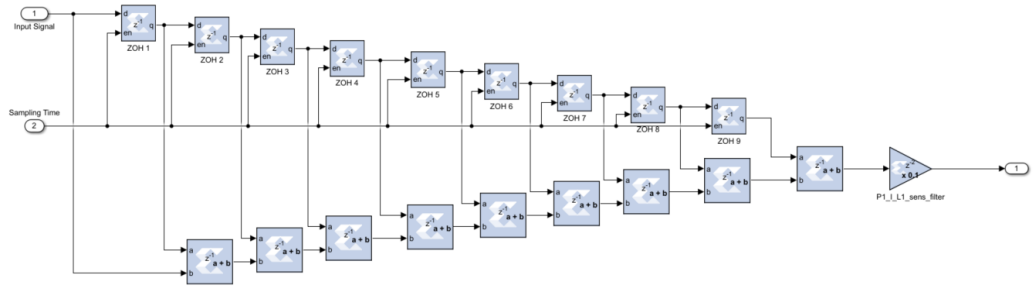


Figure 14. Moving average filter with a window of 10. Time - step is set as 1 µs.

The dSPACE implementation of the decoupled current control presented in Figure 10 is presented in Figure 15. The d- and q-axis error signals are the input to a discrete PID controller. The output is limited to the maximum DC-link voltage. After feed-forwarding the voltage drop across the inverter-side inductor, and obtaining the reference inverter-side d- and q-axis voltages, they are fed into the inverse Clarke-Park transform. Then the reference inverter voltages are normalized by dividing by $V_{dc}/2$.

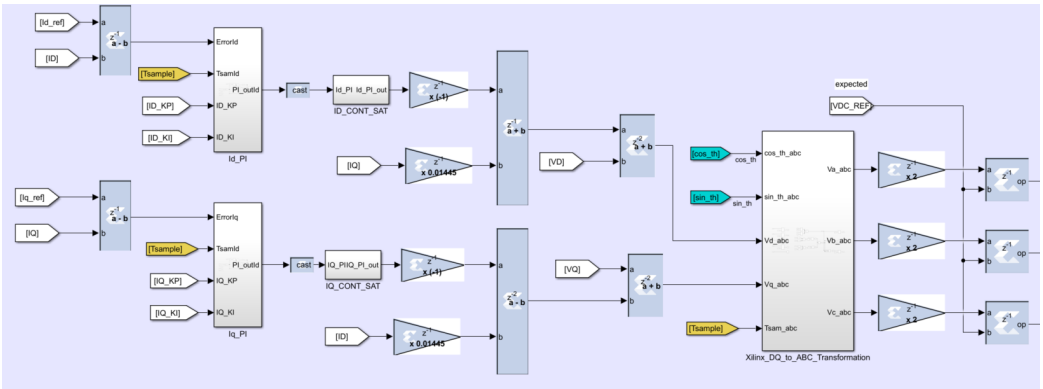


Figure 15. Decoupled current control implementation in dSPACE Xilinx FPGA program.

To further improve the system parameters like DC-link utilization, lower THD, and improved power factor, space vector PWM (SVPWM) is used instead of conventional sinusoidal PWM. In this paper, the max-min method is used to achieve SVPWM modulation. In this method, the common mode or zero sequence is subtracted from the modulation signals. The calculation is presented in Equation (44).

$$V_{common,mode} = \frac{maximum(V_A, V_B, V_C) + minimum(V_A, V_B, V_C)}{2} \quad (44)$$

By calculating the maximum and the minimum of the phase voltages, it is possible to determine the sector and inject a third harmonic waveform to further enhance the DC-link utilization. This method requires less computational effort.

5. Prototyping and Experimental Validation of T-Type AFE

In this section, the overall prototyping will be presented. The features of the T-type AFE system can be listed as follows:

- **Relay+ Pre-charge circuit**: When the DC-link capacitors are fully discharged, connection with the grid without any resistance will result in an impulse short circuit current. This current is rectified passively using the body-diodes of the semiconductors, and hence it should be avoided. To do so, the most common method is to charge the system with a pre-charge resistance connected in parallel to 3 relays on the AC side. The resistance is used to limit the inrush current and hence protect the system from damage. Later, the relays are connected, and a no-resistance path is created as in Figure 16.
- **Voltage Sensor**: For voltage sensing, AMC3330 reinforced isolated voltage sensing amplifier is selected. A voltage divider circuit is used such that the voltage across the divider is equal to 1 V when the input voltage is 1000 V. The same voltage divider circuit is used for both the grid voltage and the DC-link voltages. A sensor board is made, which is also used in a dual active bridge converter design. The sensor board is presented in Figure 17a
- **Current Sensor**: For current sensing a shunt resistor of 500 µΩ is used. AMC 1302 50 mV reinforced isolation amplifier is used. Hence, the maximum current that can be measured with the sensor board is 100 A. The sensor board is presented in Figure 17b
- **Gate Driver Board**: The gate driver board consists of 4 CGD15SG00D2 gate drivers.
- **Single-Phase T-type Power Board**: This board consists of 2 line (C3M0021120K) + 2 neutral (C3M0025065K) switches. 2 × 470 µF capacitors, heatsink and fan.

The single-phase T-type power board and overall finalized system are presented in Figure 18a, and Figure 18b, respectively.

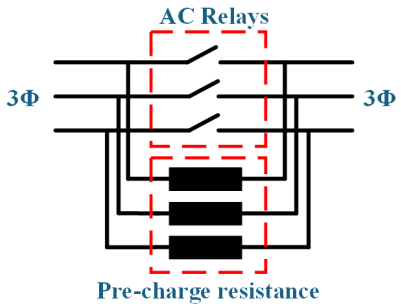
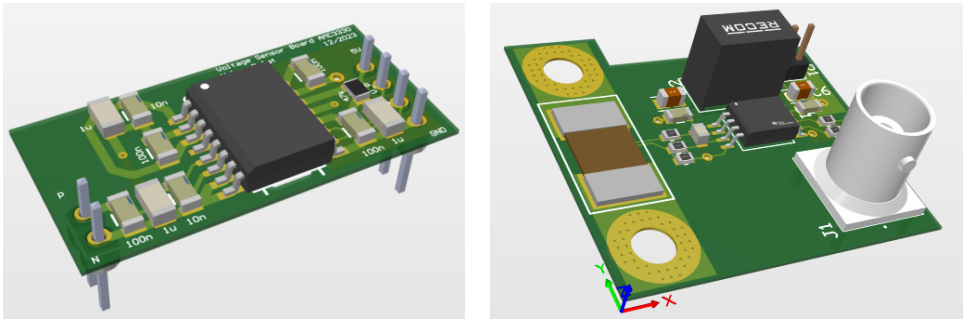
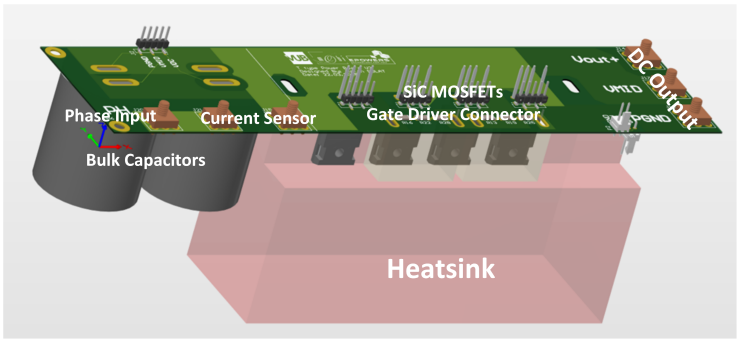


Figure 16. Pre-charge circuit illustration for T-type AFE.

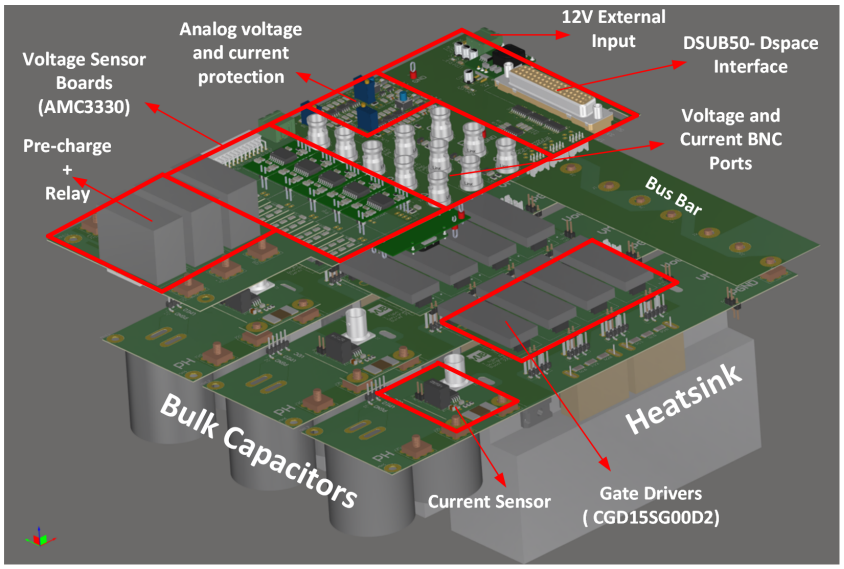


(**a**) (**b**)

Figure 17. (**a**) AMC3330 based voltage sensor and (**b**) AMC1302 based current sensor boards.



(**a**)



(**b**)

Figure 18. (**a**) Single-phase T-type power board. (**b**) Overall 3-phase T-type AFE system design including the gate-driver, relay, measurement, and control boards.

5.1. Experimental Results

In this section, the T-Type AFE results will be presented. The system is tested at different DC-link voltages. The test setup is presented in Figure 19, where "Cinergia GE&EL+ vAC/DC" is used as a bi-directional grid emulator capable of supplying or absorbing power. The testing parameters are presented in Table 6. Digatron acts as a battery with various voltages. The control is implemented using a dSPACE MicroLabBox FPGA domain. The Q-axis current is set to zero (no reactive power). By controlling the D-axis

current, it is possible to transfer power in both G2V and V2G directions. The efficiency and THD data are measured using a Yokogawa Power Analyzer WT1800.

Table 6. T-type AFE testing parameters.

Parameters	Value Range
Modulation Method	Decoupled current control
Power Rating (P_{rated})	10 kW
Rated Input Voltage (V_{in})	400 $V_{l-l,rms}$
Rated Input Current (I_{in})	15 A_{rms}
Output Voltage (V_{out})	650-700-750 V_{DC}
Rated Output Current (I_{out})	16 A

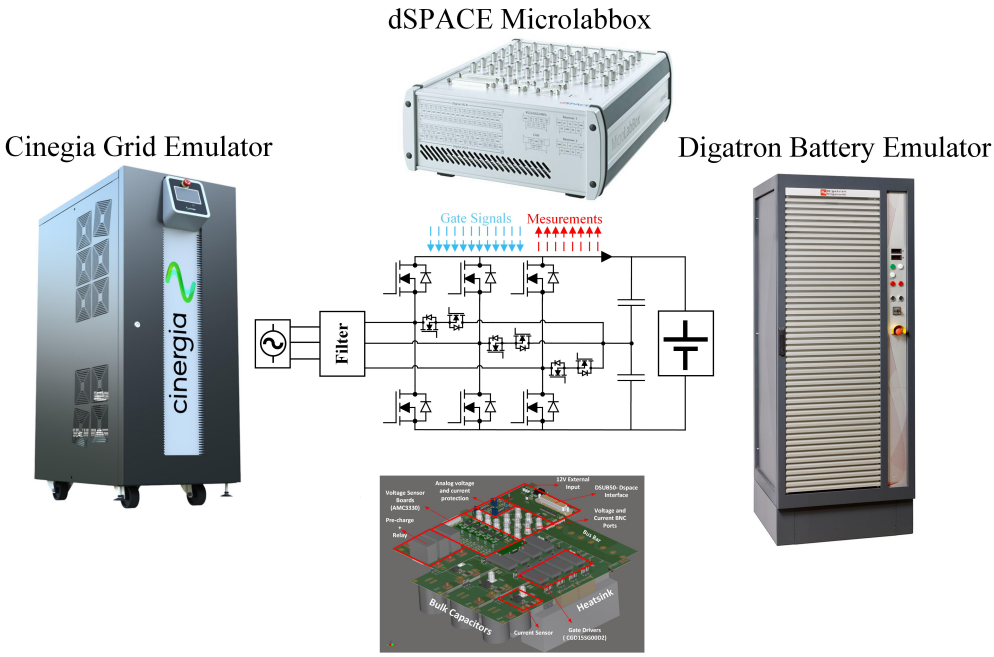


Figure 19. Illustration of the testing setup for T-type AFE. The grid is replaced with a grid emulator. The control is performed in the dSPACE Microlabbox. The battery is replaced with a bi-directional power supply that is capable of emulating a battery.

The D-axis current is changed between +25 A and −25 A, resulting in G2V/V2G power flow between +11 kW and −11 kW. The system is tested for V_{dc} = 650, 700, 750 V. The efficiency results are presented in Figure 20. The peak efficiency for V2G is measured for 650 V ≈ 98.3% while this value is ≈98.5% for the G2V case. The current waveform for $I_{d,ref} = 5, 10, 20, 25$ A and for $V_{DC} = 700$ V are presented in Figure 21. Moreover, the PWM is enabled and the cascaded two stage controller achieved a rise time of 50 ms as in Figure 22 under full load.

The total harmonic distortion (THD) can be calculated as in Equation (45). The THD of the grid-side current is recorded as in Figure 23. The THD shows a steady decline as the load increases for both G2V and V2G conditions. The <5% THD condition is achieved for loading conditions higher than 4 kW. The fast Fourier transform (FFT) plots of the grid currents for $I_{d,ref} = 5, 10, 20, 25$ A and for $V_{DC} = 700$ V are presented in Figure 24. As the power increases, there is a significant drop in the odd-number harmonics. There are almost no harmonics in the multiples of 3 due to the 3-phase 3-wire input. Also, there are almost no even-order harmonics since the system draws AC purely.

$$\text{THD}_I = \left(\frac{\sqrt{\sum_{n=2}^{\infty} I_n^2}}{I_1} \right) \times 100\% \tag{45}$$

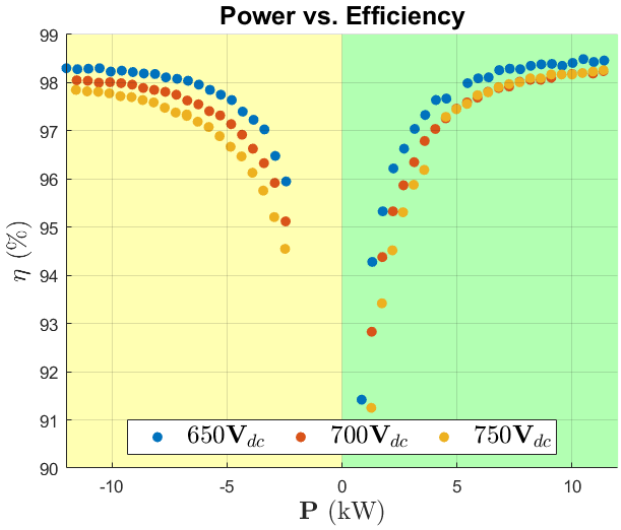


Figure 20. T-type AFE efficiency results for both G2V and V2G modes for 650, 700, and 750 V at the DC-link. The D-axis current is changed between +25 A and −25 A, resulting in G2V/V2G power flow between +11 kW and −11 kW. The input is 400 $V_{l-l,rms}$.

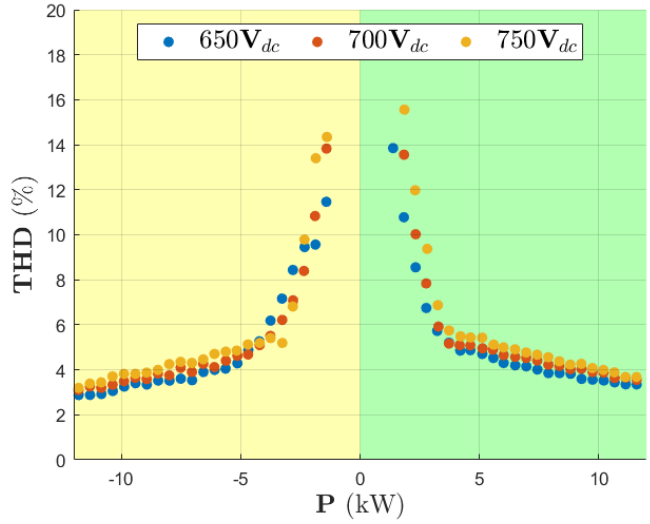


Figure 21. T-type AFE THD (Total harmonic distortion) results for both G2V and V2G modes for 650, 700, and 750 V at the DC-link. The input is 400 $V_{l-l,rms}$.

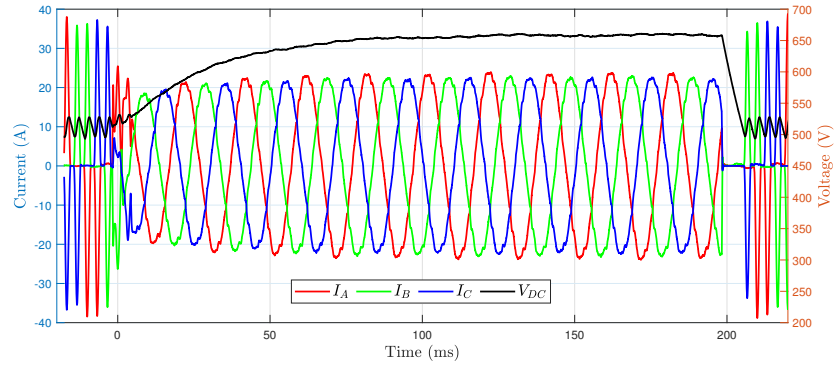
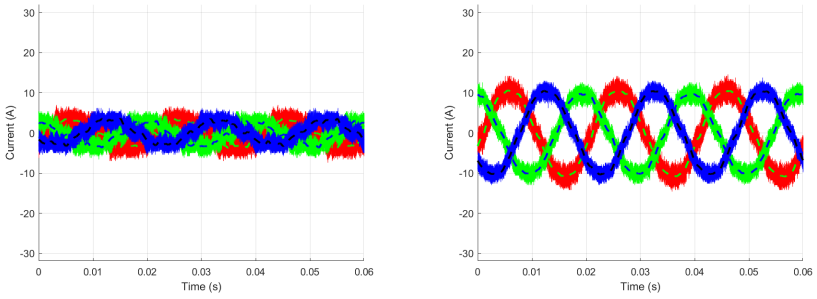
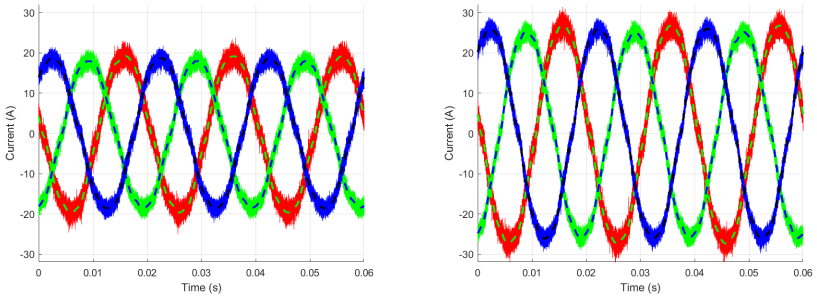


Figure 22. Step change from passive rectification (V_{dc} = 540 V) to full load at V_{DC} = 650 V, $I_{d,ref}$ = 25 A, 11.5 kW for the T-type AFE. The load is purely resistive. The input is 400 $V_{l-l,rms}$.

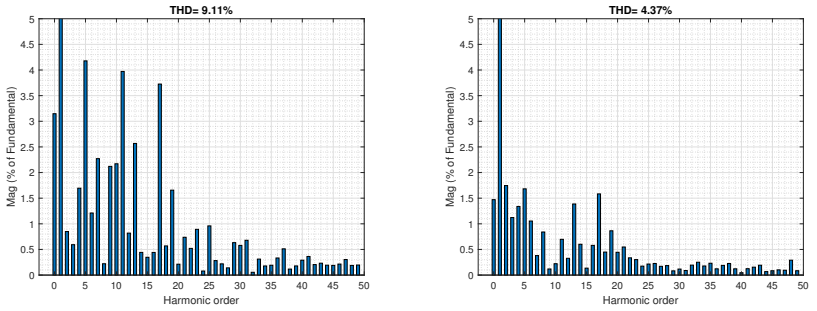


(**a**) $I_{d,ref} = 5$ A (**b**) $I_{d,ref} = 10$ A

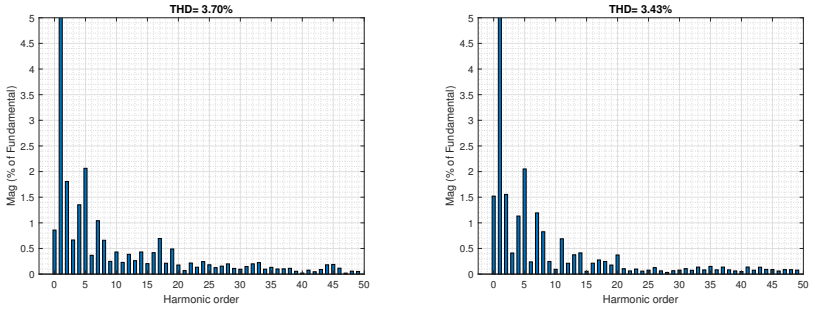


(**c**) $I_{d,ref} = 20$ A (**d**) $I_{d,ref} = 25$ A

Figure 23. T-type AFE grid side current waveforms for $V_{dc} = 700$ V and $I_{d,ref} = 5, 10, 20, 25$ A. The input is 400 $V_{l-l,rms}$.



(**a**) FFT at $I_{d,ref} = 5$ A (**b**) FFT at $I_{d,ref} = 10$ A



(**c**) FFT at $I_{d,ref} = 19$ A (**d**) FFT at $I_{d,ref} = 25$ A

Figure 24. T-type AFE grid side current THD FFT plots for $V_{dc} = 700$ V and $I_{d,ref} = 5, 10, 19, 25$ A. The input is 400 $V_{l-l,rms}$.

5.2. Integrated System Results

So far, the prototyping and testing results for the DAB and T-type AFE have been presented separately. However, the full modular system consists of two stages, namely T-Type AC/DC, followed by DAB isolated DC/DC stage. The overall system illustration is presented in Figure 25.

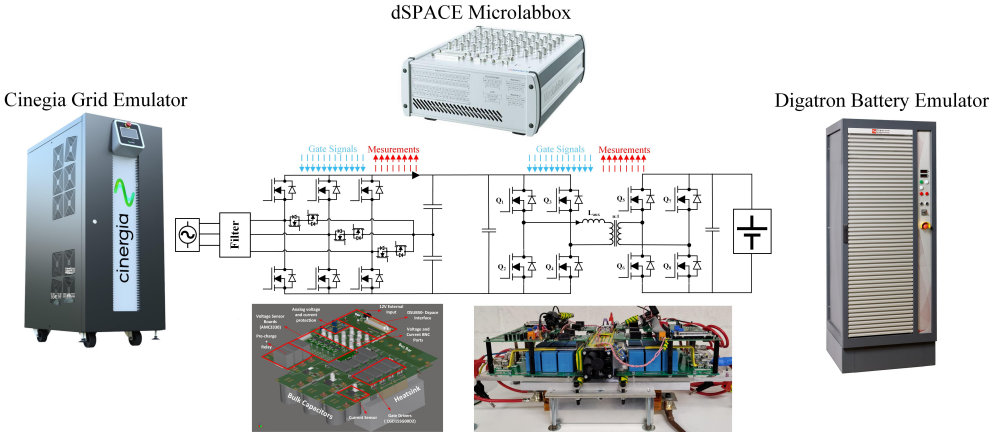


Figure 25. The full integrated power electronics interface.

For G2V operation, the T-type operates in voltage control mode. The DC-link voltage error is used to create the d-axis current reference denoted as i_d. The q-axis current i_q is set to be zero since the unity power factor is desired. After the DC-link voltage is set to the desired value, depending on the power demand from the battery, the output current is controlled. A small time delay is implemented between the enablement of the T-type and DAB to avoid uncontrollable DC-link voltage sag and swells. During normal turn-on, the DAB output current is increased slowly (ramp) to further ensure DC-link voltage stability. Similarly, during normal turn-off, the output current is initially reduced, and then the first DAB is turned off. During idle mode, the DC-link is kept charged, and if full grid disconnection is desired, additional AC relays can be placed at the grid connection. However, it is omitted for prototyping purposes.

For G2V testing, the grid voltage is set to 400 V_{l-l}–50 Hz. The DC-link voltage is set to 650 V, and the output voltage is swept between 200–450 V emulating a battery with 400 V nominal voltage. The output current is controlled from 5–20 A, resulting at 10 kW at 450 V_{DC}. The calculated efficiencies are presented in Figure 26. The complete PEI has been tested for a single use-case that is a 400 V EV battery charging case. The input voltage is set as 400 $V_{l-l,rms}$. The DC-link is set as 650 V_{DC} and the output voltage is varied between 200–450 V. The output current is rated at 20 A. The complete charging profile is presented in Figure 27. In the figure, the DAB primary, secondary voltages, and auxiliary inductance current are shown. The DAB switching frequency is 35 kHz. The division for auxiliary inductance current is 50 A/div. Triple phase shift modulation is used for DAB control [25]. For the T-type AFE, the grid currents are presented.

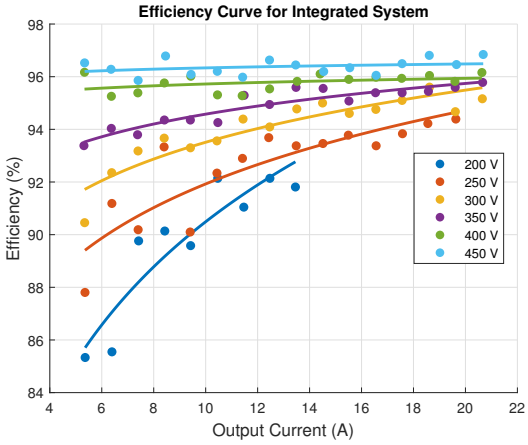


Figure 26. Efficiency map for integrated two-stage solution.

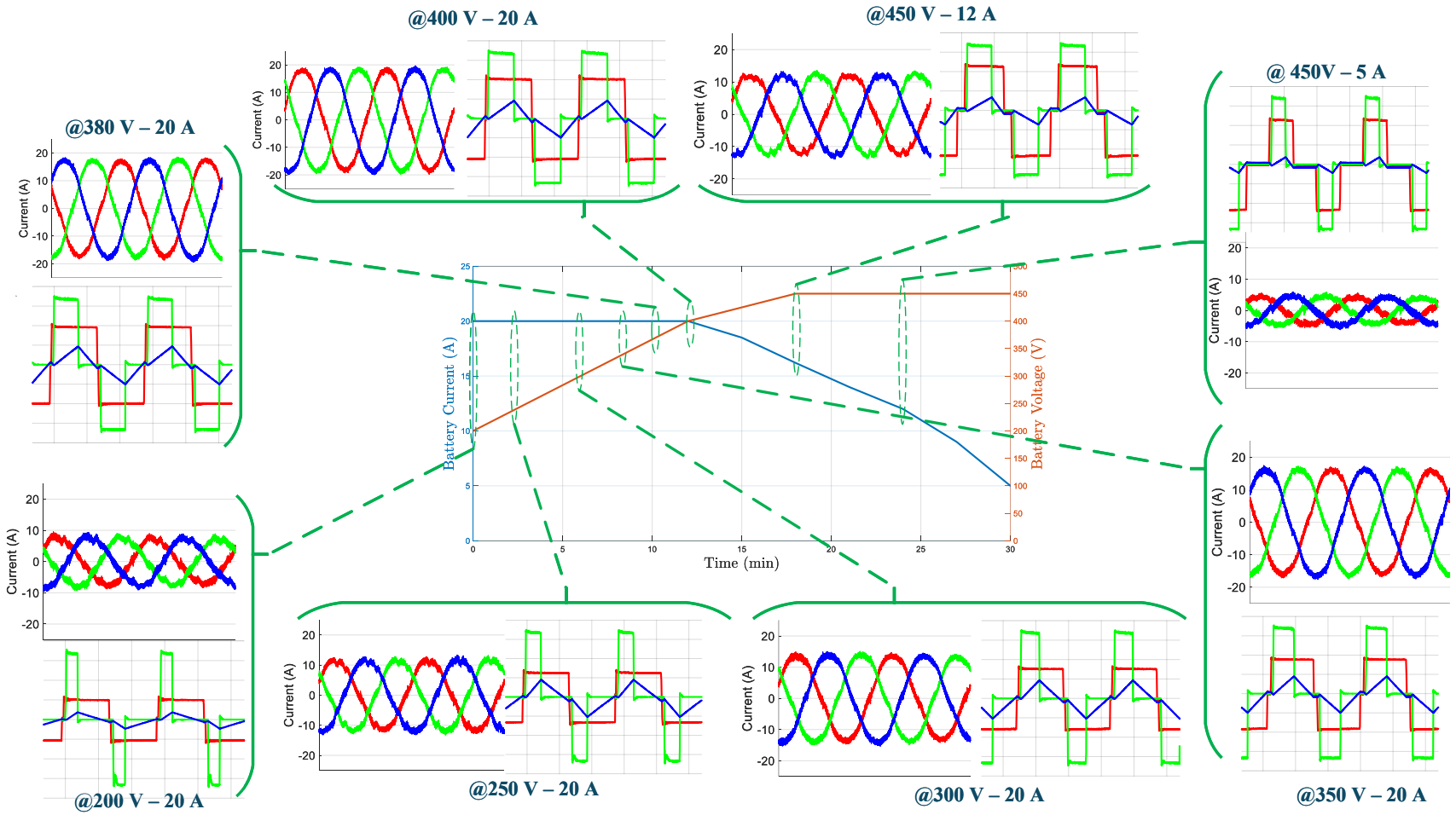


Figure 27. G2V charging profile and testing results for 400 V EV battery charging.

https://doi.org/10.3390/en19030656

6. Conclusions

In this paper, a T-type AFE that was previously optimized for its lifetime and PCB layout is subject to a multi-objective optimization to design the overall system. The optimization successfully minimized the overall loss and volume of the passive LCL filter and the DC-link capacitors. The optimized solution is later modeled analytically to achieve a systematic method to tune the decoupled current controller PIDs. During the controller tuning, the plant model is modeled in detail, adding the sensor delays and low pass filters as well as the poles due to sampling and the switching itself. The designed controllers are later realized in hardware in the loop (HiL) dSPACE-FPGA. The designed highly modular, flexible T-type AFE prototype is tested from +11 kW to −11 kW, and the efficiencies and the THDs are plotted for three different voltage levels (650–700–750 V). According to the results, the T-type AFE has successfully delivered power in both G2V and V2G directions, achieving a THD of a minimum 3% at 11 kW loading. Moreover, the system has lower THD than 5% for any power and DC-link voltage above 4 kW. The designed AFE achieved the highest efficiency of 98.5% at 11 kW for 650 V. Finally, a conventional DAB converter is connected as the second stage, and a full 400 V battery charging profile is also presented.

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Abbreviations

Abbreviations used in this manuscript:

AC	Alternating Current
ADC	Analog to Digital Converter
AFE	Active Front End
BEV	Battery Electric Vehicle
DAB	Dual Active Bridge
DC	Direct Current
DSP	Digital System Processor
EV	Electric Vehicle
FPGA	Field Programmable Gate Arrays
G2V	Grid to Vehicle
iGSE	Improved Generalized Steinmetz Equation
LUT	Look Up Table
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
PID	Proportional-Integral-Derivative
PWM	Pulse Width Modulation
SVPWM	Space Vector Pulse Width Modulation
THD	Total Harmonic Distortion

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