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Novel PWM Pattern for AC–DC Matrix Converter with Low Switching Voltage Stress and Low Common-Mode Voltage

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Abstract

The AC–DC matrix converter (AMC) has promising application prospects; however, its widespread application is constrained by issues such as excessive common-mode voltage (CMV) and switching voltage stress. Previous studies have primarily focused on optimizing CMV as a single objective, while neglecting the optimization of switching voltage stress. This paper investigates switching voltage stress and CMV in a unified framework and proposes a PWM pattern that simultaneously suppresses switching voltage stress and CMV. The proposed PWM pattern divides each original sector into two subsectors and optimizes the zero-vector selection according to the instantaneous input-voltage relationship while arranging the active vectors in opposite sequences in the respective subsectors, thereby simultaneously suppressing switching voltage stress and CMV. First, three different PWM patterns are introduced. Then, the switching voltage stress and CMV characteristics of the three PWM patterns are analyzed. Finally, a simulation model and a hardware prototype are developed to evaluate the three PWM patterns, thereby validating the effectiveness and feasibility of the proposed PWM pattern.

Keywords: AC–DC matrix converter; switching voltage stress; common-mode voltage; space vector modulation

1. Introduction

Compared with conventional AC–DC converters, the AC–DC matrix converter (AMC) can achieve buck-type rectification and boost-type inversion in a single stage. In addition, the AMC offers several advantages, including a controllable input power factor, bidirectional power flow, and a compact structure without bulky electrolytic capacitors, showing promising application potential in fields such as vehicle-to-grid (V2G) systems and vehicle chargers [1,2]. However, its widespread application in the aforementioned fields is constrained by issues such as excessive common-mode voltage (CMV) and high switching voltage stress.

CMV is critical to the reliable operation of the AMC. Owing to its inherent high-frequency characteristics, CMV can induce common-mode leakage currents with high frequencies and large amplitudes, which may cause malfunctions or nuisance tripping of protection devices and consequently lead to system shutdown, thereby affecting the normal operation of the system. Moreover, it can generate severe common-mode electromagnetic interference (EMI) [3,4], which may adversely affect the normal operation of other control systems or electronic devices. CMV suppression methods can be broadly classified into two categories. The first category suppresses CMV mainly by adding auxiliary circuits or

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common-mode filters [5,6]. These methods generally do not degrade the input current quality; however, the additional hardware increases the cost and reduces the power density of the converter. The second category suppresses CMV by optimizing the modulation strategy [7]. Although such methods may increase the total harmonic distortion (THD) of the input current, they offer lower cost and higher power density than the former category and therefore exhibit greater advantages.

Switching voltage stress is also critical to maintaining the reliability of the AMC. Excessive voltage stress across the switching devices may accelerate device aging and increase the risk of failures such as thermal faults, thereby reducing system reliability [8,9]. In addition, reducing the switching voltage stress is essential for the proper selection of switching devices. The methods for suppressing switching voltage stress can also be mainly classified into two categories: improving the existing topology by adding auxiliary circuits and optimizing the modulation strategy to reduce the switching voltage stress of the converter.

At present, only a limited number of studies have addressed the simultaneous suppression of CMV and switching voltage stress. In [10], an improved current source rectifier (CSR) topology is proposed, in which additional diodes and capacitors are introduced to construct a common-mode current path, thereby simultaneously suppressing the common-mode current and switching voltage stress. In [11], a hybrid pulse width modulation (PWM) pattern is proposed, in which the switching states of different PWM patterns are modified to simultaneously reduce the CMV and switching voltage stress of the CSR. However, the above methods are only applicable to CSR and are difficult to extend to AMC.

Research on the CMV and switching voltage stress of AMC has mainly focused on CMV suppression, while simultaneous suppression of switching voltage stress remains difficult to achieve. In [12], an improved common-mode suppression method with a bidirectional freewheeling circuit is proposed for the AMC. An external freewheeling circuit is employed to equivalently construct virtual zero vectors for CMV suppression. However, two additional switching devices are required, which increases the converter cost and reduces its power density. In [13], an improved space vector modulation strategy is proposed for the AMC. Without requiring any additional circuit topology, this method reduces the peak CMV by 50% simply by replacing the zero vectors with two active vectors. However, it suffers from a large number of switching commutations and high input current THD. Therefore, developing a simple and cost-effective method capable of simultaneously suppressing CMV and switching voltage stress is of significant practical importance.

To develop a simple and cost-effective method that simultaneously suppresses CMV and switching voltage stress, this paper proposes a novel PWM pattern that optimizes the original zero-vector selection in each sector by selecting between two adjacent basic zero vectors, thereby suppressing both switching voltage stress and CMV. Compared with existing studies, the main contributions and innovations of this paper are summarized as follows:

(1) A PWM pattern capable of simultaneously suppressing CMV and switching voltage stress is proposed, addressing the limitation of conventional common-mode suppression methods that cannot simultaneously suppress switching voltage stress.
(2) Unlike conventional common-mode suppression methods that replace zero vectors with active vectors or constructed virtual vectors, the proposed method simultaneously suppresses CMV and switching voltage stress solely by optimizing the selection of basic zero vectors within the same sector, resulting in lower cost and simpler implementation.

Finally, a prototype controlled by a DSP + FPGA-based platform is developed, and both simulation and experimental results verify the correctness and effectiveness of the proposed method.

2. Analysis of Three Different PWM Patterns

The topology of the AMC is shown in Figure 1. Each bidirectional switch S_{xy} consists of two switching devices, S_{xy1} and S_{xy2}, connected in a common-source configuration, where x = a,b,c and y = p,n. The filter composed of L_x and C_x connects the converter to the grid-side voltage source U_x, with O denoting the grounding point. I_x is the grid-side current obtained after filtering the input current I_{rx}. V_{pn} denotes the high-frequency output voltage of the AMC. U_o and I_o are the voltage and current of the load R_L, respectively, and L_o is the output filter inductor.

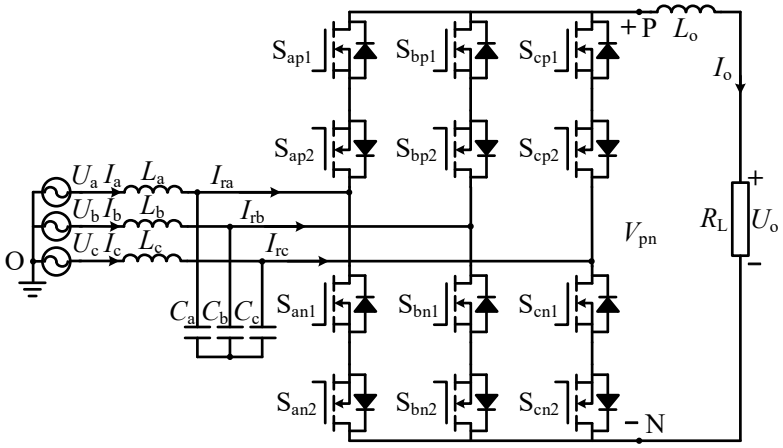


Figure 1. The topology of the AMC.

The space vector modulation (SVM) strategy is a modulation method that allows flexible switching among different PWM patterns. As shown in Figure 2, the SVM strategy divides the input phase voltage into six sectors, with each sector spanning an angular interval of $\pi/3$ rad. Since the AC-side capacitors must not be short-circuited and the DC load-side inductor must not be open-circuited, the AMC is controlled by nine switching states, each corresponding to one vector. These vectors include six active vectors, $\boldsymbol{I}_1$~$\boldsymbol{I}_6$, and three zero vectors, $\boldsymbol{I}_7$~$\boldsymbol{I}_9$. The reference current vector $\boldsymbol{I}_{ref}$ is synthesized within one switching period using two adjacent active vectors and one zero vector. The numbers "1" and "0" denote the ON and OFF states of the switches, respectively, based on which different operating modes can be defined.

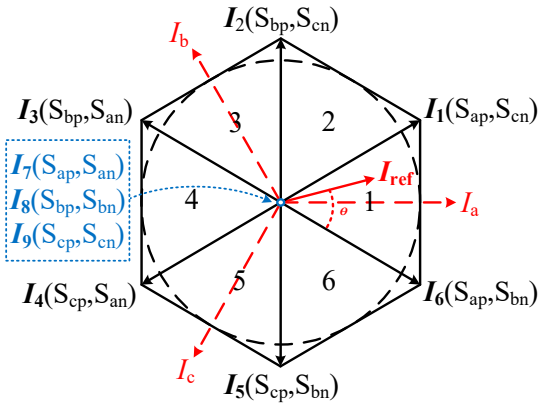


Figure 2. Switching vector diagram.

2.1. Conventional PWM Pattern

Taking Sector 1 as an example, in the conventional PWM pattern, the reference current vector $\boldsymbol{I}_{\mathrm{ref}}$ is synthesized within one switching period T_{s} using two adjacent active vectors, $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$, together with one zero vector, $\boldsymbol{I}_7$. Thus, $\boldsymbol{I}_{\mathrm{ref}}$ can be expressed as

$$\boldsymbol{I}_{\mathrm{ref}} T_{\mathrm{s}} = \boldsymbol{I}_1 T_1 + \boldsymbol{I}_6 T_6 + \boldsymbol{I}_7 T_0 \tag{1}$$

where T_1 and T_6 denote the dwell times of the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$, respectively, within one switching period, and T_0 denotes the dwell time of the zero vector. The dwell times of the respective vectors are given as

$$\begin{cases} T_6 = mT_{\mathrm{s}} \sin(\pi/3 - \theta) \\ T_1 = mT_{\mathrm{s}} \sin(\theta) \\ T_0 = T_{\mathrm{s}} - T_6 - T_1 \end{cases} \tag{2}$$

where m denotes the modulation index, and θ denotes the angle between the reference vector and the active vector $\boldsymbol{I}_6$. Figure 3 illustrates the four-step commutation process of the lower-arm switches during the transition from active vector $\boldsymbol{I}_6$ to active vector $\boldsymbol{I}_1$, while Figure 4 shows the corresponding switching timing diagram. As can be seen from the figures, the current transfer from the phase-b lower arm to the phase-c lower arm is completed through a four-step commutation process. In the following discussion, this process is referred to as "switching commutation."

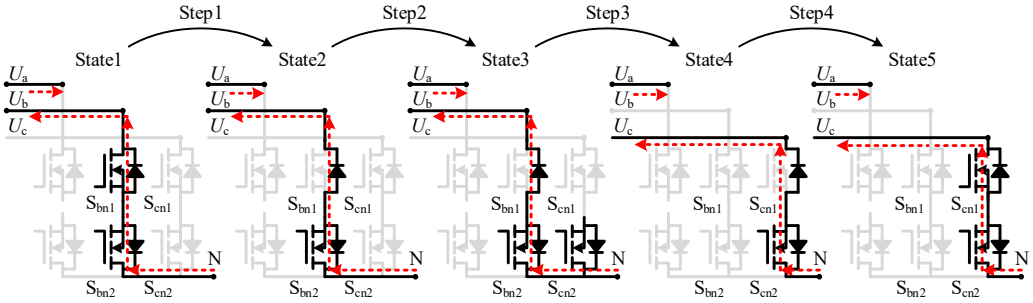


Figure 3. Switching sequence of the four-step commutation process.

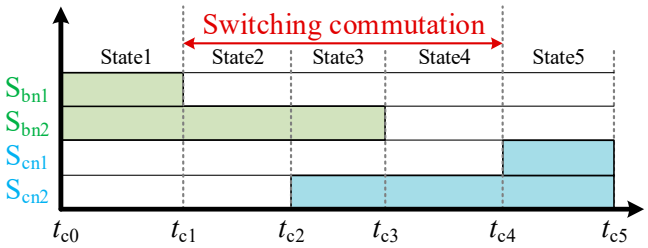


Figure 4. Corresponding switching timing diagram for the four-step commutation process.

The sequence of the applied vectors and the corresponding PWM pattern are shown in Figure 5a. Each PWM pattern synthesizes the corresponding input current vector while producing the corresponding output voltage. Within each switching period in Sector 1, there are five operating modes: t_0~t_1 corresponds to Mode 1 (100100), in which vector $\boldsymbol{I}_1$ is synthesized and the output voltage is U_{ab}; t_1~t_2 corresponds to Mode 2 (100001), in which vector $\boldsymbol{I}_6$ is synthesized and the output voltage is U_{ac}; t_2~t_3 corresponds to Mode 3 (110000), in which vector $\boldsymbol{I}_7$ is synthesized and the output voltage is zero; t_3~t_4 corresponds to Mode 4 (100001), in which vector $\boldsymbol{I}_6$ is synthesized and the output voltage is U_{ac}; and t_4~t_5 corresponds to Mode 5 (100100), in which vector $\boldsymbol{I}_1$ is synthesized and the output

voltage is U_{ab}. The transition between any two consecutive operating modes involves the commutation of only one bidirectional switch. In this paper, a four-step commutation method is employed to implement this switching transition [14].

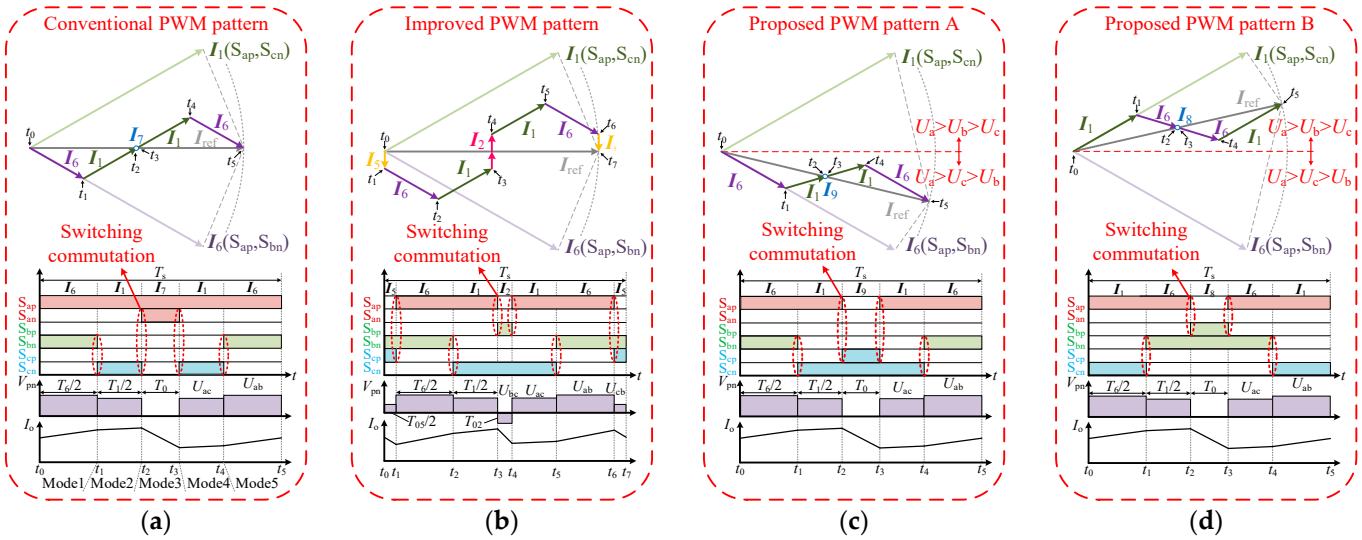


Figure 5. Sequence of applied vectors and corresponding switching states for three different PWM patterns. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern A; (**d**) proposed PWM pattern B.

In practical implementation, a finite commutation interval is required for the four-step commutation of the bidirectional switches. Unlike the dead time employed in conventional voltage source inverters [15], this commutation interval is introduced to ensure safe current transfer without short-circuiting the input voltage source or interrupting the load current. Although the finite commutation interval may introduce short transient deviations during switching transitions, it does not change the steady switching states or the basic vector sequence of the proposed PWM pattern.

2.2. Improved PWM Pattern

An improved common-mode suppression PWM pattern is proposed in [4]. In Sector 1, the active vectors $\boldsymbol{I}_6$, $\boldsymbol{I}_1$, $\boldsymbol{I}_5$, and $\boldsymbol{I}_2$ are used to synthesize the reference vector $\boldsymbol{I}_{ref}$, which can be expressed as

$$\boldsymbol{I}_{ref}T_s = \boldsymbol{I}_1T_1 + \boldsymbol{I}_6T_6 + \boldsymbol{I}_5T_{05} + \boldsymbol{I}_2T_{02} \tag{3}$$

The sequence of the applied vectors and the corresponding PWM pattern are shown in Figure 5b. The dwell times of the respective vectors are given as

$$\begin{cases} T_6 = mT_s\sin(\pi/3-\theta) \\ T_1 = mT_s\sin(\theta) \\ T_{05} = \dfrac{T_s - T_6 - T_1}{2} \\ T_{02} = \dfrac{T_s - T_6 - T_1}{2} \end{cases} \tag{4}$$

2.3. Proposed PWM Pattern

To ensure that the transition between any two operating modes involves the commutation of only one bidirectional switch, this paper proposes an optimized PWM pattern in which the original zero-vector selection in each sector is optimized through the selection of one of two adjacent basic zero vectors, thereby achieving simultaneous suppression of

CMV and switching voltage stress. The magnitude relationships among the input phase voltages and line voltages in each sector are shown in Figure 6a. Taking Sector 1 as an example, the input phase-voltage magnitude relationships in this sector can be divided into two regions, namely, $U_a > U_c > U_b$ and $U_a > U_b > U_c$. When the reference vector falls into different regions, the voltage stresses across the switching devices are different. Therefore, Sector 1 is divided into two regions, and different PWM patterns are employed in the respective regions.

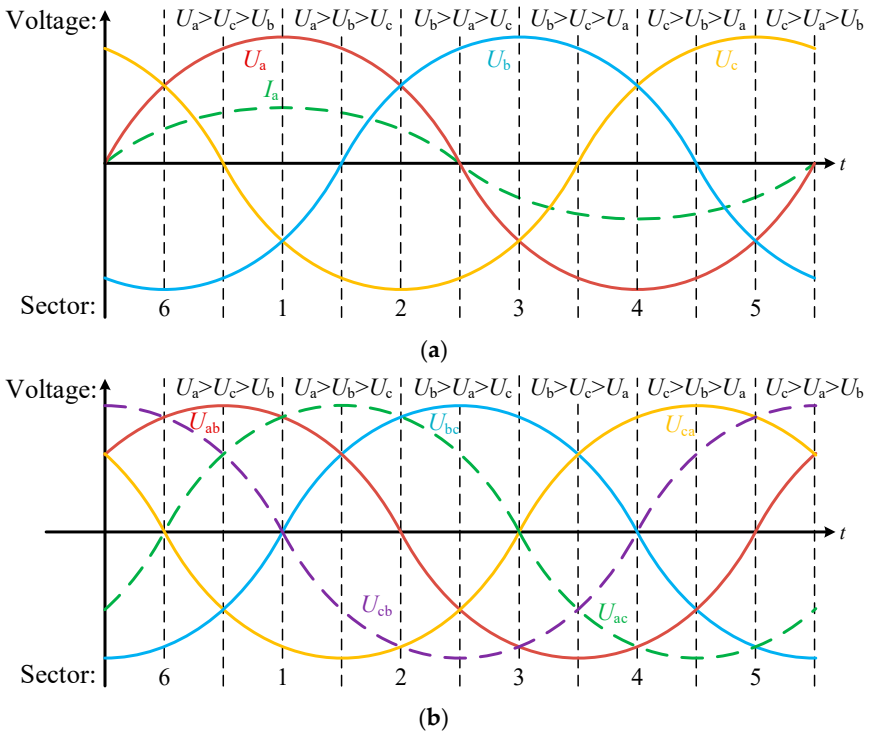


Figure 6. Distribution of phase voltages and line voltages in each sector. (**a**) Phase voltage; (**b**) line voltage.

(1) $U_a > U_c > U_b$

When the reference vector $\boldsymbol{I}_{ref}$ lies within this region, the active vectors $\boldsymbol{I}_6$ and $\boldsymbol{I}_1$, together with the zero vector $\boldsymbol{I}_9$, are used to synthesize $\boldsymbol{I}_{ref}$ within one switching period. $\boldsymbol{I}_{ref}$ can be expressed as

$$\boldsymbol{I}_{ref}T_s = \boldsymbol{I}_1T_1 + \boldsymbol{I}_6T_6 + \boldsymbol{I}_9T_0 \quad (5)$$

The sequence of the applied vectors and the corresponding PWM pattern are shown in Figure 5c, and the dwell times of the respective vectors are determined according to Equation (2).

(2) $U_a > U_b > U_c$

When the reference vector $\boldsymbol{I}_{ref}$ lies within this region, the active vectors $\boldsymbol{I}_6$ and $\boldsymbol{I}_1$, together with the zero vector $\boldsymbol{I}_8$, are used to synthesize $\boldsymbol{I}_{ref}$ within one switching period. $\boldsymbol{I}_{ref}$ can be expressed as

$$\boldsymbol{I}_{ref}T_s = \boldsymbol{I}_1T_1 + \boldsymbol{I}_6T_6 + \boldsymbol{I}_8T_0 \quad (6)$$

The sequence of the applied vectors and the corresponding PWM pattern are shown in Figure 5d, and the dwell times of the respective vectors are determined according to Equation (2).

Unlike the improved PWM pattern, which replaces the zero vector with additional active vectors, the proposed PWM pattern does not introduce any additional active vector.

Instead, the original zero-vector selection is optimized by selecting an appropriate basic zero vector within the same sector according to the instantaneous input-voltage relationship. Table 1 lists the optimized zero-vector selections for the proposed PWM pattern in each sector.

Table 1. Optimized zero-vector selection in different sectors.

Sector	Zero Vectors
1	$\boldsymbol{I}_9$,$\boldsymbol{I}_8$
2	$\boldsymbol{I}_8$,$\boldsymbol{I}_7$
3	$\boldsymbol{I}_7$,$\boldsymbol{I}_9$
4	$\boldsymbol{I}_9$,$\boldsymbol{I}_8$
5	$\boldsymbol{I}_8$,$\boldsymbol{I}_7$
6	$\boldsymbol{I}_7$,$\boldsymbol{I}_9$

3. Analysis of Switching Voltage Stress and Common-Mode Voltage for Different PWM Patterns

From the above description of the AMC topology and the three different operating modes, it can be seen that, within one switching period, the AMC alternately applies two active vectors and a zero vector to generate the output voltage and synthesize the reference vector. During this process, different vectors produce different switching voltages and CMV when applied. The improved PWM pattern is designed primarily to suppress CMV, while the suppression of switching voltage stress is neglected. In contrast, the proposed PWM pattern is capable of suppressing both CMV and switching voltage stress. Taking Sector 1 as an example, this section first analyzes the switching voltage stress under the three different PWM patterns and then analyzes their CMV, thereby theoretically demonstrating that the proposed PWM pattern can simultaneously suppress CMV and switching voltage stress.

3.1. Switching Voltage Stress

Switching voltage stress is defined as the peak-to-peak value of the voltage across a switching device during operation, i.e., the difference between the maximum and minimum voltages across the switching device within one switching period. Let V_{xyi} (i = 1,2) denote the voltage across the switching device under the application of each vector. Then, the voltage stress U_{xyi} across the switching device within one switching period can be expressed as

$$U_{\mathrm{xyi}} = V_{\mathrm{xyimax}} - V_{\mathrm{xyimin}} \tag{7}$$

where V_{xyimax} and V_{xyimin} denote the maximum and minimum values, respectively, of the voltage V_{xyi} across the switching device within one switching period. Taking the $U_{\mathrm{a}} > U_{\mathrm{c}} > U_{\mathrm{b}}$ region in Sector 1 as an example, when the conventional PWM pattern is employed, the active vectors $\boldsymbol{I}_6$ and $\boldsymbol{I}_1$ and the zero vector $\boldsymbol{I}_7$ are applied. The voltages V_{an1} across the switching device $\mathrm{S}_{\mathrm{an1}}$ corresponding to these vectors are U_{ab}, U_{ac}, and 0, respectively, as shown in Figure 7. Therefore, $V_{\mathrm{an1max}} = U_{\mathrm{ab}}$ and $V_{\mathrm{an1min}} = 0$, and the voltage stress U_{an1} across $\mathrm{S}_{\mathrm{an1}}$ is U_{ab}.

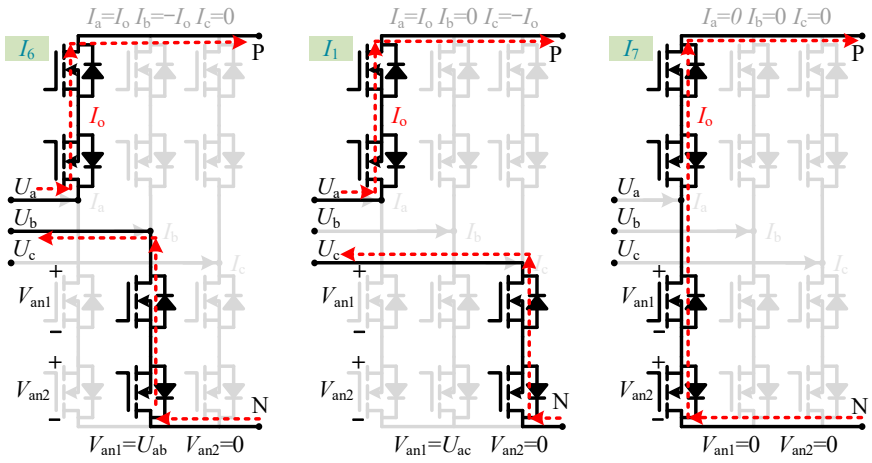


Figure 7. Current paths and switching voltage stresses under active vectors I_6 and I_1 and zero vector I_7.

The voltage stresses of the other switching devices can be derived in the same manner and are therefore not further elaborated. To investigate the switching voltage stresses under the three different PWM patterns, Table 2 lists the voltages across each switching device when the active vectors $\boldsymbol{I}_1$, $\boldsymbol{I}_2$, $\boldsymbol{I}_5$, and $\boldsymbol{I}_6$ and the zero vectors $\boldsymbol{I}_7$, $\boldsymbol{I}_8$, and $\boldsymbol{I}_9$ are applied in the $U_a > U_c > U_b$ region of Sector 1.

Table 2. Switching voltages under different vectors.

Switches Voltage	$\boldsymbol{I}_1$	$\boldsymbol{I}_2$	$\boldsymbol{I}_5$	$\boldsymbol{I}_6$	$\boldsymbol{I}_7$	$\boldsymbol{I}_8$	$\boldsymbol{I}_9$	Switches Voltage	$\boldsymbol{I}_1$	$\boldsymbol{I}_2$	$\boldsymbol{I}_5$	$\boldsymbol{I}_6$	$\boldsymbol{I}_7$	$\boldsymbol{I}_8$	$\boldsymbol{I}_9$
V_{ap1}	0	0	0	0	0	0	0	V_{ap2}	0	U_{ab}	U_{ac}	0	0	U_{ab}	U_{ac}
V_{an1}	U_{ac}	U_{ac}	U_{ab}	U_{ab}	0	U_{ab}	U_{ac}	V_{an2}	0	0	0	0	0	0	0
V_{bp1}	U_{ab}	0	U_{cb}	U_{ab}	U_{ab}	0	U_{cb}	V_{bp2}	0	0	0	0	0	0	0
V_{bn1}	0	0	0	0	0	0	0	V_{bn2}	U_{cb}	U_{cb}	0	0	U_{ab}	0	U_{cb}
V_{cp1}	U_{ac}	0	0	U_{ac}	U_{ac}	0	0	V_{cp2}	0	U_{cb}	0	0	0	U_{cb}	0
V_{cn1}	0	0	U_{cb}	U_{cb}	0	U_{cb}	0	V_{cn2}	0	0	0	0	U_{ac}	0	0

As shown in Figure 6b, the line voltages satisfy $U_{ab} > U_{ac} > U_{cb}$. Combined with Table 2, it can be concluded that the maximum switching voltage stress is U_{ac} only when the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_9$ are employed; otherwise, the maximum switching voltage stress is U_{ab}. The conventional PWM pattern employs the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_7$, resulting in a maximum switching voltage stress of U_{ab}. The improved PWM pattern employs the active vectors $\boldsymbol{I}_1$, $\boldsymbol{I}_2$, $\boldsymbol{I}_5$, and $\boldsymbol{I}_6$, for which the maximum switching voltage stress is also U_{ab}. In contrast, the proposed PWM pattern employs the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_9$, resulting in a maximum switching voltage stress of U_{ac}. Therefore, the proposed PWM pattern reduces the maximum switching voltage stress from U_{ab} to U_{ac}. As shown in Figure 8b, U_{lm} denotes the peak value of the input line voltage. The proposed PWM pattern reduces the switching voltage stress from U_{lm} to $0.866U_{lm}$.

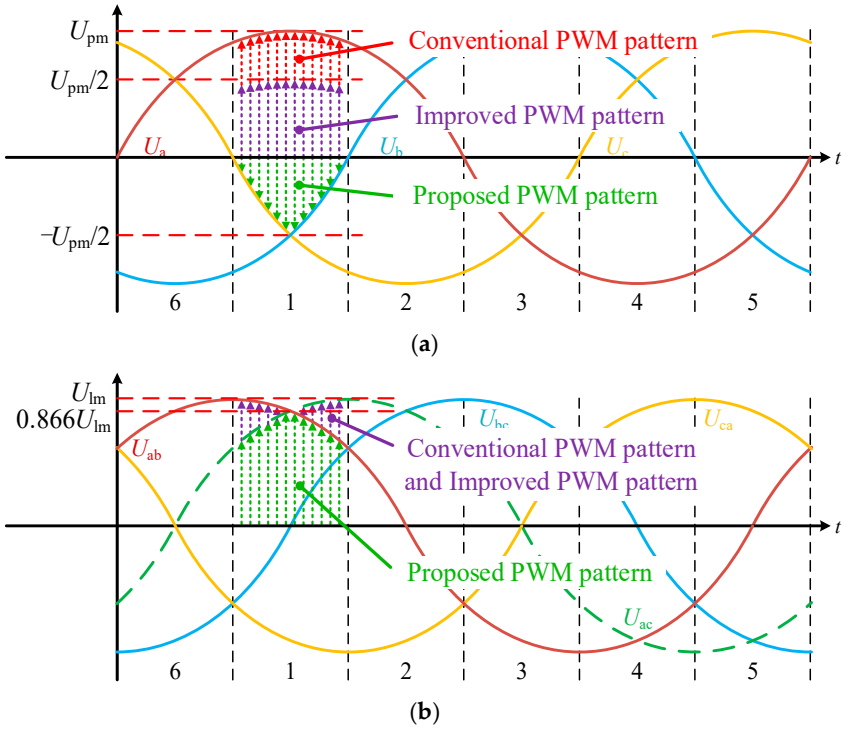


Figure 8. Peak phase and line voltages under three different PWM patterns. (**a**) Peak phase voltage; (**b**) peak line voltage.

3.2. Common-Mode Voltage

The common-mode voltage is defined as the average of the output phase voltages, i.e., the sum of the output phase voltages divided by the number of output phases. For the AMC, it can be expressed as

$$U_{CMV} = \frac{(U_{PO} + U_{NO})}{2} \tag{8}$$

where U_{PO} and U_{NO} denote the voltages of points P and N, respectively, with respect to the grounding point O. Their values depend on the applied vectors, and different vectors result in different values of U_{PO} and U_{NO}.

Taking Sector 1 as an example, when the active vector $\boldsymbol{I}_6$ is applied, as shown in Figure 7, the bidirectional switches S_{ap} and S_{bn} are turned on, yielding $U_{PO} = U_a$ and $U_{NO} = U_b$, and the common-mode voltage U_{CMV} is $-0.5U_c$. When the active vector $\boldsymbol{I}_1$ is applied, the bidirectional switches S_{ap} and S_{cn} are turned on, yielding $U_{PO} = U_a$ and $U_{NO} = U_c$, and U_{CMV} is $-0.5U_b$.

The CMV values corresponding to the other vectors can be calculated using Equation (8) and are therefore not discussed further. To investigate the common-mode voltages associated with the three different PWM patterns, Table 3 lists the corresponding U_{CMV} values when the active vectors $\boldsymbol{I}_1$, $\boldsymbol{I}_2$, $\boldsymbol{I}_5$, and $\boldsymbol{I}_6$ and the zero vectors $\boldsymbol{I}_7$, $\boldsymbol{I}_8$, and $\boldsymbol{I}_9$ are applied in Sector 1. As shown in Figure 6a, $|U_a| > |U_b|$ and $|U_a| > |U_c|$ in Sector 1. Combined with Table 3, it can be seen that the conventional PWM pattern employs the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_7$, resulting in a maximum common-mode voltage of U_a. The improved PWM pattern employs the active vectors $\boldsymbol{I}_1$, $\boldsymbol{I}_2$, $\boldsymbol{I}_5$, and $\boldsymbol{I}_6$, resulting in a maximum common-mode voltage of $0.5U_a$. The proposed PWM pattern employs the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_9$ in the first half of the sector, and the active vectors $\boldsymbol{I}_1$ and $\boldsymbol{I}_6$ together with the zero vector $\boldsymbol{I}_8$ in the second half of the sector. Its maximum common-mode voltage is also $0.5U_a$. As shown in Figure 8a, U_{pm} denotes the peak value

of the input phase voltage. The proposed PWM pattern can suppress the CMV to $0.5U_{pm}$ while simultaneously reducing the switching voltage stress to $0.866U_{lm}$.

Table 3. Common-mode voltage under different vectors.

Value of CMV	I_1	I_2	I_5	I_6	I_7	I_8	I_9
U_{cmv}	$-0.5U_b$	$-0.5U_a$	$-0.5U_a$	$-0.5U_c$	U_a	U_b	U_c

It is worth noting that, since $|U_b| < 0.5|U_a|$ and $|U_c| < 0.5|U_a|$ in Sector 1, the CMV produced by using the zero vectors I_9 and I_8 within a single switching period is lower than that produced by using the active vectors I_2 and I_5. The root-mean-square (RMS) value of the common-mode voltage, U_{CMVrms}, can be expressed as

$$U_{CMVrms} = \sqrt{\frac{1}{T_S}\int_0^{T_S} U_{CMV}(t)^2 dt} \tag{9}$$

As shown by the shaded areas in Figure 8a, the shaded area corresponding to the proposed PWM pattern is smaller than that corresponding to the improved PWM pattern. Therefore, the proposed PWM pattern also achieves a lower RMS value of the common-mode voltage.

Based on the aforementioned analysis, the peak-to-peak values of the CMV within one input voltage period under three different PWM patterns are shown in Figure 9. It can be seen that the peak-to-peak value of the CMV of the AMC under the proposed PWM pattern is less than that under the conventional PWM pattern and the improved PWM pattern within each input voltage period.

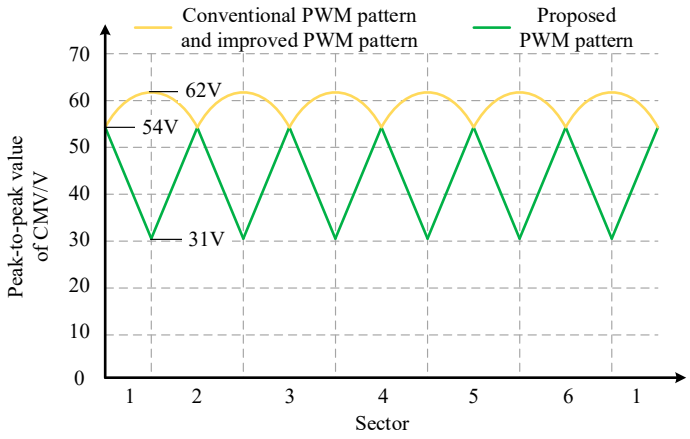


Figure 9. Calculated peak-to-peak value of the CMV under three different PWM patterns.

4. Simulation and Experimental Verification

To verify the correctness and effectiveness of the proposed PWM pattern, a MATLABR2024a/Simulink-based simulation model and a DSP + FPGA-based experimental prototype are established to analyze and validate the three different PWM patterns. Since the AMC contains six bidirectional switches comprising a total of 12 switching devices, analyzing the voltage stress of every switching device would be redundant. Therefore, taking the bidirectional switch S_{ap} as an example, the voltage waveforms across the switching devices S_{ap1} and S_{ap2} are presented. The key parameters of the simulation model and experimental prototype are summarized in Table 4.

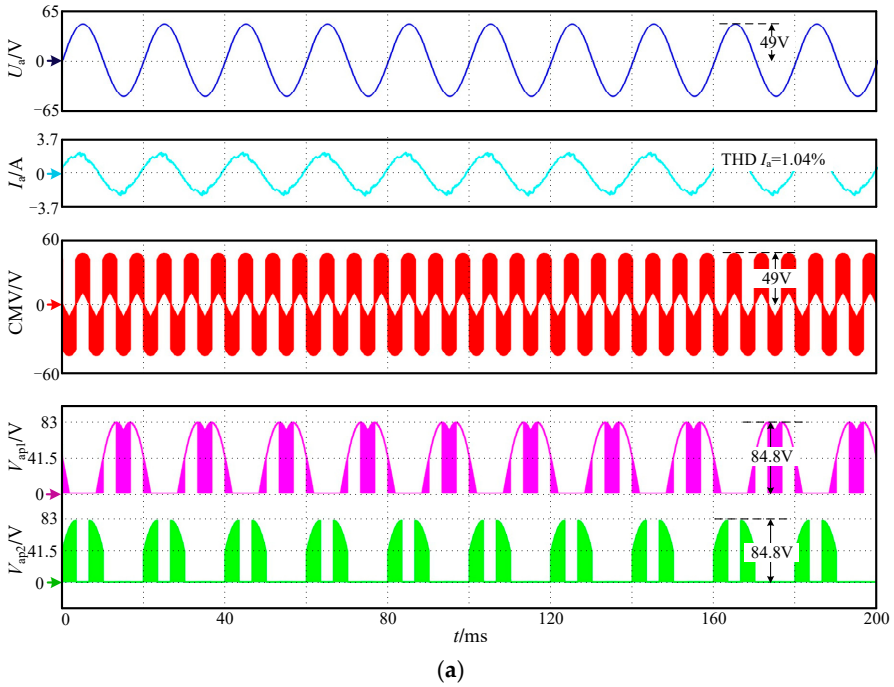
Table 4. Simulation and experimental parameters.

Parameters	Value
L_a,L_b,L_c	220 uH
C_a,C_b,C_c	1.5 uF
f_s	50 kHz
f_g	50 Hz
L_o	2 mH
R_L	20 Ω
m	1

4.1. Simulation Verification

The simulation results are shown in Figure 10, with the output voltage U_o set to 50 V. Figure 10 presents the waveforms of the grid-side voltage U_a, grid-side current I_a, CMV, and the voltages V_{ap1} and V_{ap2} across the switching devices S_{ap1} and S_{ap2}, respectively, under the three different PWM patterns. The switching voltage stress and CMV under different PWM patterns are analyzed separately.

Among the three different PWM patterns, neither the conventional PWM pattern nor the improved PWM pattern specifically considers the voltage stress of the switching devices. A detailed analysis of the switching voltage stress is presented in Section 3.1. By applying the proposed PWM pattern, the switching voltage stress can be reduced to 0.866 times the peak value of the input line voltage. As shown in Figure 10a,b, when the conventional PWM pattern and the improved PWM pattern are employed, the maximum switching voltage stress is 84.8 V. After applying the proposed PWM pattern, as shown in Figure 10c, the switching voltage stress is reduced from 84.8 V to 73 V, corresponding to approximately 0.86 times its original value. These results verify the theoretical analysis of the different PWM patterns presented in Section 3.1.



(**a**)

Figure 10. *Cont.*

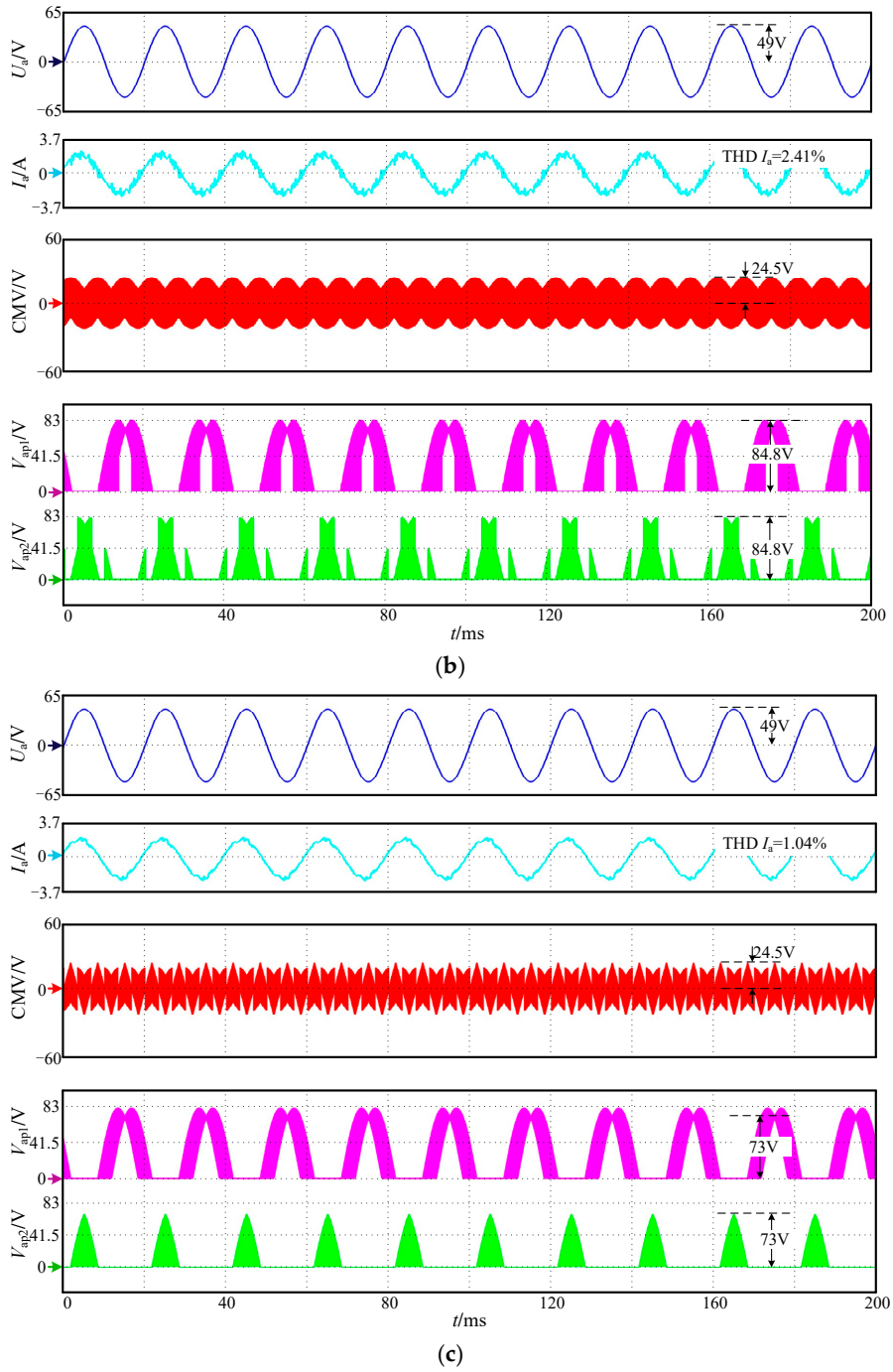


Figure 10. Simulation results under three different PWM patterns. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern.

Figure 11 shows the voltage waveforms of switch S_{ap1} under different PWM patterns within one switching period, providing a more intuitive illustration of the advantage of the proposed PWM pattern in terms of voltage stress. As shown in Figure 11, the switching voltage stress under both the conventional PWM pattern and the improved PWM pattern is U_{ca} within one switching period, whereas that under the proposed PWM pattern is U_{cb}. Since $U_{cb} < U_{ca}$, the proposed PWM pattern effectively suppresses the switching voltage stress.

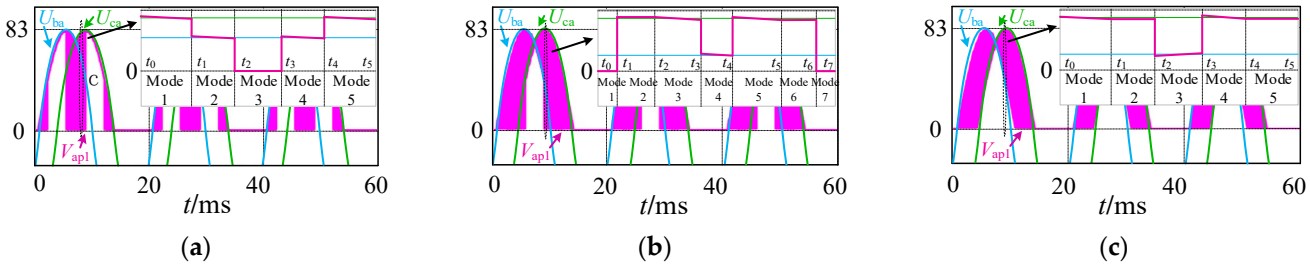


Figure 11. Voltage across switch S_{ap1} under different PWM patterns within one switching period. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern.

It is worth noting that the zero vectors do not affect the input current, whereas the active vectors do, as shown in Figure 7. Since the improved PWM pattern replaces the zero vector with two active vectors, additional input current harmonics are introduced. The simulation results confirm this observation. As shown in Figure 10, the input current THD is 2.41% when the improved PWM pattern is employed, whereas it is 1.04% for both the proposed PWM pattern and the conventional PWM pattern.

4.2. Experimental Verification

To further verify the feasibility of the proposed method, a DSP + FPGA-based experimental prototype was developed. The prototype and experimental setup are shown in Figure 12. SiC MOSFETs FDA59N30 are employed as the switching devices, and each bidirectional switch consists of two discrete MOSFETs connected in reverse series. The sampling circuit acquires the grid-side voltage U_a as the reference signal, which is fed into the DSP28335 after analog-to-digital conversion to calculate the duty cycles and determine the sector. The calculated signals are then sent to the EPM570T144C5N FPGA to generate the gate signals, which are subsequently converted by the gate-driver circuit into voltage signals ranging from +15 V to −8 V to control the ON and OFF states of the switching devices. Sampling is performed once during each switching period. Therefore, the sampling frequency is the same as the switching frequency, i.e., 50 kHz. The output voltage U_o is regulated to 50 V, and the switching voltage stress and CMV under different PWM patterns are analyzed.

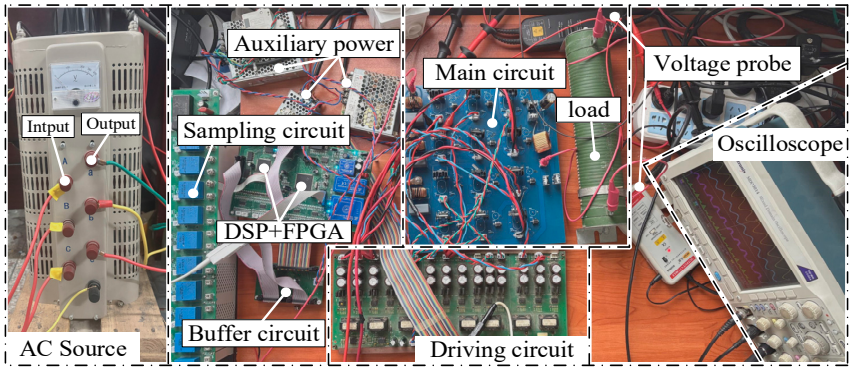


Figure 12. Experimental platform.

The experimental results are shown in Figure 13. As shown in Figure 13a,b, neglecting the effect of voltage ripple, the maximum switching voltage stress is approximately 110 V when the conventional PWM pattern and the improved PWM pattern are employed. After applying the proposed PWM pattern, as shown in Figure 13c, the switching voltage stress is reduced from 110 V to 96 V, corresponding to approximately 0.86 times its original value.

This further verifies the theoretical analysis of the different PWM patterns presented in Section 3.1.

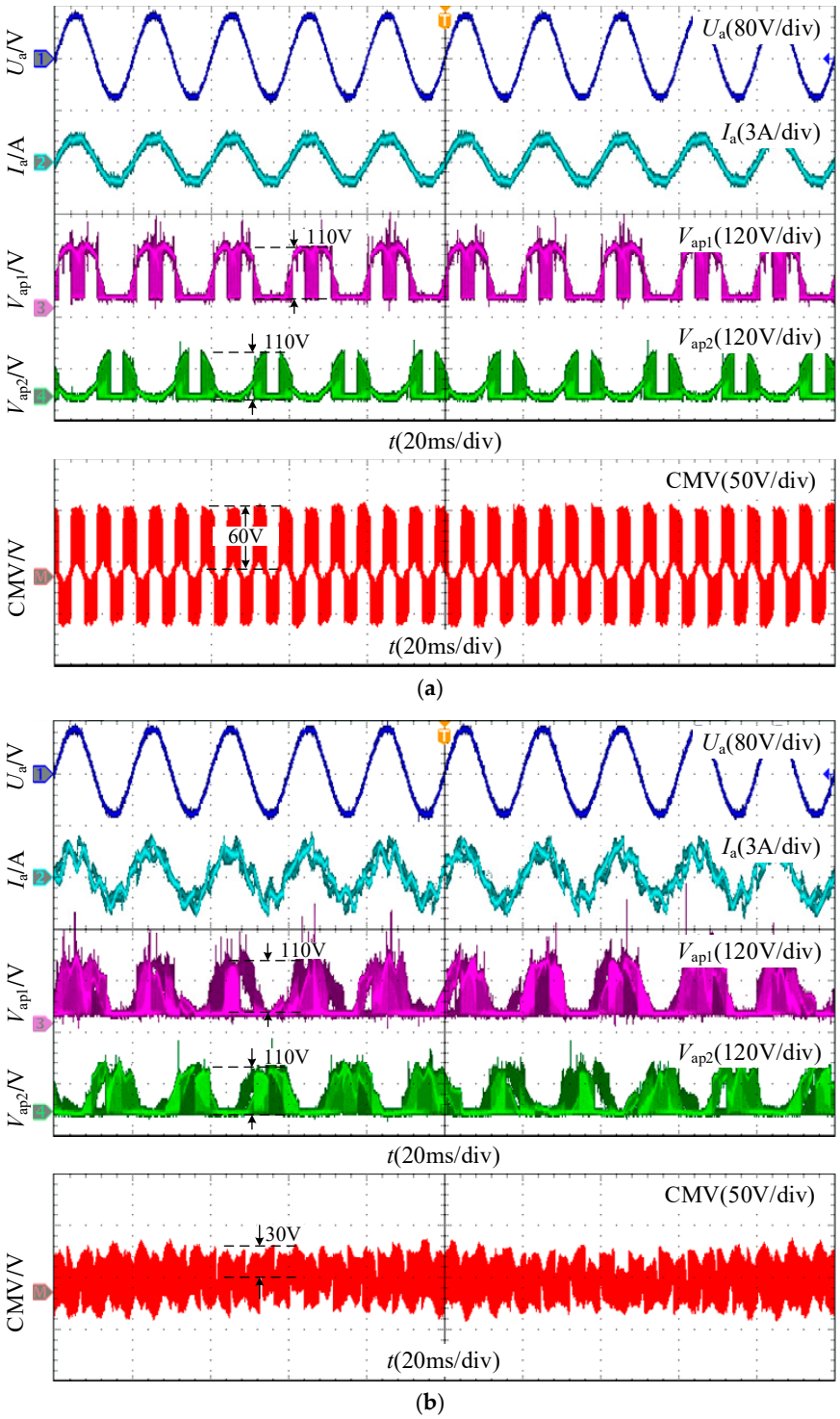


Figure 13. *Cont*.

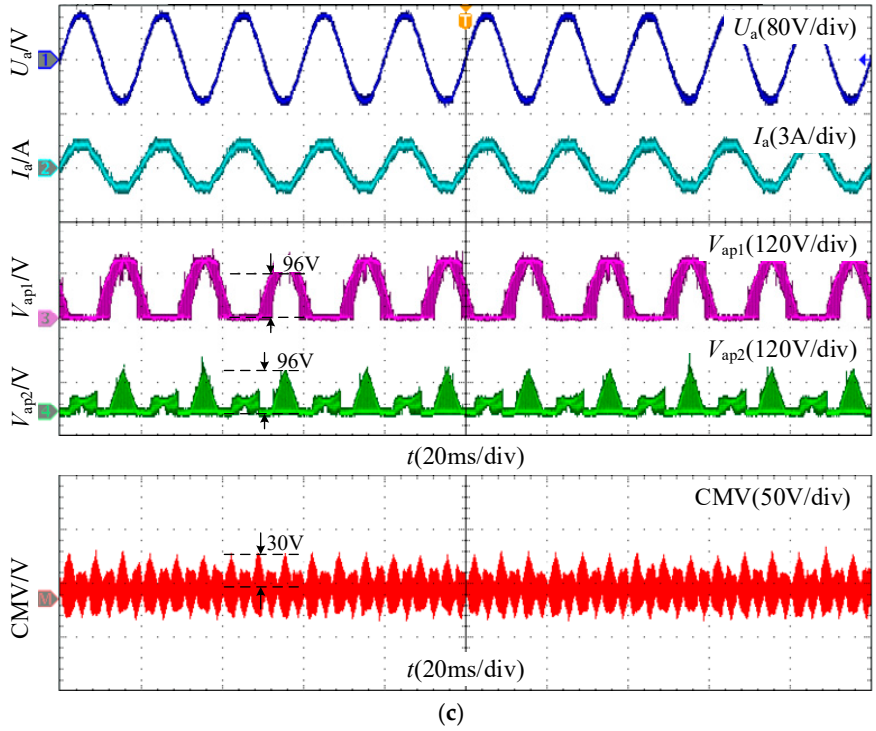


Figure 13. Experimental results under three different PWM patterns. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern.

As shown in Figure 13a, when the conventional PWM pattern is employed, the peak CMV is 60 V. After applying the improved PWM pattern, as shown in Figure 13b, the peak CMV is reduced to 30 V, i.e., half of its original value, while the maximum switching voltage stress remains 110 V. After applying the proposed PWM pattern, as shown in Figure 13c, the peak CMV is also 30 V, while the switching voltage stress is simultaneously reduced from 110 V to 96 V. In addition, the RMS value of the CMV is significantly reduced. These results further verify the theoretical analysis of the different PWM patterns presented in Section 3.2.

Since the improved PWM pattern replaces the zero vector with active vectors, additional input current harmonics are introduced. As shown in Figure 14, the grid-side current THD under the improved PWM pattern is 21.99%, which is substantially higher than the corresponding values of 4.21% and 4.02% under the conventional and proposed PWM patterns, respectively. This further verifies the analysis of the input current presented in Section 4.1.

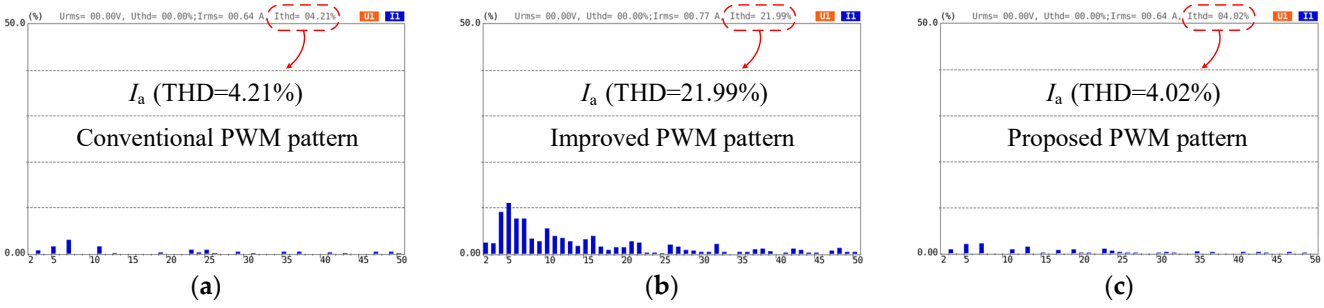


Figure 14. Experimental THD results under three different PWM patterns. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern.

4.3. Discussion

The switching voltage stress and RMS value of the CMV of the converter under the three different PWM patterns at different output power levels are shown in Figure 15. The proposed PWM pattern can simultaneously suppress the switching voltage stress and CMV over the entire output power range.

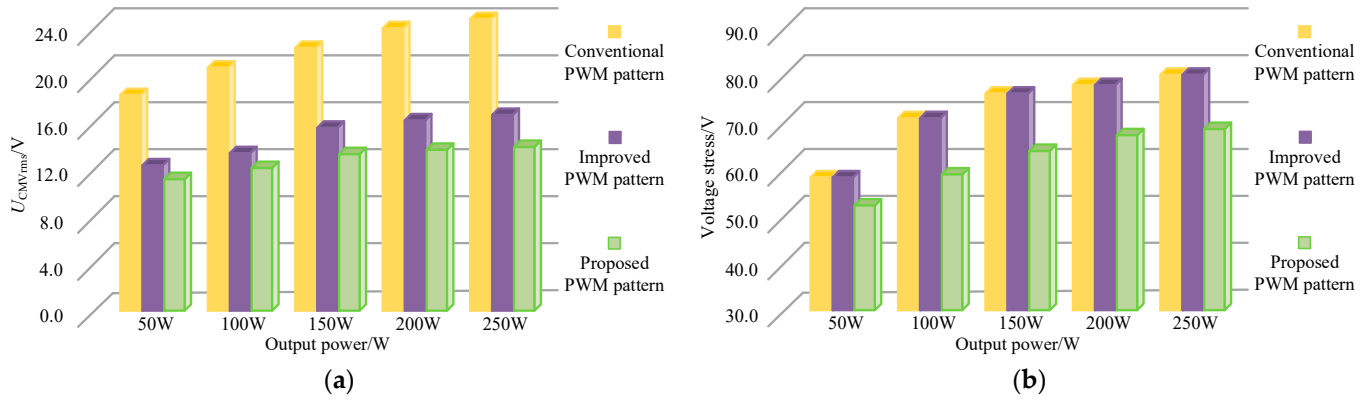


Figure 15. RMS value of the CMV and switching voltage stress at different output power levels when $m = 1$. (**a**) RMS value of the common-mode voltage; (**b**) switching voltage stress.

Figure 16 presents the RMS value of the CMV and the switching voltage stress under different modulation indices. The proposed PWM pattern maintains lower RMS values of the CMV and lower switching voltage stress over the entire range of modulation indices.

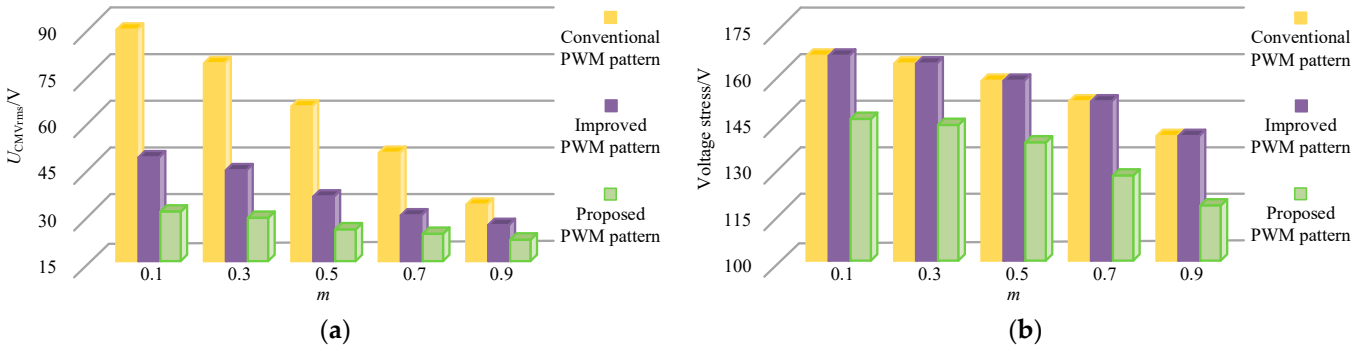


Figure 16. RMS value of the CMV and switching voltage stress under different modulation indices m. (**a**) RMS value of the common-mode voltage; (**b**) switching voltage stress.

The improved PWM pattern introduces two additional switching commutations within each switching period, resulting in extra switching losses. Therefore, the application of the improved PWM pattern significantly reduces the converter efficiency. In contrast, the proposed PWM pattern does not increase the number of switching commutations within a single switching period and introduces only one additional switching transition at each sector boundary, as shown in Figure 17.

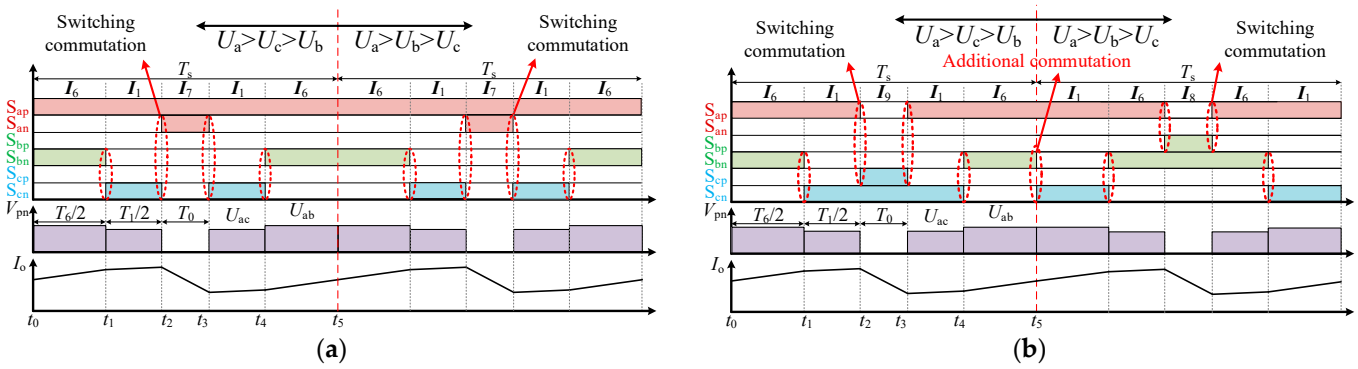


Figure 17. Switching commutation at sector boundaries under different PWM patterns. (**a**) Conventional PWM pattern; (**b**) proposed PWM pattern.

The switching loss of a single switching device is calculated as

$$P_{\mathrm{xyi}} = \frac{1}{2} V_{\mathrm{xyi}} I_{\mathrm{xyi}} f_{\mathrm{s}} (t_{\mathrm{rise}} + t_{\mathrm{fall}}) \tag{10}$$

where V_{xyi} and I_{xyi} denote the voltage across and the current flowing through the switching device, respectively; f_{s} is the switching frequency; and t_{rise} and t_{fall} denote the turn-on and turn-off transition times of the switching device. As shown in Figure 18, compared with the conventional PWM pattern, the additional commutation at the sector boundary results in a moderate increase in switching loss from 2.5825 W to 3.3756 W. Nevertheless, the switching loss remains substantially lower than the 13.7457 W obtained with the improved PWM pattern. Moreover, since no additional active vectors are introduced and the dwell times of the original active vectors remain unchanged, the proposed method does not significantly deteriorate the input-current harmonics and does not introduce any additional limitation on the modulation-index range.

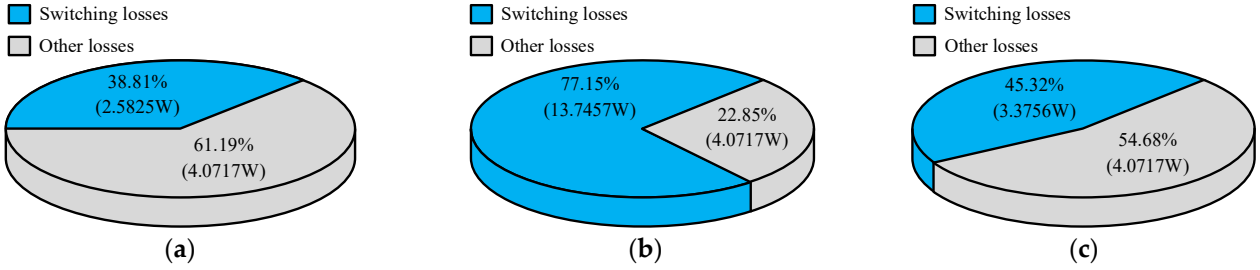


Figure 18. Loss analysis at an output power of 200 W. (**a**) Conventional PWM pattern; (**b**) improved PWM pattern; (**c**) proposed PWM pattern.

As shown in Figure 19, compared with the conventional PWM pattern, the proposed PWM pattern exhibits slightly lower efficiency under light-load conditions. However, as the output power increases, its efficiency approaches that of the conventional PWM pattern. More importantly, the proposed PWM pattern can simultaneously suppress the switching voltage stress and CMV of the converter. Therefore, compared with the other two PWM patterns, the proposed PWM pattern still provides the best overall performance.

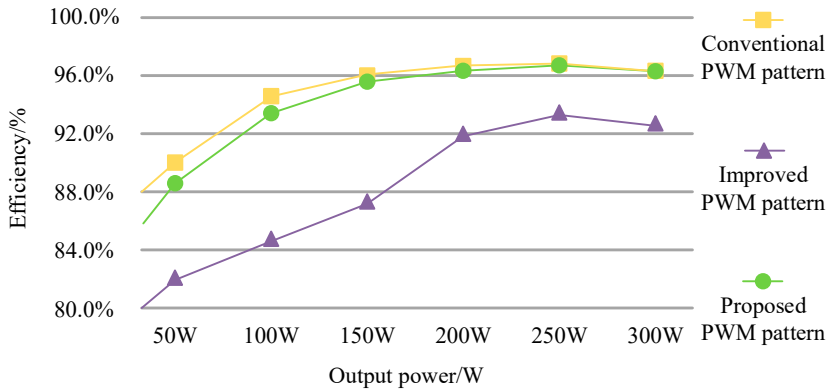


Figure 19. Efficiency curves under different PWM patterns.

Table 5 compares the PWM pattern proposed in this paper with other existing methods for the AMC. Although the method presented in [12] can reduce the CMV to $0.433U_{lm}$, it requires two additional switching devices, thereby increasing the hardware cost, as shown in Figure 20. The improved PWM pattern proposed in [13] can reduce the CMV to $0.5U_{lm}$; however, it results in relatively high input-current THD and does not effectively mitigate switching voltage stress. In contrast, the proposed PWM pattern requires no additional switching devices, simultaneously reduces the switching voltage stress and CMV, and maintains a low input-current THD, making it a promising option for practical applications.

Table 5. Comparison with other methods.

Comparison Items	Conventional Methods [1,2]	Hu [12]	Liu [13]	Proposed
Input current THD	1.04%	1.05%	2.41%	1.04%
Additional devices	None	Two switches	None	None
Switch voltage stress	U_{lm}	U_{lm}	U_{lm}	$0.866U_{lm}$
CMV	U_{pm}	$0.433U_{lm}$	$0.5U_{pm}$	$0.5U_{pm}$
Efficiency	96.78%	96.03%	91.82%	96.41%

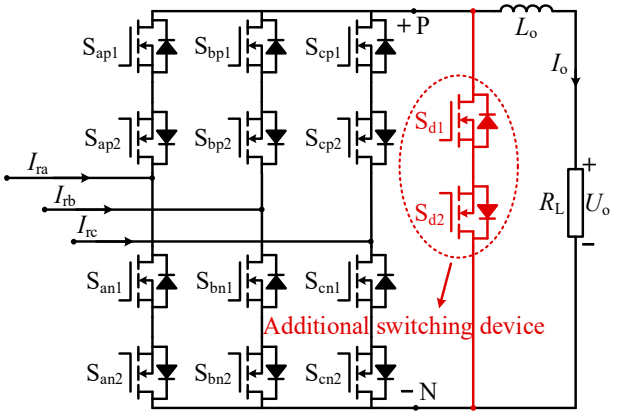


Figure 20. The topology proposed in [12].

The proposed PWM pattern focuses on reducing CMV and switching voltage stress and does not specifically ensure ZVS. Therefore, hard turn-on may still occur and cause additional switching loss and high-frequency EMI. ZVS-oriented modulation, such as leading-edge-aligned modulation, will be considered in future work.

5. Conclusions

This paper jointly investigates switching voltage stress and CMV and proposes a PWM pattern capable of simultaneously suppressing both. First, three different PWM patterns are introduced. Then, the switching voltage stress and CMV of the three PWM patterns are theoretically analyzed. Subsequently, the switching voltage stress and CMV under the three PWM patterns are verified through both simulations and experiments. The simulation and experimental results demonstrate that the proposed PWM pattern can simultaneously suppress switching voltage stress and CMV. Specifically, the experimental results show that the peak CMV is reduced from approximately 60 V to 30 V, corresponding to a reduction of 50%, while the maximum switching voltage stress is reduced from approximately 110 V to 96 V, corresponding to a reduction of approximately 12.7%. In addition, the measured input-current THD under the proposed PWM pattern is 4.02%. At an output power of 200 W, the conversion efficiency of the proposed PWM pattern is 96.41%, which is only 0.37 percentage points lower than that of the conventional PWM pattern. Finally, compared with other existing methods, the proposed PWM pattern requires no additional switching devices, can simultaneously suppress switching voltage stress and CMV, and maintains a low input-current THD, making it a promising option for practical applications.

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