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Investigation into Combined AC–DC Insulation Stress Evolution Mechanism and Combined Withstand Voltage Test Method for 40.5 kV Capacitor Bank Circuit Breaker Breaks

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Abstract

With the large-scale construction of renewable energy collection stations and distribution networks, the frequent switching of 40.5 kV reactive power compensation capacitor banks has become a routine operation. To accurately evaluate the insulation safety risk at the breaker break during the switching process of 40.5 kV capacitor bank circuit breakers, this paper comparatively investigates the dynamic transient processes and electric field evolution laws under four typical operating conditions: normal opening/closing, electrode plate short-circuit, non-synchronous opening/closing, and arc restriking. The microscopic failure mechanism under combined AC–DC stress is revealed, and a physical-equivalent combined AC–DC withstand voltage test scheme is proposed and experimentally validated. The results indicate that arc restriking introduces a secondary strong excitation during the unattenuated transient period, causing a surge in overvoltage on the capacitor side, making it the most severe condition inducing transient insulation degradation at the break. Insulation risk evaluation must be grounded on the true instantaneous potential difference between both sides of the break. Under the arc restriking condition, the voltages on both sides exhibit strong opposite-polarity superposition, resulting in a peak instantaneous potential difference of up to 129.0806 kV (busbar side: −49.4861 kV; capacitor side: +79.5945 kV), which substantially exceeds the 1 min power-frequency withstand voltage standard value (118 kV based on IEC 62271-100) for 40.5 kV circuit breaker breaks. Three-dimensional electrostatic field and space charge simulations further reveal the microscopic failure mechanism: under combined AC–DC stress, unipolar free charges undergo directional migration and steady-state accumulation at defects such as micro-protrusions on the contact surface on the DC residual voltage side, forming local high electric field regions and inducing field emission—an effect that cannot be effectively excited in traditional pure AC tests. Consequently, the non-physical extreme value superposition method is abandoned, and a combined AC–DC withstand voltage testing scheme comprising "AC power-frequency −49.4861 kV (peak) and DC +79.5945 kV" is recommended. This study provides deep theoretical insights and numerical evidence for evaluating the insulation margin and revising the type test standards of reactive power compensation circuit breaker breaks.

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Keywords: reactive power compensation capacitor bank; 40.5 kV circuit breaker; arc restriking; combined AC–DC stress; space charge; combined withstand voltage test

1. Introduction

With the large-scale integration of renewable energy generation and the increasing complexity of distribution network structures, fluctuations in reactive power within power systems have intensified, thereby imposing higher demands on the regulation capability of reactive power compensation devices [1–3]. As a core device for reactive power compensation in medium-voltage distribution networks, the 40.5 kV shunt capacitor bank has seen increasingly frequent switching operations. Currently, the primary devices responsible for switching such capacitive loads are predominantly air-insulated switchgear, which have been widely deployed in regional power grids such as Ningxia. However, during long-term service, the electromagnetic transient processes induced by frequent switching pose a serious challenge to the insulation performance of both circuit breakers and capacitor banks. Insulation breakdown faults occur frequently, representing a prominent hidden risk that constrains the safe and stable operation of power grids [4–6].

During the normal switching of capacitor banks, closing operations generate high-frequency inrush currents while opening operations produce transient recovery voltages (TRV) with high steepness [7–9]. Particularly severe are the back-to-back switching conditions—when multiple capacitor banks operate in parallel, energizing one bank causes other already charged banks to discharge into the newly energized unit via the busbar. This results in a significant increase in both the amplitude and frequency of the inrush current compared to single-unit switching, leading to cumulative damage to the circuit breaker contacts [10,11]. Studies have shown that the inrush current can lead to surface welding of the contacts. During subsequent opening operations, the welded areas are forcibly separated, generating metal particles and irregular surfaces that significantly reduce the dielectric withstand capability of the contact gap [12,13]. Moreover, during the opening operation, the recovery voltage across the contact gap exhibits a high-steepness characteristic. In three-phase interruption, the recovery voltage of the first-opening phase can reach up to 2.5 times the phase voltage, accelerating irreversible degradation of the insulating material and potentially leading to through-type breakdown.

A substantial number of simulation and experimental studies have been conducted to address the transient issues associated with capacitor bank switching [14–16]. A transient equivalent circuit for power capacitor switching was established, and the influencing factors of the closing transient process were analyzed [17]. A model of the electric field and gas flow field in a 40.5 kV SF_6 arc-extinguishing chamber was established, and the influence of different nozzle structures on interrupting performance was analyzed [18]. Badrzadeh B investigated the transient recovery voltage (TRV) of vacuum circuit breakers during switching operations of shunt capacitor banks in wind farms, focusing on the effects of different capacitor bank configurations on TRV. It was pointed out that the installation of current-limiting reactors may lead to circuit breaker failure under certain severe operating conditions [19]. Kafshgari N A et al. considered the high-frequency models of system components and grounding system parameters, employing EMTP-RV simulations to analyze the effects of grounding grid structure, soil resistivity, and other factors on transient recovery voltage (TRV). They emphasized the importance of high-frequency grounding models for accurate TRV prediction [20]. In addition, Eliyan T et al. compared the synergistic suppression effects of arresters, pre-insertion resistors (PIR), and RC snubber components. They pointed out that, under severe back-to-back switching

conditions of capacitive loads, a single nonlinear clamping element may leave a high-frequency protection dead zone, and they demonstrated the necessity of introducing a composite transient damping network to ensure sufficient insulation withstand margin for the equipment [21].

Standard dielectric evaluation systems (e.g., IEC 62271-1 and IEC 62271-100) specify conventional power-frequency withstand (118 kV RMS for 40.5 kV open contact gaps) and lightning impulse tests to verify switchgear insulation [22]. However, field operating experience and transient reverse-analysis reveal critical technical limitations when applying these standards to 40.5 kV capacitor bank switching [23]. Specifically, the capacitive current switching tests (Classes C1/C2) in IEC 62271-100 focus primarily on arc-extinguishing and restrike performance within milliseconds post-interruption, whereas standard 1 min AC withstand tests apply only symmetric, pure sinusoidal voltage stresses [24]. This test paradigm fails to replicate the asymmetric combined AC/DC electric field created by the long-term trapped DC residual voltage (up to 1.0 p.u.) on the load-side capacitor coupled with the reverse-polarity swing of the bus-side AC voltage [25]. Furthermore, while alternating fields in standard pure AC tests prevent net charge accumulation, the persistent DC bias component in actual combined AC/DC stress drives unipolar charge migration and localized space-charge accumulation at solid–gas interfaces (e.g., moisture-affected insulating rods) and contact micro-burrs within air-insulated switchgear [26,27]. This space-charge effect severely distorts local electric fields and triggers field emissions or breakdown. The fundamental mismatch between standard static AC testing conditions and actual dynamic, polarity-inverted physical stresses explains why circuit breakers that pass standard 118 kV AC tests still suffer unanticipated insulation failures during real-world capacitive switching.

To address the aforementioned issues, this paper systematically investigates the insulation stress evolution mechanism and the combined AC–DC withstand voltage test method for 40.5 kV capacitor bank circuit breaker breaks. First, the dynamic transient processes of the system under four typical operating conditions—normal opening/closing, inter-pole short-circuit, non-synchronous opening/closing, and arc restriking—are comparatively analyzed. An insulation risk evaluation principle based on the true instantaneous potential difference between both sides of the break is established, revealing the macroscopic overvoltage mechanism where the peak instantaneous potential difference (up to 129.0806 kV) induced by polarity reversal under arc restriking exceeds the current 1 min power-frequency withstand voltage standard value (118 kV). Second, combined with three-dimensional electrostatic field and space charge dynamics simulations, the microscopic failure mechanism is elucidated: under combined AC–DC stress, the DC residual voltage induces the directional accumulation of unipolar free charges, which distorts the local electric field and triggers field emission. Finally, rejecting the non-physical algebraic summation of peak values, an equivalent combined AC–DC withstand voltage testing scheme of "AC −49.4861 kV (peak) and DC +79.5945 kV" is proposed and experimentally validated. The findings of this study provide theoretical foundations and numerical evidence for the insulation design optimization, margin assessment, and revision of type test standards for 40.5 kV capacitor switching circuit breakers.

2. Analysis of Transient Processes During Capacitor Bank Switching

2.1. Transient Analysis of Closing

When the circuit breaker closes onto the capacitor bank, it is equivalent to instantaneously connecting an uncharged or residual-voltage-carrying capacitor to the power supply. Since the voltage across the capacitor cannot change instantaneously, a severe transient process will occur in the circuit if the supply voltage is non-zero at the instant of

closing. To analyze this phenomenon, a single-phase equivalent circuit model is established using the lumped-parameter method, as shown in Figure 1. All parameter values are quantified based on a standard 40.5 kV/6 Mvar capacitor bank system with a 6% series reactor deployed in the local grid, as summarized in Table 1.

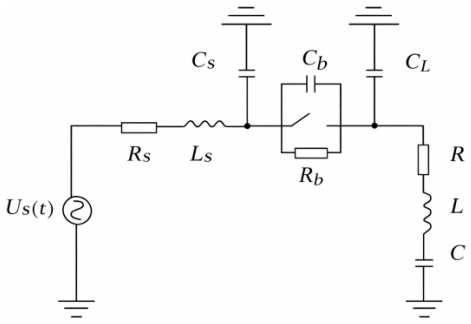


Figure 1. Single-phase Equivalent Circuit Model.

Table 1. Parameters of the single-phase equivalent circuit model shown in Figure 1.

Parameter	Description	Typical Value & Unit	Source/Derivation Basis
$U_s(t)$	Instantaneous source phase voltage	$33.07\sin(\omega t + \psi)$	Peak phase voltage of 40.5 kV system ($40.5 \times \sqrt{2}/\sqrt{3}$)
R_s	System equivalent resistance on source side	0.05 Ω	Equivalent calculation based on short-circuit ratio $X/R \approx 10$
L_s	System equivalent inductance on source side	1.27 mH	Equivalent calculation based on short-circuit capacity S_k = 400 MVA
C_s	Stray capacitance to ground on busbar side	10 nF	Distributed capacitance to ground of 40.5 kV insulated busbars and bushings
C_b	Parasitic capacitance across open contact gap	100 pF	Stray capacitance between moving and fixed contacts of the interrupter
R_b	Contact and conductor loop resistance	0.02 Ω	Circuit breaker main circuit resistance specifications
C_L	Stray capacitance to ground on load side	2.0 nF	Stray capacitance of capacitor bank enclosure and connecting leads to ground
L	Total loop inductance ($L_S + L_k$)	28.10 mH	Includes 6% series reactor inductance (L_k = 26.83 mH)
C	Main capacitance of the capacitor bank	11.64 μF	Rated capacitance corresponding to 6 Mvar/40.5 kV
R	Equivalent loop damping resistance	0.25 Ω	Accounts for high-frequency skin effect and reactor losses

The equivalent circuit for the closing operation of a single capacitor bank can be simplified to a series RLC circuit. According to Kirchhoff's Voltage Law, the governing differential equation is given by [7]:

$$L_s \frac{di}{dt} + Ri + \frac{1}{C}\int idt = U_m \sin(\omega t + \psi) \quad (1)$$

where L is the total loop inductance, equal to the sum of the system equivalent inductance Ls and the series reactor inductance L_k; C is the equivalent capacitance of the capacitor bank; R is the equivalent resistance of the loop; i is the loop current; $U_m \sin(\omega t + \psi)$ represents the supply voltage; and ψ is the closing initial phase angle. Under the ideal condition where R is neglected, the closing current $i(t)$ consists of a fundamental frequency component i_{find} and a transient high-frequency component i_{trans}:

$$i(t) = i_{fund}\cos(\omega t + \phi) - i_{fund}\cos\phi \cdot \cos(\omega_0 t) + \frac{U_m \sin\phi}{L\omega_0}\sin(\omega_0 t) \quad (2)$$

here, for a 40.5 kV system, with a 6% reactor configured, the natural oscillation frequency f_0 is governed by the total loop inductance L and capacitance C via $f_0 = 1/2\pi\sqrt{LC}$. For standard capacitor banks rated at 3–12 Mvar (phase capacitance $C \approx 5.82$ μF~23.28 μF), when equipped with a 6% series reactor, the reactor inductance is $L_k = 0.06/\omega^2 C$ (L_k = 26.83 mH for 6 Mvar). The primary oscillation frequency can be estimated by $f_0 = f/\sqrt{0.06} \approx 204.1$ Hz. Considering the system source inductance L_S (1.27 mH), the actual f_0 ranges between 200 Hz and 500 Hz. Conversely, without a series reactor (L_k = 0), the loop inductance drops to only the system short-circuit inductance L_S (0.5~1.7 mH) or busbar inductance L_{b2b} (10~30 μH), causing f_0 to surge to several kHz or tens of kHz.

The most severe operating condition occurs when closing takes place at the peak voltage instant ($\psi = 90°$). Under this operating condition, the transient current consists of a fundamental frequency component and a high-frequency free component.

The rationale for neglecting the loop resistance R during the analytical derivation of transient peak values is based on the extremely high-quality factor ($Q = \sqrt{L/C}/R \approx 196.5$) and underdamped nature ($\xi \approx 0.0025$) of the 40.5 kV capacitor bank circuit. At the instant of the first transient peak ($t_p = \pi/\omega_0$), the damping attenuation factor is $e^{-atp} = e^{-\xi\pi} \approx 0.992$, meaning that R reduces the peak amplitude by less than 0.8%. Consequently, setting $R \to 0$ allows for closed-form analytical expressions of the worst-case envelope peaks (e.g., Equation (3) for peak inrush current and Equation (5) for TRV limits), aligning with conservative insulation design practices. In Section 2, the full high-frequency resistance R and skin effects are rigorously incorporated into numerical simulations to capture the exact decay characteristics. The system's free oscillation frequency f_0 is much higher than the power frequency f, and the peak inrush current I_{max} can be approximated as

$$I_{max} \approx U_m\sqrt{\frac{C}{L}} = \frac{U_m}{Z_0} \quad (3)$$

where Z_0 is the characteristic impedance of the loop. For back-to-back switching of capacitor banks, since the already energized capacitor bank discharges into the incoming capacitor bank through the busbar, the loop inductance is limited to only the busbar and lead inductance, resulting in extremely low impedance. This leads to high-frequency inrush currents that can reach several dozen to even over one hundred times the rated current.

2.2. Transient Analysis of Disconnection

When a capacitor bank is disconnected, ideally the current is interrupted at the zero crossing, and the residual voltage across the capacitor terminals is the supply peak voltage

U_m. As the supply voltage varies according to a cosine law, after half a cycle it becomes $-U_m$, at which point the recovery voltage across the circuit breaker contacts reaches its maximum value of $2U_m$.

If, within half a cycle after opening, the dielectric strength between the moving and fixed contacts of the circuit breaker fails to recover rapidly, or if metallic vapor remains between the contacts, the gap may experience restrike under the high voltage of $2U_m$. At the moment of restrike, the voltage across the capacitor undergoes a violent oscillation, rapidly transitioning from U_m toward the supply voltage $-U_m$, thereby generating a high-frequency oscillatory overvoltage. The above derivation indicates that, in the case of a single restrike, the theoretical maximum overvoltage can reach $3U_m$. If multiple restrikes occur, the voltage, through a cumulative effect, may reach $5U_m$ or even higher, posing a serious threat to the insulation of 40.5 kV systems.

If a restrike occurs at the moment $t_{restrike}$, the circuit will be re-closed. This constitutes a high-frequency oscillatory process, and the physical mechanism can be described as follows [20]:

$$L_s \frac{di}{dt} + \frac{1}{C}\int idt + u_C(t_{restrike}) = u_s(t) \tag{4}$$

where L_s is the equivalent inductance on the system supply side, and $u_s(t) = U_m \cos(\omega t)$ is the supply voltage. The above equation is a second-order homogeneous differential equation, whose solution corresponds to the voltage across the capacitor and can be expressed as

$$u_C(t) = u_s(t) + [u_C(t_{restrike}) - u_s(t_{restrike})] \cdot \cos(\omega_0 t) \tag{5}$$

where $\omega_0 = \frac{1}{\sqrt{LC}}$ is the angular frequency of the high-frequency oscillation. The high-frequency oscillatory frequency f_0 during the opening transient is primarily determined by the loop inductance L and the capacitor bank capacitance C, and is only weakly influenced by the opening phase angle. The free oscillation solution indicates that the current and voltage exhibit a form of high-frequency damped oscillation, with their amplitudes and decay rates being influenced by the loop damping resistance R. Parameter sensitivity analysis reveals that increasing the inductance L reduces the dominant frequency f_0, and slows the voltage rise rate, while increasing the capacitance C lowers the dominant frequency and increases the initial stored energy of the system. When the damping resistance R is relatively large, the oscillation decays more rapidly and the peak voltage is reduced, whereas its influence on the dominant frequency is not significant. These analytical results can be compared with simulation data to verify the validity of the theoretical model, and they provide a foundation for analyzing opening transients under various operating conditions.

2.3. Analysis of Pre-Breakdown and Recovery Voltage (TRV) Characteristics of Circuit Breakers

Based on the opening circuit model and free oscillation analysis established earlier, this section further analyzes the definition and calculation method of the transient recovery voltage (TRV) peak at the contact gap, in order to quantify the impact of the opening transient on the insulation of the contacts [7,17].

The peak value of the transient recovery voltage (TRV) across the contact gap after opening is defined as

$$v_{gap}(t) = u_s(t) - v_c(t) \tag{6}$$

where $u_s(t) = U_m \cos(wt + \phi_s)$ (or sin provided the phase convention is consistent) contains, $v_c(t)$ in the short term, both a free oscillation component and a forced component:

$$v_c(t) = v_c(0) + A\cos(w_0 t) + B\sin(w_0 t) + v_{forced}(t) \tag{7}$$

In the absence of restrike, the theoretical peak value of the TRV in the first half-cycle can reach $2U_m$, which occurs when the residual voltage on the capacitor is opposite in polarity to the system voltage and has an amplitude close to U_m. If a single restrike occurs accompanied by a high-frequency transient oscillation before final arc extinction, the superimposed oscillation can increase the peak TRV to $3U_m$. Cascading multiple restrikes may further raise the peak value (commonly in the range of $3U_m$ to $5U_m$, with the exact magnitude depending on L, C, Δv and the number of restrikes).

The dielectric recovery strength (i.e., the deionization and insulation restoration capability) can be approximately represented by a simple single-exponential model:

$$V_{recovery}(t) = V_{final}(1 - e^{(-t/\tau_{recovery})}) \tag{8}$$

where $\tau_{recover}$ is the dielectric recovery time constant. The restrike trigger condition can be expressed as the existence of a time t such that

$$v_{gap}(t) > V_{recovery}(t) \tag{9}$$

That is, the TRV curve breaks through the dielectric recovery curve at a certain moment, causing the gap to break down again.

The typical rise rate of the TRV is related to the dominant mode of the circuit, and an engineering approximation is given as follows:

$$(\frac{du}{dt})_{\max} \approx w_0 \cdot \Delta V \tag{10}$$

where ΔV represents the magnitude of the driving voltage difference (for example, the voltage difference between the capacitor residual voltage and the system voltage at the instant of closing or opening), w_0 is defined as the natural high-frequency angular frequency of the opening/restrike circuit. If the maximum rate of voltage change $(\frac{du}{dt})_{\max}$ exceeds the permissible rise rate threshold of the circuit breaker or the dielectric, the risk of restrike becomes significant.

Restrike is by no means a simple single-arc re-ignition; rather, it is a complex physical process involving high-frequency charge injection, step-like residual voltage elevation, inter-electrode voltage baseline offset, and positive feedback of electric field intensity accumulation. The initial restrike establishes a low-impedance conduction path, triggering high-frequency oscillations. The arc quenches at the high-frequency natural current zero, leaving behind an elevated residual voltage reference. This elevates the baseline for the subsequent transient recovery voltage (TRV) rise, thereby facilitating secondary restrikes. The repetition of this sequence establishes positive feedback, energy accumulation, and voltage cascaded amplification until the transient energy is fully dissipated or dielectric recovery is complete. Fundamentally, it is a nonlinear positive-feedback transient process driven by the coupling between the natural reversal of the power-frequency voltage phase and the charge trapping effect induced by forced arc interruption at high-frequency current zeros. The initial restrike provides a path for charge reversal, while the high-frequency quenching locks the elevated potential reference, ultimately causing the inter-electrode voltage stress to escalate in an arithmetic progression ($2U_m \rightarrow 4U_m \rightarrow 6U_m$).

To explain from the perspectives of thermodynamics and electromagnetic energy conversion why energy does not dissipate immediately but gradually accumulates, a phase-plane analysis method is introduced. The capacitor voltage vc(t) is normalized as the abscissa, and the high-frequency current $i_{hf}(t) \cdot Z_0$ is normalized as the ordinate. The entire cascading process manifests as an unclosed, outward-expanding spiral trajectory (as shown in Figure 2).

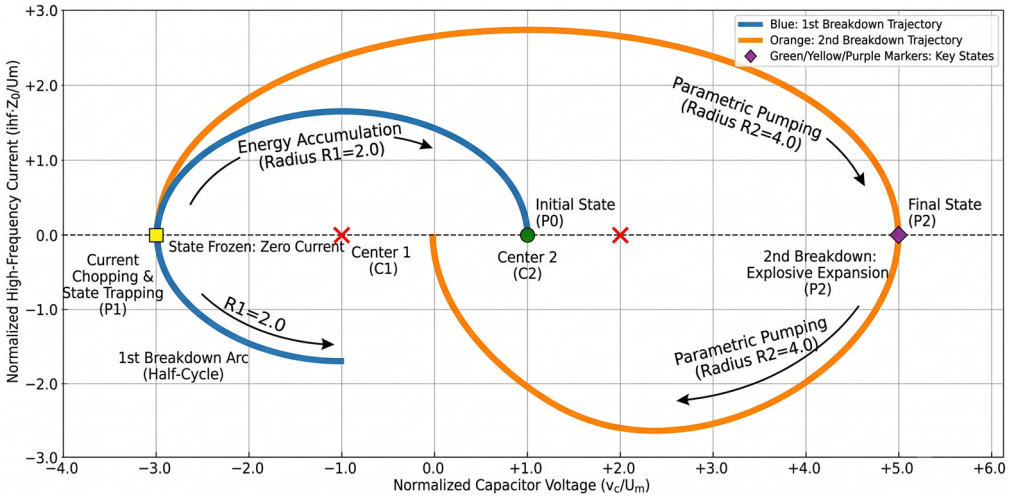


Figure 2. Phase-plane State Expansion Trajectory of Capacitor Charge and Current during Cascaded Restrikes.

Figure 2 illustrates that the source potential (the equilibrium center) alternates at power frequency between $\pm 1.0 U_m$. Coupled with the "state locking" effect from high-frequency arc chopping, this potential switching acts as a "parametric pumping" mechanism, which drives a step-wise, cascaded amplification of the energy stored in the LC system. Whether the cascaded amplification process can persist depends on the competition between the dielectric recovery rate of the circuit breaker and the rates of rise and amplitude growth of the TRV. Figure 3 illustrates how the insulation recovery curve is continuously "pierced" following the residual voltage baseline elevation.

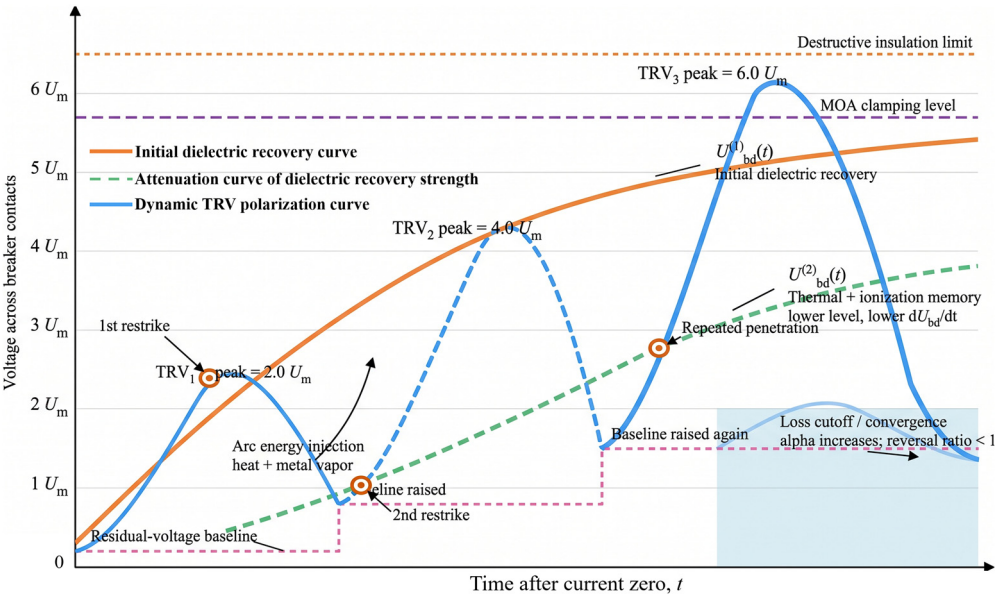


Figure 3. Competitive Attenuation Model between Dielectric Insulation Recovery Strength $V_{bd}(t)$ and Inter-electrode TRV.

In Figure 3, $V_{bd}{}^{(1)}$(t) represents the dielectric recovery curve during the initial interruption. After the occurrence of the initial restrike, the injection of substantial energy (heat and metal vapor) by the high-frequency arc causes the inter-contact dielectric recovery curve to shift downward and suffer slope attenuation, decaying to $V_{bd}{}^{(2)}$(t). The cascaded amplification does not proceed indefinitely; its termination is governed by one of three boundary conditions: (1) the inter-electrode voltage exceeds the withstand capability

of the circuit breaker interrupter, bushings, or capacitor terminal insulation, leading to dielectric breakdown or flashover damage; (2) metal-oxide arresters (MOAs) operate to absorb high-frequency energy and clamp overvoltage; or (3) as the voltage escalates, the increase in arc resistance R_{arc}, skin effect, and high-frequency resistive loop losses raises the damping coefficient α, reducing the high-frequency reversal ratio below unity and forcing the cascading process to converge.

3. Transient Process Simulation Based on a Wideband Model

To investigate the electromagnetic transient phenomena during the opening operation of capacitor bank circuit breakers and their impacts on breaking performance, numerical simulations of transient processes under various operating conditions were performed based on the transient model established above. Figure 4 depicts the developed transient simulation model of the 40.5 kV capacitor bank circuit breaker. This model incorporates the power source, circuit breaker, capacitor bank, and parasitic parameters. To guarantee reproducibility and model validity, the component parameter values of the three-phase electromagnetic transient equivalent circuit (Figure 4) were explicitly configured based on typical 40.5 kV distribution network benchmarks. The three-phase power source voltages (E_A, E_B, E_C) have a peak amplitude of 33.07 kV. The system short-circuit inductance is Lsys = 1.27 mH (corresponding to a 400 MVA short-circuit capacity), with an internal resistance R_{sys} = 0.05 Ω. Parasitic and stray components include a contact gap grading capacitance $C_{grading}$ = 100 pF, busbar-to-ground stray capacitance C_{bus_stray} = 10 nF, loop stray inductance L_{stray} = 15 μH, and high-frequency damping resistance $R_{damping}$ = 0.20 Ω. For each 6 Mvar capacitor bank, the phase effective capacitance is C_{effA} = C_{effB} = C_{effC} = 11.64 μF, paired with a 6% series reactor L_{series} = 26.83 mH.

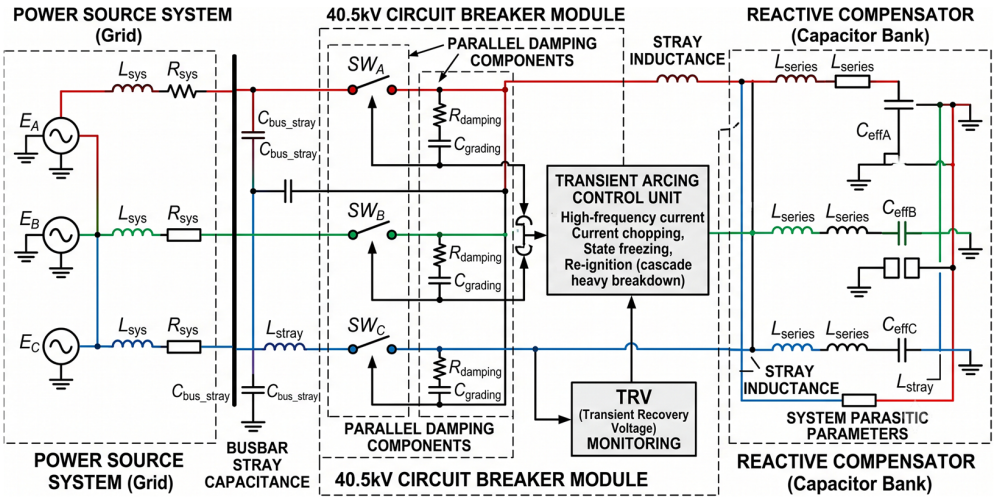


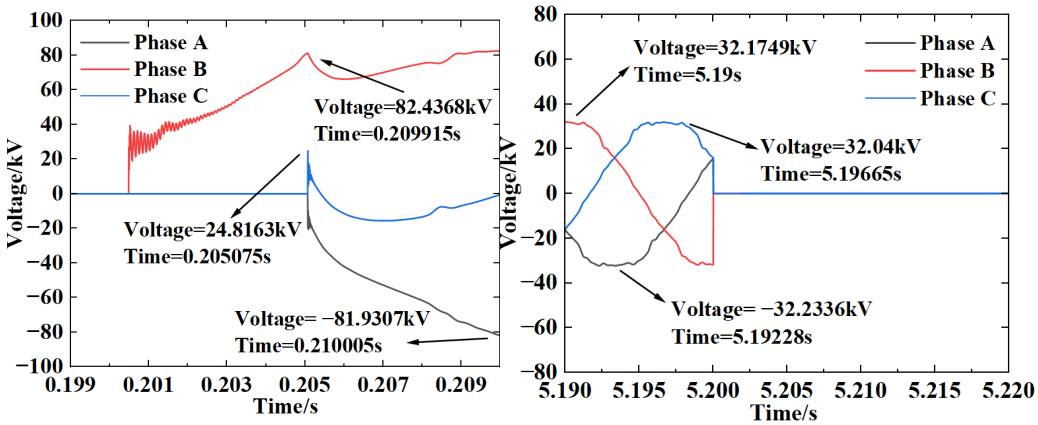
Figure 4. Three-phase Electromagnetic Transient Equivalent Circuit Model of the Capacitor Bank Circuit Breaker.

To investigate the opening and closing (switching) characteristics of the capacitor bank circuit breaker under various fault and non-ideal operating conditions, four capacitor bank configurations are established in the equivalent circuit simulation model. Simulation analyses are performed for the following four typical cases: (1) Capacitor Bank 1: Simulates the normal opening and closing operations of the circuit breaker, serving as the baseline case; (2) Capacitor Bank 2: Analyzes the impact of an inter-plate short-circuit fault within the capacitor on the switching operations; (3) Capacitor Bank 3: Investigates the transient effects induced by non-simultaneous (asynchronous) opening and closing operations;

(4) Capacitor Bank 4: Focuses on the condition of arc re-ignition occurring during breaker operations.

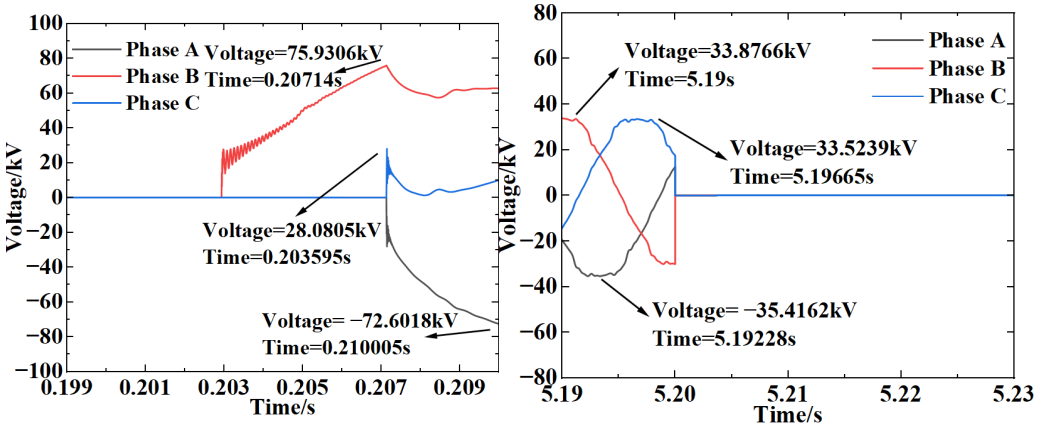
For Bank 1 (the baseline normal switching condition), a simultaneous (three-phase mechanically synchronized) switching scheme is implemented. During the closing operation, the contacts of all three phases are closed simultaneously at the same time instance. During the opening operation, although the mechanical contact separation is initiated simultaneously across all three phases, the arc extinction is governed by the 120° phase difference in the three-phase AC current. Specifically, the current in each phase is interrupted at its respective natural current zero crossing, meaning that the remaining two phases clear 60° electrical degrees (approximately 3.33 ms) after the first-pole-to-clear. This setup excludes mechanical scatter, providing a baseline for comparison with asynchronous switching (Bank 3).

To compare the actual instantaneous voltage stress sustained by the breaker contacts under different conditions, the node voltages on both sides of the interrupter at identical time instances are evaluated using the developed three-phase electromagnetic transient equivalent circuit model. Furthermore, the instantaneous differential voltage across the contact gap is calculated to accurately reflect the voltage stress imposed on the inter-contact insulation. Figures 5–7 present the analyzed transient voltages across the circuit breaker contacts for Capacitor Banks 1, 2, and 3, respectively, while Figure 8 depicts the corresponding results for Capacitor Bank 4.



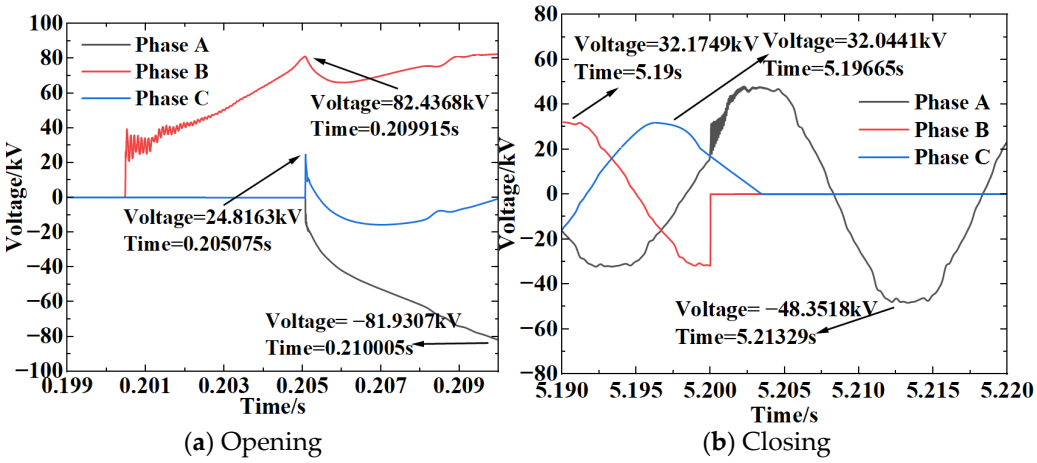
(**a**) Opening (**b**) Closing

Figure 5. Per-phase peak potential difference across the gap of capacitor bank circuit breaker No. 1.



(**a**) Opening (**b**) Closing

Figure 6. Per-phase peak potential difference across the gap of capacitor bank circuit breaker No. 2.



(**a**) Opening (**b**) Closing

Figure 7. Per-phase peak potential difference across the gap of capacitor bank circuit breaker No. 3.

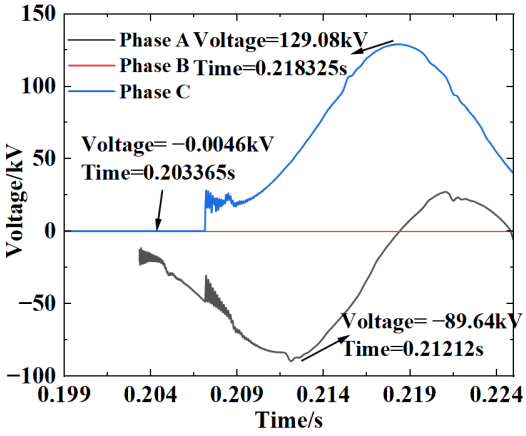


Figure 8. Per-phase peak potential difference across the gap of capacitor bank circuit breaker No. 4.

As revealed in Figures 5–7, under the first three operating conditions, the inter-contact differential voltage waveforms during the opening operation consistently exhibit high-frequency oscillations, with peak voltage differences occurring after the subsidence of these high-frequency oscillations. Regarding the closing operation, high-frequency oscillations in the differential voltage waveforms are negligible under the first two cases. However, under asynchronous switching conditions, a substantial potential difference can still develop across the contacts during closing, accompanied by high-frequency oscillations. The timing of the peak voltage difference under this condition aligns closely with that of the opening operation, with both being predominantly concentrated at the conclusion of the high-frequency transient phase.

Regarding the arc re-ignition case shown in Figure 8, the inter-contact differential voltage waveform similarly exhibits high-frequency oscillation characteristics. Comparative analysis reveals that the instantaneous differential voltage across the contact gap under various operating conditions reflects the actual voltage stress more accurately than measurements obtained from a single-sided monitoring node. Tables 2 and 3 present the inter-contact differential voltage results during the opening and closing operations, respectively, while Table 4 summarizes the corresponding results for Capacitor Bank 4 under the arc re-ignition condition.

Table 2. Inter-Contact Differential Voltages of Circuit Breakers for Capacitor Banks 1–3 During Opening Operation.

/	Group No.	Overvoltage (kV)
Phase A	Capacitor Bank 1	−81.9307
	Capacitor Bank 2	−72.6018
	Capacitor Bank 3	−81.9307
Phase B	Capacitor Bank 1	82.4368
	Capacitor Bank 2	75.9306
	Capacitor Bank 3	82.4368
Phase C	Capacitor Bank 1	24.8163
	Capacitor Bank 2	28.0805
	Capacitor Bank 3	24.8163

Table 3. Inter-Contact Differential Voltages of Circuit Breakers for Capacitor Banks 1–3 During Closing Operation.

/	Group No.	Overvoltage (kV)
Phase A	Capacitor Bank 1	−32.2336
	Capacitor Bank 2	−35.4162
	Capacitor Bank 3	−48.3518
Phase B	Capacitor Bank 1	32.1749
	Capacitor Bank 2	33.8766
	Capacitor Bank 3	32.1749
Phase C	Capacitor Bank 1	32.0441
	Capacitor Bank 2	33.5239
	Capacitor Bank 3	32.0441

Table 4. Inter-Contact Differential Voltages of Circuit Breaker for Capacitor Bank 4 During Arc Re-ignition Process.

/	Group No.	Overvoltage (kV)
Phase A	Capacitor Bank 4	−89.6367
Phase B	Capacitor Bank 4	−0.0046
Phase C	Capacitor Bank 4	129.0806

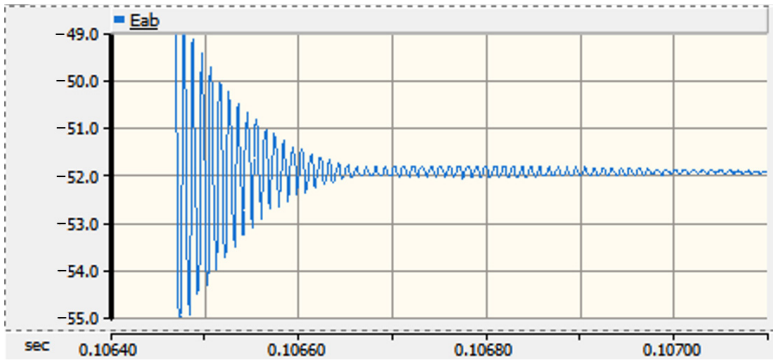
As indicated in Table 2, for the first three operating conditions, the maximum inter-contact differential voltage during the opening operation occurs in Phase B of the circuit breakers for Capacitor Banks 1 and 3, both peaking at 82.4368 kV, which establishes a substantial instantaneous potential difference across the contact gap. Waveform analysis reveals that this peak voltage difference primarily arises after the subsidence of high-frequency transient oscillations. This indicates that the abrupt mutation in system parameters, together with the rapid redistribution of electromagnetic energy at the instant of contact separation, are the primary drivers behind the significant surge in inter-contact differential voltage. Consequently, the opening operation represents one of the most critical stages regarding voltage stress on the breaker contacts, imposing stringent requirements on the inter-contact insulation performance.

As indicated in Table 3, a notable instantaneous differential voltage is also developed across the contact gap during the closing operation, with the peak magnitude reaching −48.3518 kV in Phase A of the circuit breaker for Capacitor Bank 3. Overall, the intensity of high-frequency oscillations during the closing operation is milder than that observed during the opening operation. As summarized in Table 4, during the arc re-ignition process of the circuit breaker for Capacitor Bank 4, the maximum inter-contact differential voltage occurs in Phase C, with a peak value of 129.0806 kV. Analysis reveals that arc re-ignition not only induces pronounced high-frequency oscillations but also causes the voltage across the contact gap to rapidly diverge again within a short duration, thereby generating a significantly higher differential voltage amplitude. Consequently, the inter-contact insulation faces much more severe challenges under the arc re-ignition condition, rendering it one of the key adverse factors compromising the safe operation of the circuit breaker.

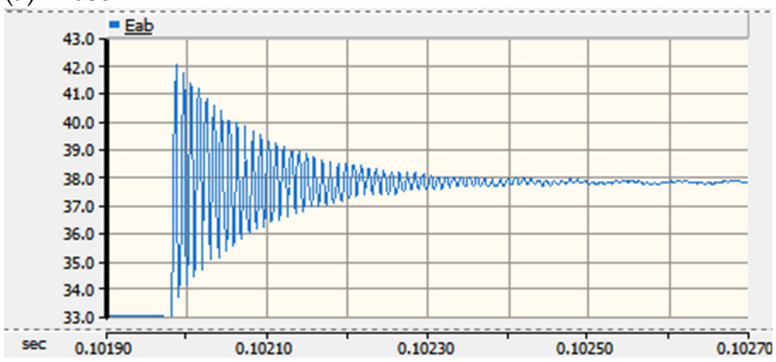
A deeper physical breakdown of the transient waveforms in Figures 5–8 and numerical results in Tables 2–4 reveals the underlying circuit and arc dynamics: (1) Opening Operation Phase Discrepancy: In Banks 1–3, Phase B exhibits the highest opening voltage difference across the gap (82.4368 kV). This is attributed to the first-pole-to-clear effect, where Phase B current reaches its zero crossing first. Upon interruption, Phase B traps a maximum residual DC voltage (+1.0U_m) on the capacitor side while shifting the system neutral point. Half a cycle later, as the busbar AC voltage swings to −1.0U_m, an extreme anti-phase voltage superposition occurs across the Phase B gap. (2) Closing Operation Phase Discrepancy: Closing overvoltage is governed by the closing phase angle. Phase A closes near the peak of the AC source voltage wave ($\psi \approx 90^\circ$), yielding the largest instantaneous mismatch $\Delta V = U_s - U_c$. In Bank 3 (asynchronous closing), contact scatter further synchronizes Phase A closure with the peak source voltage, amplifying the voltage difference peak to −48.3518. (3) Re-ignition Dynamics in Bank 4: During the re-ignition of Bank 4, a low-impedance high-frequency plasma arc column breaks down the Phase B contact gap. This conductive channel short-circuits the breaker terminals, causing the instantaneous voltage difference across Phase B to plunge to near zero (−0.0045 kV). However, this arc breakdown triggers massive high-frequency current oscillations that couple energy through the neutral point into Phase C. This parametric energy transfer escalates the Phase C capacitor voltage, resulting in a severe anti-phase voltage difference peak of 129.0806 kV across the Phase C interrupter gap.

Overall, assessing the inter-contact insulation risk based solely on single-sided voltage waveforms is prone to underestimating the actual stress sustained by the interrupter. The results indicate that the evaluation of inter-contact voltage stress should be grounded in the synchronized differential voltage between both sides at identical time instances, rather than a simplistic superposition of their individual voltage levels. Consequently, based on these findings, a combined AC–DC voltage test incorporating an AC voltage of −49.4861 kV and a DC voltage of +79.5945 kV is strongly recommended.

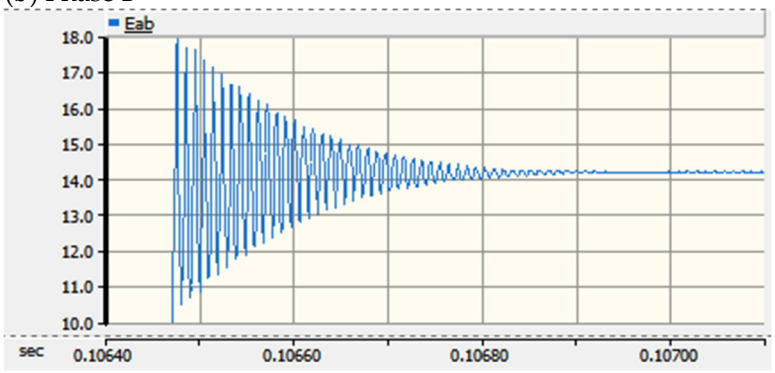
The high-frequency damped oscillation is excited by a local LC circuit formed by the small capacitance at the contact gap and the series reactor. Its peak value decreases from cycle to cycle, and the oscillation mainly exists within the first few hundred microseconds after the opening instant. The residual voltage plateau across the capacitor is determined by the coupling at the contact gap and the energy stored in the capacitor, while the high-resistance discharge resistor has a negligible effect during the short-duration transient. Comparison of the busbar-side, capacitor-side, and contact-gap voltages collectively reveals the overall characteristics of the opening transient. For ease of observation, the high-frequency damped oscillation characteristics here are taken from the three phases of the capacitor bank under the first basic operating condition. The decay waveforms are shown in Figure 9.



(**a**) Phase A



(**b**) Phase B



(**c**) Phase C

Figure 9. Partial View of Oscillation Decay.

During the opening transient, the voltage across the capacitor initially experiences a single abrupt jump at the instant of opening, followed by a local high-frequency oscillation that decays from cycle to cycle. When the oscillation amplitude decreases to a negligible level, the voltage stabilizes at a non-zero plateau, namely the residual voltage. Therefore, the residual voltage is not artificially set, but rather a stable plateau voltage naturally formed by contact-gap coupling, capacitor energy storage, and the opening transient conditions, making it one of the important characteristics of the opening transient. The presence of the residual voltage plateau is instructive for subsequent switching operations and equipment safety, and it also serves as an important basis for the analysis and theoretical validation of the opening transient. As this is a partial view, extending the simulation time allows observation of the residual voltage decaying to a stable value and then continuing to decrease to zero through the discharge resistor.

To quantitatively evaluate the impact of mechanical contact scatter on interrupter insulation stress, a parametric sensitivity sweep was conducted based on the baseline asynchronous condition of Bank 3, yielding the results shown in Figure 9. The simulation conditions for Figure 9 are defined as follows: the circuit parameters match those in Figure 4,

with Phase A contact movement set as the reference ($t_A = t_0$), while the contact delays for Phase B and Phase C (Δt) are continuously swept from −5 ms to +5 ms. A clear physical and logical relationship exists between Figures 7 and 9: Figure 7 provides a single-point time-domain snapshot at a representative delay (e.g., Δt = 2.0 ms, where Phase A closing peak reaches −48.3518 kV), whereas Figure 9 maps the continuous envelope of peak gap voltage stress across the entire delay range. The results indicate that the global maximum overvoltage in Figure 9 occurs when the asynchronous delay forces contact touching to coincide precisely with the AC source voltage peak ($\psi = 90°$). Thus, Figure 9 generalizes the transient behavior captured in Figure 7 and establishes a quantitative criterion for the allowable mechanical synchronization threshold ($\Delta t < 1.5$ ms).

4. Investigation of Internal Electric Field Within Circuit Breakers Under Combined AC–DC Stress

The preceding section analyzed the transient behavior of a 40.5 kV class circuit breaker under capacitor bank switching operations. Traditional AC withstand voltage tests merely reflect the capacitive electric field distribution dominated by dielectric permittivity. However, during actual interruption transients, the DC voltage component on the capacitor side induces carrier migration and space charge accumulation within the insulating media (e.g., the ceramic/epoxy outer insulation surfaces of vacuum interrupters or SF_6 gas gaps). To ensure physical rigor in modeling microscopic dielectric recovery and re-ignition breakdown, the AC and DC voltage components applied in Section 3 are directly derived from the worst-case transient conditions during capacitor bank switching analyzed in Section 2. As calculated from the system transients, the most severe electrical stress across the interrupter gap occurs during the arc re-ignition phase, where the two contacts experience opposing voltage polarities. At this instant, the bus-side (source-side) voltage reaches an AC instantaneous value of −49.4861 kV, while the capacitor-side voltage reaches a DC component of +79.5945 kV. Consequently, the maximum instantaneous potential difference across the gap reaches 129.0806 kV, which exceeds the standard 1 min power-frequency withstand voltage test rating of the interrupter gap (118 kV). Based on these worst-case transient results, the Section 3 microscopic simulation applies boundary conditions of +79.5945 kV at the capacitor-side contact and −49.4861 kV at the bus-side contact. This explicit mapping accounts for the severe space-charge distortion under reverse polarity and provides a physical foundation for recommending an AC (−49.4861 kV) and DC (+79.5945 kV) combined voltage test to evaluate the dielectric integrity of vacuum interrupters under heavy capacitor-switching duty. The electric field distribution within the insulating media is governed by Poisson's equation and the charge continuity equation [28]:

$$\nabla \cdot (\varepsilon \nabla E) = \rho \tag{11}$$

$$\frac{\partial \rho}{\partial t} + \nabla \cdot J = 0 \tag{12}$$

$$J = \mu \rho E - D \nabla \rho \tag{13}$$

where ρ is the space charge density, J is the current density, μ is the carrier mobility, and D is the diffusion coefficient.

Under a superimposed AC–DC electric field, the DC voltage component drives ion migration and accumulation toward opposite-polarity electrodes or the gas–solid interface (dominated by the conductivity σ), whereas the AC component continuously alters the polarization direction. This nonlinear superposition induces severe local electric field distortion, which readily triggers micro-discharges across the breaker contact gap or along the insulating surface, eventually escalating into breakdown. Figure 10 illustrates the

charge distribution evolution and the associated electric field distortion under such a composite field. Figure 10b depicts the capacitive, uniform electric field distribution under pure AC excitation, whereas Figure 10c presents the electric field distribution after half a cycle of combined AC–DC superposition. It is clearly observed that the interfacial charge accumulation induced by the DC residual voltage elevates the peak local electric field strength at the cathode triple junction by approximately 35%. The substantial increase in the electric field here is attributed to the physical superposition of the peak applied voltage introduced by the DC bias, which simultaneously disrupts the charge dissipation equilibrium of the AC field. Driven by continuous unidirectional charge injection and the conductivity/permittivity mismatch at the gas–solid interface, high-density space and interface charges accumulate. Consequently, the profound superposition of the self-built electric field and the geometric electric field jointly leads to severe distortion and multiplication of the local electric field.

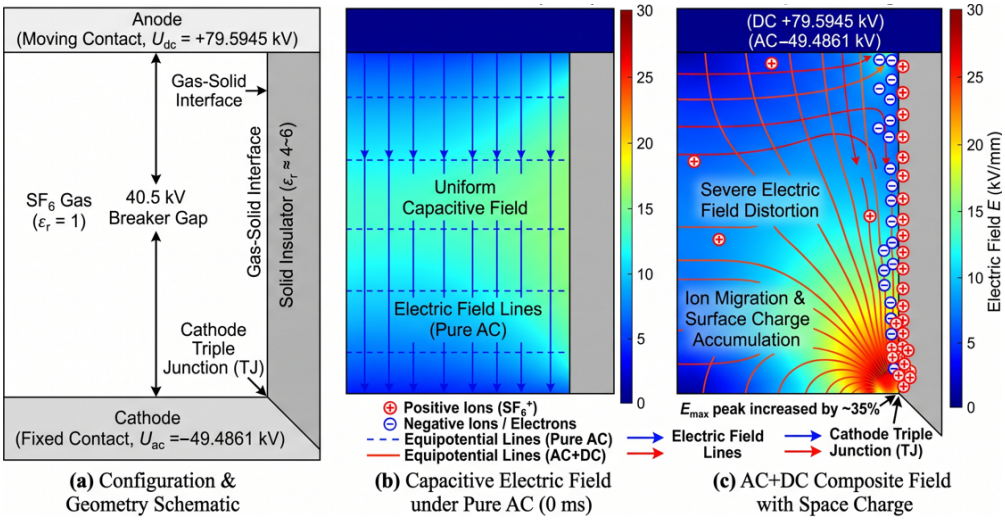


Figure 10. Space charge distribution and electric field distortion across the circuit breaker inter-contact gap and gas–solid interface under combined AC–DC voltage.

To gain deeper insight into the microscopic impact of combined AC–DC stress on the inter-contact insulation of high-voltage (HV) circuit breakers, numerical simulations were performed to evaluate the electric field and space charge distributions in the presence of micro-protrusion insulation defects; the results are depicted in Figure 11. As observed in Figure 11, the electric field between the HV breaker contacts under pure AC stress exhibits uniform field lines. Conversely, under combined AC–DC stress—particularly near the contact on the DC residual voltage side—the directional migration and accumulation of space charge induce a sharp local intensification of the electric field strength, giving rise to localized high-field regions, especially around the micro-protrusion. This reveals the underlying damage mechanism of the combined stress from a microscopic perspective. To explicitly clarify the localized space charge effect, the "DC residual voltage side" specifically corresponds to the capacitor-bank-side contact. Upon capacitor bank de-energization, this contact retains a high negative DC residual voltage (e.g., $U_{dc} \approx -1.0$ p.u., corresponding to approximately -33.07 kV), while the source-side contact experiences the sinusoidal AC system voltage $u_s(t)$. Consequently, the total voltage stress across the interrupter gap becomes $u_{gap}(t) = u_s(t) - U_{dc}$, reaching up to 2.0 p.u. during the worst-case half-cycle. The capacitor-bank-side contact exhibits significantly stronger space charge accumulation and electric field distortion due to the following mechanism: under the persistent negative DC bias, this contact continuously functions as the post-arc cathode. High-mobility free electrons evacuate rapidly toward the source-side contact (post-arc anode), whereas heavy

copper ions (Cu^+) are electrostatically attracted to and trapped near the capacitor-side contact surface, forming a dense positive ion sheath ($n_i \gg n_e$). This net positive space charge accumulation, coupled with the high negative potential, severely compresses the potential gradient and intensifies the localized surface electric field at the capacitor-side contact, making it the primary site for dielectric breakdown and arc re-ignition.

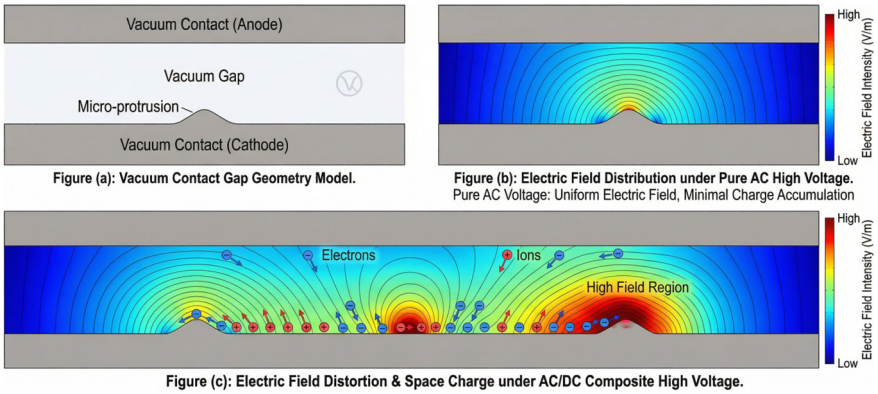


Figure 11. Space charge distribution and electric field distortion at a micro-protrusion insulation defect under combined AC–DC voltage.

Figure 11c qualitatively depicts the spatial and temporal distribution dynamics of charged species during the post-arc dielectric recovery and breakdown processes. The physical species in the simulation are explicitly identified as copper ions (dominated by Cu^+, with a minor fraction of Cu^{2+}) resulting from CuCr50 contact vapor, and free electrons (e^-), represented by the ion density n_i and electron density n_e, respectively. A qualitative physical analysis of the species evolution reveals three main phases: (1) Initial Quasi-Neutral Phase: At current zero, the residual plasma in the interrupter gap maintains a quasi-neutral state, with ions and electrons distributed uniformly and exhibiting balanced densities ($n_i \approx n_e$). (2) Sheath Expansion and Charge Separation Phase: As the transient recovery voltage (TRV) builds up, the high-mobility free electrons (e^-) rapidly evacuate toward the post-arc anode under the reverse electric field. This causes a drastic depletion of electron quantity and density near the post-arc cathode. In contrast, heavy copper ions (Cu^+) lag behind due to their high inertia, forming a dense positive ion sheath near the cathode. This significant spatial charge separation ($n_i \gg n_e$) concentrates the electric field inside the thin cathode sheath. (3) Re-ignition Avalanche Phase: The intense electric field distortion inside the ion sheath triggers field electron emission and subsequent impact ionization avalanches, causing an exponential surge in local electron density near the cathode, which re-establishes a highly conductive arc channel and leads to dielectric re-ignition. Sustained unipolar DC bias prevents the effective recombination of free charges on the contact surface or within the solid insulating medium; instead, these charges accumulate along a preferential direction, forming a stable space charge layer. These space charge layers severely distort the macroscopic electric field distribution across the inter-contact gap. Particularly at contact micro-protrusions or dielectric surface defects, such field distortion can trigger field emission, compromise the local breakdown strength, and potentially accelerate thermal degradation of the insulation. Crucially, this phenomenon cannot be adequately captured or excited under conventional pure AC withstand testing.

5. Insulation Stress Analysis of Equipment and Limitations of Existing Test Methods

During the frequent switching operations of 40.5 kV reactive power compensation capacitor banks, circuit breakers and associated capacitive and inductive equipment are

subjected not only to the impacts of macroscopic overvoltage magnitudes, but also to severe cumulative degradation of insulating media caused by microscopic, high-frequency electromagnetic transients. To accurately evaluate such engineering hazards, this section analyzes the spatial distribution characteristics of broadband transient stress, exposes the underlying limitations of existing international and national standards in insulation equivalence testing, and accordingly proposes a novel insulation evaluation method that aligns more closely with realistic operational boundaries. Furthermore, based on the transient physical evolution mechanisms across the inter-contact gap, targeted comprehensive mitigation strategies are proposed and evaluated across three dimensions: macroscopic passive protection, structural optimization of the breaker body, and cutting-edge active controlled switching technologies.

5.1. Transient Stress Distribution Characteristics and High-Frequency Gradient Concentration Effect

Under power-frequency (50 Hz) steady-state conditions, the internal electric field distribution within series reactor windings and multi-element series shunt capacitor banks is primarily governed by equivalent inductances or series capacitances, exhibiting a linearly uniform profile. However, during high-frequency transient processes (10 kHz–1 MHz) excited by circuit breaker closing inrush currents or opening restrikes, the parasitic distributed capacitance network comes to dominate the electric field distribution, giving rise to a severe concentration of high-frequency voltage gradients.

The internal longitudinal structure of the equipment (such as inter-turn insulation of series reactor windings or series element chains of capacitors) is modeled as an equivalent distributed parasitic capacitive–inductive ladder network, as illustrated in Figure 12a. Let L_0 denote the unit physical inductance, R_0 the high-frequency high-order skin-effect resistance, C_s the longitudinal series parasitic capacitance (inter-turn/inter-layer capacitance of windings or series capacitance between capacitor elements), and C_g the transverse parasitic capacitance from each node to ground or the enclosure. At the initial instant $t \to 0^+$ upon the impact of a high-steepness transient wavefront ($\mathrm{d}u/\mathrm{d}t > 50$ kV/μs) induced by a restrike, the inductive reactance $Z_L = \omega L_0 \to \infty$ renders the inductance L_0 effectively an open circuit. Consequently, the circuit potential distribution is governed entirely by the capacitance network formed by C_s and C_g. Defining the normalized axial position of the equipment as $x \in [0, 1]$ (where $x = 0$ corresponds to the transient impact terminal and $x = 1$ to the distal end), the spatial potential distribution along the axial direction in the complex frequency domain (ss-domain) satisfies the following linear partial differential equation [29]:

$$\frac{\partial^2 U(x,s)}{\partial x^2} - \gamma^2(s) U(x,s) = 0 \tag{14}$$

where the propagation coefficient $\gamma(s)$ is expressed as

$$\gamma(s) = \sqrt{\frac{sC_g \cdot (sC_s + \frac{1}{R_0 + sL_0})}{sC_s \cdot \frac{1}{R_0 + sL_0} + 1}} \tag{15}$$

Under the high-frequency limit ($\omega \to \infty$), the asymptotic expression simplifies to

$$\alpha = \lim_{s \to \infty} \gamma(s) = \sqrt{\frac{C_g}{C_s}} \tag{16}$$

Analytically solving this boundary value problem (with the line-end boundary condition $u(0) = U_{\text{in}}$ and the grounded terminal boundary condition $u(1) = 0$) yields the spatial potential distribution function:

$$u(x) = U_{in} \cdot \frac{\sin h(\alpha(1-x))}{\sin h(\alpha)} \tag{17}$$

Taking the negative spatial derivative with respect to x yields the distribution of the axial local electric field intensity $E(x)$:

$$E(x) = -\frac{\partial u(x)}{\partial x} = U_{in} \cdot \frac{\cos h(\alpha(1-x))}{\sin h(\alpha)} \tag{18}$$

The line-end local electric field concentration factor K_E is defined as the ratio of the line-end electric field to the uniformly distributed electric field:

$$K_E = \left.\frac{E(x)}{U_{in}}\right|_{x=0} = \alpha \cot h(\alpha) \tag{19}$$

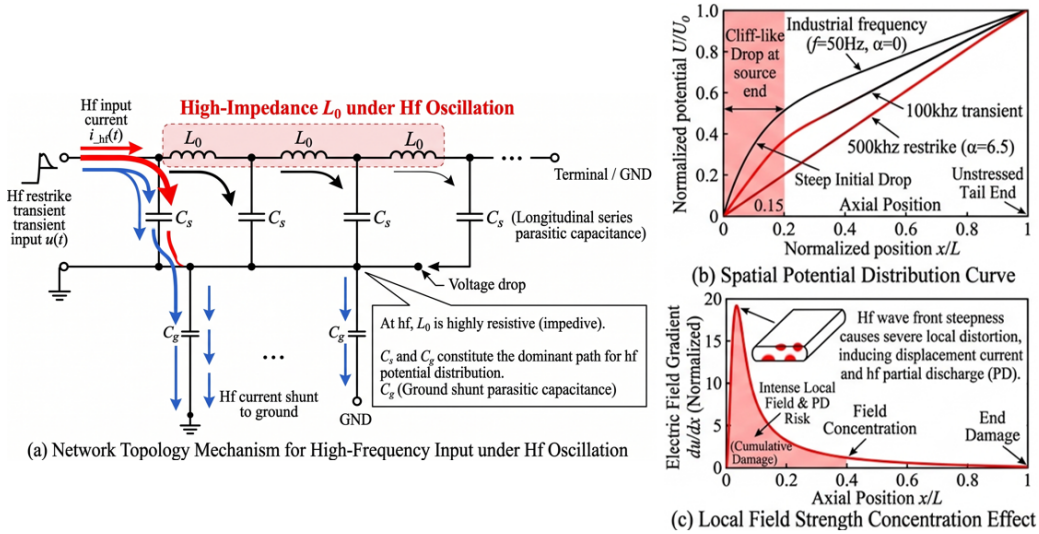


Figure 12. Distribution topology of high-frequency transient waves within the equipment and the longitudinal gradient concentration effect.

Based on the above derivation, the spatial electric field distribution exhibits strong frequency dependence:

(1) Power-frequency/low-frequency limit ($\alpha \to 0$):

$$\lim_{\alpha \to 0} u(x) = U_{in}(1-x), \lim_{\alpha \to 0} E(x) = U_{in} \tag{20}$$

The potential decreases linearly along the axial direction, resulting in a uniform axial electric field intensity everywhere, with $K_E = 1$.

(2) High-frequency restrike transient limit ($\alpha \gg 1$): To accurately determine the parameter values for the distributed capacitance-inductance ladder network model, the distributed capacitances of a physical 40.5 kV series reactor winding were measured using a high-precision LCR meter (Keysight E4980A) at 100 kHz. The detailed measurement procedure and derived parameters are as follows: (1) Ground Capacitance (C_g): With the line and neutral terminals short-circuited together, the total capacitance between the winding and the grounded structural frame was measured, yielding C_g

= 4.32 nF (varying between 3.2 and 6.4 nF across samples). (2) Series Capacitance (C_s): Using a three-terminal guarded measurement setup to eliminate ground stray effects, the inter-turn/inter-layer series capacitance across the winding terminals was measured as C_s = 120 pF (varying between 100 and 200 pF).

The initial voltage distribution factor α is defined as $\alpha = C_g/C_s$. Substituting the measured parameters yields the baseline value:

$$\alpha = \sqrt{\frac{4.32\text{nF}}{120\text{pF}}} = 6 \tag{21}$$

Accounting for structural tolerances and frequency dependence (Cg/Cs ratio ranging from 16 to 64), α varies between 4 and 8, with α = 6 selected as the representative baseline parameter. This parameter rigorously quantifies the localized electric field concentration near the line-side turns under fast voltage transients. In this case, over 75% of the total transient surge magnitude is concentrated within an extremely narrow region near the line end ($x \in [0, 0.15]$).

At the microscopic level, the high-frequency gradient concentration effect leads to irreversible degradation of the insulation medium through the following physical mechanisms [30]:

(1) Displacement Current Thermal Effect

According to Maxwell's equations, a high du/dt induces a high displacement current density J_d inside the line-end insulation medium:

$$J_d = \frac{\partial D}{\partial t} = \varepsilon_0 \varepsilon_r \frac{\partial E(x,t)}{\partial t} \tag{22}$$

As the high-frequency displacement current passes through the dielectric medium with a loss tangent tanδ, the resulting volumetric heating power density p_v is given by

$$p_v = \omega \varepsilon_0 \varepsilon_r \tan\delta \cdot E^2(x) \tag{23}$$

At an oscillation frequency of 500 kHz, the localized volumetric heating power of the line-end dielectric increases dramatically by 10^4 times compared to that under power frequency, triggering localized thermal breakdown or hot-spot degradation.

(2) High-Frequency Partial Discharge (HF-PD) and Electrical Treeing

When the line-end local electric field intensity exceeds the gas ionization threshold field strength E_{ion} within micro-voids inside the dielectric medium, high-frequency partial discharge occurs. Under high frequencies, the PD repetition rate is extremely high; the resulting electron bombardment and energetic ions sever the polymer backbone chains, forming electrical treeing channels that progressively erode the main insulation.

To visually demonstrate the severe distortion of the internal potential drop and the concentration effect of the line-end electric field gradient under high-frequency oscillatory surges, Figure 12 presents the ladder network topology, the spatial potential distribution curves $u(x)$ under different α parameters, and a spatial comparison of the local electric field gradient du/dx.

As depicted in Figure 12, upon high-frequency restrike transient input, the inductance L_0 exhibits high impedance, while the longitudinal capacitance C_s and transverse capacitance to ground C_g form a capacitive potential divider network. A substantial portion of the high-frequency current is shunted to ground through C_g, causing a sharp reduction in current along the propagation direction. Under power-frequency steady-state conditions,

the potential decreases linearly along the axial direction (α = 0). As the restrike oscillation frequency increases to 500 kHz, α rises to 6.5, causing the potential curve to drop precipitously near the line end (x = 0∼0.15), while the distal-end insulation experiences negligible voltage stress. Concurrently, the high-steepness wavefront surge induced by restrikes generates intense displacement currents and high-frequency partial discharges within the line-end insulation medium, culminating in severe cumulative electro-thermal degradation of the line-end insulation.

5.2. Analysis on Equivalence Limitations of Existing Insulation Testing Standards

Currently, insulation type tests for 40.5 kV switchgear and capacitor banks primarily rely on IEC 62271-100 (high-voltage circuit breakers), GB/T 1984, and GB/T 11024 (shunt capacitors). However, these standards are established within the framework of conventional power-frequency switching and standardized lightning/switching impulse voltages, failing to cover composite insulation stresses under frequent switching transients [31].

(1) Analysis of Biased Electric Field and Space Charge Accumulation Effects

Following the opening of the capacitor bank, the residual charge on the capacitor side maintains a DC voltage $U_{\mathrm{dc}} \approx \pm 1.0 U_m$, whereas the busbar side experiences an AC voltage $u_{ac}(t) = U_m \cos(\omega_0 t)$. The composite voltage across the breaker gap is expressed as:

$$u_{gap}(t) = U_m \cos(\omega_0 t) \mp U_m \tag{24}$$

This voltage exhibits a 100% DC bias characteristic. Under prolonged DC-biased electric fields, severe space charge accumulation occurs inside solid insulation (such as epoxy resin operating rods, basin-type insulators, and insulation rod surfaces) and at dielectric interfaces. The space charge evolution satisfies the one-dimensional drift-diffusion equation [28]:

$$\frac{\partial \rho_v(x,t)}{\partial t} + \frac{\partial}{\partial x}\left(\mu(E)\rho_v(x,t)E(x,t) - D_d \frac{\partial \rho_v(x,t)}{\partial x}\right) = s(x,t) \tag{25}$$

coupled with Poisson's equation:

$$\frac{\partial E(x,t)}{\partial x} = \frac{\rho_v(x,t)}{\varepsilon_0 \varepsilon_r} \tag{26}$$

where μ is the carrier mobility, D_d is the diffusion coefficient, and s is the injection source term.

When a restrike occurs at the instant of the reverse AC voltage peak, the applied electric field reverses instantaneously. However, the accumulated homocharge cannot dissipate immediately due to its large dissipation time constant ($\tau_d = \varepsilon/\sigma \gg 10$ s). Consequently, the electric field generated by the resulting heterocharge superimposes constructively with the applied reverse transient electric field, escalating the local electric field distortion factor K_{sc} of the dielectric up to

$$E_{local,max} = E_{applied} + E_{space_charge} = K_{SC} E_{applied} (K_{SC} \approx 1.4 \sim 1.8) \tag{27}$$

This process directly triggers surface flashover at the solid–gas interface or internal dielectric breakdown. Standard power-frequency withstand voltage tests, owing to their rapid voltage alternation (10 ms per half-cycle), fail to establish the physical process of space charge accumulation.

(2) Dielectric Relaxation Loss and Debye Polarization Lag

During rapid polarity reversals under high-frequency restrikes (10 kHz–100 kHz), the orientational polarization of dipoles within the dielectric medium fails to keep pace with the alternating electric field, giving rise to Debye relaxation lag. The imaginary part $\varepsilon''(\omega)$ of the complex permittivity $\varepsilon^*(\omega) = \varepsilon'(\omega) - j\varepsilon''(\omega)$ reaches its peak within this frequency band [32]:

$$\varepsilon''(\omega) = (\varepsilon_s - \varepsilon_\infty)\frac{\omega\tau_{relax}}{1 + (\omega\tau_{relax})^2} \tag{28}$$

where τ_{relax} denotes the dipole relaxation time. This relaxation hysteresis causes substantial electric field energy to be converted into internal thermal energy within the dielectric, inducing a rapid temperature rise in the insulating medium and severe degradation of the dielectric dissipation factor (tanδ). Standard power-frequency tests are inherently incapable of evaluating such high-frequency polarity-reversal losses.

To delineate the disparity between traditional type tests and actual transient stresses during capacitor bank switching operations, Figure 13 presents a comparative diagram featuring the IEC standard power-frequency withstand voltage waveform, the standard lightning impulse waveform, and the actual composite stress waveform characterized by a "DC residual voltage bias coupled with high-frequency restrike cascades."

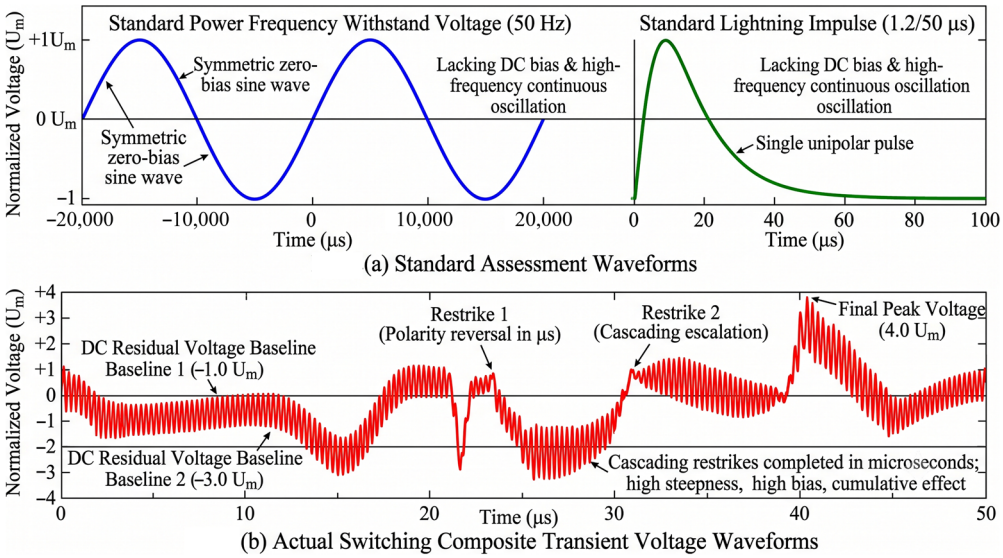


Figure 13. Comparison between standard insulation testing waveforms and actual switching composite transient voltage waveforms.

As shown in Figure 13, the power-frequency withstand voltage is a symmetrical zero-biased sinusoidal wave, whereas the standard lightning impulse (1.2/50 μs) is a single unidirectional impulse. Neither of these standard waveforms incorporates DC bias components or high-frequency continuous oscillatory dynamics. In contrast, the actual switching composite transient voltage waveform undergoes severe oscillations centered around the DC residual voltage baseline ($-1.0U_m$, $-3.0U_m$). Restrikes accomplish full polarity reversals within a few microseconds, driving the peak voltage across the breaker gap up to $4.0U_m$. This highlights the harsh insulation environment in field engineering, characterized by high wavefront steepness, elevated DC bias, and continuous cascading transients.

5.3. Novel Insulation Testing Method Based on Combined AC–DC Withstand Voltage

To overcome the limitation of conventional static tests in equivalently evaluating high-frequency transient composite stresses, this paper proposes a novel combined AC–DC withstand voltage testing method based on a dual-independent-source coupling architecture. This method precisely reproduces the most severe asymmetric electrical boundary

conditions across the breaker gap during capacitive load de-energization transients, as illustrated in Figure 14.

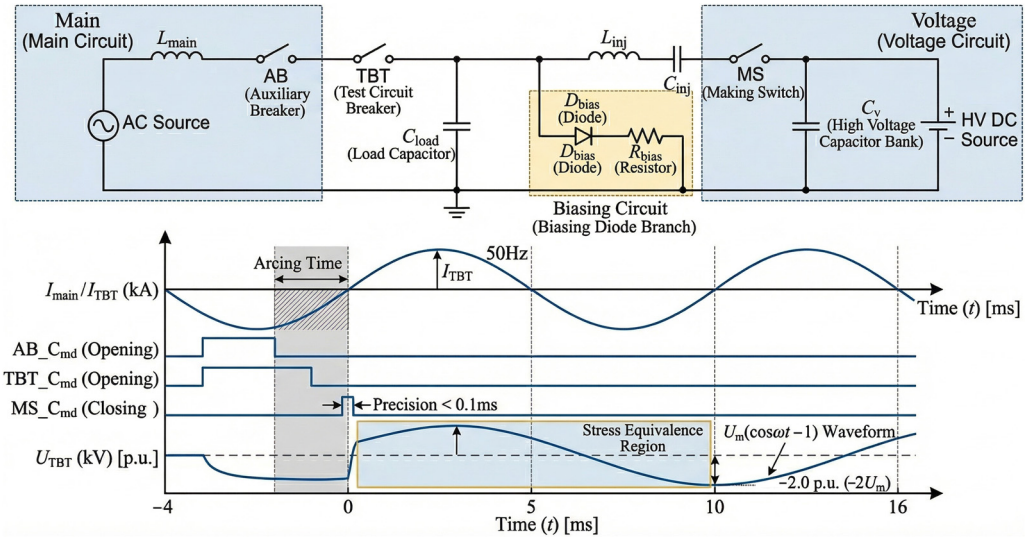


Figure 14. Schematic diagram of the proposed combined AC–DC withstand voltage testing system.

As shown in Figure 14, the energy input to the entire system is supplied by independent AC and DC test power sources. These two power supply channels are jointly connected to a core combined AC–DC voltage generator, which precisely superimposes the AC and DC high voltages according to specific timing sequences and waveforms. This accurately replicates the extremely severe "AC + DC" composite overvoltage conditions experienced across the circuit breaker contacts during the interruption of a capacitor bank with residual charges. The synthesized high voltage is directly applied to the 40.5 kV circuit breaker under test (BUT) and its downstream simulated capacitor bank load for insulation withstand testing. During the testing process, a high-voltage divider connected in parallel safely and proportionally steps down the high-voltage signals, transmitting them to the measurement system for high-precision waveform and data acquisition. Concurrently, serving as the system's central brain, the control and data acquisition unit not only receives and processes these real-time measurement data to assess the insulation state of the circuit breaker, but also issues precise synchronized triggering and action control commands to the AC/DC generators as well as the breaker under test. This establishes a highly automated, data-closed-loop, advanced high-voltage insulation evaluation platform.

6. Experimental Validation

To quantitatively evaluate the equivalence of the proposed test scheme (50 Hz AC at −49.4861 kV combined with DC at +79.5945 kV) against actual capacitor switching re-ignition transients, this paper quantitatively compares the key characteristic physical parameters of the two waveforms. The specific comparison results are as follows: (1) Reproduced Aspects: The proposed combined test accurately reproduces the maximum peak gap voltage stress of 129.0806 kV (exceeding the 1 min power-frequency withstand rating of 118 kV) and the worst-case opposite-polarity configuration. Consequently, key physical phenomena—such as positive ion sheath compression, intense space-charge distortion, and localized electric field enhancement—are fully captured. (2) Non-Reproduced Aspects and Justification: Actual re-ignition transients involve steep wavefronts (dv/dt > 10 kV/μs) and high-frequency oscillations (10^2 kHz–MHz), which are omitted in the 50 Hz AC + DC test waveform. However, by substituting microsecond-scale high-frequency surges with a longer millisecond-scale duration at peak stress (129.08 kV), the proposed 50 Hz AC + DC

test imposes a more conservative and stringent dielectric challenge on the interrupter. Furthermore, this method offers superior laboratory reproducibility and implementation feasibility compared to ultra-fast impulse test setups.

To precisely apply phase-controlled superimposed AC–DC voltages across both sides of the circuit breaker gap, an experimental circuit for the combined AC–DC withstand voltage test was established, as shown in Figure 15. The breaker under test (BUT) remains in the open position. Side A of the breaker gap is subjected to a power-frequency AC peak voltage $u_{ac}(t) = U_{ac_m}\sin(\omega t)$, while Side B is applied with a residual DC bias voltage U_{dc} preset by the capacitor bank. The resultant composite spatial voltage stress u_{total} (t) experienced across the gap is expressed as

$$u_{total}\ (t) = u_{ac}\ (t) - u_{dc} = u_{ac_m}\sin(\omega t) - u_{dc} \tag{29}$$

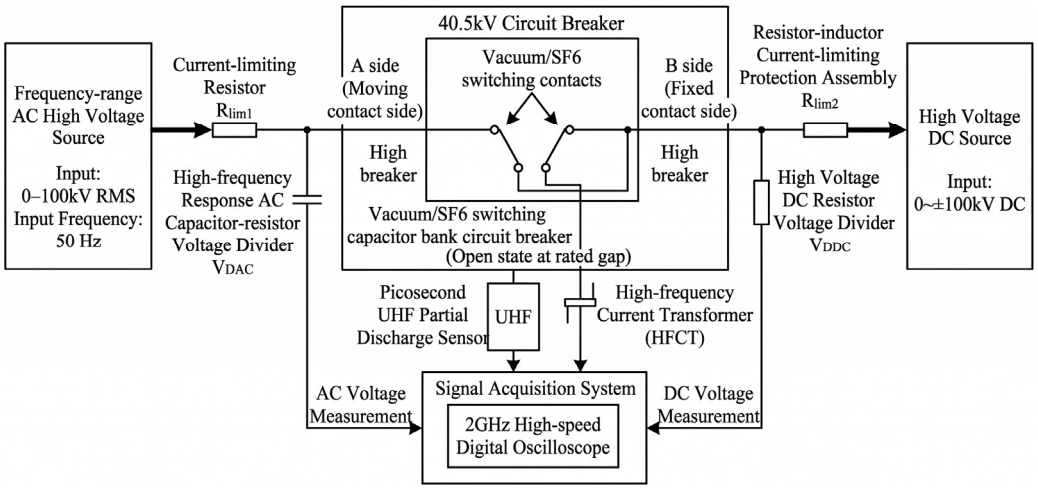


Figure 15. Topology and measurement principle of the combined AC–DC withstand voltage test for the 40.5 kV circuit breaker.

When the AC voltage reaches its negative half-cycle peak $-u_{ac_m}$ and the DC voltage exhibits a positive polarity $+u_{dc}$, the maximum reverse superimposed peak voltage u_{peak} across the gap escalates to

$$u_{peak} = |u_{ac_m}| + |u_{dc}| \tag{30}$$

For a 40.5 kV system, based on the aforementioned investigation, the standard peak value for the combined AC–DC withstand voltage test is specified as 129.1 kV (corresponding to 3.0 p.u. of the system phase-voltage peak), with a continuous withstand duration of 1 min or an application of 50 half-cycle polarity-reversal impulses. Inside the shielded high-voltage and high-power test hall, three representative test cases were conducted on a 40.5 kV vacuum circuit breaker (equipped with a ceramic vacuum interrupter and a polymer composite insulating pull-rod), successfully capturing detailed experimental waveforms and discharge characteristics.

(1) Case 1: Combined AC–DC Withstand Test on a Qualified Circuit Breaker (Successful Withstand Waveform)

An AC voltage of u_{ac} = 35.0 kV RMS (peak value of 49.5 kV) was applied to Side A of the breaker gap, while a DC bias voltage of u_{dc} = +79.6 was applied to Side B. Consequently, the maximum composite peak voltage across the gap reached 129.1 kV, which was sustained for a duration of 60 s. The experimental results are shown in Figure 16.

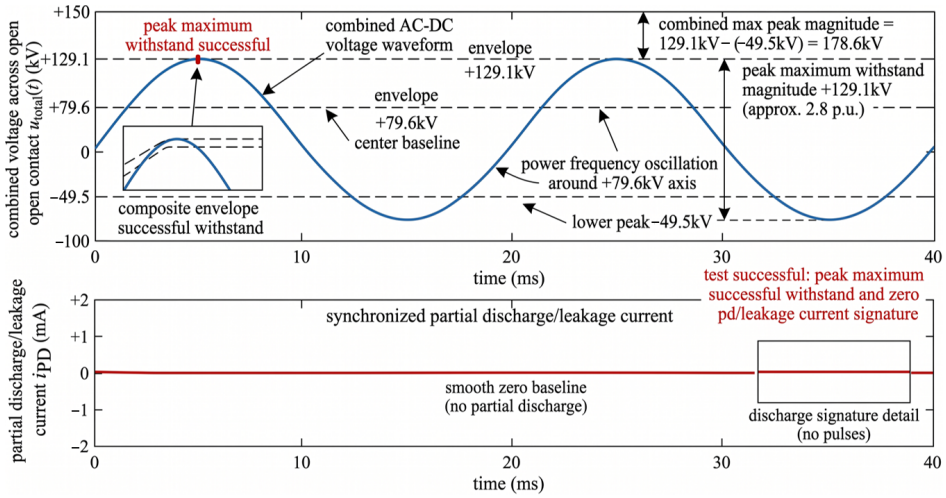


Figure 16. Combined AC–DC withstand voltage test waveforms of a qualified 40.5 kV circuit breaker.

Under the 129.1 kV combined AC–DC voltage, the electric field distribution within the breaker gap transitions from a capacitive electric field (governed by the relative permittivity ε_r) to a steady-state resistive electric field (governed by the volume resistivity ρ of the dielectric). Owing to the absence of microscopic void defects within the insulation media of the test specimen (including the vacuum interrupter contacts, ceramic envelope, and composite pull-rod), as well as the fine surface polishing treatment applied to the electrodes to suppress local field concentration, the maximum local electric field intensity remained strictly below the critical threshold for field emission ($E_{max} < 10$ kV/mm).

No inter-electrode micro-discharges were triggered throughout the test, with the measured partial discharge (PD) magnitude remaining below 5 pC. This demonstrates that the metallic contact materials inside the vacuum interrupter and the external composite pull-rod of the 40.5 kV circuit breaker fully satisfy the stringent insulation withstand requirements under severe restrike conditions.

(2) Case 2: Surface Flashover of the Insulating Pull-Rod (Flashover Waveforms During the AC–DC Superimposed Polarity-Reversal Phase)

Under identical combined voltage stress, a composite insulating pull-rod specimen subject to surface salt-contamination and moisture-ingress defects was evaluated. At t = 32.4 s into the test, an external surface insulation flashover occurred across the breaker gap. The AC–DC voltage waveforms and partial discharge (PD) current pulses at the instant of surface flashover along the composite insulating pull-rod are illustrated in Figure 17.

As depicted in Figure 17, a steep discharge arc pulse with a peak current reaching 185 A was generated at t = 32.4 s. It can be observed from Figure 17 that during the polarity reversal of the combined AC–DC voltage, the electric field distribution both within the dielectric volume and along its surface undergoes severe transient redistribution. Specifically, the high DC voltage injects charges onto the surface of the moist, contaminated pull-rod, resulting in space charge accumulation. When the AC voltage enters its negative half-cycle, the high-amplitude reverse AC electric field superimposes constructively with the field generated by the accumulated residual space charges, leading to extreme electric field distortion at both ends of the pull-rod. Concurrently, Joule heating produced by localized leakage currents evaporates the surface water film, giving rise to a “dry band.” This dry band sustains the vast majority of the combined AC–DC potential difference, thereby triggering localized dry-band corona discharges. These corona discharges rapidly propagate along the wet-polluted channel enriched with high-density ions, evolving into thermal sparks and ultimately causing a full-surface AC–DC flashover across the insulating pull-rod.

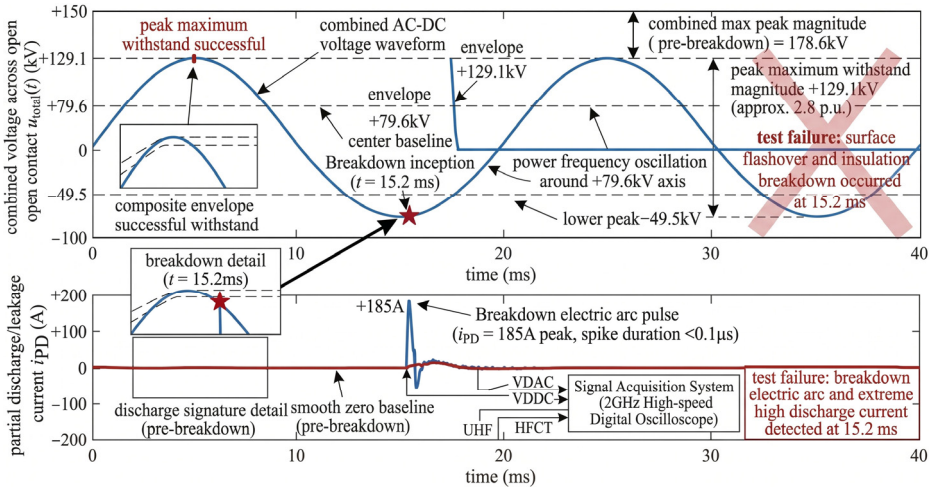


Figure 17. Transient AC–DC voltage waveforms and PD pulses at the instant of surface flashover breakdown along the composite insulating pull-rod.

(3) Case 3: Micro-Discharge and Restrike Evolution Inside the Vacuum Interrupter (From Field Emission to Gap Breakdown)

Under high combined AC–DC stress, a vacuum interrupter (VI) specimen featuring micro-metallic surface burr defects on its electrodes was evaluated. The complete evolution process, progressing from microscopic field-emission electron avalanches to main-gap vacuum breakdown, was captured. The evolution process of "field emission—micro-discharge—main-gap breakdown" in the vacuum interrupter under combined AC–DC stress is illustrated in Figure 18.

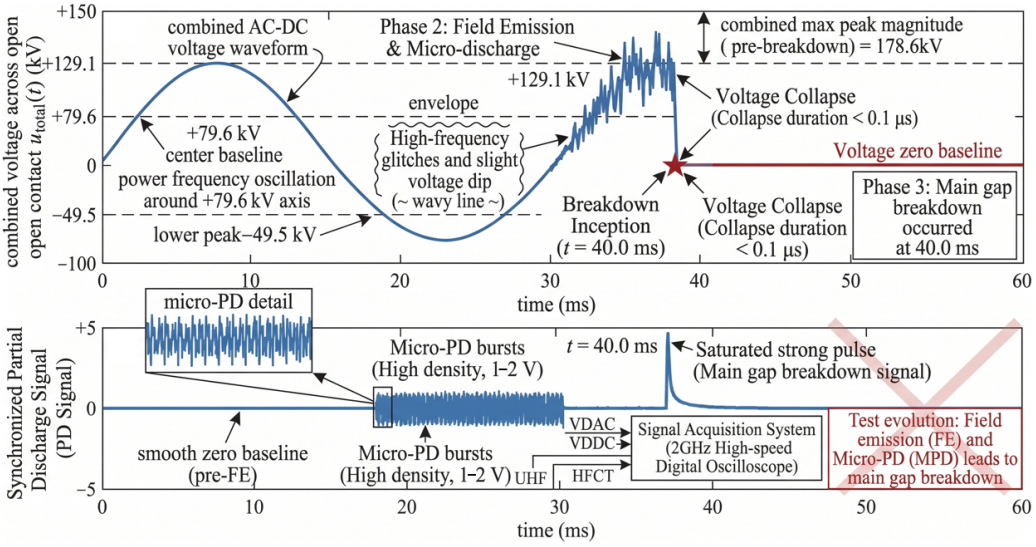


Figure 18. Evolution waveforms of the "field emission—micro-discharge—main-gap breakdown" sequence in the vacuum interrupter under combined AC–DC stress.

Figure 18 depicts the microscopic breakdown physics of the vacuum medium under combined AC–DC stress: (1) High-Field Emission (Fowler–Nordheim Effect): When the peak combined AC–DC voltage of 129.1 kV is applied across the fixed and moving contacts of the vacuum interrupter, micro-scale cathode burrs on the contact surface amplify the localized electric field intensity to $E_{local} = \beta E_{avg} > 10^7$ V/cm. Under this intense electric field, cathode electrons are extracted from the surface via quantum tunneling, giving rise to a field-emission electron beam. (2) Metal Vapor Cloud Formation and Breakdown: The

energetic electron beam generated by field emission bombards the anode contact, causing localized surface vaporization and forming a metal vapor cloud. As the density of the metal vapor reaches a critical threshold, impact ionization of electrons within the vapor occurs rapidly. Frequent micro-discharge current pulses emerge and swiftly transition into a low-impedance vacuum arc, ultimately inducing a full restrike breakdown across the vacuum interrupter gap.

Based on the above analysis, it can be concluded that while the proposed combined AC/DC voltage test for 40.5 kV capacitor bank circuit breakers has drawbacks such as circuit complexity, stringent synchronization control requirements, and high equipment investment, its primary advantages lie in faithfully reproducing the electric field distortion under capacitor-side residual DC voltage and reverse-polarity superposition. By acting as a 'defect amplifier,' this method accurately captures latent risks such as moisture-induced surface flashover of insulating rods and micro-discharges caused by contact burrs, thereby providing robust theoretical and data support for evaluating contact gap insulation margins and revising type test standards. Compared with the conventional AC voltage test, the performance comparison of the proposed method is shown in Table 5.

Table 5. Performance Comparison.

Evaluation Metric	Pure AC Voltage Test (Conventional Standard Scheme)	Combined AC/DC Voltage Test (Recommended Equivalent Scheme)
Test Voltage & Peak Stress	1 min power-frequency withstand standard value (118 kV peak)	Reverse-polarity superposition of AC (−49.5 kV peak) and DC (+79.6 kV), reaching a maximum contact gap peak of 129.1 kV (3.0 p.u.)
Electric Field Distribution Characteristics	Relatively uniform electric field distribution, primarily governed by relative permittivity εr (static electric field)	Transition from static electric field to steady-state resistive electric field (governed by resistivity ρ), accompanied by severe field redistribution and distortion during polarity reversal
Space Charge Excitation Capability	Incapable of effectively exciting directional migration and accumulation of space charge	Significantly excites directional migration, steady-state accumulation, and localized electric field distortion within dielectric media and on surfaces
Re-ignition Condition Equivalence	Significantly underestimates actual contact gap stress; fails to simulate DC residual voltage on the capacitor side and strong reverse-polarity superposition across both sides	Fully reproduces the most severe transient insulation stress during "arc re-ignition/polarity reversal" in reactive power compensation circuit breakers
Insulation Defect Detection Sensitivity	Low; microscopic burrs, trace moisture, and other hidden defects are easily missed	Extremely high; effectively triggers flashover along damp insulating rods (micro-discharges/dry-band corona) and field emission (Fowler–Nordheim effect) from micron-scale contact burrs

7. Conclusions

To address the insulation safety challenges of 40.5 kV reactive power compensation capacitor bank circuit breakers during switching operations, this paper performs a comparative analysis on the transient response characteristics under four typical operating conditions: normal switching, capacitor inter-plate short circuit, asynchronous switching, and arc restrike. The dynamic evolution of inter-gap insulation stress and the space-charge-induced failure mechanism are elucidated, based on which an equivalent combined AC–DC withstand voltage testing scheme is proposed. The main conclusions are summarized as follows:

(1) Normal switching exhibits smooth transient responses, serving as the benchmark operating condition. Inter-plate short circuits modulate transient oscillation characteristics by altering the branch topology and energy storage distribution. Asynchronous switching exacerbates high-frequency switching surges due to initial phase mismatches. Most critically, arc restrike injects a secondary intense excitation during the unattenuated transient phase, resulting in a sharp escalation of overvoltage on the capacitor side; this renders arc restrike the most severe condition inducing transient gap insulation degradation.

(2) A microscopic physical mechanism governing the sharp reduction in localized breakdown strength under combined stress is revealed. In contrast to the uniform electric field distribution observed under pure AC voltage, combined AC–DC high voltage (particularly on the side with residual DC voltage) drives the directional migration and steady-state accumulation of free charges at electrode defects such as surface micro-protrusions. The long-term accumulation of this space charge layer severely distorts the macroscopic electric field across the breaker gap, creating high-field regions that readily trigger field emission and accelerate insulating thermal aging. This space-charge accumulation effect cannot be effectively activated in conventional pure AC tests, confirming the necessity of implementing combined AC–DC withstand voltage testing.

(3) The study demonstrates that relying solely on single-sided voltage measurements significantly underestimates the actual voltage stress experienced across the breaker gap; hence, the gap insulation withstand capability must be evaluated based on the real-time instantaneous potential difference between both sides at identical timestamps. Under the open-circuit condition, the maximum gap potential difference is 82.4368 kV (bus side: +31.4714 kV; capacitor side: −50.9654 kV). Under the most severe arc restrike condition, strong opposite-polarity superposition occurs, escalating the peak instantaneous gap potential difference to 129.0806 kV (bus side: −49.4861 kV; capacitor side: +79.5945 kV). This value substantially exceeds the standard 1 min power-frequency withstand voltage requirement (118 kV) for 40.5 kV breaker gaps, proving that opposite-polarity voltage superposition across both sides is the physical root cause of gap restrike.

(4) Abandoning non-physical equivalence methods based on the simple algebraic summation of peak voltages from both sides, an equivalent combined AC–DC withstand testing scheme consisting of "power-frequency AC at −49.4861 kV (peak) and DC at +79.5945 kV" is recommended, formulated on the precise real-time mapping of instantaneous potential differences. This proposed scheme faithfully reproduces the spatial electric field distortion and composite insulation stress experienced by the breaker under the most severe restrike condition, thereby providing a theoretical foundation and empirical support for evaluating the insulation margin of reactive power compensation circuit breakers and revising type-testing standards.

(5) Combined AC/DC space charge exerts no substantial impact on either the insulation design or switching strategies of circuit breakers. In terms of insulation design, standard insulation margins fully accommodate charge accumulation; since space charge acts merely as a 'defect amplifier,' strictly controlling manufacturing processes to eliminate defects ensures safe operation without incurring redesign costs. In terms of operating strategies, a severe timescale mismatch exists between microsecond-to-millisecond switching actions and extremely slow charge evolution. Furthermore, any minor charge effects are masked by gas blasting and the mechanical scatter of the operating mechanism, eliminating the need to modify operating speeds, controlled switching, or arc-extinguishing designs.

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Conflicts of Interest: Authors Guoliang Zhang, Longcheng Dai, Jianpeng Ma, Hui Zha and Tao Bai were employed by State Grid Ningxia Electric Power Co., Ltd. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as potential conflicts of interest. The authors declare that this study received funding from the Science and Technology Project of State Grid Ningxia Electric Power Co., Ltd. The funder was not involved in the study design, collection, analysis, interpretation of data, the writing of this article or the decision to submit it for publication.

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