

Article

A Practical Controller-Aware LDC Parameter Design Method for SVRs Considering Bidirectional Power Flow

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Abstract

The increasing penetration of distributed energy resources (DERs), particularly photovoltaic (PV) ones, has introduced significant challenges in distribution system voltage regulation due to bidirectional power flows and rapid voltage fluctuations. Consequently, conventional step voltage regulator (SVR) control schemes based on static line drop compensation (LDC) parameters are no longer sufficient to maintain stable voltage profiles under such dynamic operating conditions. This paper proposes a method for deriving bidirectional LDC parameters that can be directly implemented in practical SVR controllers by incorporating the operational characteristics and parameter structure of real SVR devices in distribution feeders with high DER penetration. The proposed method determines forward and reverse LDC parameters separately by considering deadband characteristics of practical SVR controllers, depending on the direction of power flow. To incorporate a piecewise control structure corresponding to bidirectional power flow conditions, the LDC parameter optimization problem is formulated as a mixed-integer quadratic programming (MIQP) problem. The effectiveness of the proposed method is validated through MATLAB R2024b(MathWorks, Natick, MA, USA)-based simulations on a distribution feeder under various load conditions and PV penetration scenarios. The results demonstrate that the proposed approach achieves superior voltage regulation performance compared to conventional single LDC methods and piecewise LDC approaches that do not explicitly consider SVR operational characteristics.

Keywords: step voltage regulator; line drop compensation; mixed-integer quadratic programming; distributed energy resources; voltage regulation



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1. Introduction

The increasing deployment of distributed energy resources (DERs), particularly photovoltaic (PV) systems, can cause reverse power flow in distribution systems, leading to problems such as voltage rise, voltage fluctuation, and violation of the allowable voltage range [1–3]. These impacts can be more pronounced on long or weak distribution feeders. In particular, when DERs are unevenly distributed among feeders, the maximum and minimum voltage deviations across the system can be widened, which may require the coordinated control of multiple voltage regulation resources [4]. Voltage regulation in distribution systems has traditionally been performed using devices such as on-load tap changers (OLTCs), step voltage regulators (SVRs), and switched capacitor banks. Among these, SVRs adjust their tap position based on local voltage and current measurements to keep customer voltage within the allowable range, and are widely deployed on distribution

feeders [5]. In conventional SVR operation, a line drop compensation (LDC) scheme is used to estimate the voltage at a remote load center and determine the tap action.

A fundamental limitation of conventional LDC schemes, however, is that their parameters are static values determined under a limited set of operating states, such as peak-load or light-load conditions, and applied unchanged thereafter [6,7]. Because conventional LDC parameters are designed under the assumption of unidirectional power flow, a single fixed parameter set cannot represent the voltage drop and voltage rise patterns that vary with load, PV output, and power flow direction on DER-interconnected feeders, and the virtual load-center voltage calculated by the LDC may fail to reflect the actual voltage regulation requirements [6,8]. In addition, LDC parameters designed without considering the deadband-based discrete tap operation of an actual SVR can increase unnecessary tap operations or fail to properly regulate the system voltage. A modern SVR controller, one of the most recent SVR controllers in use in Korea, supports bidirectional power flow and DER interconnected conditions by providing configurable operating modes and LDC control settings for both forward and reverse directions [9–11]. Therefore, LDC parameter design must conform not only to system-level voltage regulation performance but also to the parameter structure and operational characteristics of an actual SVR controller.

A variety of studies have been conducted to improve conventional LDC schemes in DER interconnected distribution systems. One study proposed an MLDC-based method for determining the tap position of a ULTC transformer [12]. Another approach adjusts the SVR reference voltage, considering line loading conditions and reverse power flow, to re-establish a virtual load center [6]. The optimal compensation rate of an SVR has also been determined by additionally considering the OLTC output voltage [13]. In addition, a method was proposed that derives multiple candidate LDC parameters from historical power flow data and dynamically selects among them using a Mixture of Experts (MoE) model [14]. Similarly, other studies have optimized the SVR reference voltage and deadband to limit the number of tap operations [7,15,16]. However, these studies focus on adjusting LDC settings to system conditions or tuning the reference voltage and deadband, and do not comprehensively derive forward- and reverse-direction LDC parameters in a form implementable in an actual commercial SVR controller.

On distribution feeders with bidirectional power flow, determining the SVR control direction is also important. Misidentifying the regulation side can cause tap-changer runaway, leading to severe voltage rise or drop on the weak side of the SVR. To address this, local and bi-directional inhibition algorithms have been proposed that identify the weak side by estimating the voltage-change slope from test taps [17,18]. This need is also reflected in actual commercial controllers, such as the FLEXDG mode of a modern SVR controller, which determines the regulation direction based on the secondary side voltage change resulting from a tap operation. However, these studies focus on identifying the control direction and do not address the design of the LDC parameters that should actually be applied in each direction. In addition, studies have also been conducted that coordinate multiple voltage regulating devices based on predefined rules or that determine tap positions and reactive power using optimization techniques such as MILP and convex optimization [19–22]. However, these studies likewise do not address the design of LDC parameters for an individual SVR. Therefore, an LDC parameter design method is needed that can address bidirectional power flow conditions on distribution feeders with multiple interconnected DERs while explicitly considering the operational characteristics and parameter structure of an actual SVR controller. In this paper, we propose a mixed-integer quadratic programming (MIQP)-based method for deriving bidirectional LDC parameters applicable to an actual SVR controller. The proposed method reflects the deadband characteristics of the SVR controller and separately derives forward- and reverse-

direction LDC parameters in a form directly applicable to an actual controller, thereby enabling the method to accommodate diverse operating conditions on DER-interconnected distribution feeders. The remainder of this paper is organized as follows. Section 2 describes conventional SVR- and LDC-based voltage control methods for distribution systems, along with an overview of an actual SVR controller and its voltage regulation scheme. Section 3 presents the proposed MIQP-based method for deriving bidirectional LDC parameters. Section 4 presents the performance comparison results under various simulation conditions, Section 5 discusses the limitations and implementation issues, and Section 6 concludes the paper.

2. Background and Motivation

2.1. Distribution Voltage Control with SVR and LDC

SVR is a voltage regulating device installed at the midpoint of a distribution feeder or at sections with a large voltage drop, in order to keep the feeder voltage within an allowable range. An SVR is defined as a voltage regulating device that automatically or manually adjusts, on a per-phase basis, the voltage variation on a 22.9-kV-Y distribution feeder to maintain a constant voltage. A distribution SVR can typically regulate voltage within approximately $\pm 10\%$ of the rated voltage, and its main installation targets include long feeders, feeders with a large voltage drop, feeders with loads exhibiting large voltage fluctuation, and feeders with distributed generation interconnected along the line [23].

Voltage regulation by an SVR is performed by discretely changing the tap position. Figure 1 illustrates the basic tap control operation of an SVR [24]. The SVR controller compares the measured voltage with a reference voltage and determines whether the measured voltage lies within a deadband defined around the reference. If the measured voltage exceeds the upper bound, $V_{set} + \frac{\text{Deadband}}{2}$, a tap lowering action is required to reduce the voltage. If the measured voltage falls below the lower bound, $V_{set} - \frac{\text{Deadband}}{2}$, a tap raising action is required to raise the voltage. However, since the tap-changing mechanism of an SVR is an electromechanical device, it does not respond instantaneously to momentary voltage fluctuations. A tap control command is issued only when the voltage violation persists for longer than the preset time delay. This structure is intended to prevent unnecessary tap operations caused by short-duration voltage fluctuations and to limit the operating frequency of the tap changing mechanism.

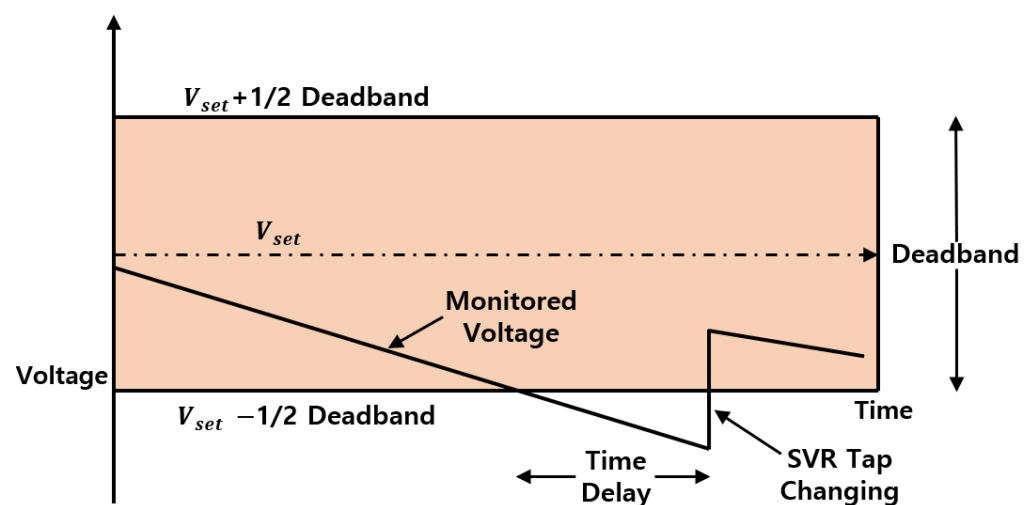


Figure 1. Concept of SVR tap control operation.

On long distribution feeders, keeping only the SVR secondary-side voltage constant may not be sufficient to properly maintain the voltage profile along the entire feeder. To

compensate for this, an LDC scheme is used. The LDC scheme estimates the voltage at a virtual load center downstream of the SVR using the voltage and current measured at the SVR installation point, and controls the tap so that this estimated voltage is maintained within the setpoint range. Figure 2 illustrates the basic operating concept of LDC. As the load increases, the line current increases, and the resulting voltage drop on the feeder downstream of the SVR also increases. Conversely, under light load conditions, the line current decreases, and the voltage drop decreases accordingly. LDC compensates for the voltage drop caused by the equivalent impedance (Z_{eq}) between the SVR installation point and the virtual load center and by the current measured at the SVR, thereby adjusting the SVR output voltage so that the voltage at the virtual load center is maintained near the reference voltage.

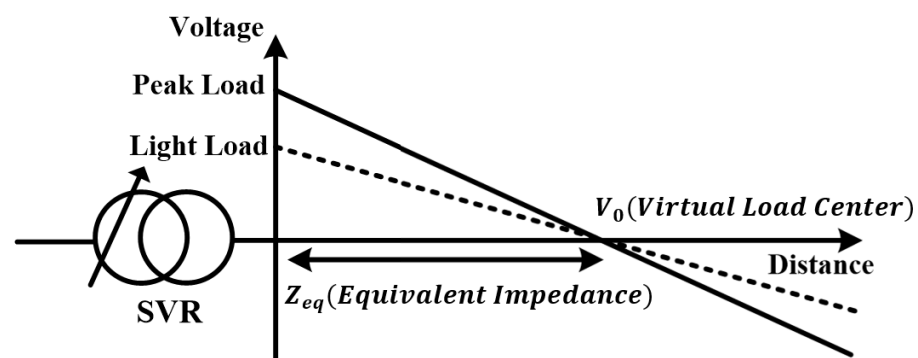


Figure 2. Basic operating concept of LDC.

Figure 3 shows the configuration concept of the LDC-based voltage regulation scheme. The SVR controller measures the SVR secondary side voltage (V_{SVR}) and the current (I_{SVR}) using a potential transformer (PT) and a current transformer (CT), respectively. If the equivalent impedance between the SVR installation point and virtual load center is denoted as $Z_{eq} = R + jX$, the estimated voltage V_0 at the virtual load center is calculated as shown in Equation (1) [6].

$$V_0 = V_{SVR} - Z_{eq}I_{SVR} \quad (1)$$

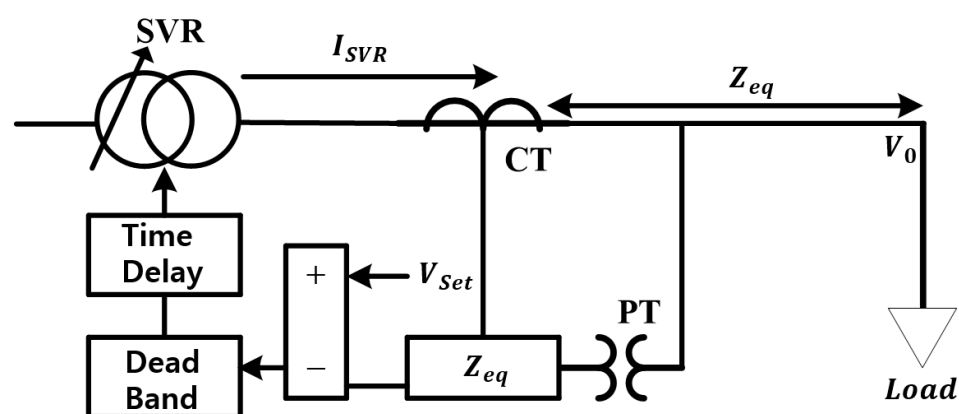


Figure 3. LDC-based SVR voltage regulation structure.

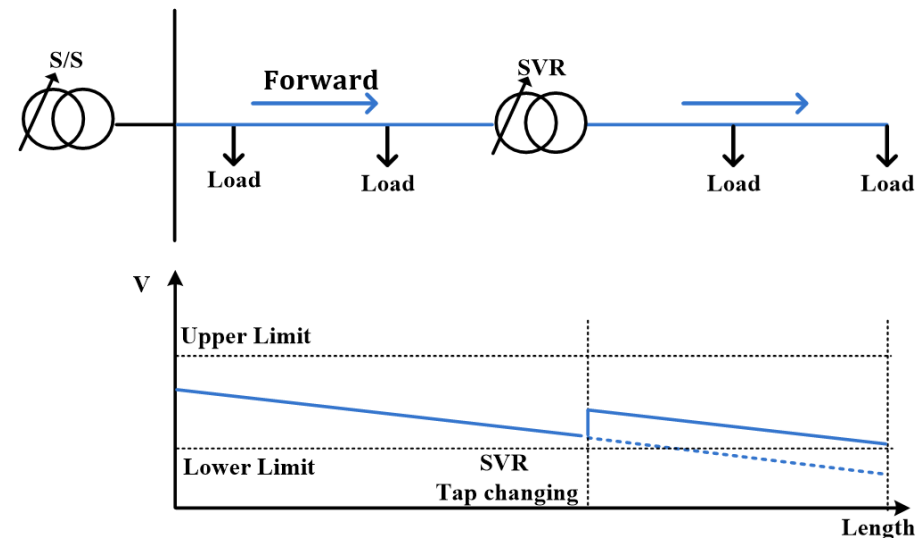
In Equation (1), V_{SVR} is the voltage measured at the SVR secondary side, I_{SVR} is the current flowing through the SVR, and Z_{eq} is the equivalent line impedance from the SVR installation point to the virtual load center. This expresses the basic principle of LDC, in which the load center voltage is estimated by compensating the SVR secondary side voltage for the line voltage drop component. The controller then determines whether the estimated

V_0 lies within the range of $V_{\text{set}} \pm \frac{\text{deadband}}{2}$. If it falls outside this range, the controller raises or lowers the tap after the preset time delay.

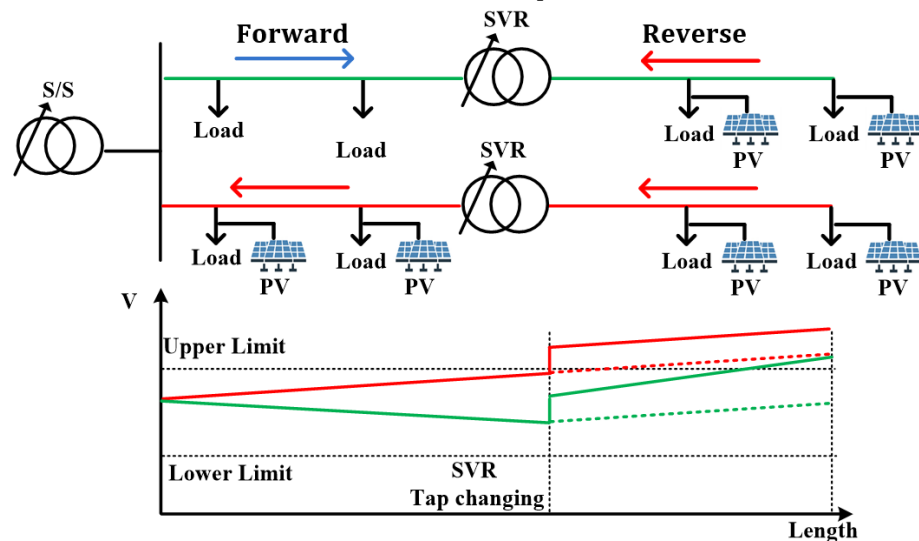
2.2. Limitations of Conventional LDC Parameter Settings

Conventional LDC-based voltage control schemes for SVRs have primarily been designed under the assumption of a unidirectional power flow environment, in which power flows from the substation toward the load. The basic principle of LDC control is to estimate the voltage at the virtual load center using the voltage and current measured at the SVR installation point, together with the equivalent impedance between the SVR and the virtual load center, and to control the tap so that the estimated voltage is maintained within the setpoint range [25]. This control structure can be effectively applied to conventional radial distribution feeders, in which the line voltage drop increases with the load current and the voltage gradually decreases toward the end of the feeder. Figure 4a illustrates the typical voltage regulation concept under such load-dominated, unidirectional power flow conditions. In this case, the feeder voltage decreases toward the downstream end, and the SVR raises its tap to alleviate the undervoltage, thereby raising the downstream voltage. However, a fundamental limitation of conventional LDC parameter settings is that the LDC control parameters V_{ref} , R and X are static parameters predetermined based on a representative operating condition. In general, LDC parameters are calculated under a limited set of operating states, such as peak-load or light-load conditions, and once set, the same parameter set is applied across all subsequent time periods and operating states [6,7]. This structure can be practical for conventional distribution feeders in which the load pattern changes relatively gradually and the direction of power flow remains constant. However, in DER-interconnected distribution feeders, where load demand, PV output, and the direction of power flow change frequently over time, a single fixed set of LDC parameters cannot adequately reflect the voltage regulation requirements of all operating conditions. In particular, when DERs such as PV are interconnected downstream of an SVR, the conventional voltage-drop pattern, in which the voltage decreases toward the downstream end, can be reversed. As PV output increases, the direction of the current on the SVR secondary side may reverse, in which case the downstream voltage rises due to DER output rather than load. Figure 4b illustrates the limitations that conventional LDC-based SVR control can exhibit under such reverse power flow conditions caused by PV interconnection. With the downstream voltage already elevated by PV, the conventional LDC scheme raises the tap as it would under load-dominated conditions, thereby aggravating the overvoltage. The overvoltage can vary depending on the location and capacity of the PV, and prior studies have also confirmed that when large-scale DERs are interconnected downstream of an SVR, the virtual load-center voltage calculated by the LDC scheme may fail to reflect the actual voltage regulation requirements, resulting in voltage problems [6,8]. In addition, conventional LDC parameter settings do not account for the actual tap-operation characteristics of an SVR controller. An actual SVR is not a continuous controller but an electromechanical device with a deadband, a time delay, and discrete tap operation. Therefore, the adequacy of LDC parameters should be evaluated not only in terms of how accurately they estimate the voltage drop, but also in terms of how they affect the actual number of tap operations and the frequency of voltage violations [7,16]. In systems with large DER output variability in particular, inadequately designed LDC parameters can either increase unnecessary tap operations or, conversely, fail to properly regulate the system voltage. In summary, the core limitation of conventional LDC parameter settings is that a single, static parameter set designed under the assumption of unidirectional power flow cannot simultaneously represent the diverse operating states encountered on DER-interconnected feeders. On such feeders, the relative influence of voltage drop and voltage rise changes over time

depending on the load and PV output, and the required direction and characteristics of voltage compensation vary accordingly. Therefore, an LDC parameter design method is needed that goes beyond a single static setting, can account for bidirectional power flow conditions, and is compatible with the structure of an actual SVR controller, with direction specific LDC parameters.



(a) Load-dominated unidirectional power flow condition.



(b) Reverse power flow condition due to PV interconnection.

Figure 4. Characteristics of conventional LDC-based SVR voltage control under changing operating conditions.

2.3. Practical SVR Controller Characteristics

2.3.1. Overview of a Representative Modern SVR Controller

A representative modern SVR Controller is an actual controller used for the operation, automation, monitoring, and setting management of a distribution step voltage regulator. Such a controller provides operating modes suited to modern distribution systems that include DERs. Based on the measured secondary-side current, the controller determines the power flow region and issues tap control commands according to the configured operating mode. This subsection describes the power flow region determination of a representative modern SVR controller, its operating modes and the BIASMODE-based structure for de-

termining the voltage regulation direction, and the actual controller structure that allows forward and reverse LDC settings to be applied separately [9].

2.3.2. Criteria for Power Flow Region Determination in a Modern SVR Controller

A modern SVR controller determines the power flow region based on the magnitude and phase of the measured current, and the tap control direction is determined according to the operating mode and the identified region. As shown in Figure 5, the overall power flow region is divided into a forward power flow region, a reverse power flow region, and a no-torque region. The forward and reverse current thresholds are defined as 50FWDP and 50REVP, respectively. When the measured current exceeds the forward current threshold (50FWDP), the controller identifies the condition as the forward power flow region. Conversely, when the measured current exceeds the reverse current threshold (50REVP), the controller identifies the condition as the reverse power flow region. Between the two thresholds, the current magnitude is considered insufficient to clearly indicate either forward or reverse power flow, and the controller designates this intermediate region as the no-torque region. In the no-torque region, the current magnitude is too small to reliably distinguish the power flow direction, and the actual voltage regulation action in this region is determined by the configured operating mode and the BIASMODE parameter setting [10].

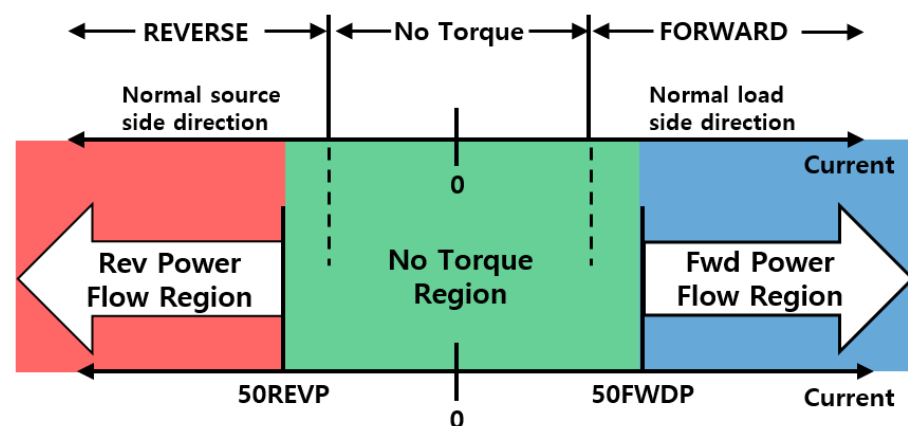


Figure 5. Power flow region determination criteria based on the measured current magnitude in a modern SVR controller. The dashed lines separate the reverse and forward directions; the sections between each dashed line and 50REVP/50FWDP are reverse/forward currents whose magnitude is below the setting, and are treated as the no-torque region.

2.3.3. Operating Modes and BIASMODE-Based Voltage Regulation Direction

The overall voltage regulation behavior of a modern SVR controller is selected via the operating mode setting. The available operating modes include Locked Forward (LOCKFWD), Locked Reverse (LOCKREV), Idle Reverse (IDLEREV), Bidirectional (BIDIR), Cogeneration (COGEN), and FLEXDG mode, each of which defines the logic that determines, for a given power flow region, in which direction the controller regulates voltage and which control settings are applied. Figure 6 shows the voltage regulation direction of each operating mode according to the power flow region [10,11]. When an actual SVR is modeled, the behavior of the controller that is not captured by the LDC calculation itself should also be considered. The tap command is issued only after the preset time delay and the tap mechanism requires an actuation time, and the controller switches its regulation behavior as the operating mode and the power flow region change. In addition, the reference voltage and the power flow region are determined from the voltage and current measured

through the PT and CT, and thus the measurement errors of these transformers affect the controller operation.

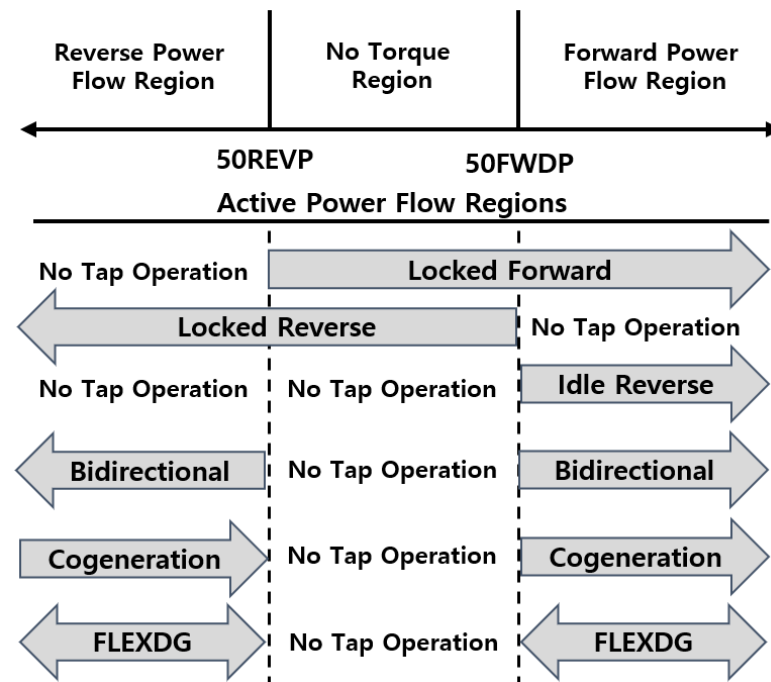


Figure 6. Voltage regulation direction of each operating mode according to the power flow region in a modern SVR controller.

Among these operating modes, the domestic distribution SVR operating standard specifies that the operating mode of an SVR interconnected with DERs be set uniformly to COGEN across all phases [23]. Hence, for DER-interconnected distribution feeders, it is important to consider the operating characteristics of the COGEN mode. This study accordingly focuses on the operating logic associated with COGEN mode and DER-interconnected systems. COGEN mode is designed to account for conditions in which DERs interconnected downstream of the SVR may cause reverse power flow. In this mode, even when reverse power flow occurs, voltage regulation is still performed in the forward direction, and tap control commands are issued based on the normal load-side voltage (V_L). The detailed behavior of the no-torque Region under COGEN mode depends on the BIASMODE setting. BIASMODE determines the voltage regulation direction and the applied control settings within the no-torque region, where the current magnitude is too small to clearly distinguish between forward and reverse power flow. In the controller, the BIASMODE parameter can be configured for operating modes that account for bidirectional power flow conditions and can be set to OFF, FWD, or REV. When BIASMODE is set to OFF, no tap operation is performed in the no-torque Region. When BIASMODE is set to FWD, the same behavior as in the forward power flow region is applied in the no-torque Region, whereas setting BIASMODE to REV applies the same behavior as in the reverse power flow region. Figure 7 shows the COGEN submodes that are activated according to the power flow region and the BIASMODE setting under COGEN mode. In the figure, COGEN(fwd) and COGEN(rev) denote the COGEN operating states in which the forward direction and reverse direction LDC settings, respectively, are applied. These states indicate not only the voltage regulation direction of the controller but also which LDC parameter set is activated in the corresponding region. This structure demonstrates that the controller can selectively apply different LDC settings depending on the power flow region and the BIASMODE configuration. Therefore, in order to design LDC parameters that are compatible with an

actual SVR controller on DER interconnected distribution feeders, an approach is required that derives forward direction and reverse direction LDC parameters separately, rather than a single LDC parameter set.

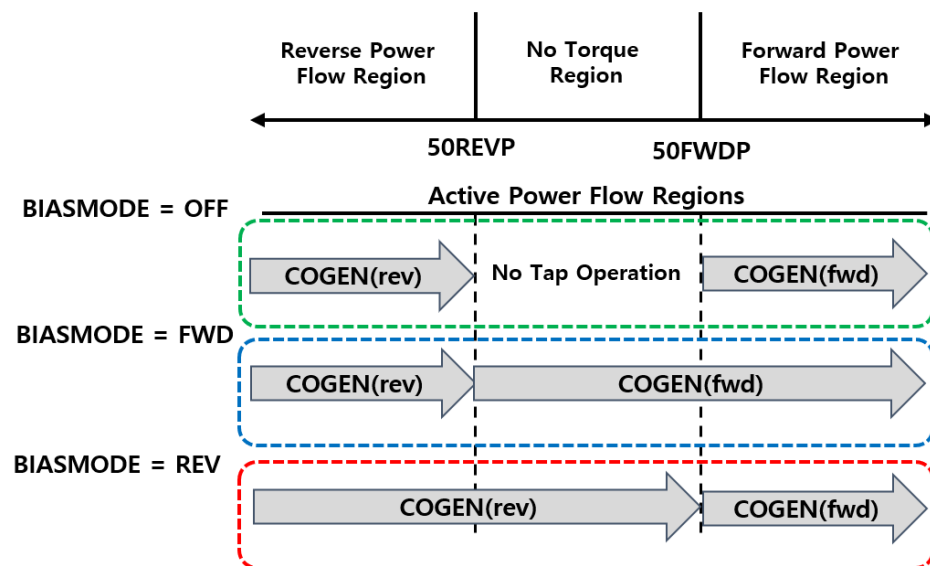


Figure 7. COGEN submodes activated according to the power flow region and BIASMODE setting.

2.3.4. LDC Settings of a Modern SVR Controller

As described in Section 2.1, the LDC compensates the measured voltage for the voltage drop across the equivalent impedance Z_{eq} in Equation (1). In a modern SVR controller, this compensation is not entered as an impedance in ohms. Instead, the resistive component V_R and the reactive component V_X of the compensation are entered as voltages in volts on the secondary side of the controller. The controller provides these settings separately for the forward and reverse power flow directions, so that a different compensation can be applied to each direction. The values of V_R and V_X are obtained by converting the resistance R and the reactance X per unit length of the line (Ω/km) through the PT ratio ($PT_{Prim}:PT_{Sec}$) and the CT ratio ($CT_{Prim}:CT_{Sec}$), as $R \times \frac{PT_{Sec}}{PT_{Prim}} \times CT_{Prim}$ and $X \times \frac{PT_{Sec}}{PT_{Prim}} \times CT_{Prim}$, and multiplying the results by the length of the line section between the SVR installation point and the virtual load center. In this study, the PT ratio is 13,200:120 and the CT ratio is 400:0.2. In the controller, V_R and V_X are entered in steps of 0.1 V. Therefore, the I_{fwd} and I_{rev} obtained in Section 3 are converted into V_R and V_X rounded to 0.1 V when they are entered into the controller, and the effect of this rounding on the voltage control results is examined in Section 4.6. Using the entered settings and the measured current, the controller calculates the voltage drop of this line section and subtracts it from the voltage measured at the SVR installation point as in Equation (1). The tap control is then performed based on the resulting estimated voltage, which is compared with $V_{set} \pm \frac{\text{deadband}}{2}$. The forward or reverse setting is applied according to the power flow region and the BIASMODE setting described in Sections 2.3.2 and 2.3.3. The length of the line section applied in this process is the LDC parameter designed in Section 3. The reference voltage V_{ref} designed in Section 3 is expressed in p.u. of the rated voltage of the controller (120 V), and it is entered as the band center V_{set} of the controller after being converted to volts by multiplying it by 120 V. Likewise, the current threshold I_{dir} designed in Section 3 is expressed in p.u. of the rated current of the controller (0.2 A), and its magnitude is entered as 50FWDP or 50REVP of the controller after being converted to amperes by multiplying it by 0.2 A [9–11].

3. Proposed MIQP-Based LDC Parameter Design Method

This paper proposes an MIQP-based design method for deriving LDC parameters for an SVR in DER-interconnected distribution feeders. The method is developed for the case in which a single SVR is installed on the feeder, and the coordination of multiple SVRs connected in series is not considered. The chapter is organized as follows. First, the time-varying optimal sending end reference voltage (V_{SER}) for maintaining the voltage downstream of the SVR near the nominal voltage is determined using the results of power flow analysis. Next, the derived V_{SER} is approximated in the form of Single and Piecewise LDC parameters applicable to an actual SVR. The practical limitations of V_{SER} -fitting-based LDC parameter design are then analyzed, and based on these limitations, a Practical SVR-aware PiecewiseDB parameter design method is proposed. Figure 8 shows the overall flowchart of the proposed methods.

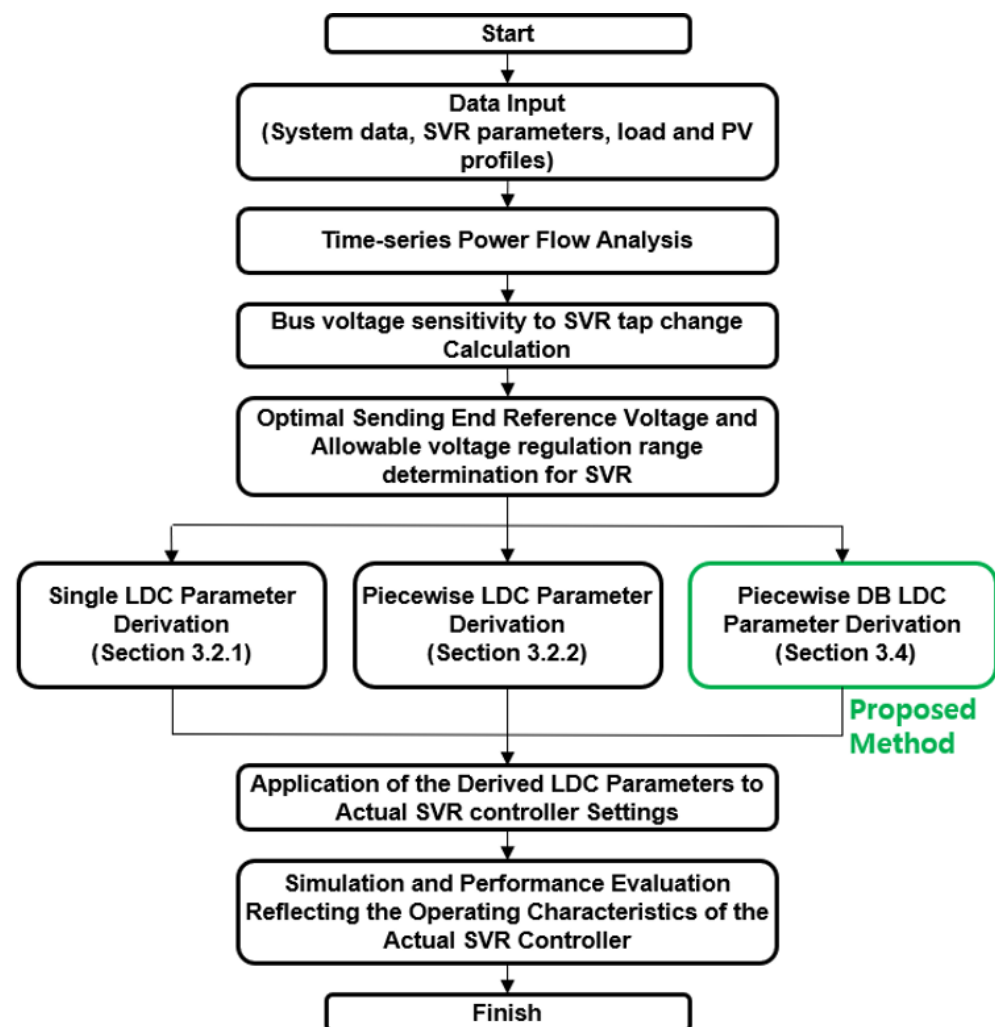


Figure 8. Overall flowchart of the proposed LDC parameter design method.

3.1. Optimal V_{SER} Derivation Based on Load Flow Analysis

This subsection describes the method for deriving the time-varying optimal V_{SER} , which serves as the reference data for LDC parameter design. Through LDC control, an SVR adjusts its secondary side sending end voltage to keep the voltage at downstream buses within the voltage regulation zone within the allowable range. Deriving in advance the SVR's theoretical optimal V_{SER} for keeping the downstream bus voltage close to the nominal voltage is the starting point of LDC parameter design. To this end, V_{SER} is derived

from the results of power flow analysis using system data together with historical load and DER data. Throughout this paper, t denotes the discrete time index corresponding to each 15-min interval over the analysis horizon. First, using the system data and the load and DER profiles, the initial voltage profile is derived through time-varying power flow analysis without reflecting SVR tap control. SVR tap control affects the entire downstream bus voltage by adjusting the secondary-side sending-end voltage, and the magnitude of this effect varies with the bus location and the system configuration. Accordingly, the tap sensitivity, which indicates how much each downstream bus voltage responds to a given tap change, is calculated from the power flow analysis results. By incorporating the tap sensitivity, the effect of the SVR tap operation on the downstream voltage distribution can be precisely quantified on a per-bus basis when deriving the optimal sending-end voltage. The tap sensitivity at time t is calculated as shown in Equation (2), using the resulting change in each downstream bus voltage after the SVR tap is changed to +1 and −1, respectively.

$$S_{\text{tap}}(i, t) = \frac{1}{2} \left(\frac{V_{i,t}^{(0)} - V_{i,t}^{(+1)}}{V_{\text{SVR},t}^{(0)} - V_{\text{SVR},t}^{(+1)}} + \frac{V_{i,t}^{(0)} - V_{i,t}^{(-1)}}{V_{\text{SVR},t}^{(0)} - V_{\text{SVR},t}^{(-1)}} \right) \quad (2)$$

Here, $V_{i,t}^{(n)}$ is the magnitude of the i -th bus voltage at tap position n and time t , and $V_{\text{SVR},t}^{(n)}$ is the magnitude of the SVR secondary side voltage at tap position n and time t . The average of the sensitivities calculated under the +1 and −1 tap positions is used to reduce the one directional sensitivity estimation error caused by the nonlinearity of the distribution system.

Based on the derived initial voltage profile and the bus voltage sensitivity to the SVR tap change, the optimal correction ΔV_t is derived to keep the voltage at the downstream buses within the SVR's voltage regulation zone close to the nominal voltage. To this end, the following least squares problem is formulated to minimize the error between the nominal voltage and the voltage estimated at downstream bus i when ΔV_t is applied, where D denotes the set of buses belonging to the voltage regulation zone of the SVR.

$$\min f = \sum_{i \in D} (\hat{V}_{i,t} - V_{\text{nom}})^2 \quad (3)$$

$$\hat{V}_{i,t} = V_{i,t}^0 + S_{\text{tap}}(i, t) \Delta V_t \quad (4)$$

Here, V_{nom} is the nominal voltage (1.0 p.u.) and $\hat{V}_{i,t}$ denotes the voltage estimated at the i -th bus when the optimal correction ΔV_t is applied. Substituting Equation (4) into Equation (3) and expanding the objective function as a function of ΔV_t the analytical solution for the optimal correction can be obtained from the first-order optimality condition ($\frac{\partial f}{\partial \Delta V_t}$), as given in Equation (5).

$$\Delta V_t^* = - \frac{\sum_{i \in D} S_{\text{tap}}(i, t) (V_{i,t} - V_{\text{nom}})}{\sum_{i \in D} S_{\text{tap}}(i, t)^2} \quad (5)$$

The numerator of Equation (5) is the sum of the voltage deviations at the downstream buses of the SVR, weighted by the tap sensitivity, and dividing this by the sum of the squared tap sensitivities yields ΔV_t^* as the correction coefficient obtained by least squares fitting of the voltage deviations against the tap sensitivity. When the voltage deviations are negative, $\Delta V_t^* > 0$ is obtained, raising the sending end voltage, whereas in the opposite case, $\Delta V_t^* < 0$ is obtained, lowering the sending end voltage. The calculated optimal correction ΔV_t^* must satisfy the SVR's physical voltage regulation range and the voltage

limit violation prevention condition. An SVR is not a continuous controller that adjusts precisely to the reference voltage. It is a discrete controller that tolerates an error within the deadband even after a tap operation. As a result, even if the estimated voltage is calculated to lie within the allowable voltage range, the actual voltage during operation may exceed this range. Therefore, when determining the allowable voltage range, a margin corresponding to this deadband must be considered to impose the constraint, and the allowable maximum and minimum corrections are calculated as given in Equation (6).

$$dV_{\max,t} = \min_{i \in D} \left[\frac{V_{\max} - \frac{DB}{2} - V_{i,t}^0}{S_{\text{tap}}(i, t)} \right], dV_{\min,t} = \max_{i \in D} \left[\frac{V_{\min} + \frac{DB}{2} - V_{i,t}^0}{S_{\text{tap}}(i, t)} \right] \quad (6)$$

Here, $V_{\max} = 1.02$ p.u. and $V_{\min} = 0.96$ p.u. are the upper and lower bounds of the allowable voltage range, and DB is the deadband of the SVR controller. $dV_{\max,t}$ and $dV_{\min,t}$ are derived from the voltage limit violation prevention condition at each bus. Since this condition must be satisfied simultaneously for all downstream buses the upper bound $dV_{\max,t}$ is determined as the minimum among the upper bound values required by each bus, and the lower bound $dV_{\min,t}$ is determined as the maximum among the lower bound values required by each bus. This means that the conditions of the most vulnerable bus determine the allowable range of the correction for the entire system. Applying the constraint in Equation (6) together with the SVR's physical voltage regulation limit of $\pm 10\%$ to the calculated ΔV_t^* , the final correction ΔV_t is determined as given in Equation (7).

$$\Delta V_t = \begin{cases} dV_{\max,t} & \text{if } \Delta V_t^* > dV_{\max,t} \\ dV_{\min,t} & \text{if } \Delta V_t^* < dV_{\min,t} \\ \Delta V_t^* & \text{otherwise} \end{cases}, \Delta V_t = \begin{cases} 0.1 & \text{if } \Delta V_t' > 0.1 \\ -0.1 & \text{if } \Delta V_t' < -0.1 \\ \Delta V_t' & \text{otherwise} \end{cases} \quad (7)$$

This determined ΔV_t represents the correction to the SVR secondary side sending end voltage that brings the voltage across all downstream buses closest to the nominal voltage. Accordingly, the optimal sending end voltage that the SVR should target at time t , $V_{\text{SER},t}$, is defined as the sum of the SVR's initial sending end voltage $V_{\text{SVR},t}^0$ and this correction ΔV_t , as given in Equation (8). Likewise, the upper and lower bounds of $V_{\text{SER},t}$ are defined as in Equation (9).

$$V_{\text{SER},t} = V_{\text{SVR},t}^0 + \Delta V_t \quad (8)$$

$$V_{\text{SER},\max,t} = V_{\text{SVR},t}^0 + dV_{\max,t}, V_{\text{SER},\min,t} = V_{\text{SVR},t}^0 + dV_{\min,t} \quad (9)$$

$V_{\text{SER},\max,t}$ and $V_{\text{SER},\min,t}$ define the allowable sending end voltage range that satisfies the voltage limit violation prevention condition.

3.2. V_{SER} -Fitting-Based LDC Parameter Design

This subsection describes the method for deriving the LDC parameters of the SVR based on $V_{\text{SER},t}$ obtained in Section 3.1. Sections 3.2.1 and 3.2.2 describe, respectively, the single LDC method, which does not distinguish the direction of power flow, and the piecewise LDC method, which applies separate parameters for the forward and reverse power flow directions.

In the LDC parameter design, the downstream network of the SVR is reflected only through the optimal sending end voltage obtained from the power flow analysis in Section 3.1 and the SVR secondary side current, and neither the number nor the configuration of the downstream buses is directly included in the optimization problems. Since the size of the MIQP is determined by the number of time steps, a larger network is not expected to significantly affect the solution of the MIQPs in Sections 3.2.2 and 3.4. In addition, once the parameters are derived, they can be applied to the SVR controller in the

same form, namely the forward and reverse LDC settings and the current threshold, and the controller operates on its locally measured voltage and current in the same manner regardless of the network size.

3.2.1. Single LDC Parameter Design

The reference voltage $\hat{V}_t$ calculated by the LDC control of the SVR is computed from the measured SVR secondary side current $I_{SVR,t}$ and the LDC parameters as given in Equation (10).

$$\hat{V}_t = (R_{pu}I_{R,t} + X_{pu}I_{X,t}) \cdot l + V_{ref} \quad (10)$$

Here, R_{pu} and X_{pu} are the resistance and reactance per unit length of the line (p.u./km), and $I_{R,t}$ and $I_{X,t}$ are the active and reactive components of the SVR secondary side current, defined as $I_{SVR,t} \cos \theta_t$ and $I_{SVR,t} \sin \theta_t$, respectively. l is the line length (km) and V_{ref} is the reference voltage, with l and V_{ref} being the LDC parameters to be designed. To express this concisely and to use it commonly in the formulations of Sections 3.2.2 and 3.4 g_t is defined as follows.

$$g_t = R_{pu}I_{R,t} + X_{pu}I_{X,t} \quad (11)$$

Using Equation (11), the LDC reference voltage can be expressed as $\hat{V}_t = l \cdot g_t + V_{ref}$, and the LDC parameter derivation problem is formulated as the problem of estimating l and V_{ref} that best approximate $V_{SER,t}$. The single LDC method does not distinguish between forward and reverse power flow, and estimates a single LDC parameter pair over the entire operating period. This is formulated as the following constrained least squares problem.

$$\min \sum_{t=1}^T (\hat{V}_t - V_{SER,t})^2 \quad (12)$$

$$V_{SER,min,t} \leq \hat{V}_t \leq V_{SER,max,t}, \forall t \quad (13)$$

$$0 \leq l \leq l_{max}, V_{ref,min} \leq V_{ref} \leq V_{ref,max} \quad (14)$$

Equations (12)–(14) constitute a constrained least squares problem with an objective function and linear inequality constraints that are linear in the decision variables l and V_{ref} . The objective function in Equation (12) minimizes the sum of squared errors between the LDC reference voltage $\hat{V}_t$ and $V_{SER,t}$ over the entire operating period, thereby determining the LDC parameters so that they best approximate the time-varying optimal sending end voltage of the system. Equation (13) is an inequality constraint that ensures the derived reference voltage lies within the allowable sending end voltage range $[V_{SER,min,t}, V_{SER,max,t}]$ obtained in Section 3.1, so that the derived LDC parameters are determined under the condition that the allowable voltage range of all buses within the voltage regulation zone is satisfied. The first condition in Equation (14) constrains the line length to be determined within a range that can be set according to the system conditions, and the second condition constrains the reference voltage to be maintained within the allowable voltage range of the system. Figure 9 shows an example of the parameter derivation results of the single LDC method. The scatter plot shows the time-varying $V_{SER,t}$ as a function of the SVR secondary side current magnitude I_{pu} , and it can be confirmed that a single line approximates $V_{SER,t}$ over the entire operating period.

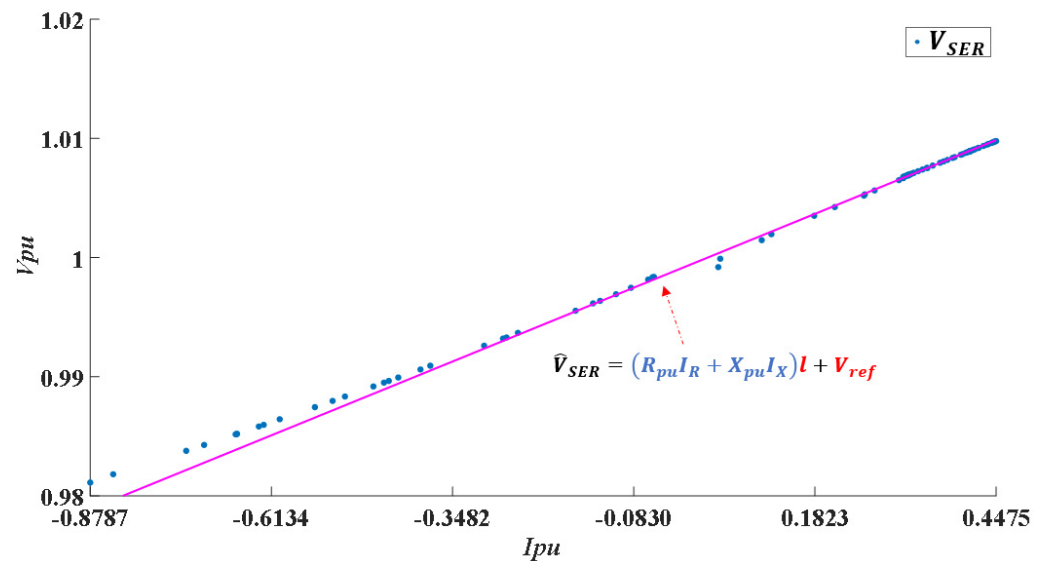


Figure 9. V_{SER} fitting result using the single linear LDC parameterization method.

3.2.2. Piecewise LDC Parameter Design

The single LDC method does not reflect the difference in $V_{SER,t}$ characteristics between forward and reverse power flow, and thus the $V_{SER,t}$ fitting accuracy may deteriorate in systems with a high proportion of reverse power flow caused by DERs. To address this, this paper introduces a piecewise LDC method that applies separate LDC parameters depending on the direction of power flow. The modern SVR controller, which is already installed and in operation in the domestic distribution system, supports the individual setting of LDC parameters according to the direction of power flow. Specifically, the FWD LDC parameters are applied during forward power flow, and the REV LDC parameters are applied independently during reverse power flow. The direction of power flow is determined based on the magnitude and phase of the current measured at the SVR secondary side, and the current threshold parameters 50FWDP and 50REVP are set in the controller for this purpose. The piecewise LDC method directly utilizes this parameter structure of the controller, and is thus practically significant in that it can be applied as is to an already installed SVR controller without additional metering equipment or communication infrastructure.

In the piecewise LDC, the reference voltage $\hat{V}_t$ is defined such that the LDC parameters applied to the forward and reverse power flow intervals are distinguished by the binary variable Z_t , as given in Equation (15).

$$\hat{V}_t = \begin{cases} (R_{pu} I_{R,t} + X_{pu} I_{X,t}) \cdot I_{fwd} + V_{ref,fwd} & \text{if } Z_t = 1 (\text{forward power flow}) \\ (R_{pu} I_{R,t} + X_{pu} I_{X,t}) \cdot I_{rev} + V_{ref,rev} & \text{if } Z_t = 0 (\text{reverse power flow}) \end{cases} \quad (15)$$

The binary variable Z_t is determined by comparing the active current component $I_{R,t}$ defined earlier, at the SVR secondary side with the current threshold I_{dir} , as given in Equation (16).

$$Z_t = \begin{cases} 1 & \text{if } I_{R,t} \geq I_{dir} \\ 0 & \text{if } I_{R,t} < I_{dir} \end{cases} \quad (16)$$

The controller can independently set the forward and reverse power flow regions through the two current thresholds 50FWDP and 50REVP. However, when BIASMODE is set, the forward and reverse power flow regions can be distinguished using a single current threshold. Accordingly, this paper defines a single current threshold I_{dir} as an optimization variable, whose sign and allowable range vary depending on the type of

BIASMODE. Expressing this using the binary variable b_{pos} yields the linear inequality given in Equation (17).

$$-0.1 + 0.11 \cdot b_{pos} \leq I_{dir} \leq -0.01 + 0.11 \cdot b_{pos} \quad (17)$$

In Equation (17), when $b_{pos} = 1$, $I_{dir} \in [0.01, 0.1]$, which corresponds to the BIASMODE = REV setting. In this case, the setting of 50REVP has no effect, so that I_{dir} is entered as the value of 50FWDP. When $b_{pos} = 0$, $I_{dir} \in [-0.1, -0.01]$, corresponding to the BIASMODE = FWD setting. In this case, the setting of 50FWDP has no effect, so that the magnitude of I_{dir} is entered as the value of 50REVP. The current threshold I_{dir} is expressed as a per unit value of the rated secondary current of the CT (0.2 A), and the allowable range in Equation (17) corresponds to 1% to 10% of the rated current, which is the setting range of the current thresholds 50FWDP and 50REVP of the controller (0.002 to 0.02 A). Once b_{pos} and I_{dir} are determined through optimization, the BIASMODE setting to be applied and the corresponding current threshold are established, and Z_t is determined at each time step by comparing the measured active current component $I_{R,t}$ with I_{dir} , so that the LDC parameters appropriate for the corresponding power flow region are applied. The piecewise LDC parameter derivation problem is formulated as the MIQP given in Equations (15)–(24). As in the single LDC method, the objective function minimizes the sum of squared errors between the LDC reference voltage $\hat{V}_t$ and $V_{SER,t}$ over the entire operating period, while the forward and reverse LDC parameters ($I_{fwd}, V_{ref,fwd}, I_{rev}, V_{ref,rev}$), the current threshold I_{dir} , and the binary variable b_{pos} are simultaneously optimized.

$$\min \sum_{t=1}^T (\hat{V}_t - V_{SER,t})^2 \quad (18)$$

In addition, as inequality constraints, Equation (19) applies the same allowable sending end voltage range constraints as Equation (13) in Section 3.2.1. Equation (20) constitutes the same constraints as in the single linear LDC parameter design, constraining the line length to be determined within a range that can be set according to the system conditions and the reference voltage to be maintained within the allowable voltage range of the system, applied to the FWD and REV parameters, respectively. Equation (21) indicates that Z_t and b_{pos} are binary variables.

$$V_{SER,min,t} \leq \hat{V}_t \leq V_{SER,max,t}, \forall t \quad (19)$$

$$0 \leq I_{fwd}, I_{rev} \leq I_{max}, V_{ref,min} \leq V_{ref,fwd}, V_{ref,rev} \leq V_{ref,max} \quad (20)$$

$$Z_t \in \{0,1\}, b_{pos} \in \{0,1\} \quad (21)$$

In this study, the bounds in Equation (20) are set to $I_{max} = 18$, $V_{ref,min} = 0.96 \text{ p.u.}$, and $V_{ref,max} = 1.02 \text{ p.u.}$ Equations (15) and (16) are implemented in the solver through the following big-M constraints.

$$-M(1 - Z_t) \leq \hat{V}_t - (g_t \cdot I_{fwd} + V_{ref,fwd}) \leq M(1 - Z_t), \forall t \quad (22)$$

$$-MZ_t \leq \hat{V}_t - (g_t \cdot I_{rev} + V_{ref,rev}) \leq MZ_t, \forall t \quad (23)$$

$$-M(1 - Z_t) \leq I_{R,t} - I_{dir} \leq MZ_t, \forall t \quad (24)$$

Here, M is a sufficiently large constant, and $M = 10$ is used in this study. When $Z_t = 1$, Equation (22) fixes $\hat{V}_t$ on the FWD line and Equation (23) is relaxed, and the opposite holds when $Z_t = 0$. Equation (24) makes Z_t consistent with the comparison between $I_{R,t}$ and I_{dir} in Equation (16). Since g_t and $I_{R,t}$ are known at each time step, all constraints are linear in the decision variables. The MIQP formulation is solved using the Gurobi Optimizer

version 12.0.3 through the Gurobi interface of MATPOWER. The MIP gap and the feasibility and optimality tolerances were kept at the default values of Gurobi (10^{-4} , 10^{-6} , and 10^{-6} , respectively). The derived parameters can be directly applied to the LDC parameter and BIASMODE setting structure of the controller. Figure 10 shows the parameter derivation results of the piecewise LDC method. The scatter plot shows the time-varying $V_{SER,t}$ as a function of the SVR secondary side current magnitude I_{pu} , and it can be confirmed that the forward and reverse power flow intervals are distinguished by the current threshold I_{dir} , with an independent LDC line applied to each interval.

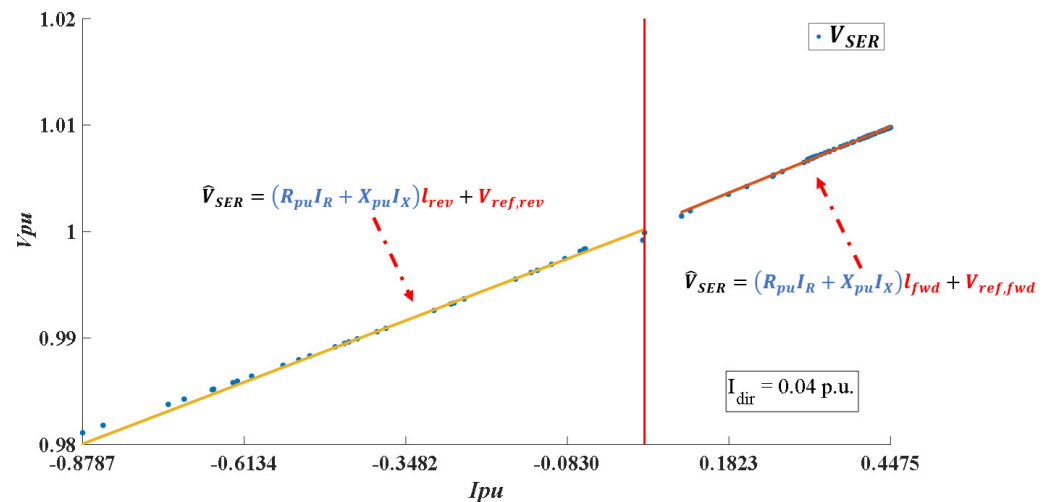


Figure 10. V_{SER} fitting result using the piecewise linear LDC parameterization method.

3.3. Practical Limitations of V_{SER} -Fitting-Based LDC Parameter Design

Both the single and piecewise LDC methods presented in Section 3.2 are formulated to minimize the tracking error between $V_{SER,t}$ and the reference voltage $\hat{V}_t$. By distinguishing between forward and reverse power flow intervals, the piecewise LDC can, in principle, approximate $V_{SER,t}$ more precisely than the single LDC. However, simulation results obtained that the piecewise LDC can in fact yield lower voltage quality than the single LDC. To identify the cause of this paradox, this section systematically analyzes the practical limitations inherent in LDC parameter design based on $V_{SER,t}$ tracking.

3.3.1. Implementable Gap Between $V_{SER,t}$ and Practical SVR

$V_{SER,t}$ is a theoretically appropriate target value for keeping downstream bus voltages close to the nominal voltage. However, the fact that $V_{SER,t}$ is a good target value does not imply that an actual SVR can implement this value exactly as specified. This section quantitatively evaluates this implementable gap.

All simulation results presented in this and the following subsections were obtained on the 13-bus distribution system shown in Figure 11. The feeder consists of a primary side section extending from the substation to the SVR installation point and a secondary side section extending from the SVR to the end of the feeder. To emulate conditions with large voltage variation, a large capacity PV is interconnected at the end of the secondary side. Three system configurations were defined by varying the ratio of load capacity allocated to the primary and secondary sections. The total load is identical across all cases at 9750 kW, with all loads assumed to have a power factor of 0.95 (lagging), differing only in how it is distributed between the primary and secondary sides. The load and PV data used in the simulation are 15-min resolution, five-day profiles, shown in Figure 12. The detailed system and scenario specifications are summarized in Table 1.

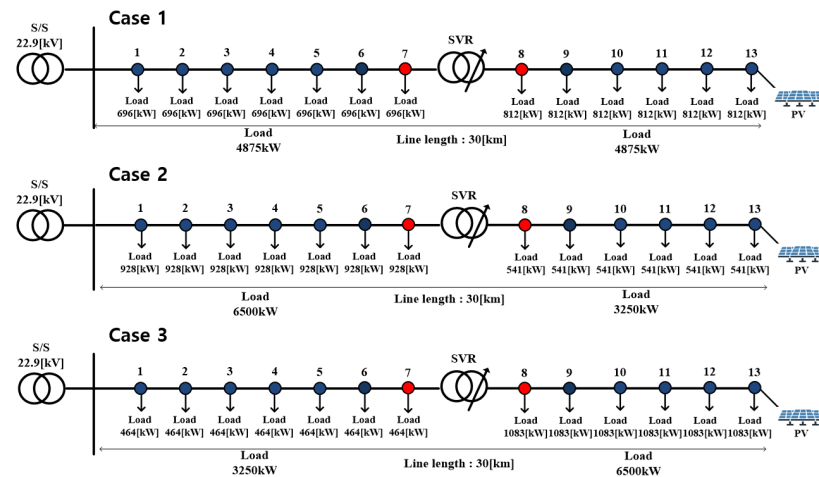


Figure 11. Modeling of the distribution system.

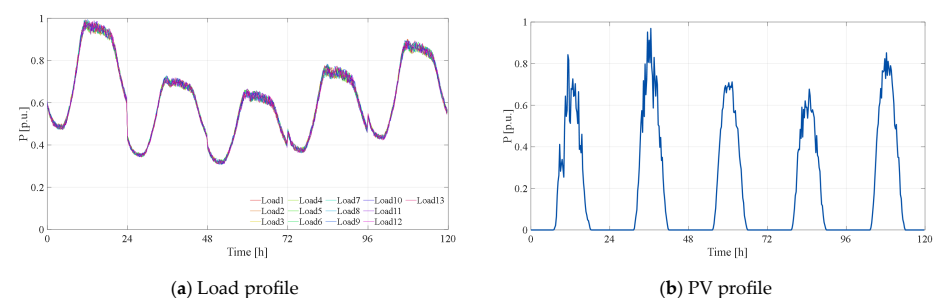


Figure 12. Load and PV profiles used in the simulation (5 days, 15-min resolution).

To evaluate the implementability of $V_{SER,t}$ itself, the following three operating modes were defined and compared for each of the nine scenarios. Base mode is an uncontrolled SVR mode in which the tap position is fixed at 0, with no tap operation. Ideal V_{SER} mode assumes that the SVR secondary voltage tracks $V_{SER,t}$ continuously and exactly at every time step, without deadband or tap constraints. Practical V_{SER} mode sets the reference voltage as $\hat{V}_t = V_{SER,t}$, but operates with the actual SVR's deadband and integer tap constraints included.

The performance of each mode was evaluated using the following indices. The System Nominal Voltage Performance Index (SNVPI) indicates how close the bus voltages remain to the nominal voltage, defined in Equation (25).

$$SNVPI = \sum_{t=1}^T \sum_{i=1}^N (V_{nom} - V_{i,t})^2 \quad (25)$$

Here $V_{i,t}$ is the voltage magnitude at bus i at time t , and V_{nom} is the nominal voltage. The value calculated over all buses is denoted $SNVPI_{all}$, and the value calculated over the set of buses downstream of the SVR is denoted $SNVPI_{downstream}$. A smaller SNVPI indicates that the corresponding bus voltages were kept closer to the nominal voltage, meaning higher voltage quality. The tracking accuracy of the SVR secondary voltage with respect to $V_{SER,t}$, is defined as TrackRMSE, given in Equation (26).

$$TrackRMSE = \sqrt{\frac{1}{T} \sum_{t=1}^T (V_{SVR,t} - V_{SER,t})^2} \quad (26)$$

Table 1. Simulation system and scenario specifications.

Category	Index	Value
System specifications	Rated Power	10 MVA
	Rated Voltage	22.9 kV
	Rated Frequency	60 Hz
	Conductor type	ACSR 160 mm ² (0.00347 + j0.00746 p.u./km)
	Load power factor	0.95 (Lagging)
	Allowable voltage range	0.96~1.02 p.u.
SVR specifications	Tap adjustment range	±16 taps (±10%)
	Tap step size	0.625% (0.75 V)
	Deadband	0.01667 (2 V, ±1 V)
Load composition by case	Case 1 (Primary = Secondary)	Primary side: 4875 kW Secondary side: 4875 kW
	Case 2 (Primary > Secondary)	Primary side: 6500 kW Secondary side: 3250 kW
	Case 3 (Primary < Secondary)	Primary side: 3250 kW Secondary side: 6500 kW

In Equation (26), $V_{SVR,t}$ is the SVR secondary voltage at time t . TrackRMSE is meaningful only when the SVR is actually operated with reference to $V_{SER,t}$ so it is not defined for operating modes such as Base mode that do not use $V_{SER,t}$ as the tracking target. The total number of tap operations (TapOps) denotes the cumulative number of tap changes that occurred over the entire simulation period, and the maximum and minimum tap positions denote the highest and lowest tap positions reached during the simulation. Because TapOps is meaningful only when the tap position changes in integer steps, it is not defined for Ideal V_{SER} mode. The results computed using the above indices are summarized in Table 2.

The following conclusions can be drawn from the results in Table 2. First, across all nine scenarios, Ideal V_{SER} mode significantly reduces both $SNVPI_{all}$ and $SNVPI_{downstream}$ relative to Base mode. This improvement is most pronounced for Case 3, PV = 5 MW, where $SNVPI_{all}$ decreases by approximately 80.6%, from 9.595 under Base mode to 1.85983 under Ideal V_{SER} mode, and $SNVPI_{downstream}$ likewise improves substantially, from 7.928 to 0.207. This result indicates that $V_{SER,t}$ is a theoretically well founded reference value, derived by reflecting the system characteristics and sensitivity information of the feeder.

Second, even when operated with reference to the same $V_{SER,t}$, the performance of Practical V_{SER} mode does not match that of Ideal V_{SER} mode. Across all nine evaluated scenarios, $SNVPI_{all}$ under Practical V_{SER} mode is consistently larger than under Ideal V_{SER} mode, indicating a degradation in voltage quality. This occurs because the actual SVR secondary voltage does not exactly coincide with $V_{SER,t}$, a discrepancy that arises from three structural factors of the SVR, namely its deadband, discrete integer tap positions, and physical tap limits. The fact that performance degrades in the same direction under every condition indicates that this is not an exceptional phenomenon confined to a particular system configuration of PV capacity, but rather a limitation structurally inherent to actual SVRs with integer taps and a deadband.

Third, TapOps under Practical V_{SER} mode quantifies the tap operation burden required to track the continuous $V_{SER,t}$ using integer taps. In all three system configurations, TapOps increases as PV capacity increases, showing that higher PV penetration produces larger temporal variation in $V_{SER,t}$ itself, which in turn requires more frequent tap operations to track it in integer tap units. Comparing the minimum tap position also shows that

Ideal V_{SER} mode yields fractional values such as -1.87 and -3.52 whereas Practical V_{SER} mode yields integer values such as -1 and -3 . Because Ideal V_{SER} mode tracks $V_{SER,t}$ continuously without the integer step constraint of an actual tap changer, the tap position in this mode is a continuous quantity obtained by inversely mapping the required voltage correction through the fixed per tap voltage step, rather than an operationally realizable tap position. Since $V_{SER,t}$ is not constrained to align with the discrete voltage levels corresponding to integer tap positions, this inverse mapping generally does not yield an integer value. This illustrates the gap between the theoretical tap position required to track $V_{SER,t}$ most precisely and the integer tap position that can actually be implemented.

Table 2. Comparison of Base, Ideal V_{SER} , and Practical V_{SER} modes across nine scenarios.

Case	PV [MW]	Mode	SNVPI	SNVPI _{downstream}	TrackRMSE	TapOps	Max Tap	Min Tap
1	5	Base	6.58388	5.25684	-	0	0	0
		Ideal V_{SER}	1.43091	0.10926	0	-	14.01001	2.83325
		Practical V_{SER}	1.49914	0.17746	0.00460	57	13	4
	10	Base	5.35260	4.25159	-	0	0	0
		Ideal V_{SER}	1.20602	0.11013	0	-	14.01001	-1.86865
		Practical V_{SER}	1.28792	0.19208	0.00475	107	13	-1
	15	Base	4.93287	3.94773	-	0	0	0
		Ideal V_{SER}	1.14488	0.16352	0	-	14.01001	-5.83423
		Practical V_{SER}	1.23132	0.24997	0.00484	149	13	-5
2	5	Base	4.29953	3.24786	-	0	0	0
		Ideal V_{SER}	1.09494	0.04509	0	-	11.00952	1.15625
		Practical V_{SER}	1.15204	0.10219	0.00444	47	10	2
	10	Base	3.53934	2.66738	-	0	0	0
		Ideal V_{SER}	0.94289	0.07247	0	-	11.00952	-3.52222
		Practical V_{SER}	1.00613	0.13573	0.00467	95	10	-3
	15	Base	3.41896	2.63619	-	0	0	0
		Ideal V_{SER}	0.94235	0.15939	0	-	11.00952	-7.20630
		Practical V_{SER}	1.00153	0.21858	0.00466	141	10	-6
3	5	Base	9.59471	7.92835	-	0	0	0
		Ideal V_{SER}	1.85983	0.20716	0.00089	-	16	4.58374
		Practical V_{SER}	1.90927	0.25648	0.00464	67	16	5
	10	Base	7.80361	6.41970	-	0	0	0
		Ideal V_{SER}	1.55264	0.18106	0.00076	-	16	-0.36597
		Practical V_{SER}	1.63218	0.26064	0.00480	117	16	0
	15	Base	7.02519	5.79004	-	0	0	0
		Ideal V_{SER}	1.43045	0.20643	0.00072	-	16	-4.40698
		Practical V_{SER}	1.50991	0.28593	0.00483	161	16	-4

These results show that, while $V_{SER,t}$ is a theoretically appropriate target for improving bus voltage quality, relying on $V_{SER,t}$ fitting alone without further modification is not sufficient to guarantee the actual operating outcome of an actual SVR. The performance degradation of Practical V_{SER} mode relative to Ideal V_{SER} mode is not a problem with $V_{SER,t}$ itself, but rather stems from the fact that the deadband-based discrete tap control characteristics of an actual SVR are not reflected in the objective function used to derive the LDC parameters. Therefore, to achieve superior voltage-regulation performance under real SVR operating conditions, the design must go beyond simply treating $V_{SER,t}$ as the target value and must be reformulated so that the deadband decision logic and the temporal

variation characteristics of the reference voltage of an actual SVR are explicitly reflected in the LDC parameter derivation objective function. Section 3.3.2, which follows, analyzes these limitations inherent in the $V_{\text{SER},t}$ -tracking-based objective function.

3.3.2. Limitations of the Conventional Piecewise Objective Function

The piecewise LDC of Section 3.2.2 is formulated to minimize the sum of squared errors between $\hat{V}_t$ and $V_{\text{SER},t}$ over the entire operating period. $\hat{V}_t$ is a reference voltage computed according to the instantaneous power flow condition, and the actual SVR adjusts its tap to bring the measured voltage close to this reference voltage. Accordingly, the more precisely $\hat{V}_t$ is designed to approximate $V_{\text{SER},t}$, the more sensitively the reference voltage itself responds to changes in power flow and is updated in a fine-grained manner, and it is natural that tap operations following this target also become more frequent. However, an actual SVR operates with a binary decision structure in which a tap operation is performed only when the difference between the measured voltage and the reference voltage exceeds the deadband and this characteristic is not reflected in the objective function of the conventional piecewise LDC. That is, the objective function minimizes the error itself unconditionally, regardless of whether the magnitude of the error actually affects the SVR's tap decision, and consequently some of the tap operations occurring in the process of finely updating the reference voltage may in fact be unnecessary. To quantitatively evaluate this, the normalized tracking error is defined as follows.

$$r_t = \frac{|\hat{V}_t - V_{\text{SER},t}|}{\frac{\text{DB}}{2}} \times 100 [\%] \quad (27)$$

Here, DB is the deadband width set in the actual SVR controller. A time step with $r_t \leq 100$ indicates that the error lies within the actual deadband half width and therefore does not directly affect the SVR's tap decision, whereas a time step with $r_t > 100$ indicates that this half width has been exceeded.

To characterize the distribution of r_t over the entire operating period, percentiles were calculated for the r_t time series of each scenario. P50, P75, P90, and P95 denote the points at or below which the corresponding percentage of all time steps have their r_t values. For example, P50 indicates that half of all time steps lie at or below this value, and P95 indicates that 95% of all time steps lie at or below this value. Max is the largest r_t value observed among all time steps. Calculating the r_t percentiles of the piecewise LDC across all nine scenarios showed that P50 was very low in every scenario, approximately 7% on average. That is, the piecewise LDC minimizes the error down to a small fraction of the deadband half width at most time steps. This indicates that the reference voltage closely reflects even minor fluctuations in $V_{\text{SER},t}$ at most time steps.

To examine the extent of tap operations that occur when actually tracking such a finely updated reference voltage, a simulation was performed using the system, load, and PV profiles from Section 3.3.1 and reflecting the actual deadband and integer tap constraints of the SVR, in the same manner as in Section 3.3.1. The resulting cumulative number of tap operations (TapOps) of the piecewise LDC over the five-day simulation was 964 across the nine scenarios in total, the highest among the alternatives compared later. This is a result of the fine updating of the reference voltage leading to frequent tap operations, as anticipated. However, the issue is that a substantial portion of these tap operations may in fact be unnecessary. The very low P50 of r_t indicates that, at most time steps, the difference between the reference voltage and $V_{\text{SER},t}$ falls well short of the deadband half width. This suggests that the reference voltage continues to be updated to track differences that are too minor to affect the actual tap decision. Consequently, a substantial portion of the tap operations is judged to be spent tracking meaningless differences within the deadband.

To confirm this, two terms of different character were each added independently to the objective function. The first is a term that imposes a penalty only when the difference between the reference voltage and $V_{SER,t}$ exceeds a designed tolerance (DB term). This term explicitly reflects, in the objective function, the characteristic that an actual SVR does not respond to errors within the deadband. It thereby attempts to derive LDC parameters that are compatible with the actual tap control characteristics of the SVR. The objective function of the piecewise LDC has no such threshold and unconditionally minimizes the error itself, whereas the DB term imposes a penalty only when the error exceeds this threshold. The second is a term that imposes a penalty directly on the magnitude of change in the reference voltage between adjacent time steps (Smooth term). The exact mathematical formulations of both terms are presented in Section 3.4. This section examines their respective roles through the resulting changes in the r_t distribution and TapOps when each term is added independently.

The results of adding the DB term alone, DB-only, were nearly identical to those of the piecewise LDC. As shown in Figure 13, the shape and location of the r_t distribution were virtually indistinguishable between the two methods across all nine scenarios, and the total TapOps also changed only marginally, from 964 to 962. This is interpreted as follows. Although reflecting the deadband characteristic in the objective function through the DB term is a valid direction in principle, the designed deadband half width introduced at this stage was larger than the error level already achieved by the existing least squares fit of the piecewise LDC, so the constraint did not act effectively. The piecewise LDC is designed to minimize the error itself without any threshold on its magnitude, and in doing so already produces errors smaller than the designed deadband half width at most time steps. Consequently, there are hardly any time steps at which the error actually exceeds the threshold at which the DB term begins to impose a penalty, and adding the DB term therefore has no meaningful effect on the objective function. In other words, the DB term reflects the deadband characteristic in a valid direction, but its effect does not manifest when added alone on top of an already excessively precise existing fit, and the reference voltage continues to be updated unnecessarily finely, leaving tap operations unreduced. This shows that limiting the absolute magnitude of the error alone cannot resolve the problem of excessive updating of the reference voltage.

The results of adding the Smooth term alone, SmoothOnly, were, in contrast, markedly different. TapOps decreased substantially across all nine scenarios, from 964 to 725, a reduction of approximately 24.8%. This shows that suppressing the temporal variation in the reference voltage itself, rather than the absolute magnitude of the error, directly contributes to reducing the unnecessary updating identified earlier and thereby to an actual reduction in tap operations. However, this improvement came at a cost. As shown in Figure 13, the entire r_t distribution shifted noticeably above the 100% reference line, and in the three scenarios with high PV penetration (PV = 15 MW), the P50 itself already exceeded 100%, reaching 183 to 194%. This means that, in these scenarios, the reference voltage was outside the actual deadband for more than half of the total operating time. That is, the Smooth term reduces tap operations by suppressing unnecessary updating of the reference voltage, but because it does not limit the magnitude of the error at individual time steps, it fails to control the risk of the reference voltage exceeding the actual deadband range of the SVR.

These results indicate that finely updating the reference voltage does not by itself guarantee a reduction in tap operations. They further indicate that suppressing the temporal variation in the reference voltage is more effective for this purpose than limiting the absolute magnitude of the error. The DB term is an attempt to reflect the actual deadband characteristic of the SVR in the objective function, but because the existing fit of the piece-

wise LDC already produces errors more precise than this threshold, it has no meaningful effect when added alone. The Smooth term is the key mechanism that reduces unnecessary tap operations by suppressing the temporal variation in the reference voltage, but because it does not limit the magnitude of the error at individual time steps, it carries the risk of the reference voltage exceeding the actual deadband range of the SVR in this process. Therefore, to safely secure the substantial benefit produced by the Smooth term, the DB term is also required to constrain it from exceeding the deadband half width. Section 3.4 proposes a formulation that combines both terms to meet this requirement.

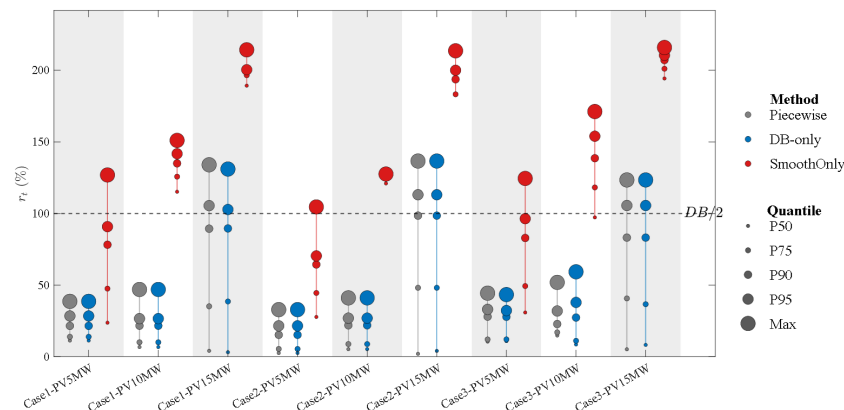


Figure 13. r_t Distribution Comparison for Piecewise, DB-only and SmoothOnly term.

3.4. Practical SVR-Aware PiecewiseDB Formulation

Based on the analysis in Section 3.3, this section proposes a PiecewiseDB (Deadband-aware Piecewise) formulation that incorporates both a deadband-aware term and a reference voltage smoothing term into the objective function of the conventional piecewise LDC. The objective function of PiecewiseDB consists of the following three terms.

$$\min\{\lambda_{\text{track}}J_{\text{track}} + \lambda_{\text{DB}}J_{\text{DB}} + \lambda_{\text{smooth}}J_{\text{smooth}}\} \quad (28)$$

$$J_{\text{track}} = \sum_{t \in T} (\hat{V}_t - V_{\text{SER},t})^2 \quad (29)$$

$$J_{\text{DB}} = \sum_{t \in T} \left[\max\left(0, |\hat{V}_t - V_{\text{SER},t}| - \frac{\text{DB}_{\text{des}}}{2}\right) \right]^2 \quad (30)$$

$$J_{\text{smooth}} = \sum_{t \in T, t \geq 2} (\hat{V}_t - \hat{V}_{t-1})^2 \quad (31)$$

The tracking term J_{track} minimizes the sum of squared errors between $\hat{V}_t$ and $V_{\text{SER},t}$ in the same manner as the conventional piecewise LDC. The deadband-aware term J_{DB} formalizes the DB term introduced in Section 3.3.2. It equals zero, and thus has no effect on the objective function, when the difference between $\hat{V}_t$ and $V_{\text{SER},t}$ lies within the designed deadband half width $\frac{\text{DB}_{\text{des}}}{2}$, and imposes a penalty proportional to the excess only when this range is exceeded. The smoothing term J_{smooth} formalizes the Smooth term introduced in Section 3.3.2, imposing a penalty directly on the magnitude of change in $\hat{V}_t$ between adjacent time steps, and its summation starts from $t = 2$ because $\hat{V}_0$ is not defined. The deadband-aware term in Equation (30) is implemented through the following slack-variable constraint, in which the absolute value is expressed by two linear inequalities.

$$\hat{V}_t - V_{\text{SER},t} \leq \frac{\text{DB}_{\text{des}}}{2} + \xi_t, \quad V_{\text{SER},t} - \hat{V}_t \leq \frac{\text{DB}_{\text{des}}}{2} + \xi_t, \quad \xi_t \geq 0 \quad (32)$$

Here, ξ_t is a slack variable that takes a positive value only when the difference between $\hat{V}_t$ and $V_{SER,t}$ exceeds the designed deadband half width and a penalty in the form of ξ_t^2 is imposed on it in the objective function. Equation (32) only constrains ξ_t from below by the excess of $|\hat{V}_t - V_{SER,t}|$ over $\frac{DB_{des}}{2}$. Since ξ_t appears in no other constraint and any increase of ξ_t only increases the penalty ξ_t^2 with $\lambda_{DB} > 0$, ξ_t takes this lower bound in the solution, as given in Equation (33).

$$\xi_t = \max\left(0, |\hat{V}_t - V_{SER,t}| - \frac{DB_{des}}{2}\right) \quad (33)$$

Applying Equations (29)–(31) requires determining the three weights λ_{track} , λ_{DB} and λ_{smooth} , as well as the deadband width. Because the three terms measure errors that differ in both frequency and magnitude, the weights are set with consideration of the raw scale each term has prior to weighting. The tracking term J_{track} is a global term that acts continuously over the entire operating period, and $\lambda_{track} = 1$ is set as the reference scale. The deadband-aware term J_{DB} is a conditional term that is activated only during time steps when the error exceeds the deadband, and its raw scale is substantially smaller because it equals zero at most time steps. Accordingly, a relatively large weight of, $\lambda_{DB} = 10^4$ is applied so that this term has a meaningful influence on the solution. The smoothing term J_{smooth} is a local regularization term that acts continuously between all adjacent time steps. Its raw scale is similar to the tracking term, and a weight of $\lambda_{smooth} = 10^2$ is applied to reflect its effect. For the deadband width in Equations (30) and (32), a value smaller than the actual deadband set in the SVR controller was applied at the parameter derivation stage. Because the deadband-aware term imposes no penalty when the error lies within the designed half width, the optimization result tends to form near this boundary. However, $V_{SER,t}$ is derived in Section 3.1 based on a linear approximation of the tap sensitivity, and $\hat{V}_t$ is likewise the result of optimization over a continuous variable. Therefore, a result formed near this boundary during optimization is not guaranteed to remain within the actual deadband when evaluated through a simulation that reflects the discrete tap operation and the default deadband setting of the SVR controller. Accordingly, the designed deadband is determined from specifications of the SVR controller rather than by tuning. The actual deadband half width is set to $\frac{DB}{2} = 0.008333$ p.u. (1 V), which is the default setting of the modern SVR controller [9–11]. The designed deadband is set to $DB_{des} = 0.0125$ p.u., so that its half width, $\frac{DB_{des}}{2} = 0.00625$ p.u. (0.75 V), is equal to the voltage change of a single tap step. This corresponds to $(\frac{DB_{des}}{2}) / (\frac{DB}{2}) = 75\%$ of the actual deadband half width. This means that, when the difference between the reference voltage and $V_{SER,t}$ lies within a single physical tap step of the SVR, it is regarded as within the normal adjustable range. In the optimization, Equations (30) and (32) penalize the deviation of $\hat{V}_t$ from $V_{SER,t}$ only beyond $\frac{DB_{des}}{2}$, while the smoothing term moves $\hat{V}_t$ away from $V_{SER,t}$ to reduce the variation in the reference voltage. Since λ_{DB} is much larger than λ_{smooth} , the deviation increases up to $\frac{DB_{des}}{2}$ and is not increased beyond it, unless $V_{SER,t}$ itself varies too rapidly. Consequently, the deviation in the solution is limited to approximately 75% of the actual half width, and the remaining 25% is retained as a margin for the discrepancy that may arise between the linear approximation and the discrete tap operation of the actual implementation. The remaining constraints, namely the piecewise model selection constraint, the power flow direction determination constraint, and the BIASMODE allowable range constraints on I_{dir} , are applied identically to those of the piecewise LDC parameter derivation formulation in Section 3.2.2. The derived LDC parameters can be directly applied to the FWD/REV LDC parameter and BIASMODE settings of a modern SVR controller, just as with the Piecewise LDC of Section 3.2.2. In this way, rather than driving $\hat{V}_t$ to precisely track $V_{SER,t}$,

PiecewiseDB is designed to allow a margin in tracking precision within the deadband range and instead to prioritize deriving a temporally smooth reference voltage trajectory.

Compared with existing approaches, PiecewiseDB differs in the following respects. Existing approaches mainly update the reference voltage, the deadband, or the LDC parameters dynamically using measurements or models of the network, which requires information from other points of the feeder or periodic parameter updates during operations. In addition, the LDC parameters are determined by minimizing the difference from the ideal sending end voltage, and the deadband characteristic of the controller is not reflected in the calculation formula in this process. In contrast, PiecewiseDB derives the forward and reverse LDC parameters offline as static controller settings and reflects the deadband of the controller in the objective function. Consequently, PiecewiseDB keeps the voltages of the downstream buses close to the nominal voltage through the LDC parameter design itself, without additional communication or online parameter updates.

4. Performance Evaluation and Validation

4.1. Simulation Setup

This chapter verifies the effect of the PiecewiseDB formulation proposed in Section 3.4 and evaluates its system level performance when applied to actual SVR operation. The simulation uses the same 13 bus distribution system and scenarios as those used in Section 3.3.1, and the evaluation was performed for nine scenarios combining the load distribution conditions of Cases 1 to 3 with PV capacities of 5, 10, and 15 MW. In each scenario, the LDC parameters were derived using 15-min interval, five-day load and PV output profiles, and the derived parameters were applied to a simulation reflecting the actual deadband and integer tap constraints of the SVR for performance evaluation. The performance was evaluated using the SNVPI and TapOps defined in Section 3.3.1, where the SNVPI was calculated both over all buses and over the buses downstream of the SVR. Voltage limit violations were evaluated by the overvoltage (OV) count and the undervoltage (UV) count, defined as the number of bus-time samples, among the 13 buses and all time steps, whose voltage exceeds 1.02 p.u. or falls below 0.96 p.u., respectively. The weighting factors of PiecewiseDB were set to the values given in Section 3.4 ($\lambda_{\text{track}} = 1$, $\lambda_{\text{DB}} = 10^4$, $\lambda_{\text{smooth}} = 10^2$), and their influence is analyzed in Section 4.4. In Sections 4.2–4.4, the LDC parameter derivation and the performance evaluation were performed on the same five-day profiles, and the validation on a different day whose load and PV profiles were not used for the LDC parameter derivation is presented separately in Section 4.5, and the effect of the controller input resolution is examined in Section 4.6.

The simulation is based on the COGEN mode described in Section 2.3.3, with BIASMODE set to FWD or REV. Since the BIASMODE setting assigns the no-torque region to either the forward or the reverse region, the power flow region is determined as a binary choice by comparing the active current component with the current threshold. Accordingly, the no-torque region is not modeled as a separate operating state, and BIASMODE is regarded as a fixed setting that is not changed during the simulation. The simulation also assumes that the tap position settles within each 15-min time step, and the time delay and the tap actuation time of the controller are not modeled.

4.2. Effect of the PiecewiseDB Formulation

This section verifies whether the PiecewiseDB formulation proposed in Section 3.4 actually produces its intended effect. To this end, the r_t quantile distribution was calculated and compared for four methods, Piecewise, DB-only, SmoothOnly and PiecewiseDB, following the same procedure as in Section 3.3.2. The resulting distributions are presented in Figure 14 and summarized in Table 3.

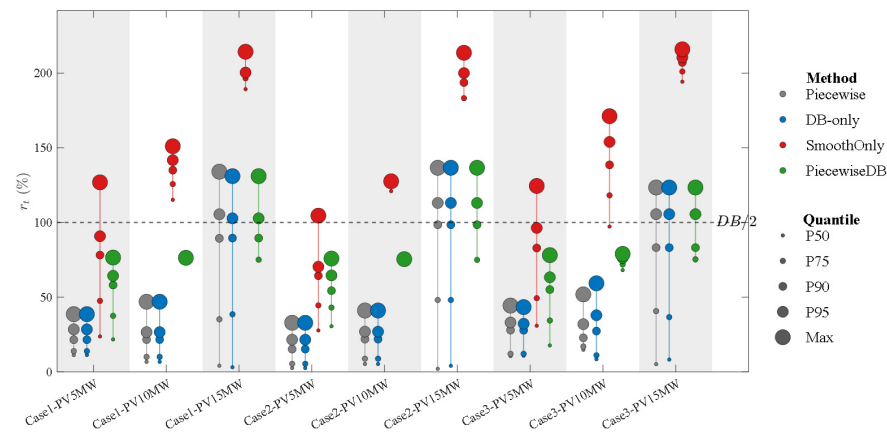


Figure 14. Validation of the PiecewiseDB formulation via r_t distribution.

The r_t distribution of PiecewiseDB showed a marked difference from that of Piecewise. Piecewise exhibited an average P50 of only about 7% and an average P75 of only about 21% across all scenarios, meaning that the difference between the reference voltage and $V_{SER,t}$ remained a small fraction of the deadband half width at most time steps. In contrast, both P50 and P75 of PiecewiseDB were higher than those of Piecewise in all nine scenarios without exception, indicating that the difference between the reference voltage and $V_{SER,t}$ was maintained much closer to the actual deadband half width. In particular, in the six scenarios with PV = 10 and 15 MW, the P50 of PiecewiseDB reached approximately 68 to 75% of the deadband half width. The upper end of this range coincides with the ratio of the designed half width to the actual deadband half width, at which the deviation is limited by Equations (30) and (32) as explained in Section 3.4. The values below 75% correspond to time steps at which the deviation does not reach this limit. That is, rather than unnecessarily narrowing the error within the deadband as Piecewise does, PiecewiseDB actively utilizes the margin over which an actual SVR does not respond in constructing the reference voltage. At the upper quantiles of P90 and above, the same tendency was maintained in the six scenarios with low or moderate PV penetration (PV = 5, 10 MW), with PiecewiseDB exhibiting values closer to DB/2 than Piecewise. This tendency was also maintained in the three scenarios with the highest PV penetration (PV = 15 MW): the P90, P95, and Max values of PiecewiseDB were equal to or closer to DB/2 than those of Piecewise in every scenario. Given that r_t had already exceeded 100% for both methods in this range, this indicates that PiecewiseDB does not exhibit any inferiority relative to Piecewise even under these extreme conditions, and maintains its consistency with $\frac{DB}{2}$. This tendency is judged to result from the greater temporal variation of $V_{SER,t}$ itself as PV penetration increases, with the magnitude of r_t in this range being primarily attributable to this sharp variation in $V_{SER,t}$ itself, rather than to the presence of the DB term or the size of the designed deadband half width. These results show how the individual effects of the DB term and the Smooth term, identified in Section 3.3.2, combine and operate in PiecewiseDB. DB-only, which applies only the DB term, exhibited a distribution nearly identical to that of Piecewise, indicating no meaningful effect when applied alone. SmoothOnly, which applies only the Smooth term, showed a P50 reaching 183 to 194% in the PV = 15 MW scenarios, with the entire distribution substantially exceeding the deadband half width. This is because the Smooth term, in suppressing the temporal variation in the reference voltage, does not constrain the magnitude of the error at individual time steps at all. By incorporating both terms together, PiecewiseDB retains the large scale shift in distribution produced by SmoothOnly, that is, the effect of raising the error close to the deadband half width, while its upper bound is constrained near the deadband half width by the DB term. That is, the DB term functions as a safeguard that keeps the reference voltage

variation produced by the Smooth term from exceeding the actual deadband range, while the Smooth term substantively relaxes the reference voltage within this safe range, thereby reducing tap operations. Neither term alone could achieve this outcome, and the marked increase in P50 and P75 and the substantial suppression of the violation rate observed for PiecewiseDB support the conclusion that this complementary interaction between the two terms is indeed realized.

Table 3. Summary of r_t quantiles by method across nine scenarios.

Case	PV [MW]	Method	P50 [%]	P75 [%]	P95 [%]	Max [%]
1	5	Piecewise	11.2	13.9	28.4	38.6
		DB-only	11.2	13.9	28.4	38.6
		SmoothOnly	23.7	47.5	90.8	126.9
		PiecewiseDB	21.7	37.5	64.3	76.5
	10	Piecewise	6.7	10.0	26.6	46.9
		DB-only	6.7	10.0	26.6	46.9
		SmoothOnly	115.2	125.7	141.7	151.1
		PiecewiseDB	74.0	74.8	75.3	76.4
	15	Piecewise	4.1	35.2	105.5	134.0
		DB-only	3.1	38.6	102.8	131.0
		SmoothOnly	189.3	196.6	200.4	214.4
		PiecewiseDB	74.5	75.1	102.8	131.0
2	5	Piecewise	2.5	5.4	21.5	32.8
		DB-only	2.5	5.4	21.5	32.8
		SmoothOnly	27.7	44.5	70.4	104.6
		PiecewiseDB	30.5	43.0	64.6	75.9
	10	Piecewise	5.2	8.8	26.9	41.1
		DB-only	5.2	8.8	26.9	41.1
		SmoothOnly	121.0	124.9	126.7	127.6
		PiecewiseDB	73.3	74.7	75.1	75.5
	15	Piecewise	2.0	48.1	113.1	136.7
		DB-only	4.0	48.1	113.1	136.7
		SmoothOnly	182.9	183.3	200.1	213.7
		PiecewiseDB	74.5	75.0	113.1	136.7
3	5	Piecewise	10.5	12.0	33.0	44.4
		DB-only	10.8	12.1	32.2	43.3
		SmoothOnly	30.8	49.3	96.4	124.5
		PiecewiseDB	17.7	34.4	63.3	78.1
	10	Piecewise	14.8	17.0	31.9	51.9
		DB-only	8.5	11.1	37.9	59.3
		SmoothOnly	97.3	118.2	154.0	171.2
		PiecewiseDB	68.1	71.9	76.3	79.0
	15	Piecewise	5.1	40.7	105.6	123.4
		DB-only	8.2	36.6	105.6	123.4
		SmoothOnly	194.3	201.1	210.5	216.0
		PiecewiseDB	74.6	75.4	105.6	123.4

The fact that PiecewiseDB forms a distribution that approaches the deadband half width without substantially exceeding it indicates that the reference voltage is being designed in a manner consistent with the binary decision structure of an actual SVR. That

is, although the reference voltage is formed near the deadband boundary, it remains largely within the range that does not affect the actual tap decision, which supports the conclusion that the objective function constructs the reference voltage by reflecting the actual control characteristics of the SVR, rather than by simply minimizing the error against $V_{SER,t}$.

4.3. Overall Voltage Quality Comparison

This section evaluates the system level voltage control performance of the proposed PiecewiseDB. To this end, the SNVPI, TapOps, and the number of OV and UV violations were compared across all nine scenarios for the three LDC design methods, Single, Piecewise, and PiecewiseDB. The results are presented in Table 4.

Table 4. Comparison of voltage control results for Single, Piecewise, and PiecewiseDB across nine scenarios.

Case	PV [MW]	Method	SNVPI	SNVPI _{downstream}	TapOps	OV Count	UV Count
1	5	Single	1.48505	0.16337	55	21	94
		Piecewise	1.48044	0.15874	55	21	94
		PiecewiseDB	1.46310	0.14115	42	1	94
	10	Single	1.25200	0.15618	115	37	73
		Piecewise	1.28591	0.19012	107	27	73
		PiecewiseDB	1.19715	0.10088	96	1	73
	15	Single	1.23954	0.25727	152	24	67
		Piecewise	1.26538	0.28360	157	26	67
		PiecewiseDB	1.18006	0.19790	144	2	67
2	5	Single	1.15689	0.10708	49	0	39
		Piecewise	1.15480	0.10497	47	0	39
		PiecewiseDB	1.13996	0.09003	35	0	39
	10	Single	1.01203	0.14165	105	5	31
		Piecewise	1.00643	0.13601	97	1	31
		PiecewiseDB	0.98208	0.11138	88	1	31
	15	Single	1.09903	0.31547	147	20	29
		Piecewise	1.06802	0.28450	139	0	29
		PiecewiseDB	1.03312	0.24945	128	0	29
3	5	Single	1.90796	0.25516	64	88	189
		Piecewise	1.91218	0.25938	66	89	189
		PiecewiseDB	1.89075	0.23758	58	54	189
	10	Single	1.54079	0.16894	116	56	139
		Piecewise	1.61647	0.24494	122	88	139
		PiecewiseDB	1.51639	0.14409	102	21	139
	15	Single	1.47604	0.25042	167	34	127
		Piecewise	1.52810	0.30371	174	94	127
		PiecewiseDB	1.40956	0.18439	158	25	127

The results in Table 4 clearly support the paradox raised in Section 3.3. Because the objective of the optimization problem defined in Section 3.1 is itself to keep the voltage at the buses downstream of the SVR close to the nominal voltage, SNVPI, which indicates whether this objective has actually been achieved, is the most critical metric in the system

level. In five of nine scenarios, however, the SNVPI of Piecewise was found to be even higher than that of Single, revealing that the piecewise LDC, which can theoretically approximate $V_{SER,t}$ more precisely than the single LDC by distinguishing between forward and reverse power flow, actually performs worse than the single LDC with respect to this core objective. This reversal is most pronounced in Case 3 with PV = 10 MW, where the SNVPI of Piecewise is actually about 4.9% worse than that of Single, and $SNVPI_{downstream}$ is also about 45% worse, increasing from 0.16894 to 0.24494. PiecewiseDB, in contrast, exhibited a lower SNVPI than both Single and Piecewise across all nine scenarios, achieving the voltage quality improvement intended by the objective function stably, without any reversal in which its performance falls below that of Single in any scenario. Even in Case3 with PV = 10 MW, the SNVPI of PiecewiseDB is improved by about 1.6% and 6.2% relative to Single and Piecewise, respectively, and $SNVPI_{downstream}$ is about 41% lower than that of Piecewise. That is, despite sacrificing some $V_{SER,t}$ tracking precision, PiecewiseDB outperformed both Single and Piecewise with respect to the ultimate objective of this paper, namely the voltage quality of the actual system. The voltage quality improvement was not achieved through more frequent tap operations. Although maintaining the voltage closer to the nominal voltage would generally be expected to require more frequent tap adjustments, PiecewiseDB also exhibited consistently lower TapOps than both Single and Piecewise across all nine scenarios. That is, PiecewiseDB simultaneously achieved SNVPI improvement and TapOps reduction, two objectives that would generally be expected to be in conflict. This is interpreted as resulting from the fact that, rather than simply tracking $V_{SER,t}$ precisely, PiecewiseDB excludes the unnecessary tracking precision within the deadband and derives a temporally smooth reference voltage, as confirmed in Section 4.2, thereby forming a reference voltage more appropriate for an actual SVR. In this way, a reference voltage consistent with the actual operating characteristics of the SVR made it possible to effectively improve voltage quality with fewer tap operations. The reduction in tap operations itself suggests that the reference voltage of PiecewiseDB was maintained stably within the actual deadband range of the SVR. Single LDC approximates the entire range with a single line regardless of the direction of power flow, and thus fails to reflect the different voltage-current relationships required under forward and reverse power flow. As a result, the reference voltage can be formed in a manner different from what is actually required, particularly in the reverse power flow region. Piecewise LDC mitigates this problem by applying separate lines to the forward and reverse power flow regions, but at the moment when the power flow direction reverses, the reference voltage can change abruptly due to the transition between the two lines. In this process, the SVR may respond excessively to a transient condition, raising the tap more than necessary. Such an excessively raised tap position can become a cause of overvoltage at subsequent time steps. PiecewiseDB, as confirmed in Section 4.2, suppresses the temporal variation in the reference voltage, including in the power flow transition region, while keeping it stably within the deadband range. Accordingly, the excessive tap increases that can occur in the other methods are suppressed, which is interpreted as leading to the marked reduction in OV count. The total OV count across all nine scenarios was 285 for Single, 346 for Piecewise, and 105 for PiecewiseDB, corresponding to a reduction of about 69.7% relative to Piecewise and about 63.2% relative to Single. In particular, in the three Case 1 scenarios, the OV count dropped sharply from 21–37 for Single and Piecewise to only 1–2 for PiecewiseDB, an improvement to a level at which overvoltage violations are effectively eliminated. To confirm these results in more concrete terms from the perspective of the bus level voltage distribution, box plots of the voltage distribution at the buses downstream of the SVR are presented in Figures 15–17 for Cases 1 to 3 under the PV = 15 MW condition, at which the differences among the three methods are most pronounced.

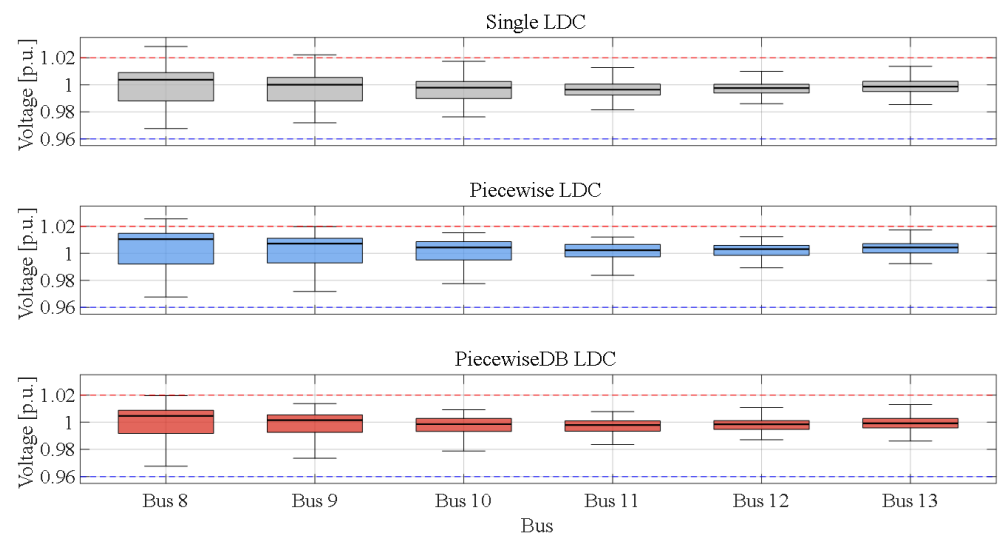


Figure 15. Voltage Distribution of Downstream Buses for Case 1, PV = 15 MW.

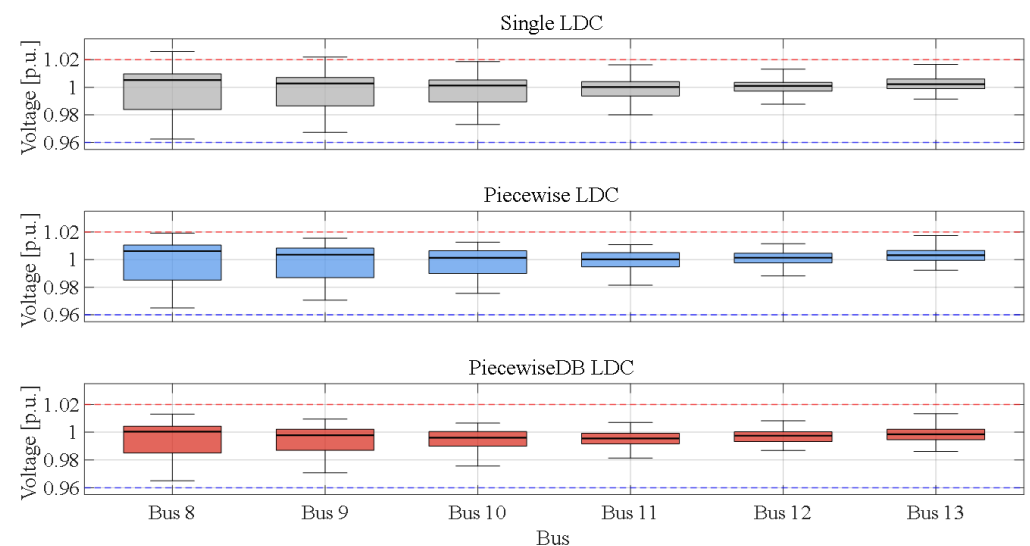


Figure 16. Voltage Distribution of Downstream Buses for Case 2, PV = 15 MW.

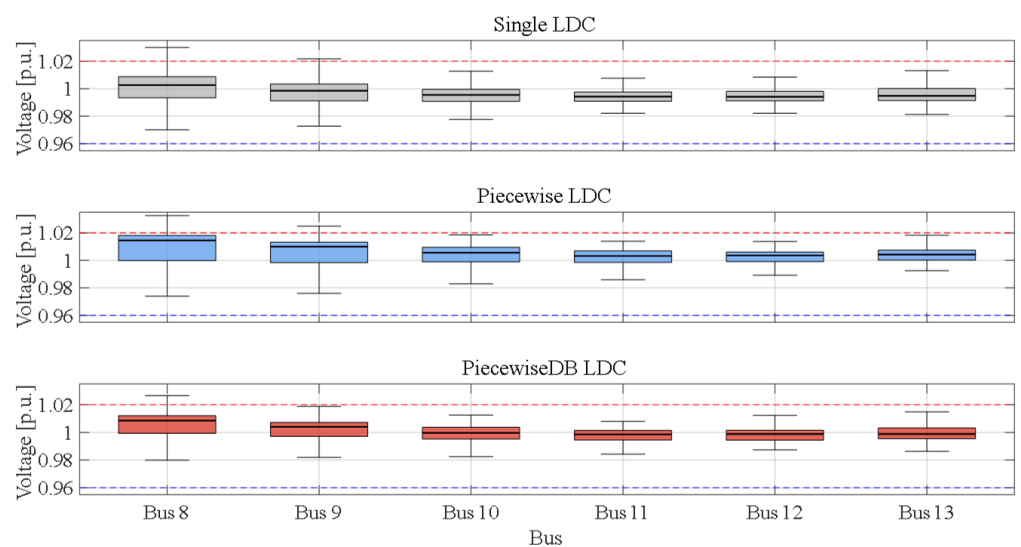


Figure 17. Voltage Distribution of Downstream Buses for Case 3, PV = 15 MW.

For Case 1, PV = 15 MW, both Single and Piecewise LDC exhibit an overvoltage at Bus 8–9, with the upper whisker exceeding the voltage limit (1.02 p.u.). In contrast, PiecewiseDB maintains the maximum voltage within the voltage limit across all buses, including Bus 8–9, improving this overvoltage condition, while the box height (IQR) is also reduced and the median is formed closer to 1.0 p.u. That is, PiecewiseDB keeps the voltage distribution closer to the nominal voltage across all buses rather than at specific buses alone.

For Case 2, PV = 15 MW, Single LDC exhibits an overvoltage at Buses 8 and 9, with the upper whisker exceeding the voltage limit, a pattern consistent with the OV count results confirmed in Table 4. In contrast, PiecewiseDB keeps the upper whisker of Buses 8 and 9 within the voltage limit, resolving the overvoltage observed for Single, while the box positions of the other buses are also closer to the nominal voltage overall, confirming that PiecewiseDB maintains the voltage distribution closest to the nominal voltage among the three methods.

Case 3, PV = 15 MW is the condition under which the differences among the three methods are most pronounced. Piecewise LDC exhibits a larger box height at Bus 8 than Single LDC, with the upper whisker clearly exceeding the voltage limit, indicating an overvoltage. This is a direct confirmation, at the bus level voltage distribution, of the reversal identified earlier in Table 4, in which both the SNVPI and the OV count of Piecewise increase relative to Single. PiecewiseDB exhibits a box position at Bus 8 that is even lower than that of Single, along with the narrowest IQR among the three methods, showing the voltage distribution closest to the nominal voltage and the most stable among the three methods. Under this condition of the highest PV penetration, however, the upper whisker of PiecewiseDB still exceeds the voltage limit at some time steps. As confirmed in Section 4.2, this is judged to result from the fact that, under very high PV penetration, the temporal variation of $V_{SER,t}$ itself becomes too large to be fully accommodated within the designed deadband half width. Even in this case, the extent and frequency of the exceedance for PiecewiseDB remain markedly reduced compared with Single and Piecewise LDC methods.

In summary, PiecewiseDB consistently achieved a superior SNVPI relative to both Single and Piecewise across all nine scenarios, and this improvement in voltage quality was accompanied by fewer tap operations and a marked reduction in the frequency of overvoltage occurrences. This tendency was also consistently confirmed through the bus-level voltage distribution analysis using box plots. These results show that, unlike conventional designs that aim only to minimize the $V_{SER,t}$ tracking error, PiecewiseDB, which reflects both the deadband-based tap decision structure that accounts for the actual operating characteristics of the SVR and the temporal variation in the reference voltage, provides superior performance in terms of voltage quality, violation frequency, and operational burden on the equipment.

4.4. Sensitivity Analysis of the Weighting Factors

This section analyzes the influence of the weighting factors of PiecewiseDB on the results. The results in Sections 4.2 and 4.3 were obtained with the weighting factors ($\lambda_{\text{track}} = 1$, $\lambda_{\text{DB}} = 10^4$, $\lambda_{\text{smooth}} = 10^2$) set in Section 3.4 on the basis of the raw scale of each term. Among them, the deadband-aware term J_{DB} is a conditional term that acts only on errors exceeding the designed deadband half width and therefore has a small raw scale, so it was given the largest weight. The analysis was performed in two steps. First, to examine the relative weight of the other two terms, λ_{track} and λ_{DB} were fixed at 1 and 10^4 respectively, and λ_{smooth} was varied among 10, 10^2 , and 10^3 ($\lambda_{\text{track}} : \lambda_{\text{smooth}} = 1 : 10, 1 : 100$, and $1 : 1000$). Second, to examine the influence of the deadband-aware term, λ_{track} and λ_{smooth} were fixed at 1 and 10^2 respectively, and λ_{DB} was varied among 10^3 , 10^4 , and 10^5 . For each setting, the LDC parameters were derived again and the performance was evaluated using the same

nine scenarios and five-day profiles as in Section 4.1. The results of PiecewiseDB for the variation of λ_{smooth} and λ_{DB} are summarized in Tables 5 and 6, respectively. The results of Single and Piecewise are independent of the weighting factors and are therefore referred to Table 4.

Table 5. Comparison of PiecewiseDB voltage control results for different λ_{smooth} settings across nine scenarios ($\lambda_{\text{track}} = 1$, $\lambda_{\text{DB}} = 10^4$).

Case	PV [MW]	$\lambda_{\text{track}}:\lambda_{\text{smooth}}$	SNVPI	SNVPI _{downstream}	TapOps	OV Count	UV Count
1	5	1:10	1.47558	0.15380	47	11	94
		1:100	1.46310	0.14115	42	1	94
		1:1000	1.46310	0.14115	42	1	94
	10	1:10	1.24169	0.14572	103	14	73
		1:100	1.19715	0.10088	96	1	73
		1:1000	1.20101	0.10481	94	5	73
	15	1:10	1.20800	0.22604	152	11	67
		1:100	1.18006	0.19790	144	2	67
		1:1000	1.17851	0.19635	144	2	67
2	5	1:10	1.16541	0.11560	43	0	39
		1:100	1.13996	0.09003	35	0	39
		1:1000	1.14141	0.09149	33	0	39
	10	1:10	0.99997	0.12949	99	1	31
		1:100	0.98208	0.11138	88	1	31
		1:1000	0.99379	0.12301	84	1	31
	15	1:10	1.04400	0.26046	139	0	29
		1:100	1.03312	0.24945	128	0	29
		1:1000	1.03279	0.24912	128	0	29
3	5	1:10	1.91074	0.25789	64	82	189
		1:100	1.89075	0.23758	58	54	189
		1:1000	1.89947	0.24632	56	59	189
	10	1:10	1.59565	0.22398	110	63	139
		1:100	1.51639	0.14409	102	21	139
		1:1000	1.51814	0.14587	100	25	139
	15	1:10	1.44142	0.21672	172	60	127
		1:100	1.40956	0.18439	158	25	127
		1:1000	1.40868	0.18351	159	25	127

Compared with the reference setting of $\lambda_{\text{smooth}} = 10^2(1:100)$, $\lambda_{\text{smooth}} = 10(1:10)$ increased the SNVPI by 0.85% to 5.23% in all nine scenarios, and the SNVPI_{downstream} also increased. TapOps increased by 5 to 14 in every scenario, and the sum of the OV counts over the nine scenarios also increased from 105 to 242. In contrast, the change was small for $\lambda_{\text{smooth}} = 10^3(1:1000)$. The SNVPI changed within 0.5% in eight scenarios, all except Case 2 with PV = 10 MW (1.19%), and the difference in TapOps was at most four. For PV = 5 and 10 MW, the SNVPI was equal to or slightly higher than that of the reference setting (0.12% to 1.19%). For PV = 15 MW, it was slightly lower (0.03% to 0.13%), but since TapOps was the same or increased by one, this can hardly be regarded as a practical improvement.

Table 6. Comparison of PiecewiseDB voltage control results for different λ_{DB} settings across nine scenarios ($\lambda_{track} = 1$, $\lambda_{smooth} = 10^2$).

Case	PV [MW]	λ_{DB}	SNVPI	SNVPI _{downstream}	TapOps	OV Count	UV Count
1	5	10^3	1.46310	0.14115	42	1	94
		10^4	1.46310	0.14115	42	1	94
		10^5	1.46290	0.14095	42	1	94
	10	10^3	1.19713	0.10086	96	1	73
		10^4	1.19715	0.10088	96	1	73
		10^5	1.19605	0.09973	98	1	73
	15	10^3	1.17986	0.19770	144	2	67
		10^4	1.18006	0.19790	144	2	67
		10^5	1.17980	0.19765	144	2	67
2	5	10^3	1.14449	0.09457	33	0	39
		10^4	1.13996	0.09003	35	0	39
		10^5	1.14883	0.09892	31	0	39
	10	10^3	0.98207	0.11138	88	1	31
		10^4	0.98208	0.11138	88	1	31
		10^5	0.98673	0.11599	86	1	31
	15	10^3	1.03312	0.24945	128	0	29
		10^4	1.03312	0.24945	128	0	29
		10^5	1.03312	0.24945	128	0	29
3	5	10^3	1.89617	0.24302	56	55	189
		10^4	1.89075	0.23758	58	54	189
		10^5	1.89075	0.23758	58	54	189
	10	10^3	1.51605	0.14374	102	21	139
		10^4	1.51639	0.14409	102	21	139
		10^5	1.52128	0.14903	100	25	139
	15	10^3	1.40868	0.18351	159	25	127
		10^4	1.40956	0.18439	158	25	127
		10^5	1.40919	0.18403	158	25	127

Summed over the nine scenarios, TapOps was 929, 851, and 840 for $\lambda_{smooth} = 10$, 10^2 , and 10^3 , respectively, and the OV counts were 242, 105, and 118, while the UV counts were the same, 788, for all settings. The setting with the lowest SNVPI was 10^2 in the six scenarios with PV = 5 and 10 MW and 10^3 in three scenarios with PV = 15 MW, and the sum of the OV counts was the smallest for 10^2 . Therefore, the setting used in Sections 4.2 and 4.3 avoids the performance degradation that occurs when λ_{smooth} is reduced to 10, and its results differ little from those obtained with 10^3 .

Table 6 shows the results for the variation of λ_{DB} . The results for $\lambda_{DB} = 10^4$ are the same as those for 1:100 in Table 5. Compared with $\lambda_{DB} = 10^4$, the SNVPI changed within 0.40% for $\lambda_{DB} = 10^3$ and within 0.78% for $\lambda_{DB} = 10^5$ in all nine scenarios, which is much smaller than the increase of 0.85% to 5.23% caused by reducing λ_{smooth} to 10. The SNVPI_{downstream} changed within 1.2% in 13 of the 18 comparisons, and the largest change was 9.87% in Case 2 with PV = 5 MW for $\lambda_{DB} = 10^5$, which corresponds to an absolute change of 0.009. TapOps differed by at most two for $\lambda_{DB} = 10^3$ and by at most four for $\lambda_{DB} = 10^5$.

Summed over the nine scenarios, TapOps and the OV counts were 848 and 106 for $\lambda_{DB} = 10^3$, 851 and 105 for $\lambda_{DB} = 10^4$, and 845 and 109 for $\lambda_{DB} = 10^5$, respectively. For all three values of λ_{DB} , PiecewiseDB showed a lower SNVPI, a lower $SNVPI_{downstream}$, and fewer TapOps than both Single and Piecewise in all nine scenarios. Therefore, the results of PiecewiseDB do not differ significantly within the range of $\lambda_{DB} = 10^3$ to 10^5 .

4.5. Validation on One-Day Profiles Not Used for Parameter Derivation

To examine whether the performance of each method is maintained under load and PV conditions that differ from the data used for parameter design, the LDC parameters derived from the five-day profiles were applied without re-optimization to one-day profiles of a different day that were not used in the derivation. Case 1 shown in Figure 11, in which the load ratios on the primary and secondary sides of the SVR are equal, was selected as the representative case. For each installed PV capacity of 5, 10 and 15 MW, the LDC parameters derived from the five-day profiles for the same PV capacity were used, and the one-day PV output profile was scaled to that capacity. Since the weight sensitivity analysis in Section 4.4 confirmed that the weighting factors used in Sections 4.2 and 4.3 are appropriate, the same weights ($\lambda_{DB} = 10^4$, $\lambda_{track} = 1$, $\lambda_{smooth} = 10^2$) were applied in the derivation of the PiecewiseDB parameters.

The other simulation conditions were identical to those in Section 4.1. The one-day profiles consist of 96 samples at 15-min intervals and were composed of four representative combinations of high and low load and high and low PV output profiles. Figure 18 shows the high-load and low-load output profiles and the high-PV and low-PV output profiles. Both profiles are given in p.u. The PV output profile is expressed in p.u. of the installed PV capacity, so the actual PV output is the profile multiplied by the installed capacity of 5, 10 or 15 MW. Therefore, the high and low PV profiles represent days with high and low PV output, not the size of the installed capacity.

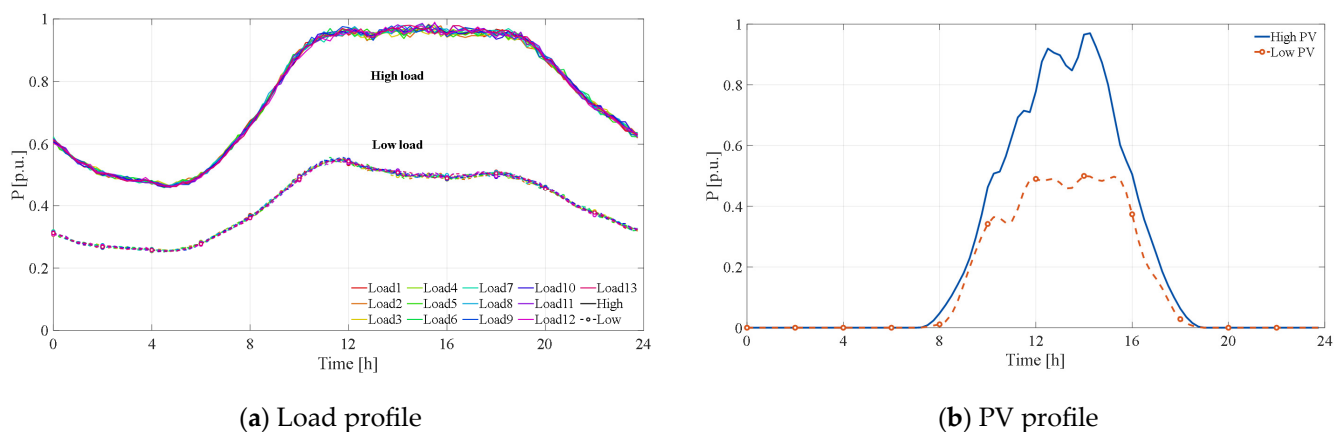


Figure 18. One-day profiles used for the validation.

Table 7 summarizes SNVPI, TapOps, OV count and UV count of Single, Piecewise and PiecewiseDB for the four combinations at each installed PV capacity, resulting in twelve scenarios in total.

Under high load, PiecewiseDB showed the lowest downstream SNVPI in five of the six scenarios, with reductions of 5.4% to 16.2% compared with Single LDC. The total OV count over these six scenarios was 38, 10 and 6 for Single, Piecewise and PiecewiseDB, respectively, whereas the UV count was identical for all three methods. PiecewiseDB also required the fewest tap operations in all twelve scenarios, with reductions of 3.8% to 38.9% compared with Single LDC. Under low load, the downstream SNVPI of PiecewiseDB was slightly higher than that of Piecewise in all six scenarios, although the absolute values were

small. The total OV count of PiecewiseDB was five (four at the installed PV capacity of 5 MW and one at 10 MW), and the maximum voltage was 1.0212 p.u., whereas no OV occurred with Piecewise. These results show that the benefit of PiecewiseDB is mainly obtained under high load, where voltage violations occur, and that a slight loss of voltage quality can appear under low load.

Table 7. Voltage control performance of the three LDC methods on the one-day validation profiles, using the LDC parameters derived from the five-day profiles.

Load/PV Output Profile	Installed PV Capacity [MW]	Method	SNVPI _{downstream}	TapOps	OV Count	UV Count	V _{max}
High Load High PV	5	Single	0.1340	18	1	25	1.0207
		Piecewise	0.1257	16	0	25	1.0186
		PiecewiseDB	0.1268	11	0	25	1.0195
	10	Single	0.1198	26	3	20	1.0222
		Piecewise	0.1142	24	4	20	1.0226
		PiecewiseDB	0.1084	21	0	20	1.0195
	15	Single	0.1442	34	18	19	1.0256
		Piecewise	0.1279	30	6	19	1.0238
		PiecewiseDB	0.1216	27	6	19	1.0238
High Load Low PV	5	Single	0.1421	14	1	28	1.0207
		Piecewise	0.1377	12	0	28	1.0186
		PiecewiseDB	0.1328	11	0	28	1.0137
	10	Single	0.1297	18	3	23	1.0222
		Piecewise	0.1235	16	0	23	1.0186
		PiecewiseDB	0.1119	15	0	23	1.0125
	15	Single	0.1281	28	12	21	1.0256
		Piecewise	0.1124	24	0	21	1.0186
		PiecewiseDB	0.1073	21	0	21	1.0126
Low Load High PV	5	Single	0.0388	12	0	0	1.0150
		Piecewise	0.0364	12	0	0	1.0150
		PiecewiseDB	0.0457	8	4	0	1.0212
	10	Single	0.0510	20	1	0	1.0203
		Piecewise	0.0487	22	0	0	1.0165
		PiecewiseDB	0.0536	19	1	0	1.0203
	15	Single	0.1079	26	0	1	1.0160
		Piecewise	0.1048	28	0	1	1.0160
		PiecewiseDB	0.1088	25	0	1	1.0160
Low Load Low PV	5	Single	0.0397	6	0	0	1.0119
		Piecewise	0.0367	6	0	0	1.0130
		PiecewiseDB	0.0390	4	0	0	1.0103
	10	Single	0.0364	14	0	0	1.0120
		Piecewise	0.0368	14	0	0	1.0130
		PiecewiseDB	0.0403	11	0	0	1.0105
	15	Single	0.0669	20	0	0	1.0101
		Piecewise	0.0549	20	0	0	1.0130
		PiecewiseDB	0.0598	17	0	0	1.0076

The reduced voltage quality of PiecewiseDB under low load can be explained by the V_{ref} of the derived parameters. Under low load, the line current is small, and the target

voltage of the LDC is determined mainly by V_{ref} rather than by the line drop term. The V_{ref} of the PiecewiseDB parameter sets differed from that of the Piecewise parameter sets by up to about one tap (≈ 0.00625 p.u.). With the parameters derived for the PV capacities of 10 and 15 MW, the lower V_{ref} kept the SVR tap position about one tap lower, so that the downstream voltages were further from the rated value. With the parameters derived for the PV capacity of 5 MW, the higher V_{ref} kept the tap position about one tap higher, which caused overvoltage events at the downstream bus. This V_{ref} offset is considered to result from the smoothness term of the PiecewiseDB objective, which reduces the discontinuity between the forward and reverse lines, and from the deadband term, which limits the resulting deviation of the target voltage from the V_{SER} of the design data to about half of the deadband width.

4.6. Effect of the Controller Input Resolution

The I_{fwd} and I_{rev} designed in Section 3 are real numbers, whereas V_R and V_X of the controller are entered in steps of 0.1 V. To examine the effect of this resolution, I_{fwd} and I_{rev} of PiecewiseDB were converted into V_R and V_X of each power flow direction using the line impedance per unit length and PT and CT ratios in Section 2.3.4, and each value was rounded to the nearest 0.1 V. The line section lengths were then recalculated from the rounded V_R and V_X , and applied as the new I_{fwd} and I_{rev} while the other parameters were kept unchanged. The nine scenarios in Section 4.1 (Cases 1 to 3, PV = 5, 10, 15 MW) were simulated again with these values, and the results were compared with those obtained with the optimized I_{fwd} and I_{rev} , which correspond to the PiecewiseDB results in Table 4. Compared with the optimized settings, the rounded settings yielded a mean absolute percentage error of 0.197% and a maximum absolute percentage error of 0.665% in the SNVPI over the nine scenarios. The total TapOps over the nine scenarios was 851 with the optimized settings and 853 with the rounded settings. Therefore, the 0.1 V resolution of V_R and V_X does not significantly affect the voltage control results of PiecewiseDB.

5. Discussion

The simulations use 15-min load and PV profiles and assume that the tap position settles within each time step, and the time delay and the tap actuation time of the controller are not modeled. In an actual SVR, a tap command is issued only when a deviation persists beyond the preset time delay, so short-duration PV fluctuations within an interval are filtered by the deadband and the time delay, whereas excursions persisting beyond the delay may not be captured by the 15-min samples. In addition, the performance in an actual installation may differ from the simulated performance because of dynamics that are not reflected in the simulation. Besides the preset time delay, there is a further delay between the output of the tap control signal from the controller and its reflection in the system, which is determined by the actuation of the tap mechanism. Therefore, the voltage change caused by a tap operation appears at the SVR secondary side later than assumed in the simulation, and this delay shifts the timing of the voltage change relative to the simulated trajectory. The shift may become more significant when the load or the PV output changes rapidly. The measurement errors of the PT and the CT may also cause the estimated voltage and the determined power flow region to deviate from those in the simulation. The effect of these dynamics, together with that of sub-minute PV variability and controller timing, on the proposed method was not evaluated and remains to be verified using high-resolution data and hardware-in-the-loop testing.

6. Conclusions

This paper proposed PiecewiseDB, an MIQP-based bidirectional LDC parameter derivation method that explicitly reflects the operating characteristics of an actual SVR controller in a distribution system with interconnected distributed energy resources. The proposed method adds a deadband-aware term and a reference-voltage smoothing term to the V_{SER} tracking objective function of the conventional piecewise LDC, thereby directly reflecting the deadband-based tap decision structure of the SVR and the temporal variation characteristics of the reference voltage at the parameter derivation stage. Through simulations on a 13-bus distribution system, a structural limitation of the conventional V_{SER} tracking-based objective function was identified. The conventional objective function does not account for the binary deadband decision structure of the SVR and therefore minimizes the error unnecessarily even in ranges that do not affect the tap decision, which was confirmed to lead to a performance reversal in which the piecewise LDC exhibits worse voltage quality than the single LDC. PiecewiseDB exhibited a lower SNVPI and fewer tap operations than both Single and Piecewise LDC, and an equal or lower number of overvoltage violations, across all nine scenarios using the five-day profiles. In particular, it completely resolved the performance reversal observed for Piecewise, achieving both improved voltage quality and reduced tap operations in these scenarios. In the validation on a different day whose load and PV profiles were not used for the LDC parameter derivation, the PiecewiseDB parameters derived from the five-day profiles retained their advantage under high load, with the lowest downstream SNVPI in five of the six scenarios, and required the fewest tap operations in all twelve scenarios, whereas a slight loss of voltage quality appeared under low load, which is attributed to a difference in the reference voltage from that of Piecewise. The derived LDC parameters can be directly applied to the setting structure of a modern SVR controller, and the proposed method can serve as a practical design approach for improving the voltage regulation performance of SVRs in distribution systems with high PV penetration.

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