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Composite Model Predictive Control Strategy for Triple-Active-Bridge-Based MMDTC-PET with Enhanced Disturbance Resilience

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Abstract

To address the delayed dynamic response and susceptibility to overcurrent surges of the triple-active-bridge (TAB)-based modular multilevel DC-link T-type converter power electronic transformer (MMDTC-PET) under load step transients, this paper proposes a composite model predictive control (MPC) strategy to enhance the system's disturbance rejection capability. The proposed strategy adopts a hierarchical control architecture comprising a proportional-integral (PI) outer power loop and an MPC inner loop. To tackle the heavy computational burden caused by multi-port coupling, dimensionality reduction is performed by equating the phase-shift ratios of the two primary-side ports of the TAB, which effectively mitigates the computational cost. Furthermore, a dynamic overcurrent hard-constraint penalty term and a control-effort smoothing term are incorporated into the multi-objective cost function. This not only achieves steady-state error-free tracking of the output voltage but also enhances physical operational safety under complex conditions at the algorithmic level. Comparative simulation results under various operating conditions demonstrate that, compared with the traditional PI-based phase-shift control, the proposed strategy exhibits a faster dynamic response under load step conditions. Moreover, it suppresses transient power overshoots and overcurrent impacts during input voltage sags and recoveries, thereby significantly improving the transient disturbance rejection capability and operational robustness of the system.

Keywords: TAB; MMDTC; power electronic transformer; model predictive control; disturbance rejection capability

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1. Introduction

Power electronic transformer (PET) is an advanced power electronic device that integrates power electronics technology with a high-frequency transformer [1–3]. Unlike conventional transformers, the PET not only provides voltage transformation and galvanic isolation but also possesses advanced regulation capabilities, such as fault isolation, power quality conditioning, and voltage and current control [4–6].

Among single-stage, two-stage, and three-stage PET configurations, the three-stage PET provides the most comprehensive functionalities and the widest regulation range [7,8]. In the three-stage architecture, to accommodate medium- and high-voltage grid integration and mitigate the voltage stress constraints on switching devices, this paper employs the modular multilevel DC-link T-type converter (MMDTC) as the input stage of the PET.

However, similar to the cascaded H-bridge (CHB) and the modular multilevel converter (MMC) [9,10], the submodule capacitors of the MMDTC suffer from low-frequency voltage ripples [11]. Suppressing these ripples typically requires bulky capacitors, which consequently increases the overall volume and hardware cost of the system. To reduce the submodule capacitance and achieve cost savings, [12] utilizes the triple active bridge (TAB) as the isolation stage of the MMDTC-PET. By leveraging the dual-input-port characteristics of the TAB structure and applying in-phase phase-shift modulation, passive ripple suppression is inherently achieved at the physical level. Nevertheless, hardware innovations inevitably introduce new challenges. Although the TAB architecture effectively addresses the ripple issue at the physical level, the inherent coupling characteristics of its dual input ports significantly increase the control complexity of the system.

Recent research on multi-port bidirectional isolated converters, particularly TABs, has heavily focused on steady-state phase-shift modulation optimization. To minimize circulating power and expand soft-switching regions under mismatched port voltages, various multi-degree-of-freedom techniques—such as combined phase-shift and duty-cycle control [13,14], unified high-frequency link current calculations [15], and multiple phase-shift strategies [16,17]—have been proposed. While these methods successfully reduce RMS currents and system losses in the steady state, their reliance on traditional PI controllers fundamentally limits their transient dynamic response capabilities.

Although the above methods successfully reduce system losses and expand the zero-voltage switching (ZVS) range in the steady state, they all rely on traditional PI controllers, which leaves their dynamic response capabilities inherently limited. When subjected to large-signal disturbances such as grid voltage sags or load steps, PI controllers often fail to respond rapidly, making the system highly prone to transient power overloads and overcurrent surges.

To accelerate the dynamic response of the ports, some scholars have proposed decoupled transient performance optimization methods for TABs. Reference [18] presented a simplified analysis model and an optimized control strategy for triple-active-bridge converters. Reference [19] proposed a decoupling control method for a half-bridge three-port converter, achieving energy management of the system and decoupling among the control loops of various ports. Reference [20] proposed a decoupling control strategy based on linear active disturbance rejection control, which employs a linear extended state observer to observe coupling disturbances, thereby realizing dynamic decoupling. In [21], a double-line-frequency power decoupling strategy based on proportional-resonant control was proposed to decouple the double-line-frequency power among different ports of the PET. However, when subjected to large-signal disturbances such as voltage sags or load steps, the decoupling effectiveness of these methods degrades significantly. They fail to effectively address the sluggish response issue in PI control. During transient processes, abrupt changes in phase-shift angles easily induce high-frequency link current surges and transient overcurrents, ultimately leading to transformer saturation and overcurrent damage to switching devices.

While recent decoupling strategies [18–21] successfully address steady-state multi-port coupling, their reliance on linear integrators inevitably causes integrator windup and transient overcurrents during large-signal disturbances. Although model predictive control (MPC) offers superior transient immunity, applying conventional multi-variable MPC to the TAB topology leads to an exponential increase in computational burden, preventing real-time execution.

Therefore, rather than merely combining known techniques, this paper proposes a customized composite hierarchical MPC architecture tailored to resolve the fundamental

paradox between computational limits and transient vulnerability. The unique contributions are as follows:

(1) **Physically Grounded Dimensionality Reduction over Mathematical Pruning:**

Rather than relying on algorithmic pruning during the search process, the proposed strategy reconstructs the predictive state-space model based on the inherent physical symmetry of the TAB's primary-side dual ports ($D_1 \approx D_2$). The inevitable physical asymmetries, which would otherwise cause model mismatches, are decoupled and compensated by an independent outer-loop PI fine-tuning variable. This approach physically collapses the optimization search space from an exponential $O(N^2)$ scale to a deterministic linear $O(N)$ scale right at the modeling stage, ensuring constant execution times without sacrificing global optimality.

(2) **Algorithmic Protection of Physical Boundaries:**

The deterministic computational efficiency unlocked by this physical reduction enables the embedding of a dynamic overcurrent hard-constraint penalty (H_{limit}) directly within the multi-objective cost function. Unlike conventional linear decoupling methods that passively react to large-signal disturbances, the proposed algorithm proactively anticipates and rejects unsafe control efforts before they are applied. This provides a proactive, algorithmic protection of physical operational boundaries—a theoretical capability that neither conventional linear controllers nor mathematically pruned MPCs can readily achieve.

2. Topology and Operating Principles of the TAB-MMDTC-PET

The TAB-based MMDTC-type power electronic transformer (hereafter referred to as TAB-MMDTC-PET) is illustrated in Figure 1. The TAB primarily consists of two H-bridges on the primary side, one H-bridge on the secondary side, and a high-frequency transformer. In Figure 1a, the three windings belonging to the same transformer are indicated by connection lines of the same color. The two active bridges on the primary side of the TAB are connected to the two half-bridge submodules (HBSMs) located in the upper and lower arms of the modular DC link, respectively. Meanwhile, the DC terminals of the active bridge on the secondary side are connected in parallel to the low-voltage DC bus. Figure 1b further presents a schematic diagram illustrating the connections between the TAB and the submodules in the upper and lower arms. Here, U_1, U_2, and U_3 represent the three port voltages, L is the equivalent inductance, i_{L} is the inductor current, io is the secondary-side output current, i_{C} is the input current of capacitor C_3, and i_3 is the load current. It is worth noting that no inductors are configured on the primary side of the high-frequency transformer (HFT) in the TAB; instead, only a small-valued external inductor is connected in series on the secondary side.

The equivalent model of the TAB is shown in Figure 2a, where u_1 and u_2 denote the voltages of the two AC ports on the primary side of the transformer, and u_3 denotes the voltage of the AC port on the secondary side. For the two full bridges on the primary side of the TAB, this paper adopts an in-phase dual-input phase-shift modulation strategy. Figure 2b further displays the PWM drive signals of the switches, along with the voltage waveforms of the three ports. Under this modulation strategy, all three full bridges employ PWM modulation with a 50% duty cycle, and the switching period is denoted as T_{s}. The phase angles of the modulation signals for the two primary-side full bridges are defined as β_1 and β_2, respectively, while the phase angle for the secondary-side full bridge is defined as β_3.

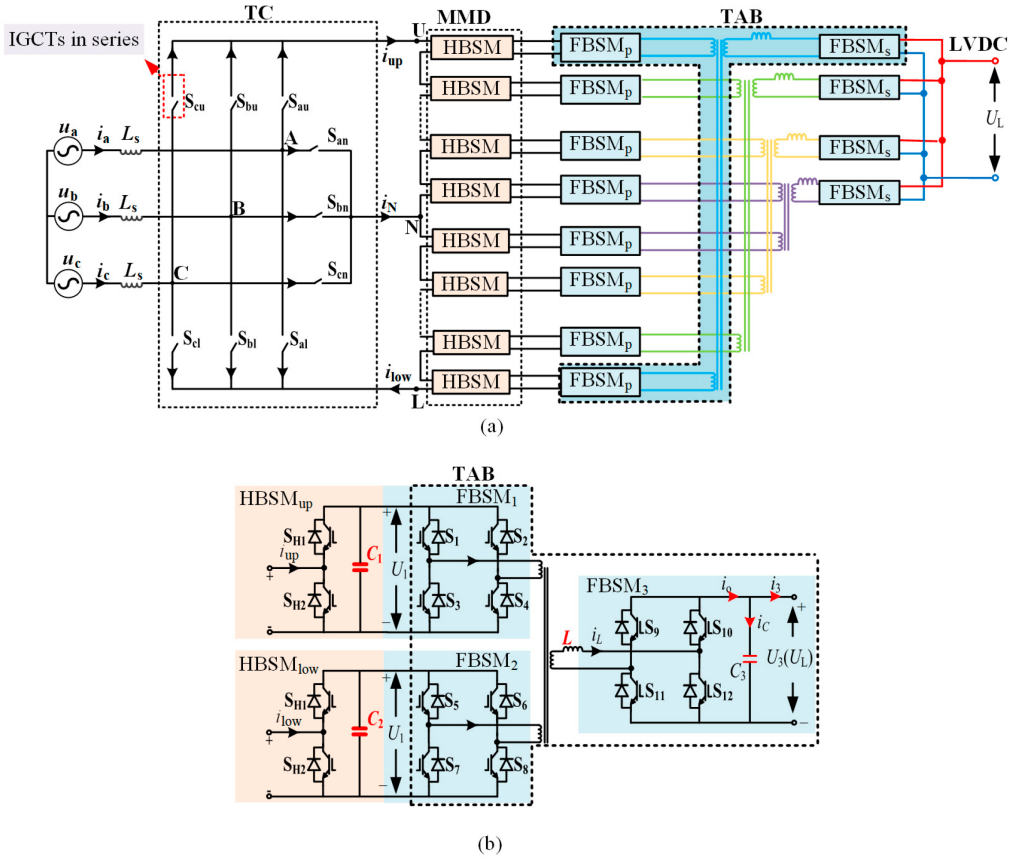

Figure 1. Schematic diagram of the TAB-MMDTC-PET structure: (**a**) overall structural diagram; (**b**) schematic diagram of the connection between the TAB and HBSMs. A, B, and C denote the three AC phases. Arrows indicate the reference directions of voltages and currents, and dashed boxes outline the converter stages or modules. In (**a**), connection lines of the same color identify the three windings belonging to the same transformer. Adapted from [13].

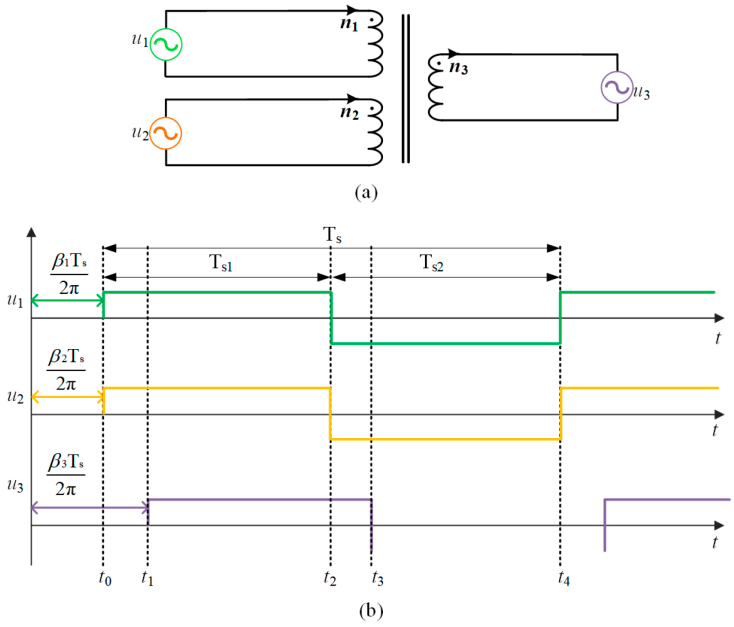

Figure 2. Equivalent model and modulation strategy of the TAB: (**a**) simplified equivalent model; (**b**) dual-input phase-shift control strategy. Green, orange, and purple denote the port voltages u_1, u_2, and u_3, respectively. Arrows in (**a**) indicate the reference current directions. Double-headed arrows in (**b**) indicate time intervals, and vertical dashed lines mark switching instants. Adapted from [13].

Under ideal conditions, if the power imbalance between the upper and lower arms and the loss discrepancies among the submodules are neglected, it can be assumed that $\beta_1 = \beta_2$. In this case, the phase-shift angle between the primary and secondary sides is defined as $\beta = \beta_1 - \beta_3$. By regulating the magnitude and polarity of the phase-shift angle β, both the magnitude and direction of the power transferred from the primary side to the secondary side can be continuously controlled.

However, under practical operating conditions, power discrepancies inevitably exist among the individual submodules. Figure 3 illustrates the traditional control scheme for the TAB-MMDTC-PET. As shown in Figure 3a, the MMDTC employs independent submodule capacitor voltage balancing control. By superimposing a reference voltage component based on the arm current direction, the PI control loop ensures each submodule voltage consistently tracks the average arm voltage. Figure 3b depicts the traditional PI-based in-phase dual-input phase-shift control for the TAB. Since the front-stage MMDTC already maintains voltage balance between the dual primary-side ports, the TAB control simplifies to a single closed-loop PI regulation of the low-voltage DC bus. This loop generates a unified phase-shift angle that is synchronously dispatched to both primary-side full bridges to regulate the overall power transfer.

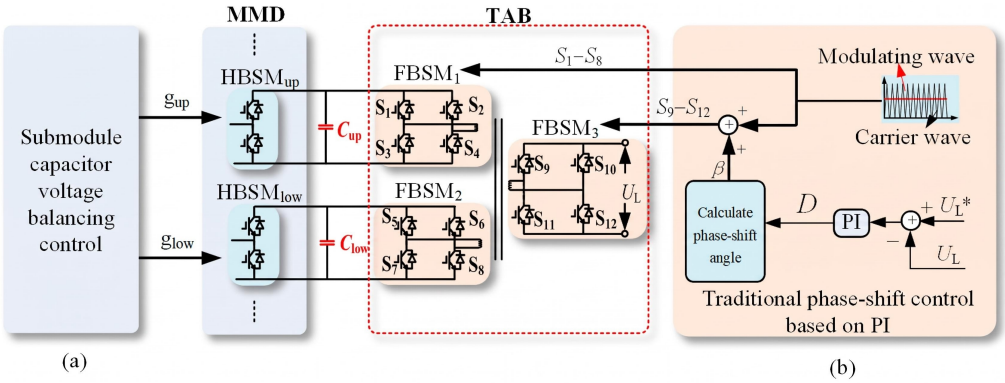

Figure 3. Control strategies of the TAB-MMDTC-PET: (**a**) independent capacitor voltage balancing control; (**b**) traditional PI-based phase-shift control. Arrows indicate the direction of control signal flow. The red dashed box outlines the TAB section, and the background colors distinguish the control and circuit blocks.

3. Model Predictive Control Design for the TAB-MMDTC-PET

In practical operating conditions, power discrepancies inevitably exist between the two input ports of the TAB. However, since the submodule capacitor voltage balancing control of the front-stage MMDTC can effectively maintain the voltage balance between these two input ports, the port balancing requirements are already satisfied. Consequently, in formulating the MPC model, this paper sets the phase-shift ratios of the two primary-side ports of the TAB to be equal (i.e., $D_1 = D_2$) and defines a net phase-shift ratio $D = D_3 - D_1$ as the core control variable. This dimensionality reduction approach not only accommodates the practical port power disparities but also simplifies the complex multi-dimensional optimization into a single-variable control, thereby effectively reducing the computational space of the MPC.

In the discrete-time domain, the state variable $x(t)$, the input variable $u(t)$, and the output variable $y(t)$ of the system are defined, respectively, as:

$$\begin{bmatrix} x(t) = [i_o(t), U_1(t), U_2(t), U_3(t)]^T \\ u(t) = D(t) \\ y(t) = U_3(t) \end{bmatrix} \quad (1)$$

where $i_o(t)$ represents the secondary-side average output current, and $U_1(t)$, $U_2(t)$, and $U_3(t)$ denote the three port voltages.

3.1. Establishment of the Discrete-Time Predictive Model

MPC predicts future outputs based on a discrete-time mathematical model of the system and transforms the control problem into an optimization problem by defining a cost function. Its operational mechanism is based on receding horizon optimization: at each control step, the optimal control command for the current interval is derived by minimizing the cost function. Compared to traditional linear control strategies, MPC can proactively anticipate future dynamics based on the current system state and offers the inherent advantage of handling physical constraints.

Tailored to the in-phase dual-input structural characteristics of the TAB converter, this section establishes a discrete-time predictive model of the system and proposes an MPC strategy applicable to the TAB-MMDTC-PET. This approach not only enhances the dynamic response performance of the system but also mitigates the significant computational burden typically incurred by the traditional finite control set during multi-dimensional optimization.

Based on the average model of the system, the equivalent average output current on the secondary side, $i_o(t)$, is primarily determined by the primary-side input voltages $U_1(t)$ and $U_2(t)$, the secondary-side output voltage $U_3(t)$, and the current net phase-shift ratio D. According to the power transfer characteristics of the system, the equivalent output current equation can be formulated as:

$$i_o(t) = \frac{(n_1 U_1(t) + n_2 U_2(t)) D(t)(1-|D(t)|)}{2 f_s L} \tag{2}$$

where $D(t)$ is the net phase-shift ratio; n_1 and n_2 are the transformer turns ratios from the primary-side Port 1 and Port 2 to the secondary side, respectively; L is the equivalent power transfer inductance of the system; and f_s is the switching frequency.

Meanwhile, according to KCL, the rate of change in the voltage across the secondary-side voltage-stabilizing capacitor C_3 is determined by both the equivalent output current and the load current. Its time-domain equation is expressed as:

$$i_C(t) = C_3 \frac{\mathrm{d}U_3(t)}{\mathrm{d}t} = i_o(t) - i_3(t) \tag{3}$$

To establish a discrete-time predictive model based on the energy transfer mechanism of the system, this paper employs the forward Euler method to discretize the system's differential equations. To obtain the predicted output voltage for the next control period, the control period of the converter, T_c, is set equal to the switching period, T_s.

At the current sampling instant k, applying the forward Euler approximation to the derivative term of the output voltage yields:

$$\frac{\mathrm{d}U_3}{\mathrm{d}t} = \frac{U_3(k+1) - U_3(k)}{t_{k+1} - t_k} = [U_3(k+1) - U_3(k)] f_s \tag{4}$$

By combining (2) and (4) and substituting them into the secondary-side node current Equation (3), the discrete-time predictive model for the output voltage of the TAB converter can be derived as follows:

$$U_3(k+1) = U_3(k) + \frac{(n_1 U_1(k) + n_2 U_2(k)) D(1-D)}{2 L C_3 f_s^2} - \frac{i_3(k)}{C_3 f_s} \tag{5}$$

where $U_3(k+1)$ is the predicted output voltage of the system at time step $k+1$; $U_1(k)$ and $U_2(k)$ are the sampled primary-side input voltages at the current time step k; $U_3(k)$ and $i_3(k)$ are the sampled secondary-side output voltage and load current at the current time step, respectively; and D(k) is the net phase-shift ratio at time step k.

3.2. Design of the Multi-Objective Cost Function

To achieve reference tracking and ensure the safe operation of the system, the cost function $J(k)$ of the MPC strategy in this paper is formulated as a composite structure that incorporates a primary tracking objective, an auxiliary smoothing term, and a constraint penalty term. Its expression is given by:

$$J(k) = \lambda_U J_U(k) + \lambda_S J_S(k) + H_{limit}(k) \tag{6}$$

where λ_U is the weighting factor for the primary tracking objective, and λ_S is the weighting factor for the auxiliary smoothing term.

(1) Voltage Tracking Objective Term $J_U(k)$

As the core control objective of the system, it is imperative to ensure that the output voltage $U_3(k)$ can track its reference value rapidly and with zero steady-state error. Therefore, this voltage tracking cost function term is defined as:

$$J_U(k) = [U_3(k+1) - U_L^*(k)]^2 \tag{7}$$

where $U_3(k+1)$ is the predicted output voltage for the next control period, derived from the discrete-time predictive model; and U_L*(k) is the given voltage reference value, utilized to maintain the desired stable voltage on the secondary side.

(2) Control Effort Smoothing Penalty Term $J_S(k)$

A control increment penalty term, $J_S(k)$, is introduced into the cost function to suppress abrupt variations in the net phase-shift ratio between adjacent control periods, thereby mitigating high-frequency oscillations in the control loop. Its expression is:

$$J_S(k) = (D(k) - D(k-1))^2 \tag{8}$$

where $D(k)$ is the candidate phase-shift ratio currently under evaluation during the optimization process, and $D(k-1)$ is the historical optimal phase-shift ratio command latched from the previous control period.

(3) Dynamic Overcurrent Constraint Penalty Term $H_{\text{limit}}(k)$

Although the in-phase dual-input TAB converter exhibits symmetric primary-side voltages ($U_1 = U_2$) under steady-state conditions, an increase in the phase-shift ratio is highly prone to inducing transient overcurrent surges during asymmetric transient processes, such as severe load steps or voltage sags. To address this, a hard-constraint-based overcurrent penalty function is designed in this paper:

$$H_{limit}(k) = \begin{cases} 0, & i_{L_peak}(k+1) \le I_{\max} \\ \infty, & \text{otherwise} \end{cases} \tag{9}$$

where $i_{\text{L_peak}}(k+1)$ is the peak inductor current flowing through the power transfer inductor, and $I_{\max}$ is the upper safety limit of the peak current for the power devices.

During the receding horizon optimization process of the MPC, the system iterates through a finite discrete set of phase-shift ratios. If a candidate phase-shift ratio is predicted to trigger a transient overcurrent violation, the penalty term Hlimit is driven to

infinity, and the control system actively rejects this candidate control effort. Through this constraint mechanism, when subjected to large-signal dynamic disturbances, the system proactively sacrifices a certain degree of instantaneous voltage tracking accuracy to clamp the phase-shift ratio within the safety boundaries. Consequently, this enhances the physical operational safety of the system at the algorithmic level.

4. MPC-Based Composite Hierarchical Control Strategy

To achieve both zero steady-state error tracking under steady-state conditions and rapid dynamic response during transients, this paper proposes a composite hierarchical control architecture comprising a PI outer power loop and an MPC inner loop for the TAB-MMDTC-PET system. In this control structure, the outer loop is primarily responsible for regulating the slow-dynamic power variables that exhibit DC characteristics, whereas the inner loop relies on the MPC algorithm to execute precise control over the high-frequency fast-dynamic variables.

4.1. Design of the Composite Hierarchical Control Strategy for the TAB-MMDTC

Figure 4 illustrates the macroscopic process flow and signal architecture of the proposed composite hierarchical control strategy. By leveraging the time-scale separation between the fast and slow control loops, this strategy dimensionally decomposes the complex multi-variable control problem into independent execution hierarchies, thereby achieving effective decoupling among various control objectives. The specific components of this control architecture are detailed as follows.

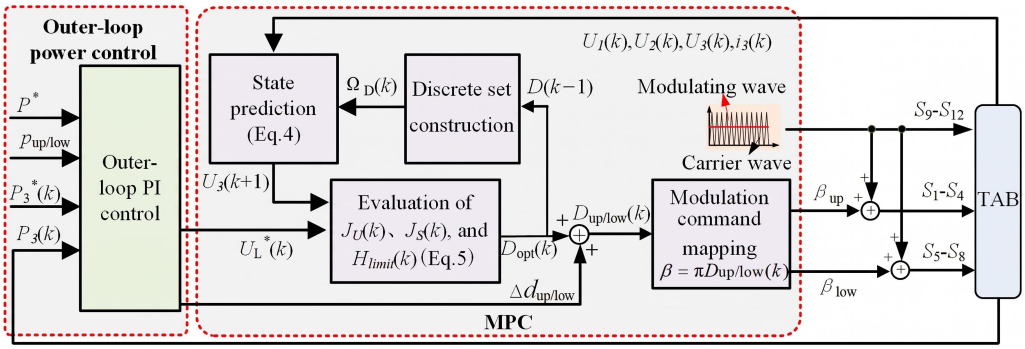

Figure 4. Block diagram of the proposed composite hierarchical MPC strategy.

The outer layer employs a power PI control loop, which is designed to maintain the global energy balance of the TAB system. The system acquires the actual secondary-side output power $P_3(k)$ and compares it with the predefined reference power $P_3{}^*(k)$ to calculate the error. Given that the output power exhibits pronounced DC characteristics under steady-state operating conditions, a traditional PI regulator is capable of achieving zero steady-state error tracking. Based on the power deviation, the PI controller generates the real-time output voltage reference command $U_L{}^*(k)$ at time step k, which is subsequently dispatched as the target value to the MPC inner loop.

Model predictive control typically treats system parameters as ideal constants. However, in practical operation, parameter uncertainties inevitably emerge due to factors such as temperature drift and magnetic core saturation. Substituting the output voltage predictive model (5) into the cost function yields:

$$J_U(k) = \left[U_3(k) + \frac{(n_1U_1(k) + n_2U_2(k))D(1-D)}{2LC_3f_s^2} - \frac{i_3(k)}{C_3f_s} - U_3{}^*(k)\right]^2 \quad (10)$$

A smaller value of $J_U(k)$ signifies a smaller deviation between the predicted output voltage for the subsequent control period and the reference voltage. According to the extreme value theorem, by setting the partial derivative of the cost function $J_U(k)$ with respect to the control variable D to zero, i.e., $\frac{\partial J_U(k)}{\partial D} = 0$, the optimal phase-shift ratio $D_{opt}(k)$ can be analytically derived as:

$$D_{opt}(k) = \frac{1 - \sqrt{1 - 4b}}{2} \tag{11}$$

where the expression for the coefficient b is given by:

$$b = \frac{2LC_3f_s^2\left[\frac{i_3(k)}{C_3f_s} - U_3(k) + U_3{}^*(k)\right]}{n_1U_1(k) + n_2U_2(k)} \tag{12}$$

As indicated by (11) and (12), the optimal phase-shift ratio $D_{opt}(k)$ at time step k is highly dependent on physical parameters such as the equivalent inductance L of the system, the output capacitor C_3, and the load current. In an idealized MPC design, to achieve dimensionality reduction in the control variables and alleviate the online computational burden, the system assumes symmetry between the primary-side dual ports and adopts a unified phase-shift ratio command. However, owing to non-ideal factors such as device variations among submodules and the asymmetry of transformer leakage inductances, power drift inevitably occurs between the dual ports. Prolonged operation under a unified command is highly susceptible to inducing port power imbalances and the divergence of submodule capacitor voltages. If the power balancing objective was directly incorporated into the MPC cost function, D_1 and D_2 would need to be decoupled into independent predictive variables, which would inevitably expand the optimization search space and substantially increase the computational overhead.

To address the aforementioned issues, this paper introduces a command synthesis stage within the composite hierarchical control strategy. In this strategy, an outer power auxiliary loop acquires the power deviation between the submodules of the upper and lower arms. Following PI regulation, a fine-tuning component Δd is generated. Subsequently, this fine-tuning component is superimposed onto the optimal baseline phase-shift ratio $D_{opt}(k)$ calculated by the MPC, thereby yielding the final independent phase-shift commands $D_{up/low}(k)$ for the respective ports. This scheme effectively resolves the power imbalance issue induced by parameter uncertainties without imposing any additional computational burden on the MPC. It should be noted that the optimal command $D_{opt}(k)$ is dynamically determined through an exhaustive search evaluation of the cost function over a finite discrete set rather than a continuous analytical calculation.

The core of the inner-loop MPC algorithm comprises three key stages: candidate set construction, state prediction, and receding horizon optimization of the cost function. In each control period, the predictive model first receives the reference command $U_3{}^*(k)$ dispatched by the outer loop. In conjunction with the latest sampled voltage and current state variables, it performs a predictive evaluation for the candidate control efforts within the discrete phase-shift set $\Omega_D(k)$. By employing the discrete-time predictive model (5), the system extrapolates the predicted output voltage $U(k + 1)$ and the predicted peak inductor current $i_{L_peak}(k + 1)$ for the subsequent period under the action of various phase-shift ratios. Subsequently, the optimizer substitutes the predicted results into the cost function $J(k)$ for a comprehensive evaluation. On the premise of proactively rejecting hazardous candidates that trigger the hard-constraint Hlimit, the optimizer performs an exhaustive search to identify the safe control effort that minimizes $J(k)$. This selected value is then designated as the optimal net phase-shift ratio $D_{opt}(k)$ for the current control period.

Specifically, the modulation module translates the optimized ratio into actual phase-shift angles. It first superimposes the fine-tuning component onto the baseline optimal ratio: $D_{up}(k) = D_{opt}(k) + \Delta d_{up}(k)$ and $D_{low}(k) = D_{opt}(k) + \Delta d_{low}(k)$. Subsequently, it maps these independent ratios to the final phase-shift angles of the TAB full bridges, i.e., $\beta_{up} = \pi \times D_{up}(k)$ and $\beta_{low} = \pi \times D_{low}(k)$, thereby generating the physical gating signals.

It is crucial to note that the dimensionality reduction assumption ($D_1 = D_2$) relies on the premise that hardware mismatches remain within standard manufacturing tolerances. Within this normal operational validity range, the minor asymmetry is effectively decoupled and compensated by the small independent outer-loop fine-tuning variables ($\Delta d_{up/low}$). However, under extreme asymmetric fault conditions, this predictive approximation would deviate significantly, requiring independent fault-protection interventions.

4.2. Execution Flow of the Discrete Algorithm

While Figure 4 shows the overall signal processing architecture, Figure 5 denotes the discrete algorithm steps executing sequentially within the digital microprocessor's code during each fixed sampling period T_c, which can be summarized into the following steps:

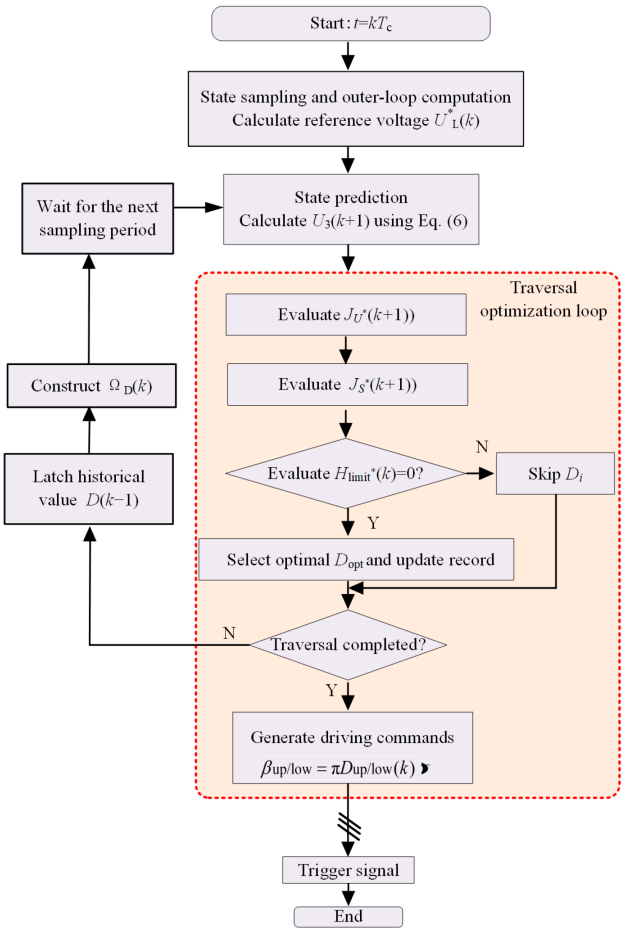

Figure 5. Execution flowchart of the discrete algorithm.

(1) State Sampling and Outer-loop Computation:

At the beginning of each control period T_c, the algorithm is synchronously triggered by a clock signal to sample and update the port voltage and current state variables. Subsequently, the outer power loop performs PI regulation based on the latest power deviation to calculate and generate the inner-loop output voltage reference command $U_L^*(k)$ for the current period.

(2) Candidate Set Construction and State Prediction:

Based on the current operating conditions and tracking error of the system, a discrete sequence of candidate phase-shift ratios, denoted as $\Omega_D(k)$, is dynamically constructed. This effectively prunes the redundant computational space for optimization. Following this, the candidate control efforts in the sequence $\Omega_D(k)$ are sequentially substituted into the discrete-time predictive model to perform forward prediction calculations, yielding the predicted output voltage $U_3(k+1)$ for the next time step.

(3) Cost Evaluation and Constraint Verification (Exhaustive Search Loop):

Utilizing the predicted results, the composite cost function $J(k)$ is calculated. During this evaluation process, a pre-verification of the overcurrent hard constraint is simultaneously executed: if a candidate effort causes the predicted peak current to exceed the safety limit, thereby triggering $H_{limit}(k) \to \infty$, this candidate is directly bypassed. Conversely, if it satisfies the safety constraints, it is included in the optimization comparison. After completing the exhaustive search over the entire discrete sequence, the control effort that minimizes the cost function is selected as the optimal net phase-shift ratio $D_{opt}(k)$ for the current period.

(4) Drive Generation and Historical State Update:

Finally, the optimized $D_{opt}(k)$ is converted into the specific phase-shift drive commands $D_{up/low}(k)$ for the switching devices of each arm, which are then transmitted to the PWM modulation unit to generate the physical gating signals. Concurrently, this optimal control effort $D_{opt}(k)$ is latched into the historical state register as $D(k-1)$. The algorithm execution for the current step is then completed. The system waits for the remaining time of the fixed control period until the next hardware timer interrupt triggers the start of the subsequent sampling cycle.

5. Simulation Verification and Analysis

5.1. Simulation of MMDTC Steady-State Output Performance

To verify the effectiveness of the proposed composite hierarchical MPC strategy, simulation models of the TAB-MMDTC-PET system based on both the traditional PI control and the proposed strategy were developed. Traditional PI control is chosen as the primary comparison benchmark because it represents the robust industry-standard baseline for high-power modular converters. To eliminate the interference of hardware parameters and clearly demonstrate the algorithmic advantages, the physical simulation parameters are kept identical for both control schemes, as detailed in Table 1. The basic parameters of the MPC loop are listed in Table 2.

Figure 6 illustrates the simulation waveforms of the output voltage, output current, arm voltage, and arm current on the MMDTC side under the two control schemes. As observed from the simulation results, the output voltage and current of the system under both control strategies exhibit low harmonic distortion, maintaining a stable output. It should be noted that the total harmonic distortion (THD) values annotated in Figure 6 are directly evaluated using the Fast Fourier Transform (FFT) analysis tool within the simulation environment. The fundamental operating characteristics of the MMDTC remain consistent, further verifying that the introduction of the proposed composite hierarchical MPC strategy does not adversely affect the inherent output performance of the MMDTC.

Table 1. The main parameters of the simulation. Adapted from [13].

Variable	Symbol	Value
Rated grid phase voltage	U_g	10 kV
AC filtering inductor	L_s	5 mH
Rated active power	P_{rated}	1 MW
Fundamental frequency	f	50 Hz
Number of SMs per arm	N	20
Voltage of submodule capacitor	u_C	750 V
Submodule capacitor	C	0.5 mF
Carrier frequency	f_c	2 kHz
LVDC bus voltage	u_{LVDC}	750 V
TAB Transformer Turn Ratio	n_1:n_2:n_3	1:1:1
TAB additional inductor	L	25 µH
Switching frequency	f_s	40 kHz

Table 2. MPC loop parameters.

Variable	Symbol	Value
Weighting factor for the primary tracking objective	λ_U	1
Weighting factor for the auxiliary smoothing term	λ_S	1000
Overcurrent hard-constraint threshold	I_{max}	80 A
Control period	T_c	25 µs
Exhaustive search step size for $\Omega_{D(k)}$	ΔD	0.005

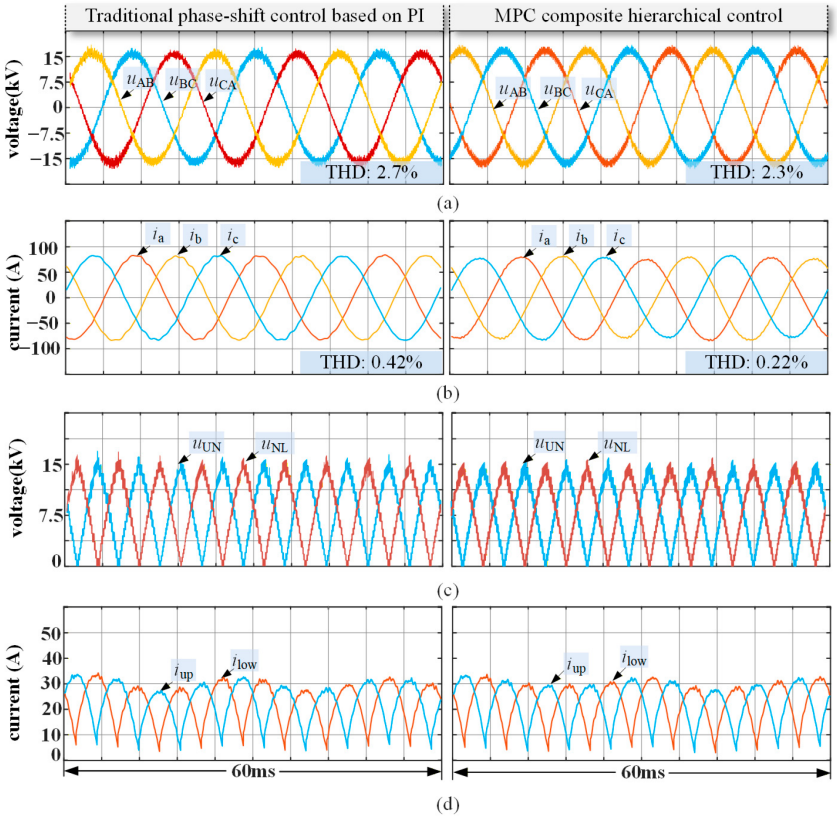

Figure 6. Output waveforms of the MMDTC: (**a**) output line voltage; (**b**) output current; (**c**) arm voltage; (**d**) arm current.

5.2. Comparative Simulation of TAB Dynamic Response Performance

To intuitively verify the dynamic response effectiveness of the proposed strategy, a single-module simulation model of the in-phase dual-input TAB is first developed for

performance evaluation prior to simulating the entire TAB-MMDTC-PET system. Its parameters are identical to those of the full system, with the initial rated load set at 50 kW. The dynamic response simulation results of the system when the secondary-side load undergoes a step increase from 50 kW to 80 kW are presented in Figure 7.

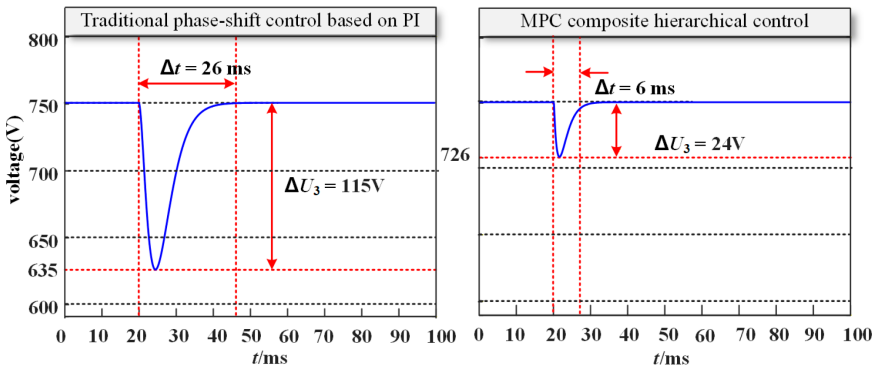

Figure 7. Output voltage waveforms of the TAB under the two control strategies. Blue curves represent the output voltage. Red arrows indicate the recovery time Δt and voltage drop ΔU_3. Vertical red dashed lines mark the load step and voltage recovery instants, while horizontal red dashed lines indicate the minimum voltage. Horizontal black dashed lines serve as voltage reference guides.

Under the traditional phase-shift control, the secondary-side voltage drops to a minimum of 635 V, and the settling time required to recover to the steady state is up to 26 ms. With the proposed composite hierarchical MPC strategy, the voltage drop amplitude of the TAB output voltage after being subjected to the disturbance is only 24 V, and the dynamic response time is 6 ms, representing a reduction of 66.7% compared to the traditional control. This comparison clearly demonstrates the significant advantages of the proposed composite hierarchical control strategy in enhancing the dynamic response speed and disturbance rejection capability of the system.

To verify the suppression effect of the proposed composite hierarchical MPC strategy on transient power overload phenomena, a transient operating condition with an abrupt input voltage sag is established in the simulation: at t = 50 ms, the dual-port voltages on the primary side simultaneously drop to 80% of their initial rated values, and then recover to their normal values at t = 60 ms. The power response waveforms of the primary-side dual ports under the two control strategies are shown in Figure 8.

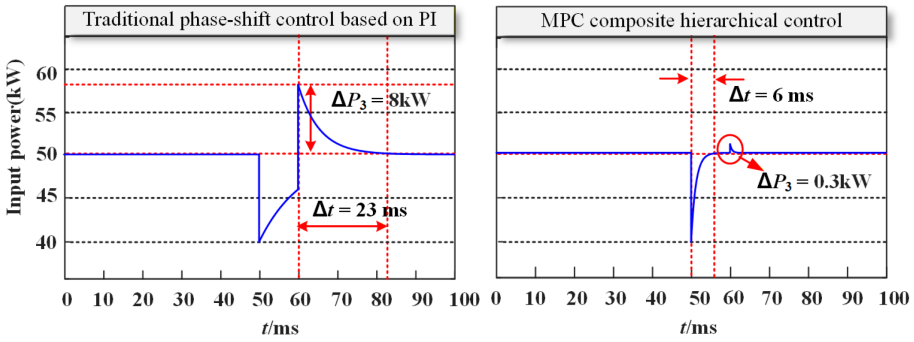

Figure 8. Power waveforms under the two control strategies. Blue curves represent the input power. Red arrows indicate the recovery time Δt and power overshoot ΔP_3. Vertical red dashed lines mark the beginning and end of the indicated recovery intervals, while horizontal red dashed lines indicate the steady-state or peak power levels. The red circle highlights the small overshoot under MPC control. Black dashed lines serve as power-level guides.

Comparing the waveforms, it can be observed that when the voltage sag occurs at t = 50 ms, the input power under both control strategies exhibits a decline. Under the composite hierarchical MPC strategy, the input power can rapidly re-track the steady-state value before the voltage recovers, with a response time of 6 ms. Furthermore, when the voltage recovers at t = 60 ms, the input power experiences only a slight overshoot before rapidly converging to the stable value. In stark contrast, under the traditional in-phase dual-input PI control, when the voltage recovers at t = 60 ms, the input power not only fails to converge in advance but conversely induces a severe transient power surge due to the lag of the phase-shift ratio, causing the primary-side peak power to instantaneously surge to 58 kW.

Figure 9 illustrates the response waveforms of the phase-shift ratio D at the input ports of the TAB under this transient operating condition. During the voltage sag period from t = 50 ms to t = 60 ms, owing to the integrator inertia of the traditional PI control, its net phase-shift ratio fails to track the power deficit promptly. At the instant of voltage recovery at t = 60 ms, the phase-shift ratio D is unable to drop synchronously. Consequently, under the combined effect of the restored high voltage and the lagging large phase-shift ratio, substantial transient power is generated, culminating in a severe power surge.

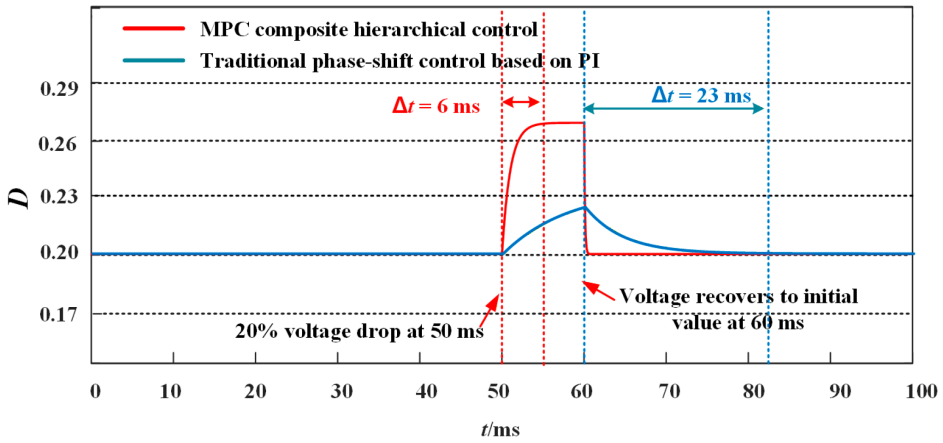

Figure 9. Response waveforms of the net phase-shift ratio under the two control strategies. Red and blue curves represent the net phase-shift ratio D under the proposed MPC and traditional PI control strategies, respectively. Double-headed arrows indicate the response times Δt, and vertical dashed lines mark the corresponding interval boundaries. Single-headed red arrows identify the voltage sag at 50 ms and voltage recovery at 60 ms. Horizontal black dashed lines serve as guides for D values.

In stark contrast, under the proposed composite hierarchical MPC strategy, D rapidly tracks the power deficit during the voltage sag stage at t = 50 ms. At the exact moment of voltage recovery at t = 60 ms, the proposed strategy achieves a rapid rollback of the phase-shift ratio, thereby effectively suppressing the occurrence of power overloads. Comparative analysis reveals that the composite hierarchical MPC strategy effectively prevents the unregulated escalation of the net phase-shift ratio during the voltage sag compensation period. Through real-time feedforward and receding horizon optimization, the MPC rapidly performs an exhaustive search over the discrete set $\Omega_D(k)$ to dispatch the optimal command D_{opt}. This intrinsically mitigates the power overload phenomenon induced at the instant of grid voltage recovery right at the algorithmic level.

Therefore, compared with conventional PI control—which suffers from integrator windup and power surges during severe grid faults—the proposed MPC strategy actively rejects disturbances by proactively enforcing physical safety boundaries, thereby ensuring superior dynamic robustness.

5.3. Verification of Capacitor Voltage Ripple Suppression Effect

To verify the impact of the proposed MPC strategy on ripple voltage suppression, a comparative simulation is conducted between the proposed method and the traditional phase-shift control. The total simulation duration is set to 1 s. The traditional in-phase dual-input phase-shift control is applied from 0 to 0.5 s, and the system switches to the proposed MPC-based hierarchical control from 0.5 to 1.0 s. The simulation results are shown in Figure 10. Under the traditional in-phase dual-input control, the ripple suppression performance is highly effective, yielding a voltage ripple ratio of λ = 2.5%. After the MPC is introduced at t = 0.5 s, the steady-state ripple amplitude of the submodule capacitor voltage slightly increases from 19 V to 25 V, resulting in a voltage ripple ratio of λ = 3.3%.

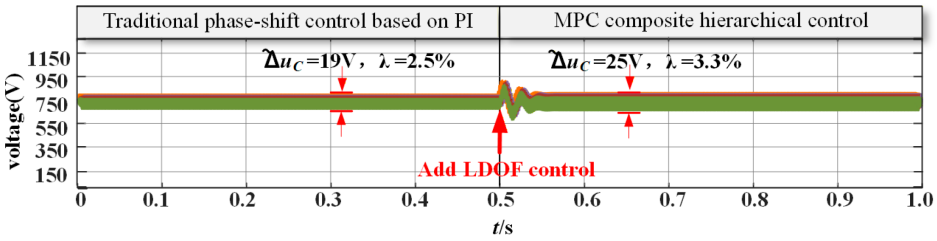

Figure 10. Submodule capacitor voltage waveforms under the two control strategies. Different colored curves represent the capacitor voltages of different submodules. Red arrows indicate the voltage ripple amplitudes and the control transition at 0.5 s.

The underlying cause for this marginal increase in ripple is that the signals acquired during the receding horizon optimization and the exhaustive search of phase-shift ratios inevitably contain high-frequency switching ripples and sampling noise. Under the traditional PI phase-shift control, the steady-state phase-shift ratio D is approximately constant. Consequently, the submodule capacitor voltage ripple Δu_C is predominantly governed by the pure physical charging and discharging processes at the switching frequency. According to the charge integration formula, the ripple under the traditional control can be expressed as:

$$\Delta u_C = \frac{1}{C}\int_0^{T_s/2} i_C(t)dt \tag{13}$$

In this case, $i_C(t)$ contains solely the high-frequency AC component at the switching frequency f_s. However, as the MPC observes the system states in real time, the signal acquisition process inevitably introduces high-frequency switching ripples and sampling noise, denoted as $\tilde{d}$. Substituting these noise-corrupted observations into the control equation, the actual dispatched phase-shift ratio command becomes:

$$\Delta D_{\text{New}} = \Delta D_{\text{opt}} + K_{\text{MPC}}\tilde{d}_{\text{noise}}(t) \tag{14}$$

where K_{MPC} represents the equivalent feedforward gain coefficient within the MPC loop.

Therefore, following the introduction of the MPC-based hierarchical control, $D_{\text{new}}(t)$ is no longer a strict constant but incorporates a minuscule high-frequency jitter term $K_{\text{MPC}} \cdot \tilde{d}_{\text{noise}}(t)$. This induces continuous micro-adjustments in the instantaneous power transferred by the TAB.

5.4. Simulation Analysis During the Startup Phase and Under Load Step Conditions

(1) Simulation Analysis During the Startup Phase

To verify the dynamic performance of the proposed scheme during the converter startup phase, a comparative simulation is conducted between the traditional phase-shift

control and the proposed composite hierarchical MPC scheme. The corresponding simulation waveforms during the startup phase are presented in Figure 11.

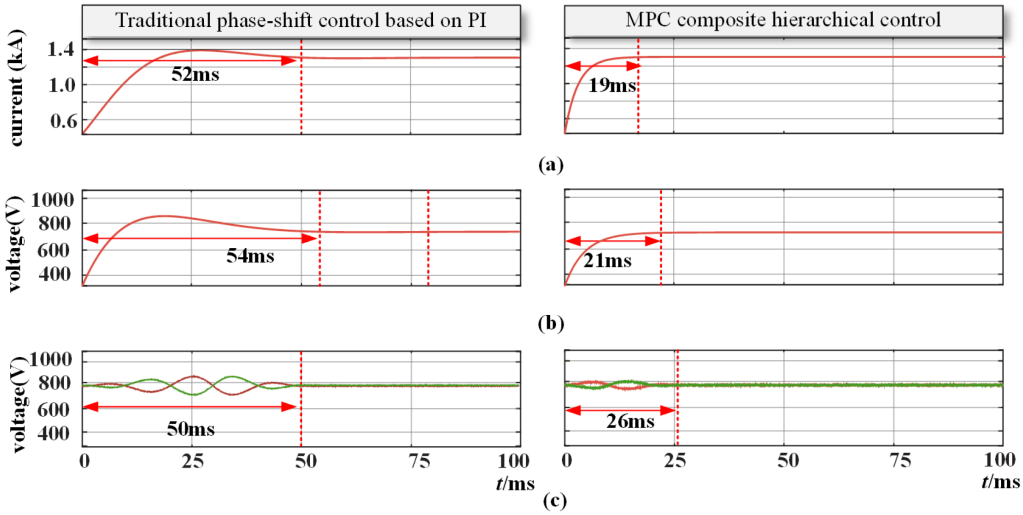

Figure 11. Simulation waveforms under the two control strategies during the startup phase: (**a**) output current of the TAB; (**b**) output voltage of the TAB; (**c**) submodule capacitor voltage. Red double-headed arrows indicate the startup settling times, and vertical red dashed lines provide time markers. The curves in (**a**,**b**) represent the TAB output current and voltage, respectively. Different colored curves in (**c**) represent the capacitor voltages of different submodules.

As observed from the simulation results, under the traditional phase-shift control scheme, the output current exhibits an overshoot phenomenon during the startup phase, and the settling time required to reach the steady state is up to 52 ms. In contrast, with the proposed composite hierarchical MPC scheme, the current response is smooth and devoid of overshoot, rapidly reaching the steady state in merely 19 ms. Concurrently, the traditional scheme suffers from a substantial voltage overshoot during startup, requiring 54 ms to recover to the steady state. Conversely, the composite hierarchical MPC scheme ensures a smooth and rapid voltage startup with negligible overshoot, significantly reducing the settling time to a mere 21 ms. Furthermore, during the initial startup stage, the submodule capacitor voltages of the upper and lower arms under the traditional scheme exhibit large fluctuation amplitudes, taking 50 ms to gradually converge. Under the proposed composite hierarchical MPC scheme, these initial voltage fluctuations are effectively suppressed, and the convergence time is shortened to 26 ms.

Since the MPC method performs optimization calculations for the phase-shift ratio of the TAB converter in every control period, it effectively minimizes the settling time during the initial regulation stage when the tracking error is substantial. Meanwhile, as the error approaches zero near the steady state, it precisely selects an appropriate control effort based on the predictive model, thereby effectively preventing the occurrence of system overshoot.

(2) Simulation Analysis Under Load Step Conditions

To analyze the dynamic response performance of the proposed scheme, a severe load step change is introduced at t = 60 ms. In this simulation condition, the system is connected to a purely resistive DC load. Specifically, the system initially operates at 50% half-load (500 kW, equivalent to a 1.125 Ω resistance). At t = 60 ms, the load resistance is abruptly stepped down to 0.5625 Ω, demanding that the system instantly output its 100% rated full-load power (1 MW). Figure 12 illustrates the transient response comparison between the traditional phase-shift control and the proposed composite hierarchical MPC scheme under this massive load transition.

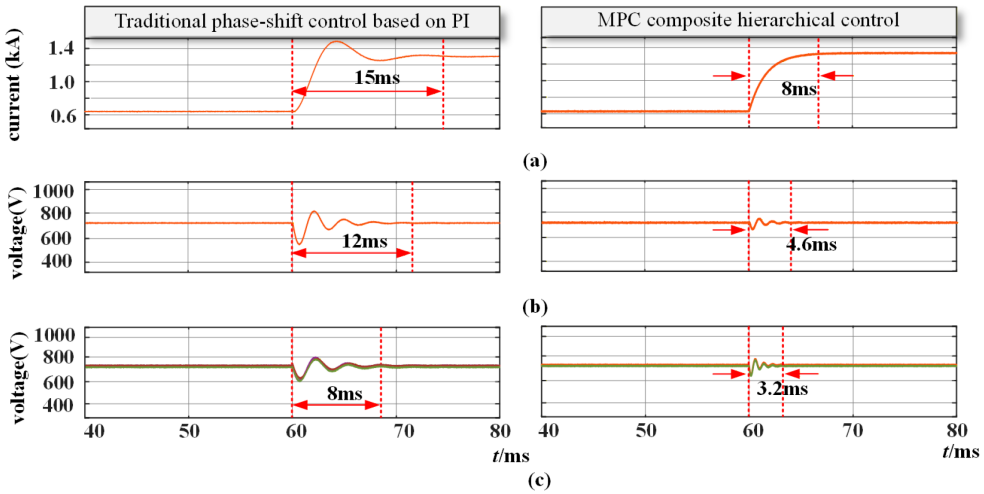

Figure 12. Simulation waveforms under the two control strategies under load step conditions: (**a**) output current of the TAB; (**b**) output voltage of the TAB; (**c**) submodule capacitor voltage. Red arrows indicate the recovery times following the load step. Vertical red dashed lines mark the load-step instant and the end of each recovery interval.

Figure 12a shows that when a load step increase occurs, the TAB output current under the traditional scheme exhibits an overshoot, requiring approximately 15 ms to regain the steady state. In contrast, the current response under the composite hierarchical MPC scheme is rapid, smooth, and devoid of overshoot, with the recovery time substantially reduced to 8 ms. As illustrated in Figure 12b, the TAB output voltage under the traditional scheme experiences a deep drop at the instant of the step change, accompanied by prolonged underdamped oscillations, taking 12 ms to completely stabilize. By comparison, the proposed composite hierarchical MPC scheme significantly mitigates the voltage drop amplitude, achieving rapid convergence in merely 4.6 ms, thereby effectively suppressing the dynamic voltage drop. Furthermore, following the step change, the submodule capacitor voltages under the traditional scheme exhibit noticeable low-frequency fluctuations, with a recovery process lasting up to 8 ms. Conversely, the proposed scheme substantially attenuates the transient impact on the capacitor voltages, rapidly recovering to the vicinity of the rated voltage within 3.2 ms.

Although the MPC-based hierarchical control strategy marginally sacrifices the capacitor ripple performance, it achieves a substantial enhancement in the system's dynamic performance. Compared with traditional control, this hierarchical strategy confronts large-signal disturbances with lower overshoot and a faster convergence rate, thereby significantly improving the overall disturbance rejection capability of the system.

To present the comparison results more intuitively, the relevant data are summarized in Table 3. Consequently, compared to traditional control, this hierarchical strategy confronts large-signal internal load disturbances with significantly lower voltage deviations and faster convergence rates. By effectively suppressing both external grid faults and internal load step impacts, the proposed strategy clearly demonstrates the enhancement of the overall disturbance rejection capability of the TAB-MMDTC-PET system.

5.5. Robustness and Sensitivity Analysis

Model-based predictive control strategies are inherently sensitive to parameter uncertainties and measurement noise. To evaluate the practical viability of the proposed composite hierarchical MPC, a dedicated robustness study was conducted. The analysis considers four typical non-ideal conditions: inductance variation, capacitance variation,

measurement noise, and parameter mismatch between ports. The corresponding dynamic behaviors are presented in Figure 13.

Table 3. Comprehensive performance comparison between the two control schemes.

Assessment Parameter	Traditional PI-Based Phase-Shift Control	Proposed Composite Hierarchical MPC	Remarks
Steady-State Current THD	0.42%	0.22%	MPC provides slightly cleaner steady-state waveforms
Load Step Voltage Drop	115 V	24 V	MPC reduces the transient voltage drop by ~79%
Dynamic Settling Time	26 ms	6 ms	MPC significantly accelerates transient recovery
Power Overshoot	Severe	Negligible	MPC actively restrains overcurrent via hard constraints
Startup Transients	Noticeable overshoot	Zero overshoot	MPC enchances safer physical initialization
Capacitor Voltage Ripple	19 V	25 V	PI exhibits better ripple suppression; MPC introduces slight high-frequency jitter
Hardware Limitations	None	Bounded by computational power	MPC requires powerful DSPs for receding horizon optimization

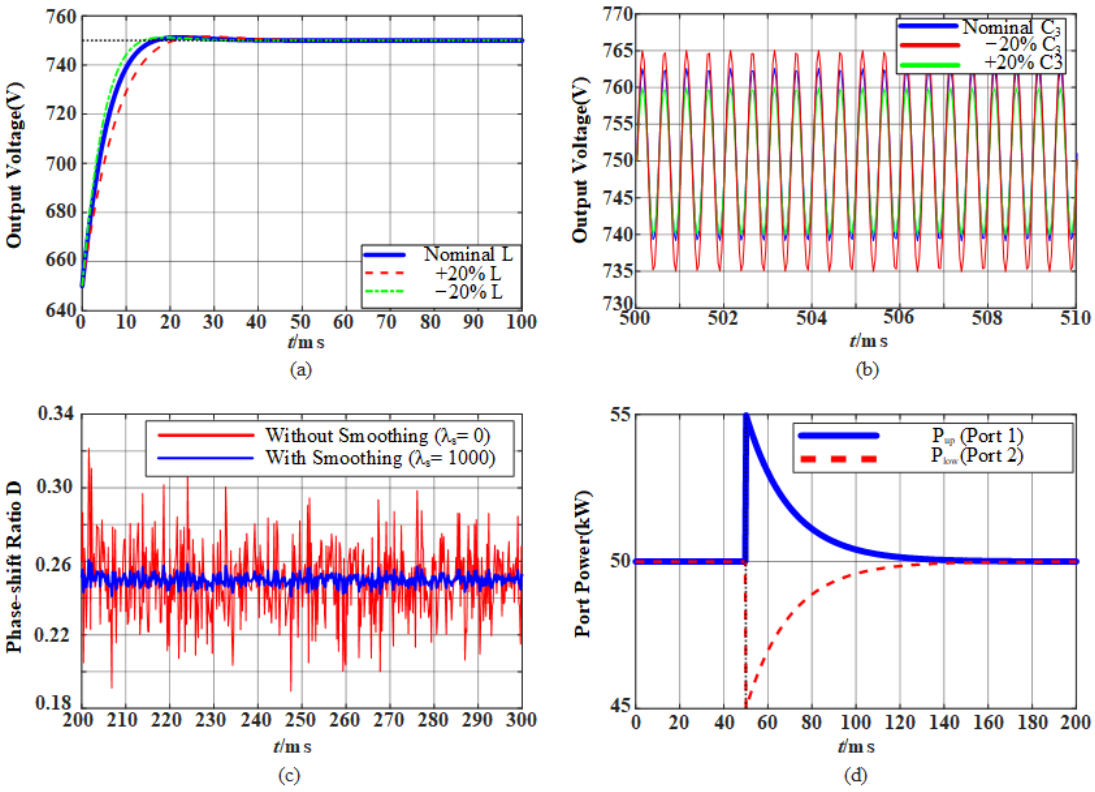

Figure 13. Parameter sensitivity analysis of (**a**) step response under L variation, (**b**) steady-state ripple under C_3 variation, (**c**) phase-shift command $D(k)$ under measurement noise, and (**d**) port power balancing under 10% impedance mismatch.

(1) Inductance Variation

Figure 13a illustrates the system's dynamic step response when the actual power transfer inductance L deviates from the nominal value of the predictive model by ±20%.

Although this parameter perturbation introduces a minor transient mismatch within the internal prediction horizon, the outer-loop PI controller effectively compensates for the deviation via its integral action. As a result, the system maintains zero steady-state error with negligible degradation in dynamic tracking performance.

(2) Capacitance Variation

To simulate component aging and thermal drift, the secondary-side capacitor C_3 was subjected to ±20% variations. As shown in Figure 13b, while the steady-state output voltage ripple slightly fluctuates in accordance with fundamental physical relationships (i.e., a smaller capacitance yields a larger ripple), the overall closed-loop stability and transient settling times remain well within acceptable operational bounds.

(3) Measurement Noise

To replicate harsh industrial environments where feedback signals are corrupted by sensor interference, explicit Gaussian white noise was injected into the sampled voltage and current channels. As depicted in Figure 13c, the incorporation of the control-effort smoothing penalty term (J_S, regulated by the weighting factor λ_S) effectively attenuates high-frequency observation perturbations. This mechanism mitigates erratic chattering in the resulting phase-shift commands, thereby supporting stable and clean switching actions.

(4) Parameter Mismatch Between Ports

The proposed physically grounded dimensionality reduction is based on the assumption of highly symmetric primary-side ports ($D_1 \approx D_2$). To test the controller's robustness against physical asymmetries, a deliberate 10% impedance mismatch was introduced between the upper and lower primary-side ports. The waveforms in Figure 13d confirm that the decoupled outer-loop auxiliary fine-tuning variables ($\Delta d_{up/low}$) successfully compensate for the asymmetric power drift. The port powers are actively rebalanced without imposing any multi-dimensional optimization burden on the core MPC algorithm.

5.6. DSP Execution-Time Verification

To practically validate the real-time feasibility of the proposed composite hierarchical MPC strategy, a hardware execution-time verification was conducted. The algorithm was deployed on a standard industrial Texas Instruments TMS320F28335 digital signal processor (DSP) operating at 150 MHz. To ensure maximum transparency and industrial relevance, the control code was developed in C utilizing the 32-bit hardware Floating-Point Unit (FPU). Furthermore, the core routines were executed directly from the zero-wait-state local RAM to minimize instruction access latency. The CCS Clock Profiling tool was utilized to precisely capture the CPU cycles consumed by the entire control sequence.

Table 4 details the exact hardware profiling breakdown. The total worst-case execution time—encompassing ADC reading, outer-loop PI regulation, predictive optimization, and PWM updates—is bounded at 14.10 μs. Given the designated discrete control period of Tc = 25 μs, the proposed algorithm consumes approximately 56.4% of the available CPU time per cycle. This leaves an adequate margin of 10.90 μs for essential background tasks, such as communication and safety protection routines. These hardware-level empirical data clearly demonstrate that the proposed physically grounded dimensionality reduction effectively bridges the gap between theoretical multi-objective optimization and the strict real-time execution limits of industrial microprocessors.

Table 4. Execution time breakdown of the proposed algorithm on TMS320F28335.

Control Module	Clock Cycles	Execution Time @ 150 MHz
ADC Data Reading and Scaling	152	1.01 μs
Outer-loop PI Controller	178	1.18 μs
Candidate Set Construction and State Prediction	75	0.50 μs
Reduced-Order MPC Optimization Loop	1645	10.97 μs
PWM Register Update	65	0.44 μs
Total Worst-Case Execution Time	2115	14.10 μs

6. Conclusions

To address the coupling characteristics of the dual input ports in the TAB-MMDTC-PET topology, as well as the inherent deficiencies of traditional PI-based phase-shift control under complex operating conditions—such as a sluggish dynamic response and susceptibility to transient overcurrents—this paper proposes a composite hierarchical control strategy based on MPC. By optimizing the cost function and the control set, this strategy substantially mitigates the computational burden while preserving the superior dynamic response characteristics and the fast multi-objective optimization advantages of MPC. Furthermore, by exploiting the natural time-scale separation between the decoupled outer-loop PI regulation and the inner-loop predictive optimization, the proposed composite control framework ensures robust dynamic coordination. Specifically, the embedded hard-constraint mechanism effectively restricts transient operational trajectories within a safe bounded region, thereby supporting Bounded-Input Bounded-Output (BIBO) stability under severe large-signal disturbances. This theoretical attribute, combined with the verified real-time DSP execution capability, demonstrates that the proposed strategy bridges the gap between advanced predictive performance and practical engineering reliability.

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