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Design of a Novel Hybrid Switched-Inductor/Switched-Capacitor DC-DC Step-Up Converter

Muhammad Uzair Shah [1,*], Zakir Ullah [2], Mohammed Alqarni [3], Muhammad I. Masud [3], Ajmal Farooq [1], Mian Muhammad Amir Ayaz [1] and Fazal Muhammad [1]

[1] Department of Electrical Engineering, University of Engineering and Technology Mardan, Mardan 23200, Pakistan; ajmal@uetmardan.edu.pk (A.F.); ayazamir94@gmail.com (M.M.A.A.); fazal.muhammad@uetmardan.edu.pk (F.M.)
[2] Centre for Wireless Communications-Radio Engineering, University of Oulu, 90570 Oulu, Finland; zakir.ullah@oulu.fi
[3] Department of Electrical Engineering, College of Engineering, University of Business and Technology, Jeddah 21361, Saudi Arabia; m.alqarni@ubt.edu.sa (M.A.); m.masud@ubt.edu.sa (M.I.M.)
* Correspondence: engruzairshah95@gmail.com

Abstract

In this paper, a new topology of a step-up DC converter is presented for renewable energy applications, yielding a high step-up conversion ratio and reduced voltage stress across the switches. The proposed converter uses a hybrid switched-inductor and switched-capacitor cell to achieve the high voltage gain. Additionally, the capacitors in the switched cell also perform the function of clamping the voltage across switches. The proposed converter utilizes only a single controlled switch and operates in only two modes of conduction. The steady-state analysis and operating principle of the proposed hybrid step-up converter are discussed in detail and various mathematical equations have been derived. The analysis shows numerous improvements over the traditional DC-DC converters. Simulation was carried out in MATLAB Simulink 2021b on a 55% duty cycle and simulation results are compared with theoretical analysis. From simulation results, it is clear the proposed converter exhibits better performance compared to conventional boost and other traditional step-up converters with the same design parameters. Finally, a 31.5-watt hardware prototype was constructed and tested in the laboratory to experimentally validate the theoretical and simulation results.

Keywords: hybrid; switched inductor; switched capacitor; high voltage gain; DC-DC boost converter

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1. Introduction

Connecting renewable micro-sources to the grid is challenging because their output voltages are inherently low and tend to fluctuate [1–4]. A standard setup of a solar system used to boost this low-DC voltage is shown in Figure 1. Engineers often rely on classic boost converters for this low-DC-to-high-DC voltage converter, which, while reaching the needed voltage, requires extreme duty ratios. Running a converter at these limits takes a toll on the hardware, leading to high voltage stress, diode reverse-recovery problems, and poor efficiency [5–8].

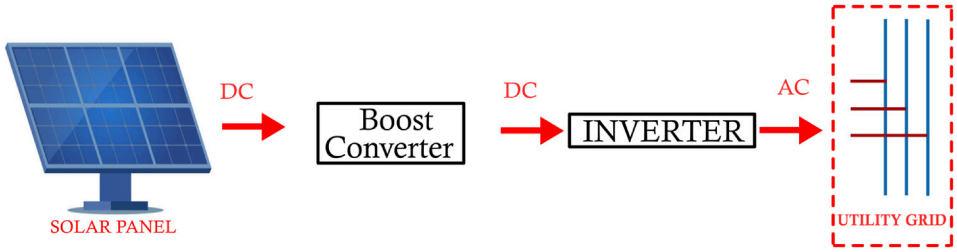

Figure 1. Block diagram of a typical photovoltaic system.

An approach to achieving high voltage gain utilizes the Dickson switched-capacitor method, in which more components are used. Using more components means high power loss, low efficiency and a system that is more prone to failure [9]. Another common option involves the use of isolated converters; however, these require high-frequency transformers. The leakage inductance from these transformers creates harmful voltage spikes on the power switches [10]. Non-isolated converters avoid this problem entirely, and since they do not use a transformer, they cost less and take up less space. To bypass the drawbacks of a maxed-out duty cycle, the focus has recently moved to switched-inductor (SL) and switched-capacitor (SC) architectures [11]. The techniques, based on Conventional Boost Converters, which use boosting techniques, involve switched inductors (SLs) [12], switched capacitors (SCs) [13], voltage multiplier cells (VMCs) [14], voltage lift techniques (VLTs) [15], multistage converters [16] and magnetic couplings [17]. The converter techniques discussed above are non-isolated, high-gain, energy-efficient, low-cost and small in size compared to transformer-based converters. Additionally, the combination of the discussed converters can be used to enhance conversion ratios, such as switched inductors with magnetic coupling [18] and switched inductors with voltage lift [19].

High voltage can be achieved using the switched-inductor technique with low voltage stress on the switch. Ref. [11] uses the Active Switching inductor technique to focus on reducing voltage stress on the switch, but the voltage stress on the diode is more than the output voltage. In [20], the ASL is combined with SC networks. The authors combine a ladder switched-capacitor network with a regenerative boost configuration with ASL in [21]. The technique produces high voltage gain; however, it is bulky in size and costly.

A hybrid switched-inductor and switched-capacitor (HSLSC) step-up converter is presented in this paper by integrating the switched-inductor and switched-capacitor cells. The proposed circuit is unique to any other topology and boasts very high voltage gain without using any transformer.

2. Working Principle of the Proposed Converter

The proposed hybrid DC-DC converter combines switched-capacitor and switched-inductor design to increase the voltage conversion ratio by a certain multiplication factor. This design offers better voltage gain and less output voltage ripple, is more efficient, and has less voltage stress across the switching device than the typical traditional boost converter. It consists of a switched-inductor cell made of two inductors and three diodes and a switched-capacitor cell made of two capacitors and two diodes. Figure 2 shows the circuit diagram for the suggested hybrid switched-inductor switched-capacitor (HSLSC) architecture.

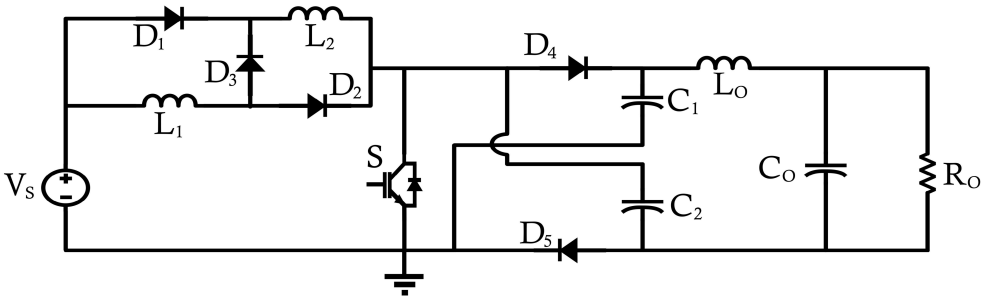

Figure 2. Proposed HSLSC topology.

2.1. Operating Principle

The total conversion is based on the power switch periodically switching to permit power transfer from the input to the output. Three inductors, five diodes, and three capacitors make up the circuit of the suggested topology, which is shown in Figure 2. Since both the standard boost converter and the proposed High-Step-Up Interleaved Conventional Boost Converter (HSICBC) use a single electrical switch, their working principles are quite similar. The usage of a switched coil and switched capacitors are the main differences between the hybrid switched-inductor switched-capacitor (HSLSC) converter and the traditional boost converter. In particular, two coils, each collectively referred to as a switched coil, replace the traditional single coil in the HSLSC DC-to-DC converter.

The suggested converter is taken to be in a steady state in order to streamline the study. We assume an ideal system to simplify the analysis: a pure-input DC voltage source (V_s), all components operating at 100% efficiency, and capacitors large enough so that voltage ripple is negligible at the switching frequency (fs). Under these conditions, the circuit operates in two primary states determined by switch S1: the ON-state when it conducts, and the OFF-state when it opens.

2.1.1. ON-Mode (0 to DTs)

During the conduction phase, the voltage source charges both inductors in parallel through diodes D_1 and D_2 and the active switch S. This configuration creates a direct, shortened path for the current to return to the source, effectively isolating the rest of the network. Meanwhile, diodes D_4 and D_5 remain reverse-biased (off) as capacitors C_1 and C_2 discharge into the load via the output inductor (L_{out}). This specific state is illustrated in the equivalent circuit diagram in Figure 3.

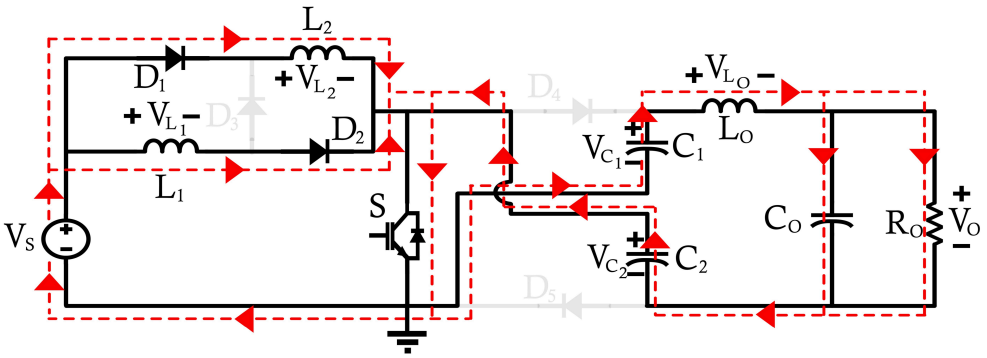

Figure 3. HSLSC ON-mode equivalent circuit.

When MOSFET S is conducting as shown in Figure 3, inductors L_1 and L_2 have the same voltage because of parallel connections. The input inductor voltages in this mode are obtained using Kirchhoff's Voltage Law (KVL):

$$V_{L1} = V_{L2} = V_S \tag{1}$$

As $L_1 = L_2 = L$, the voltage across each inductor is identical, so:

$$V_{L1} = V_{L2} = V_L = V_S \tag{2}$$

Applying Kirchhoff's Voltage Law (KVL) to the output loop, the voltage across the output inductor L_o is expressed as:

$$V_{LO} = V_{c1} + V_{c2} - V_O \tag{3}$$

As both the capacitors C_1 and C_2 have same value, their voltages are equal and are given by:

$$V_{c1} = V_{c2} = V_c \tag{4}$$

From Equations (3) and (4) we get:

$$V_{LO} = 2V_c - V_O \tag{5}$$

2.1.2. OFF-Mode (DTs to Ts)

When switch S turns off, diodes D_1 and D_2 stop conducting (reverse-biased), while diodes D_3, D_4, and D_5 turn on (forward-biased). In this state, the two inductors work together with the input source to charge capacitors C_1 and C_2 in parallel. Simultaneously, inductor Lo transfers energy to charge the output capacitor C_o, as illustrated in Figure 4.

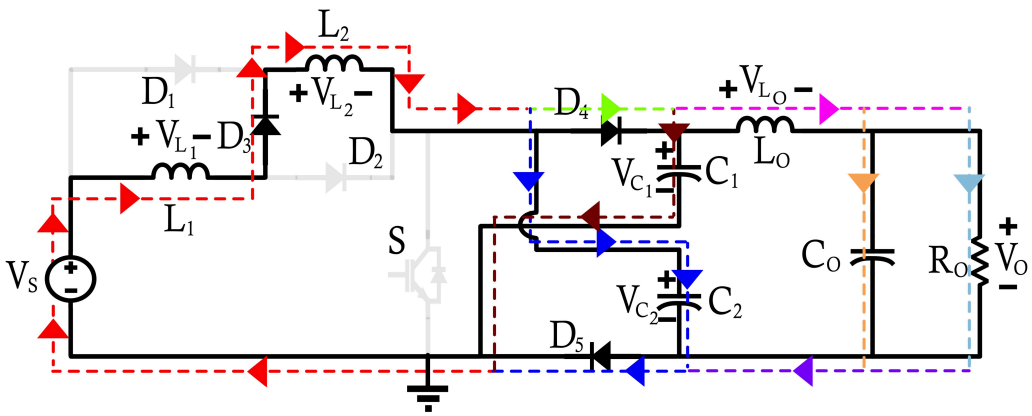

Figure 4. HSLSC OFF-mode equivalent circuit.

Applying Kirchhoff's Voltage Law (KVL) to the inner and outer loops yields the following equations:

$$V_L = \frac{V_S - V_C}{2} \tag{6}$$

$$V_{Lo} = V_c - V_o \tag{7}$$

2.2. Voltage Transfer Gain of the Proposed HSLSC Converter Topology

To find the voltage conversion ratio of the proposed HSLSC topology, we apply the inductor volt-second balance (VSB) principle to inductors L_1, L_2, and L_o. This allows us to calculate the steady-state voltage across each capacitor.

When the volt-second balance condition is applied to inductors L_1 and L_2 under the assumption that $L_1 = L_2 = L$.

With a VSB of $L_1 = L_2 = L$ we get:

$$V_{c1} = V_{c2} = V_c = \frac{1+D}{1-D} V_S \tag{8}$$

By VSB of L_o we get:

$$V_o = \frac{(1+D)^2}{(1-D)} V_S \tag{9}$$

The DC voltage gain (conversion ratio) of the converter is expressed as:

$$G_V = \frac{V_O}{V_S} = \frac{(1+D)^2}{(1-D)} \tag{10}$$

3. Steady-State Waveform of the Proposed HSLSC Topology

Figure 5 shows the main waveforms for the converter running in continuous conduction mode. It also includes zoomed-in views to clearly show how the values change. During the ON-mode interval, the gate voltage signal V_g remains at a high logic level for 55% of the complete switching period. During this stage, the current passing through L_1 and L_2 rises linearly, as depicted by the waveform labeled i_{L1}, i_{L2}. The corresponding time-domain variation (ripple) in the inductor current is denoted as Δi_L. The third waveform illustrated in Figure 5 indicates that capacitors C_1 and C_2 discharge into the output load during the ON-mode. Conversely, during the OFF-mode, these capacitors are recharged by both the input source and the energy stored in the inductors which was energized previously.

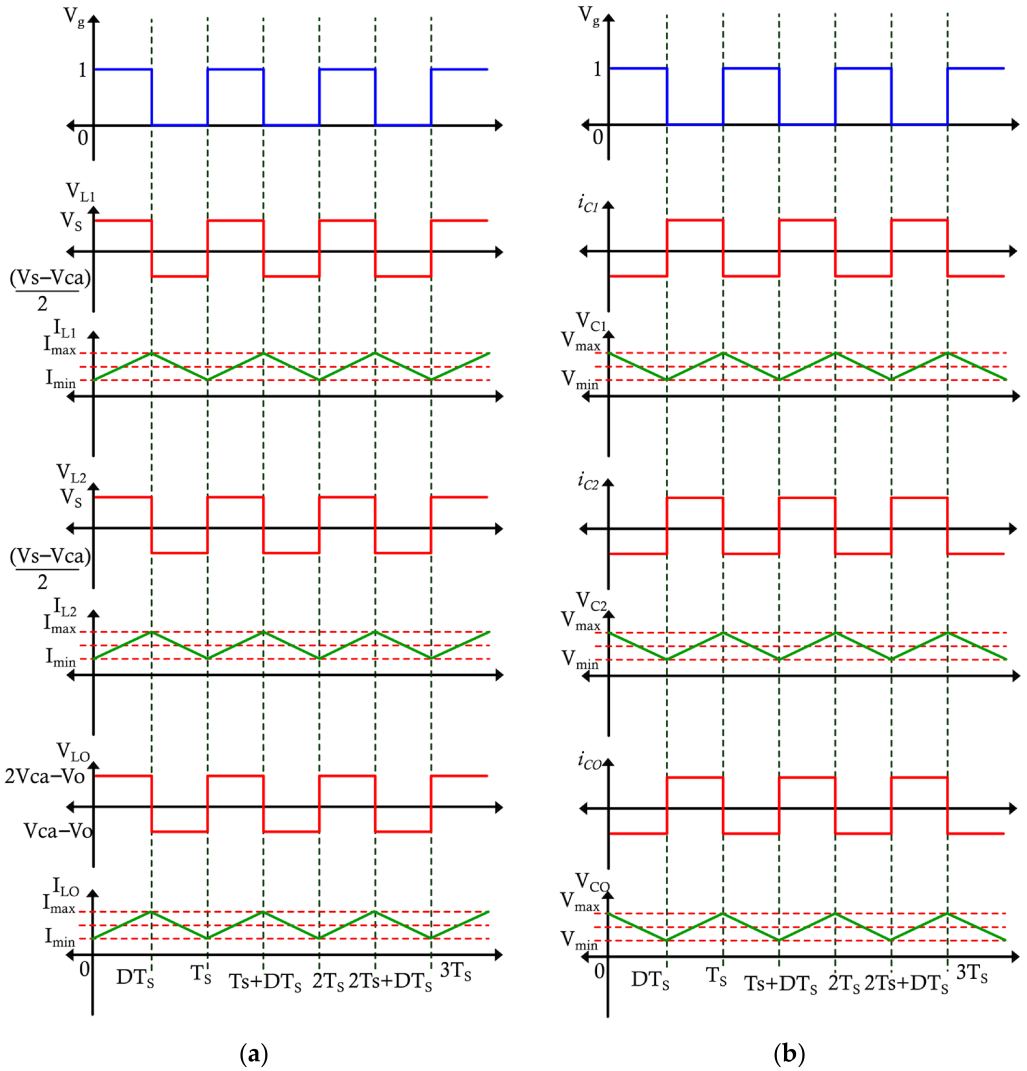

Figure 5. Steady-state waveforms of the proposed converter HSLSC. (**a**) shows the voltage and current waveform of the inductors L_1, L_2 and L_3; (**b**) shows the current and voltage waveform of the capacitors C_1, C_2 and C_{out}.

3.1. Current and Voltage Ripples

By looking into the inductor current waveform shown in Figure 5, the peak-to-peak ripple in inductors L_1 and L_2 represented by ΔI_1 and ΔI_2 can be obtained by using inductor voltage in the ON-mode of the converter as given below:

$$\Delta I_1 = \Delta I_2 = D.\frac{V_S}{f.L} \tag{11}$$

Similarly, the peak-to-peak ripple in inductor L_o represented by ΔI_O can be obtained by using inductor voltage in the OFF-mode of the converter as given below:

$$\Delta I_O = (1-D).\frac{V_c - V_O}{f.L_O} \tag{12}$$

The peak-to-peak ripples in capacitor voltage can be obtained using the same procedure as:

$$\Delta V_O = DT.\frac{V_o(1-D)}{8L_O.C_0.f_2} \tag{13}$$

$$\Delta V_{c1} = \Delta V_{c2} = \Delta V_c = \frac{DV_0}{RCf} \tag{14}$$

3.2. Voltage Stress on Semiconductor Devices

The voltage stress/maximum voltage across the main switch S and other diodes reveals they are not conducting. These voltage stresses are obtained as:

$$V_s = V_{c1} = V_{c2} = V_c = \frac{1+D}{1-D}V_S = \frac{V_O}{1+D} \tag{15}$$

Similarly, the voltage stress across diodes can be obtained as:

$$V_{D1} = V_{D2} = -\frac{V_S - V_c}{2} \tag{16}$$

$$V_{D3} = -V_S \tag{17}$$

$$V_{D4} = V_{D5} = -V_C \tag{18}$$

3.3. Discontinous Conduction Mode (DCM) Analysis

The proposed converter enters discontinuous conduction mode (DCM) when the inductor's L_1, L_2 and L_o values fall below their critical values, given in Equations (19) and (20).

$$L_{1(\min)} = L_{2(\min)} = L_{in(\min)} = \frac{D(1-D)^2R_0}{2(1+D)^3 f} \tag{19}$$

$$L_{O(\min)} = \frac{D(1-D)R_0}{2(1+D)f} \tag{20}$$

The above values are based on the CCM/DCM boundary condition when inductor current reaches zero.

$$I_{L1(avg)} = I_{L2(avg)} = \frac{\Delta I_L}{2} \tag{21}$$

$$I_{Lo(avg)} = \frac{\Delta I_{LO}}{2} \tag{22}$$

The converter remains in CCM until $L_1 = L_2 > L_{in(min)}$ and $L_o > L_{o(min)}$.

When the half value of the inductor current ripple increases to more than its average value, the converter enters DCM with a third mode in which inductor current remains zero. The circuit diagram for DCM is shown in Figure 6.

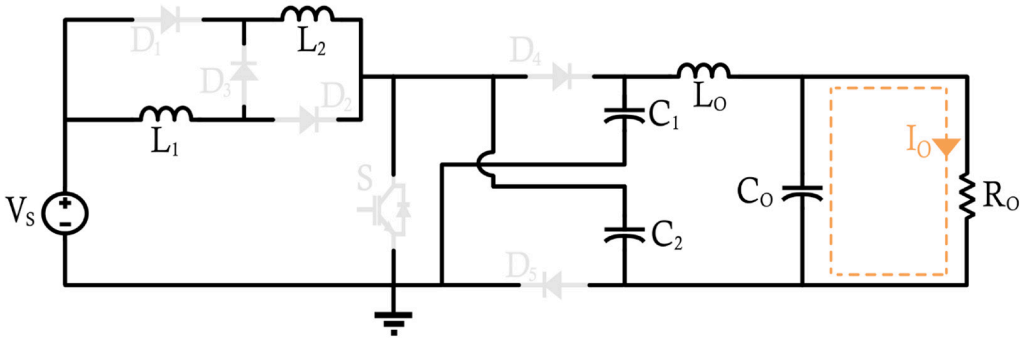

Figure 6. Discontinuous conduction mode (DCM) equivalent circuit.

The inductor current waveforms in discontinuous conduction mode (DCM) are given in Figure 7.

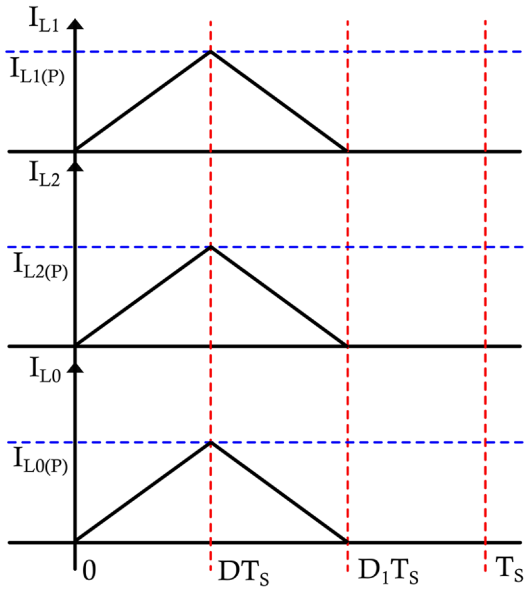

Figure 7. Discontinuous conduction mode waveforms of the proposed converter HSLSC.

The current through every inductor I_{L1}, I_{L2} and I_{L3} becomes zero due to the existence of a third mode from the D_1T_s to T_s time interval.

The voltage gain in DCM voltage is given by Equation (23):

$$\text{MDCM} = \frac{1}{2}\left[1 + \sqrt{1 + \frac{8D^2R_0}{fk}}\right] \tag{23}$$

and

$$K = \frac{2LL_0}{2L + L_0} \tag{24}$$

3.4. Dynamic Modeling

The small signal model of the proposed converter is obtained using the state-space averaging technique.

As $L_1 = L_2 = L$ and $C_1 = C_2 = C$, the state variables are:

$$X = [i_{L1}, i_{L2}, i_{LO}, v_{C1}, v_{C2}, v_O]^T \quad (25)$$

As $i_{L1} = i_{L2} = i_L$ and $v_{C1} = v_{C2} = v_C$, the reduced variables are:

$$X = [i_L, i_{LO}, v_C, v_O]^T \quad (26)$$

The control input and output are given below:

$$u = V_S \quad (27)$$

$$y = V_O \quad (28)$$

The control variable is duty cycle d(t).
The average state space model is given by the generalized equation below:

$$x'(t) = Ax(t) + BVu + B_d d \quad (29)$$

$$\begin{bmatrix} i'_L \\ i'_{LO} \\ v'_C \\ v'_O \end{bmatrix} = \begin{bmatrix} 0 & \frac{-1-D}{2L} & 0 & 0 \\ \frac{1-D}{2C} & 0 & \frac{-1+D}{2C} & 0 \\ 0 & \frac{1+D}{L_o} & 0 & \frac{-1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix} \begin{bmatrix} i_L \\ i_{LO} \\ v_C \\ v_O \end{bmatrix} + \begin{bmatrix} \frac{1+D}{2L} \\ 0 \\ 0 \\ 0 \end{bmatrix} u + \begin{bmatrix} \frac{V_S+V_C}{2L} \\ \frac{(-I_L+I_O)}{2C} \\ \frac{V_C}{L_O} \\ 0 \end{bmatrix} d$$

$$y = Cx + Du \quad (30)$$

$$y = [0,\ 0,\ 0,\ 1] \begin{bmatrix} i_L \\ i_{LO} \\ v_C \\ v_O \end{bmatrix} + 0u$$

where $x'(t)$ = derivative of x(t), x(t) is the state variable matrix, u is the input vector, y is the output vector, A is the state matrix, B_V is the input matrix, B_d is the control matrix, C is the output matrix and D is the direct transmission matrix.

$$A = \begin{bmatrix} 0 & \frac{-1-D}{2L} & 0 & 0 \\ \frac{1-D}{2C} & 0 & \frac{-1+D}{2C} & 0 \\ 0 & \frac{1+D}{L_o} & 0 & \frac{-1}{L_o} \\ 0 & 0 & \frac{1}{C_o} & \frac{-1}{R_o C_o} \end{bmatrix}, B_d = \begin{bmatrix} \frac{V_S+V_C}{2L} \\ \frac{(-I_L+I_O)}{2C} \\ \frac{V_C}{L_O} \\ 0 \end{bmatrix}, B_V = \begin{bmatrix} \frac{1+D}{2L} \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

Control to output transfer function is given by Equation (31).

$$Gvd(s) = \frac{\hat{v}_o(s)}{\hat{d}(s)} = \frac{\frac{V_S(1+D)}{L_O(1-D)}\left[s^2 - \frac{(1+D)^2}{R_O C(1-D)}s + \frac{(1-D)(3-D)}{4LC}\right]}{\left(C_O s^2 + \frac{1}{R_O}s + \frac{1}{L_O}\right)\left(s^2 + \frac{(1-D)^2}{4LC}\right) + \frac{(1+D)^2}{2CL_O}s\left(C_O s + \frac{1}{R_O}\right)} \quad (31)$$

3.5. Effieciency and Power Loss Calculation

Total power loss $P_{(Loss)}$ in the proposed converter is equal to the sum of the conduction power losses $P_{(Cond)}$ and switching losses $P_{(SW)}$.

$$P_{(Loss)} = P_{(Cond)} + P_{(SW)} \quad (32)$$

$$P_{cond} = P_{L1} + P_{L2} + P_{D1} + P_{D2} + P_{D3} + P_{D4} + P_{D5} + P_{C1} + P_{C2} + P_{CO} + P_{LO} + P_S \quad (33)$$

The switching loss in the MOSFET is given by:

$$P_{SW} = {}^{1}/_{2}[V_{S(max)} \cdot I_{S(max)} \cdot f_S \cdot (t_r + t_f)] \quad (34)$$

$V_{S(max)}$ is the maximum voltage stress of S_1, $I_{S(max)}$ is the maximum current stress of S_1, f_S is switching frequency, t_r is the rise-time of the switch and t_f is the fall-time of the switch.

The conduction power loss in each component is shown in Table 1.

Table 1. Power per component.

Component	Power Loss
L_1	$P_{L1} = I^2_{L1(rms)} \cdot R_{L1}$
L_2	$P_{L2} = I^2_{L2(rms)} \cdot R_{L2}$
D_1	$P_{D1} = I^2_{D1(rms)} \cdot R_{D1}$
D_2	$P_{D2} = I^2_{D2(rms)} \cdot R_{D2}$
D_3	$P_{D3} = I^2_{D3(rms)} \cdot R_{D3}$
S	$P_S = I^2_{D1(rms)} \cdot R_{DS(on)}$
C_1	$P_{C1} = I^2_{C1(rms)} \cdot R_{C1}$
C_2	$P_{C2} = I^2_{C2(rms)} \cdot R_{C2}$
D_4	$P_{D4} = I^2_{D4(rms)} \cdot R_{D4}$
D_5	$P_{D5} = I^2_{D5(rms)} \cdot R_{D5}$
L_O	$P_{LO} = I^2_{Lo(rms)} \cdot R_{LO}$
C_O	$P_{CO} = I^2_{CO(rms)} \cdot R_{CO}$

The rms values of the currents through the above listed devices are obtained below:

$$I_{L1(rms)} = \sqrt{I^2_{L1(avg)} + \left(\frac{\Delta I_{L1}}{2\sqrt{3}}\right)^2} = \frac{(1+D)^2}{2(1-D)} I_O \quad (35)$$

Similarly, $I_{L2(rms)}$ and $I_{LO(rms)}$ are given by:

$$I_{L2(rms)} = \frac{(1+D)^2}{2(1-D)} I_O \quad (36)$$

$$I_{Lo(rms)} = I_O \quad (37)$$

The rms currents of other components are:

$$I_{S(rms)} = \frac{(1+D)^2}{2(1-D)} I_O \sqrt{D} \quad (38)$$

$$I_{D1(rms)} = \frac{(1+D)^2}{2(1-D)} I_O \sqrt{D} \quad (39)$$

$$I_{D2(rms)} = \frac{(1+D)^2}{2(1-D)} I_O \sqrt{D} \quad (40)$$

$$I_{D3(rms)} = \frac{(1+D)^2}{2\sqrt{1-D}} I_O \quad (41)$$

$$I_{D4(rms)} = \frac{(1+D)^2}{2\sqrt{1-D}} I_O \quad (42)$$

$$I_{D5(rms)} = \frac{(1+D)^2}{2\sqrt{1-D}} I_O \tag{43}$$

$$I_{C1(rms)} = \left(\sqrt{\frac{D}{1-D}}\right) I_O \tag{44}$$

$$I_{C2(rms)} = \left(\sqrt{\frac{D}{1-D}}\right) I_O \tag{45}$$

$$I_{Co(rms)} = \frac{DV_S(1+D)}{\sqrt{12} * L_O * f_s} \tag{46}$$

4. Simulation Results

MATLAB Simulink 2021b was used to validate the theoretical analysis of the proposed HSLSC topology using the specific parameters outlined in Table 2.

Table 2. List of components and their values for simulation and hardware prototype.

Parameter	Value
Input Voltage (V_s)	14.5 V
Output Voltage (V_o)	77.4 V
Switched Capacitors ($C_1 = C_2$)	10 µF
Switched Inductors ($L_1 = L_2$)	130 µH
Output Inductor (L_o)	400 µH
Output Capacitor (C_o)	5 µF
Load Resistance (R_o)	190 Ω
Duty Cycle (D)	55%
Output Power	31.5 W
Switching Frequency (f_s)	12 kHz

Theoretical results are obtained using the parameters from Table 1 in Equations (8), (9) and (15)–(18).

From Equation (8) $V_{C1} = V_{C2} = Vc = 49.9$ volts
From Equation (9) $Vo = 77.4$ volts
From Equation (15) $V_{SW} = -49.9$ volts
From Equation (16) $V_{D1} = V_{D2} = -17.7$ volts
From Equation (17) $V_{D3} = -14.5$ volts
From Equation (18) $V_{D4} = V_{D5} = -49.9$ volts

Figure 8 shows the PWM signal with a 55% duty cycle applied to the gate of the main transistor switch. Simulation waveforms of input and output voltages are shown in Figure 9. It is clear from the waveforms in Figure 9 that the proposed converter produces an output voltage of approximately 77 volts from an input of 14.5 volts at a duty cycle of 55% and verifies Equations (9) and (10) with a gain of 5.3 at a 55% duty cycle.

Figure 10 shows the voltage stress across the MOSFET which is around 47 volts, close to the theoretical value of 49.9 volts. Simulation waveforms of capacitor C_1 and C_2 voltages are shown in Figure 11, which are 47 volts. Figures 12 and 13 show simulation waveforms of diodes D_1–D_5. The voltage stress across diodes D_1 and D_2 is around 17 volts, for D_3 it is 13 volts, and for D_4 and D_5 it is 45 volts.

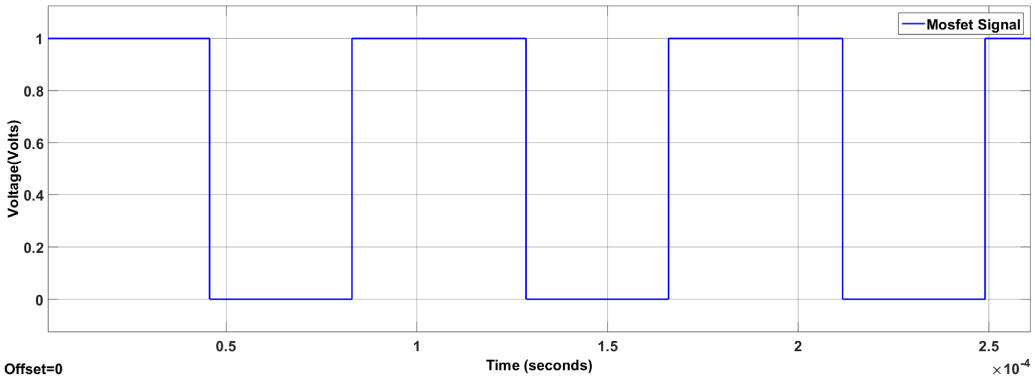

Figure 8. Pulse width modulated signal with 55% duty cycle.

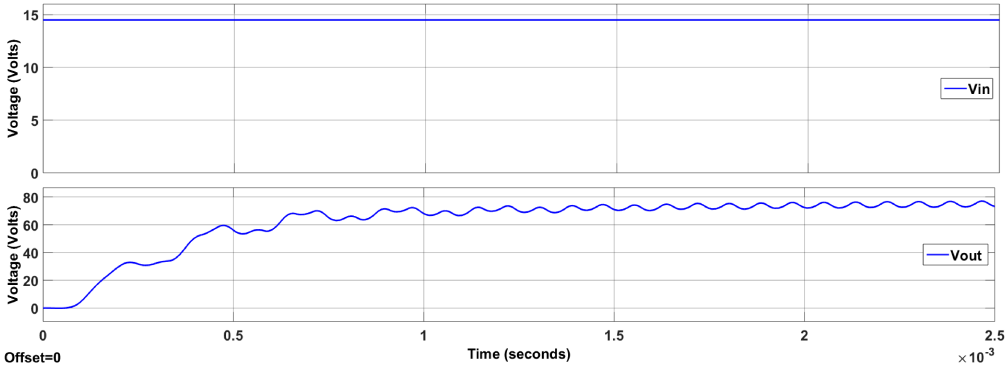

Figure 9. Simulation waveforms of input and output voltages.

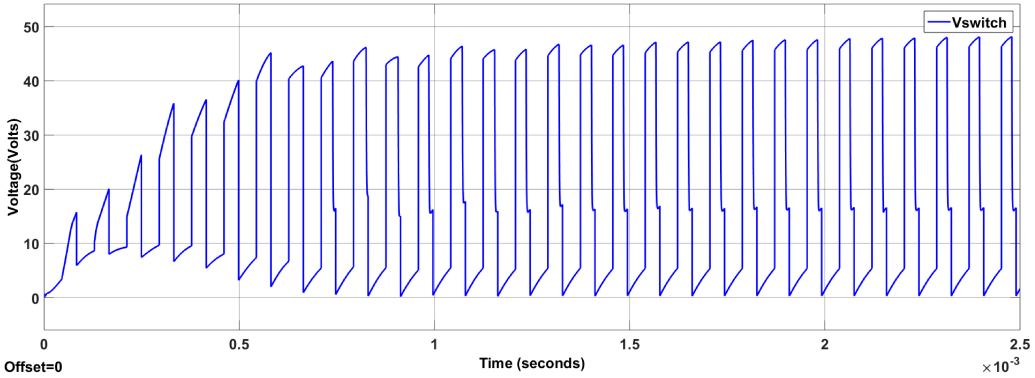

Figure 10. Voltage stress on the switch.

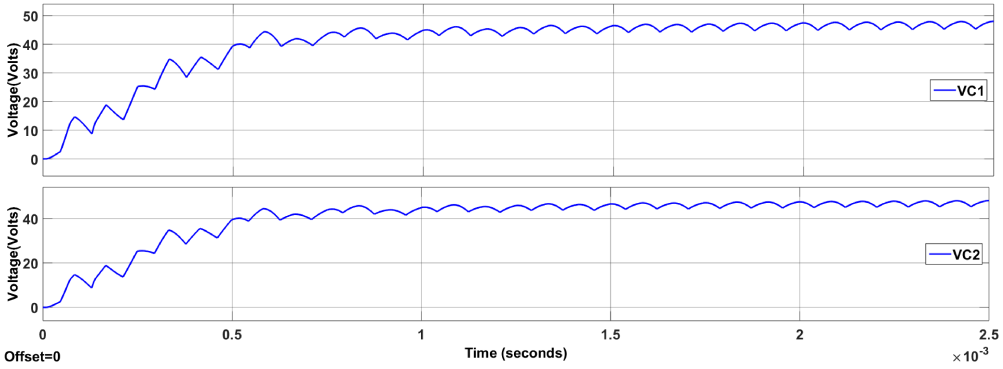

Figure 11. Voltage across each capacitor (C_1 and C_2).

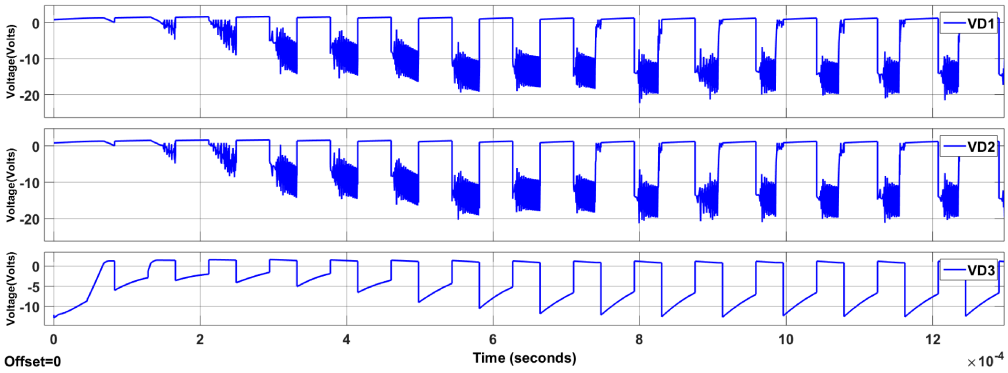

Figure 12. Voltage stress across diodes D_1, D_2 and D_3.

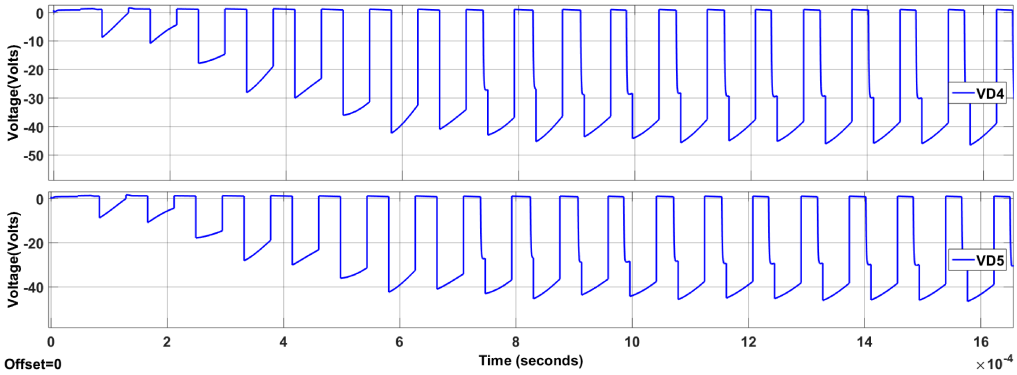

Figure 13. Voltage stress across diodes D_4 and D_5.

5. Hardware Implementation and Experimental Results

To practically validate the simulation models, we built and tested a 31.5-watt hardware prototype in the laboratory. The actual experimental setup is captured in the photograph in Figure 14.

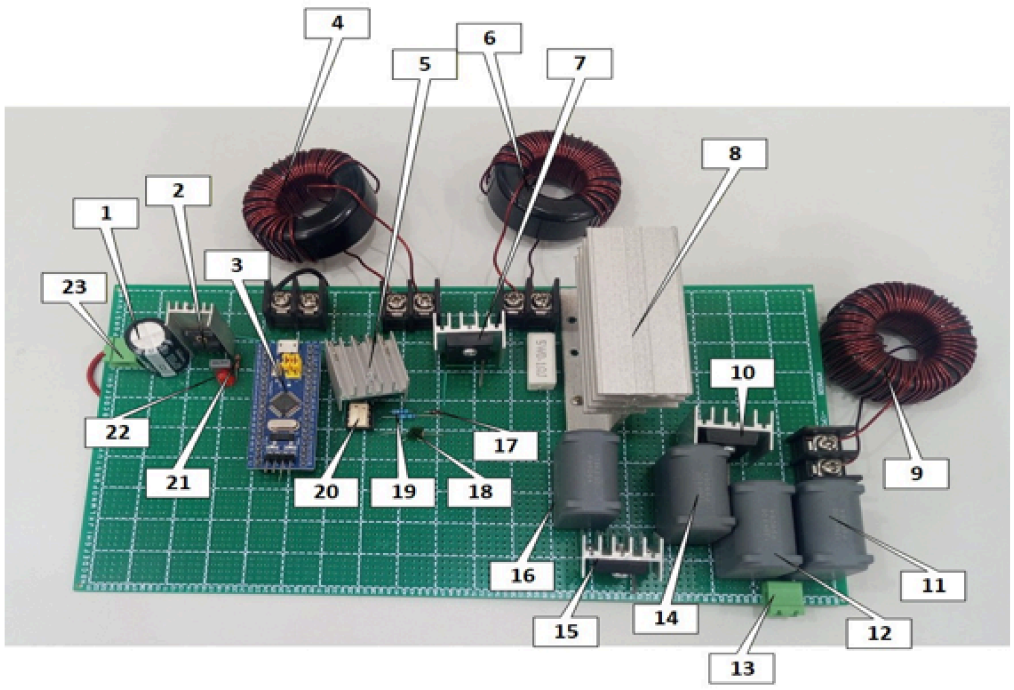

Figure 14. Photograph of hardware prototype of the proposed converter.

In Figure 14, 1 is the DC voltage source of 14.5 volts with a noise filtration capacitor; 2 is the voltage regulator 7805 IC; 3 is the STM32F103C8T6 microcontroller; 4 is switched inductor L_1; 5 is diodes D_1 and D_3 below the heat sink; 6 is switched inductor L_2; 7 is diode D_2 with a heat sink; 8 is the MOSFET with a heat sink; 9 is output inductor L_o; 10 is diode D_4 with a heat sink; 11 and 12 are output capacitor C_0, each 12 micro farad connected in series to get a 6 microfarad combination; 13 is the output terminal; 14 is switched capacitor C_1; 15 is diode D_5 with a heat sink; 16 is switched capacitor C_2; 17, 18 and 19 are the gate drive circuit; 20 is the optocoupler (TLP250H), 21 is the LED for indication, 22 is 100 nF filter capacitor and 23 is input connector. In Figure 14, the STM32F103C8T6 microcontroller is used for PWM generation and fed to the MOSFET through the drive circuit.

The same parameters listed in Table 2 are used for experimentation. Experimental waveforms verify that the proposed converter is able to produce a 77-volt output from a 14.5-volt DC input at a duty cycle of 55%. Figure 15 shows the PWM gate signal applied to the MOSFET with a 55% duty cycle and Figures 16 and 17 show the input and output DC voltages respectively. Figures 18 and 19 show the switched capacitor C_1 and C_2 voltages, which are both equal to 49 volts. Figure 20 shows the voltage stress across the MOSFET, which is 50 volts and is reduced from the output voltage of 77 volts. The voltage stresses of diodes D_1, D_2, D_3, D_4 and D_5 are shown in Figures 21–25 respectively. All the experimental results are in close agreement with simulation results.

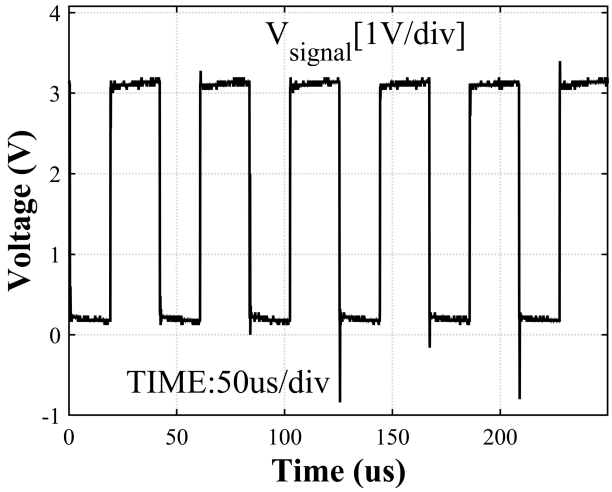

Figure 15. STM32F103C8T6 signal with 55% duty cycle.

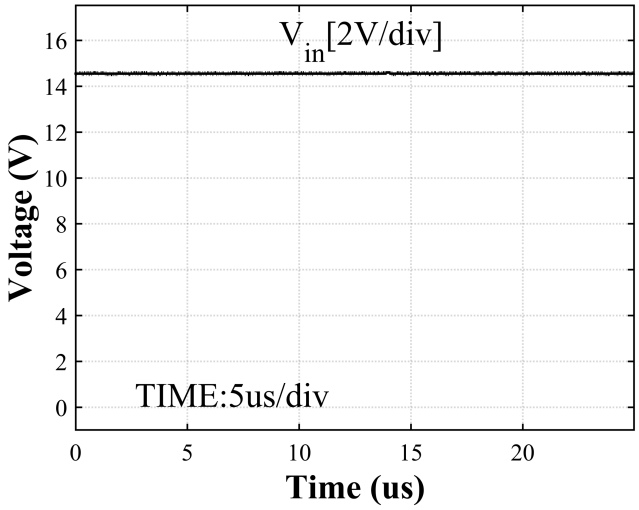

Figure 16. Input DC voltage of 14.5 volts.

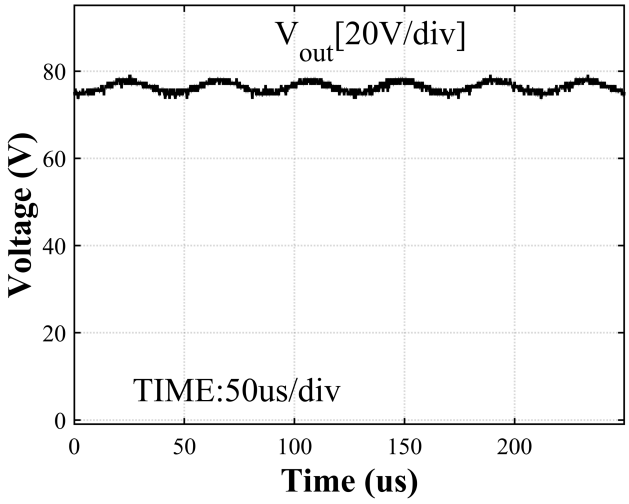

Figure 17. Output DC voltage of approximately 77 volts.

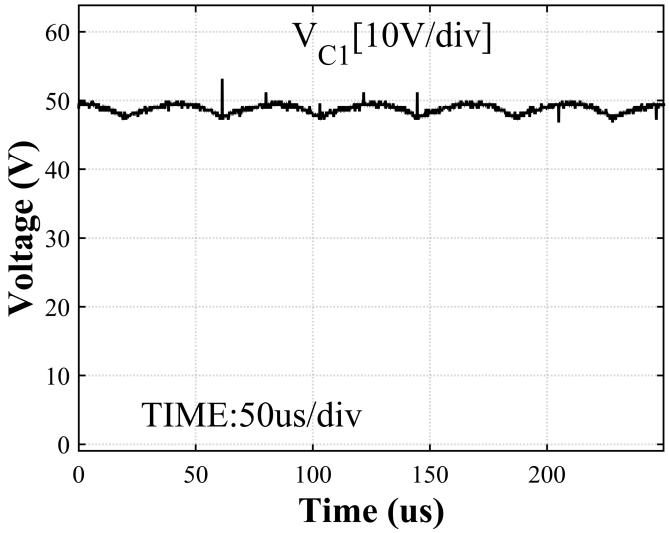

Figure 18. Voltage across capacitor C_1 is approximately 47 V.

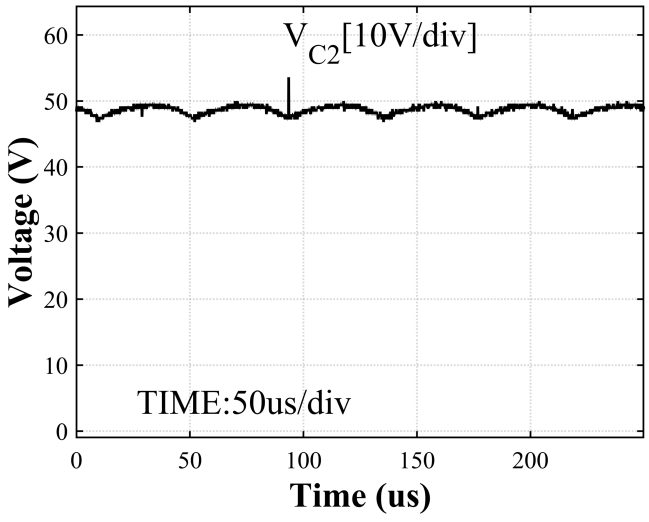

Figure 19. Voltage across capacitor C_2 is approximately 47 V.

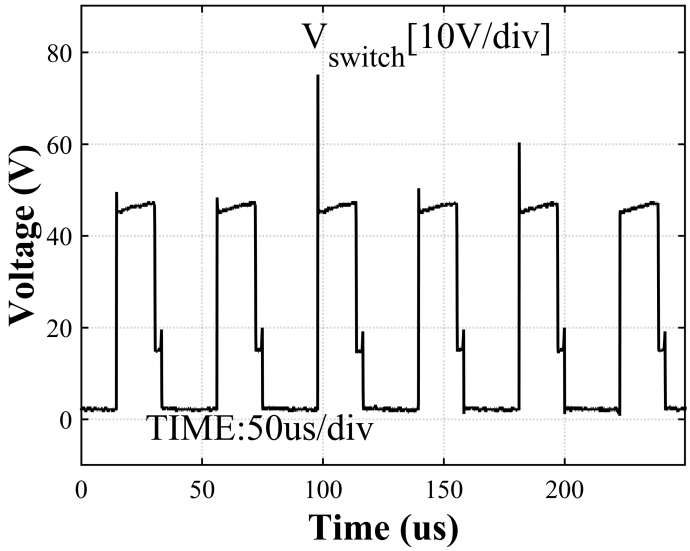

Figure 20. Voltage stress across the main switch is approximately 47 V.

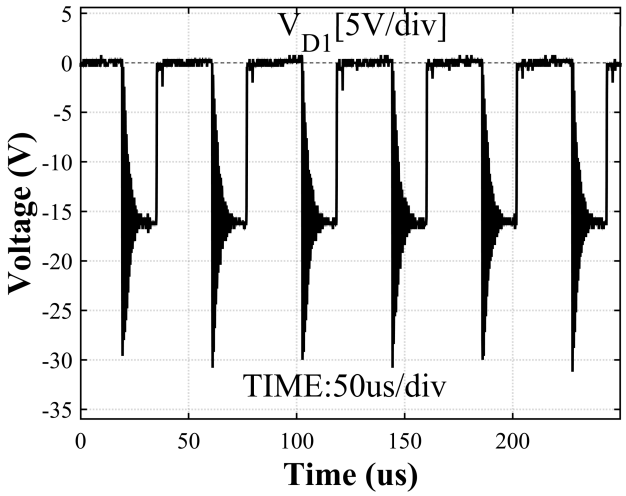

Figure 21. Voltage stress on diode D_1 is approximately 16 V.

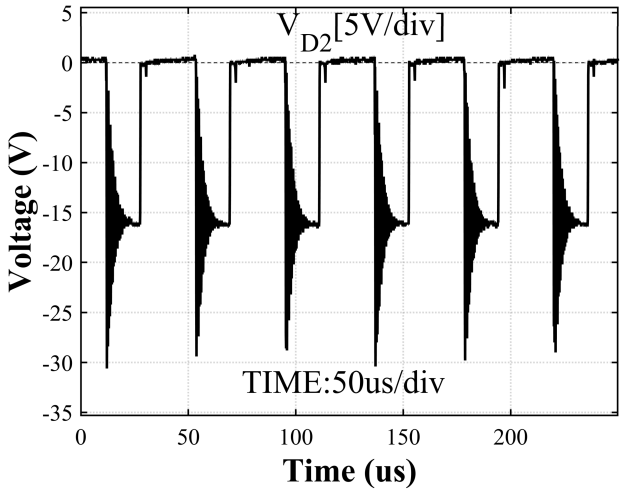

Figure 22. Voltage stress on diode D_2 is approximately 16 V.

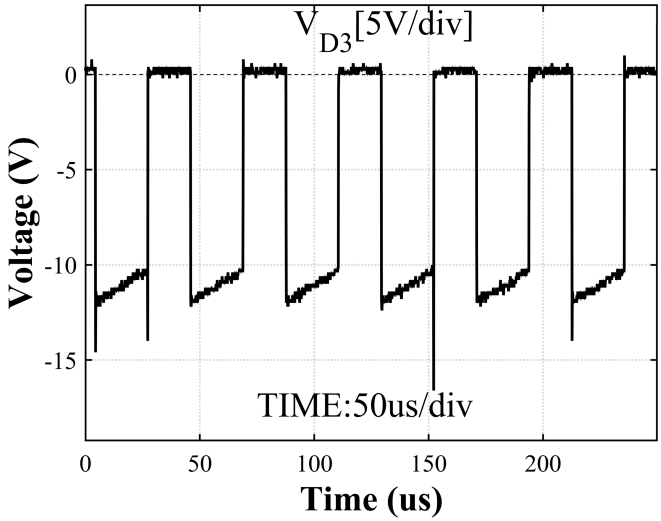

Figure 23. Voltage stress on diode D_3 is approximately 13 V.

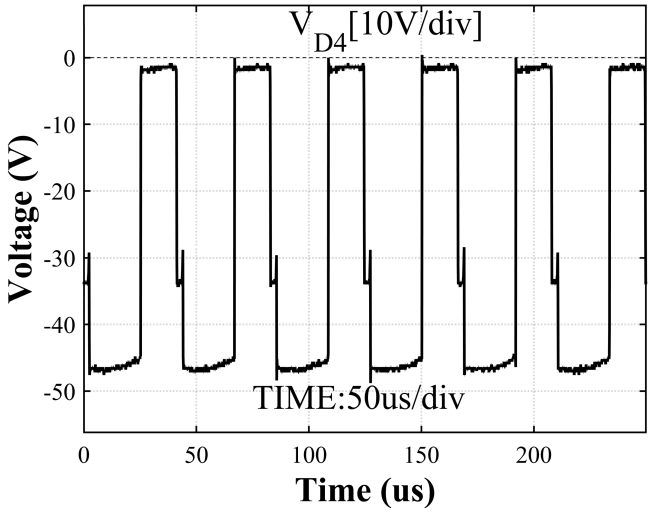

Figure 24. Voltage stress on diode D_4 is approximately 47 V.

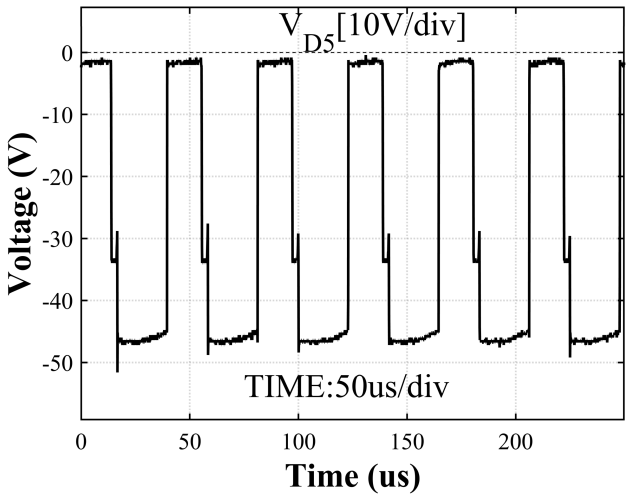

Figure 25. Voltage stress on diode D_5 is approximately 47 V.

6. Performance Comparison

A comprehensive comparison of the proposed converter with recently reported high-gain DC-DC converter topologies is presented in Table 3 below. The performance comparison shows the advantages of the proposed converter in terms of voltage gain and voltage stress reduction on the main MOSFET switch and the use of a single MOSFET to achieve a high gain.

Table 3. Performance comparison of the proposed and traditional high-gain DC-DC converters.

Topology	Voltage Gain	Voltage Stress on Controlled Switch	Voltage Stress on Output Diode	Number of Controlled Switches	Total Number of Components
Single-Switch Quadratic Boost Converter [22]	$\frac{1}{(1-D)^2}$	Vo	$-Vo$	1	8
Switched-Capacitor Converter [23]	$\frac{2-D}{D}$	$\frac{Vo}{2-D}$	$-\frac{Vo}{2-D}$	3	7
Series Boost Converter [24]	$\frac{2}{1-D}$	$\frac{Vo}{2}$	$-\frac{Vo}{2}$	2	10
Conventional Boost Converter	$\frac{1}{1-D}$	Vo	−Vo	1	4
Proposed HSLSC Converter	$\frac{(1+D)^2}{(1-D)}$	$\frac{Vo}{1+D}$	$-\frac{Vo}{1+D}$	1	12

The brick form factor of the proposed converter is 13 cm × 25 cm = 325 cm^2.

Figure 26a compares the ideal voltage gain of the proposed HSLSC converter with conventional boost, series boost, single-switch quadratic and switched-capacitor boost converter topologies. For duty cycles exceeding 0.5, the HSLSC topology exhibits substantially higher gain, making it preferable for operation in the range 0.5 < D < 0.9. Figure 26 shows a comparison of the five topologies under ideal conditions across different duty cycles. This figure shows that these converters' voltage gain conversion ratios have very little variation at low duty cycle values. However, there are noticeable differences between these topologies for duty cycle values greater than 0.5. In particular, when the duty cycle exceeds 0.5, the voltage gain conversion ratio of the HSLSC DC-DC converter is significantly larger than that of the other three topologies. Throughout the whole duty cycle range, the traditional boost topology has the lowest voltage gain; even at large duty ratios, it only slightly increases. The switched capacitor shows the highest gain but at very low duty cycles, which is not practical; while both series and quadratic variants show better gain characteristics than the traditional design, their step-up capability is still constrained. The suggested HSLSCBC topology, on the other hand, achieves significantly greater voltage conversion ratios, especially in the duty cycle region of 0.4 to 0.6, which is an ideal range for the duty cycle. Figure 26b also compares the transistor voltage stress for all topologies, showing that for ideal duty cycle operation of 0.4 to 0.6, the voltage stress in the proposed converter main transistor switch is lowest.

From experimental waveforms, it is clear that the proposed converter is superior in performance, producing 77 volts from a 14.5-volt input at a 55% duty cycle, whereas the Conventional Boost Converter produces only 32 volts from 14.5 volts at a 55% duty cycle. To produce 77 volts from 14.5 volts, the traditional boost converter will need to operate at an 81% duty cycle, which is very high. Furthermore, the voltage stress on the main transistor switch and diode in the traditional boost converter and various other topologies is equal to the output voltage, whereas in the proposed converter the MOSFET voltage stress is reduced to intermediate switched-capacitor voltage, which is 65% of the output voltage. Experimental waveforms also show that voltage stress across diodes D_1 and D_2 is

around 17 volts, across D_3 it is 13 volts, and across D_4 and D_5 it is 45 volts. These values are also reduced considerably, allowing the use of low-voltage-rated diodes.

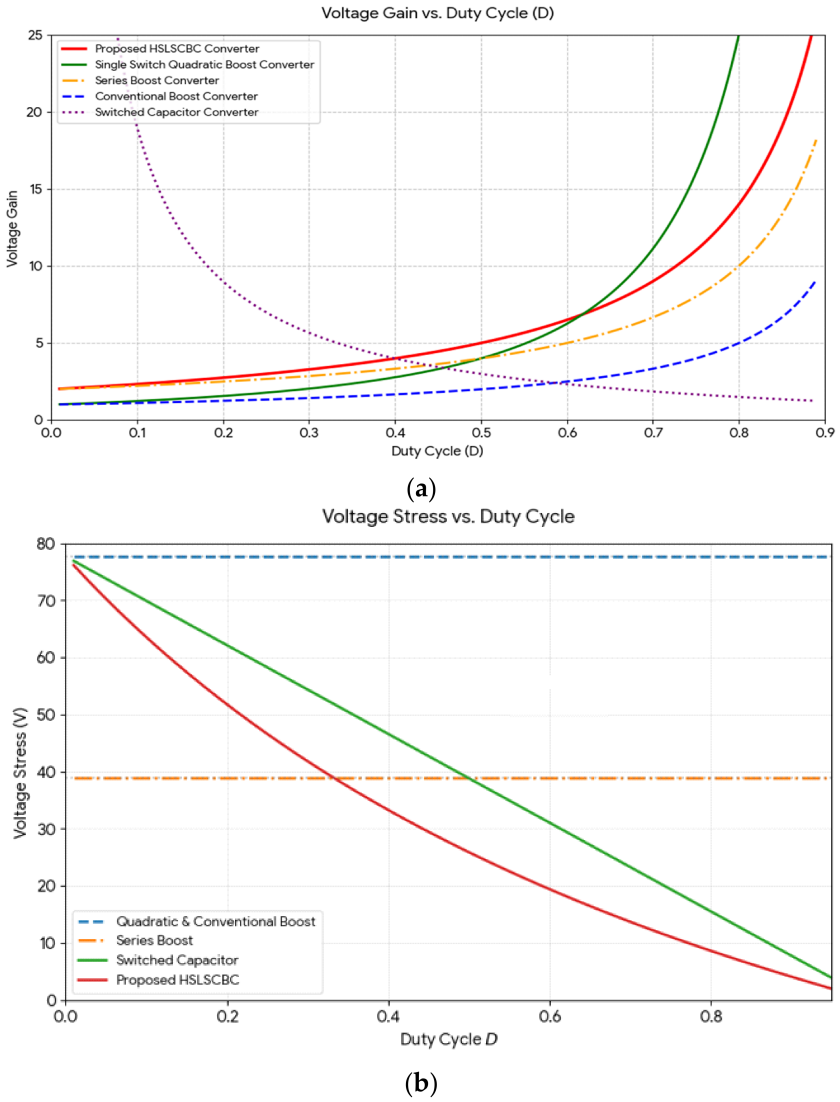

Figure 26. (**a**) Voltage conversion ratio versus duty cycle for proposed and conventional topologies; (**b**) transistor voltage stress versus duty cycle for proposed and conventional topologies.

7. Conclusions

This paper successfully demonstrated a novel HSLSC non-isolated DC-DC converter that achieves high voltage gain with reduced active switch stress, without requiring transformers, coupled inductors, or extreme duty cycles. The converter steps up a 14.5 V PV input to approximately 77 V (gain of 5.3), making it suitable for high-step-up DC-DC conversion systems of photovoltaic and other renewable-energy systems. The traditional boost converter and various other traditional DC-DC converter topologies are affected by operating on extreme duty cycle values, and by the reverse-recovery problem of boosting 14.5-volt input voltage to 77 volts. It is clear from both the simulation and experimental outcomes that the presented converter can easily achieve this voltage conversion with the appropriate value of D, and the voltage stress across the switches is also reduced. The HSLSC topology offers continuous input and output currents, low voltage stress and design simplicity. The proposed HSLC converter is well analyzed mathematically, tested through simulation and experimentation for performance validation.

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References

1. Krishna, B.; Karthikeyan, V. Ultra-voltage gain step-up DC-DC converter for renewable energy micro-source applications. *IEEE Trans. Energy Convers.* **2021**, *37*, 947–957. [CrossRef]
2. Shanthi, T.; Prabha, S.U.; Sundaramoorthy, K. Non-isolated n-stage high step-up DC-DC converter for low voltage DC source integration. *IEEE Trans. Energy Convers.* **2021**, *36*, 1625–1634. [CrossRef]
3. Sun, X.; Wang, G.; Xu, L.; Yuan, H.; Yousefi, N. Optimal performance of a combined heat-power system with a proton exchange membrane fuel cell using a developed marine predators algorithm. *J. Clean. Prod.* **2021**, *284*, 124776. [CrossRef]
4. Kang, W.; Qin, G.; Cheng, J.; Yan, H.; Katib, I.; Cao, J. Probabilistic event-triggered protocol for switched power systems under multi-strategy deception attack. *J. Frankl. Inst.* **2023**, *360*, 11623–11640. [CrossRef]
5. Sadaf, S.; Iqbal, A.; Meraj, M.; Maroti, P.K.; Samiullah, M.; Khan, I. A new type of boost converter with dual duty and high gain for dc microgrid applications. In *2022 Second International Conference on Power, Control and Computing Technologies (ICPC2T)*; IEEE: New York, NY, USA, 2022.
6. Zhang, G.; Wu, Z.; Yu, S.; Trinh, H.; Zhang, Y. Four novel embedded Z-source DC–DC converters. *IEEE Trans. Power Electron.* **2021**, *37*, 607–616. [CrossRef]
7. Jalilzadeh, T.; Rostami, N.; Babaei, E.; Maalandish, M. Ultra-step-up dc–dc converter with low-voltage stress on devices. *IET Power Electron.* **2019**, *12*, 345–357. [CrossRef]
8. Zhu, M.U.; Luo, F.L. Series SEPIC implementing voltage-lift technique for DC–DC power conversion. *IET Power Electron.* **2008**, *1*, 109–121. [CrossRef] [PubMed]
9. Lei, H.; Hao, R.; You, X.; Li, F. Nonisolated high step-up soft-switching DC-DC converter integrating Dickson switched-capacitor techniques. In *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*; IEEE: New York, NY, USA, 2018.
10. Chub, A.; Vinnikov, D.; Blaabjerg, F.; Peng, F.Z. A review of galvanically isolated impedance-source DC–DC converters. *IEEE Trans. Power Electron.* **2015**, *31*, 2808–2828. [CrossRef]
11. Pan, X.; Li, H.; Liu, Y.; Zhao, T.; Ju, C.; Rathore, A.K. An overview and comprehensive comparative evaluation of current-fed-isolated-bidirectional DC/DC converter. *IEEE Trans. Power Electron.* **2019**, *35*, 2737–2763. [CrossRef]
12. Yang, L.-S.; Liang, T.-J.; Chen, J.-F. Transformerless DC–DC converters with high step-up voltage gain. *IEEE Trans. Ind. Electron.* **2009**, *56*, 3144–3152. [CrossRef]
13. Ammar, A.M.; Spliid, F.M.; Nour, Y.; Knott, A. A 1-MHz resonant LED driver with charge-pump-based power factor correction. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 5838–5850. [CrossRef]
14. Mirzaee, A.; Moghani, J.S. Coupled inductor-based high voltage gain DC–DC converter for renewable energy applications. *IEEE Trans. Power Electron.* **2019**, *35*, 7045–7057. [CrossRef]
15. Rajabi, A.; Rajaei, A.; Tehrani, V.M.; Dehghanian, P.; Guerrero, J.M.; Khan, B. A non-isolated high step-up DC-DC converter using voltage lift technique: Analysis, design, and implementation. *IEEE Access* **2022**, *10*, 6338–6347. [CrossRef]
16. Jalilzadeh, T.; Rostami, N.; Babaei, E.; Maalandish, M. Nonisolated topology for high step-up DC–DC converters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *11*, 1154–1168. [CrossRef]
17. Javaheri Fard, H.; Sadeghzadeh, S.M. A three-winding coupled-inductor nonisolated high step-up interleaved DC–DC converter with low switch stress. *Electr. Eng.* **2022**, *104*, 4335–4346. [CrossRef]
18. Tang, Y.; Tong, H.; Afzal, R.; Guo, Y. High step-up ZVT converter based on active switched coupled inductors. *IEEE Access* **2020**, *13*, 15178–15187. [CrossRef]
19. Samiullah, M.; Iqbal, A.; Ashraf, I.; Maroti, P.K. Voltage lift switched inductor double leg converter with extended duty ratio for DC microgrid application. *IEEE Access* **2021**, *9*, 85310–85325. [CrossRef]
20. Mohammed, M.R.; Al-Sumaiti, A.S.; Beig, A.R.; Al Hosani, K.; Wang, C. A common grounded voltage quadrupler ASL/PSC hybrid converter with reduced voltage stress. *IEEE Trans. Ind. Electron.* **2023**, *71*, 4773–4784. [CrossRef]

21. Tang, Y.; Wang, T.; He, Y. A switched-capacitor-based active-network converter with high voltage gain. *IEEE Trans. Power Electron.* **2013**, *29*, 2959–2968. [CrossRef]
22. Dizangian, N.; Jovanovic, S.; Poure, P. Modeling and Experimental Verification of a Single-Switch Quadratic Boost DC–DC Converter with High Voltage Gain for Energy Harvesting. *Energies* **2025**, *18*, 5447. [CrossRef]
23. Pellitteri, F.; Di Dio, V.; Puccio, C.; Miceli, R. A Model of DC-DC Converter with Switched-Capacitor Structure for Electric Vehicle Applications. *Energies* **2022**, *15*, 1224. [CrossRef]
24. Wang, P.; Zhou, L.; Zhang, Y.; Li, J.; Sumner, M. Input-parallel output-series DC-DC boost converter with a wide input voltage range, for fuel cell vehicles. *IEEE Trans. Veh. Technol.* **2017**, *66*, 7771–7781. [CrossRef]

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