

Article

High-Performance Multilevel Inverter Integrated DVR for Comprehensive Power Quality Improvement in Power Systems

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Abstract

This paper proposes a dynamic voltage restorer (DVR) based on a new three-phase multilevel inverter (MLI). An integral component of DVRs is the power electronic converter. At medium-to-high voltage levels, MLIs are the ideal converters for DVR applications because lower voltage-rated switches are used to generate high voltages, thus minimizing power losses. The proposed three-phase MLI generates 15 levels of load voltage per phase, using a reduced component count: eight lower-rated semiconductor power switches, four primary DC voltage sources, two auxiliary DC sources, and eight driver circuits per phase. Additionally, each phase features a low-frequency transformer with voltage-boosting and galvanic isolation capabilities. The switching sequence of the proposed MLI is simpler to execute using fundamental frequency control; this methodology provides reduced switching stress and reduced switching losses as merits. Structurally, the proposed MLI is less complex and thus scalable. The proposed DVR, based on three-phase MLI, efficiently offsets power quality problems such as voltage swell, voltage sags, and harmonics for balanced and unbalanced loads. The operational performance of the proposed DVR-MLI is verified by a simulation, using PSCAD software and an experimental prototype.

Keywords: dynamic voltage restorer; voltage sag and swell; multilevel inverter; three-phase inverter; power quality



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1. Introduction

Voltage disturbances such as unbalances, voltage dips, harmonics, flickers, and voltage swell are the commonly faced power quality (PQ) drawbacks in distribution lines [1]. When these voltage disturbances are not satisfactorily resolved, they cause the breakdown of sensitive and critical loads [2]; also, they interfere and cause interruption of production lines, culminating in the loss of essential information and finances [3]. The application of sensitive loads and devices liable for the pollution of power lines has increased in recent times, hence the urgent need for the protection of power systems. Considering IEEE 1159 and 1346 standards, if the nominal voltage of a distribution line decreases from 10% to 90% for a duration lasting between half of a cycle and 60 s, then this phenomenon is described as a voltage dip [4,5]. Some of the causes of voltage dip are short circuit faults, the starting

of induction motors with high ratings, and the immediate connection of large loads [6]. The voltage swell phenomenon is described as an increase in the nominal voltage of a power line from 110% to 180% for a duration lasting no more than the frequency of the utility, from half a cycle to 60 s. Some causes of voltage swell are de-energizing large capacitor banks, switching off large capacitors, and the disconnection of large inductive loads. The consequence of voltage swell is the malfunction of industrial devices, due to overheating and tripping of AC motors, relays, and surge arresters [7,8]. Sensitive loads dislike power lines that are heavily contaminated by harmonics because the control of these devices depends largely on the zero crossing and peak value of the input voltage. Different solutions have been proposed to mitigate the consequences of power quality issues on sensitive loads over the years. Among the many presented solutions, custom power devices (CPD) are the most preferred solutions because of their essential attributes, such as flexibility, fast response, and effectiveness.

CPDs are new technologies designed to mitigate power quality issues. They are developed upon the concept of power electronics; therefore, they are commonly referred to as power electronic-based compensators. Conventionally, CPDs are categorized into three static distinct groups: (a) series compensator, (b) shunt compensator, and (c) series-shunt compensator. Examples of each of the three static compensators are DVR, DATCOM, and UPQC, respectively. The series compensators comprising SSC (static series compensators), DVC (dynamic voltage compensators), and DVR (dynamic voltage restorers) are regarded as the ideal cost-effective method of damping power quality issues. These compensator families are alike in operating principles and the structure of power circuits but differ in control techniques and design purposes. Examples of other power quality mitigating devices are flywheels, UPS (uninterruptible power supply), tap-changing transformers, and STATCOM (static compensators) [9]. DVR's functionality is maintaining load voltage at the desired characteristic by injecting voltage with a specific magnitude, phase, and frequency into the distribution line. DVRs are series-tied to the distribution line and have the potential to absorb or generate reactive and real powers [10]. Figure 1 shows the structure of a typical DVR, which consists of the grid, an injection transformer at the point of common coupling (PCC), a voltage source converter, and sensitive loads. The first practical operating DVR is situated in the USA, North Carolina, in a rug-producing company [11]. DVRs are classified into two categories, considering ESS. These are ESS-based DVRs and non-ESS-based DVRs [12]. Previously, EES-based DVRs were unable to compensate for huge and longer periods of voltage interruptions. However, with increased capacity, reduced cost, and increased application of renewable energy sources, ESS-based DVRs are the preferred option for longer and deeper voltage compensations.

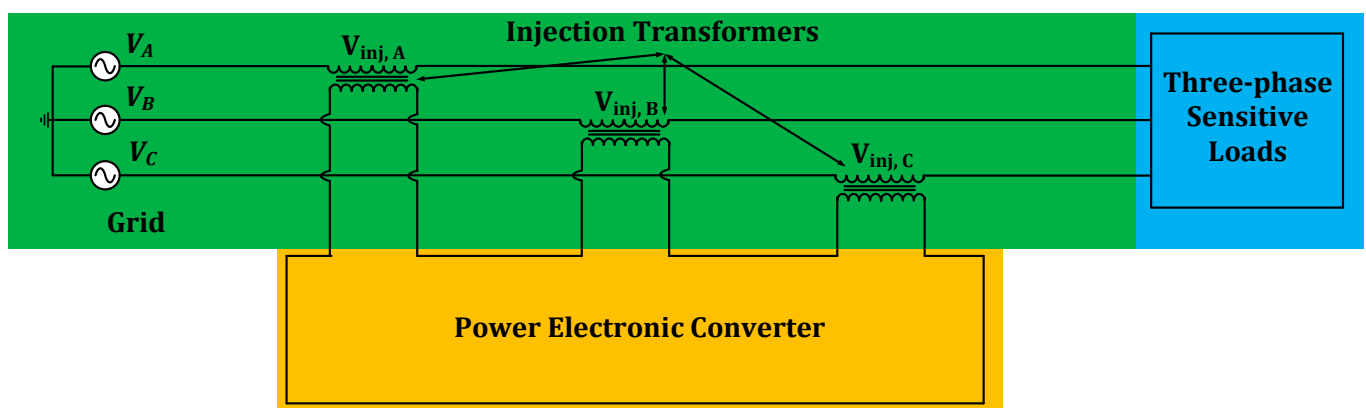


Figure 1. A typical DVR structure.

Non-ESS-based DVRs possess the following merits: reduced system size, minimum system cost because of the absence of ESS, single-stage power conversion, and longer and deeper voltage compensation capabilities. Also, DVRs are classified according to the type of power conversion, i.e., ac-ac DVR, ac-dc-ac DVR, and dc-ac DVR. Each of these topologies of DVR has advantages and disadvantages. The ac-ac topology does not require ESS and is a single-stage power converter, while the ac-dc-ac topology requires bulky capacitors and is a multi-stage power converter. Finally, DVRs are further classified into single-phase and three-phase systems [13–15].

The most frequently used converter topologies for both single-phase and three-phase DVRs are full and half H-bridges, matrix converters, multilevel inverters, Z-source inverters, 2-level six-switch inverters, four-leg inverters, and 3 H-bridge inverters [16–19]. Application of a multilevel inverter in DVRs is the optimal choice when juxtaposed with other inverter topologies: mostly the conventional 2-level inverter, which requires a higher switching frequency, thus increasing switching losses, a higher THD (total harmonic content), and the burden of controller computation [20]. However, a multilevel inverter provides the following advantages: high output voltage using smaller input voltage, high-quality output waveforms, lower THD, reduced switching losses, and better electromagnetic adaptability.

A three-phase seven-level inverter-based dynamic voltage restorer (DVR) is suggested in this paper. The proposed three-phase MLI is composed of a smaller number of circuit components (power switches, DC sources, and driver circuit) but generates high levels of output voltage. This is evident from the comparative perusal of the proposed topology and other published multilevel inverter topologies with similar characteristics. The proposed DVR, based on the new three-phase MLI, is operated under various voltage sag and swell conditions and unbalanced voltage conditions. Experimental and simulation outcomes are presented to affirm the operations of the proposed DVR, based on three-phase MLI.

2. Proposed Three-Phase MLI

The proposed three-phase MLI is an improved architecture of the conventional H-bridge inverter. Three DC voltages and four semiconductor-based switches are incorporated into the design of the classical single-phase H-bridge inverter. Therefore, the resulting new single-phase topology has one voltage source on each of the upper, lower, left, and right sides, connected in series. Each of these sides has two switches. One of the switches on the upper and lower sides is bidirectional and derived from the common emitter configuration. Using the new methodology called the “extension technique” [21], which reduces the DC source count, the proposed three-phase MLI is illustrated in Figure 2. Considering Figure 2, the component count for the proposed three-phase MLI is ten DC sources and twenty-four power switches. The proposed three-phase MLI can be used with or without transformers. For galvanic isolation purposes, such as in DVR applications, three single-phase transformers are included in the circuit of the proposed topology. Individual phases of the proposed inverter generate 15 levels of load voltage. Two DC voltage sources per phase on the right and left sides have asymmetric characteristics. Using a DC source with symmetric characteristics will reduce the levels of load voltage. The upper and lower DC sources are equal in magnitude but not equivalent to the other two DC sources. Therefore, the proposed topology has asymmetric characteristics from a voltage point of view. This characteristic enables the generation of higher load levels juxtaposed with symmetric characteristics. If an equal voltage magnitude (symmetric) is chosen at the input of the inverter, fewer step load voltages will be produced. Comparatively asymmetric and symmetric features of the proposed inverter generate 15 and 9 voltage levels, accordingly. Connecting the DC sources in any sequence other than series will reduce the levels of load voltage produced. The switching sequences of the proposed topology are illustrated in

Table 1, only showing active switches for each mode of operation. All switches in each phase contain letters A, B, and C in their subscript to show the phase they represent; thus, A, B, and C connote phase A, phase B, and phase C, accordingly. Figure 3 shows the conducting switches and current paths for some selected modes of operation.

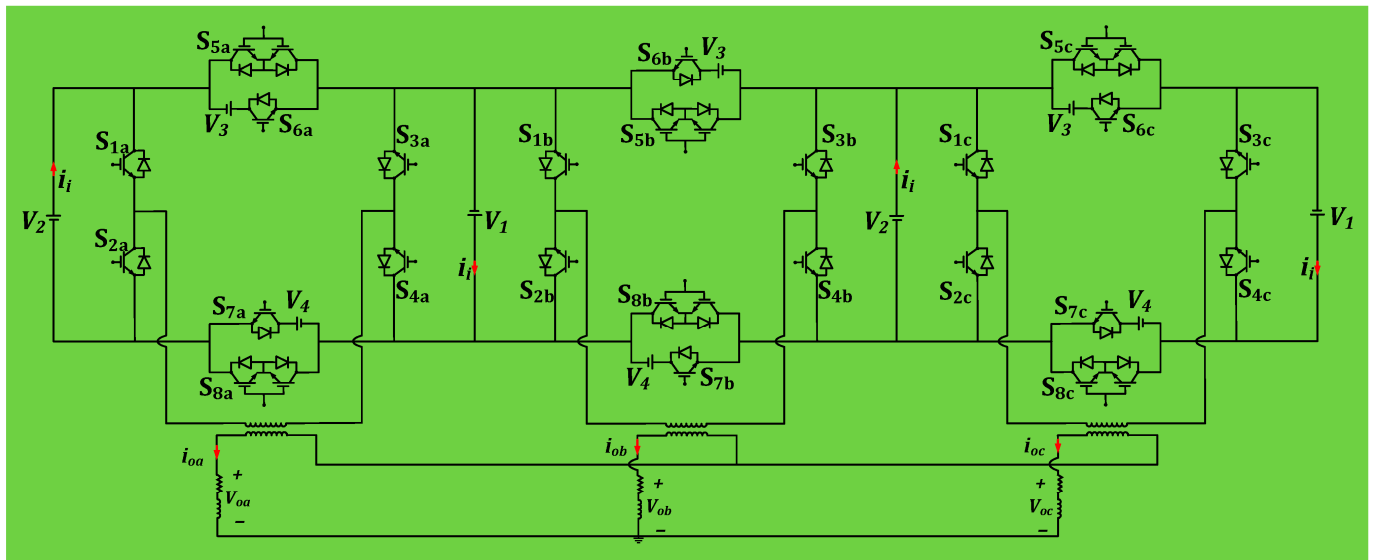
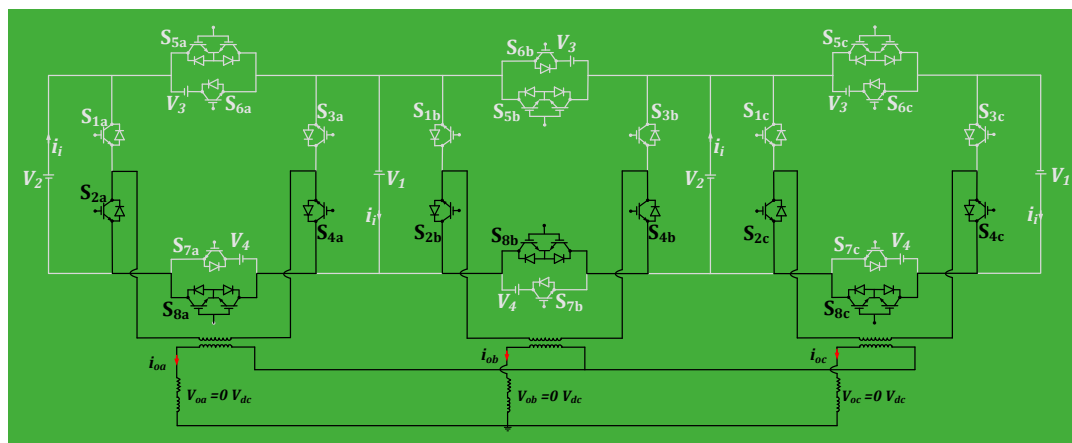
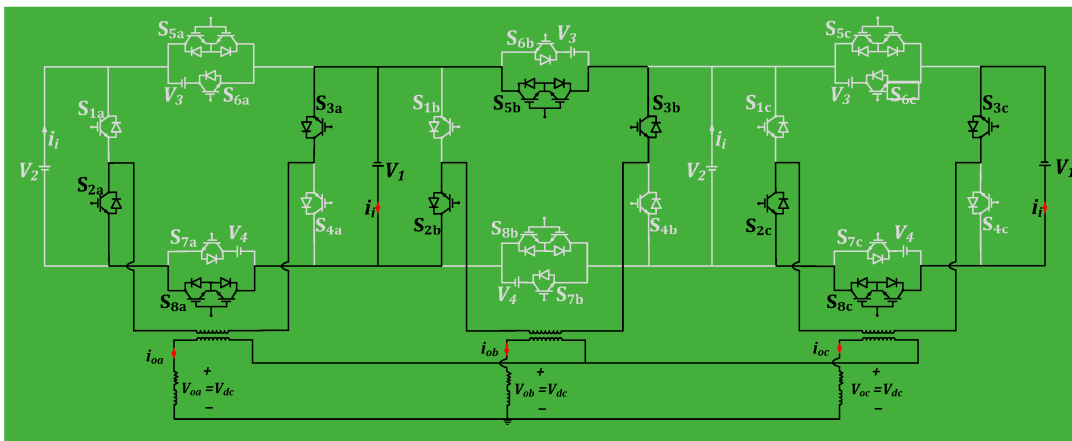


Figure 2. Proposed three-phase multilevel inverter.



(a) $V_o = 0 V_{dc}$.



(b) $V_o = V_{dc}$.

Figure 3. Cont.

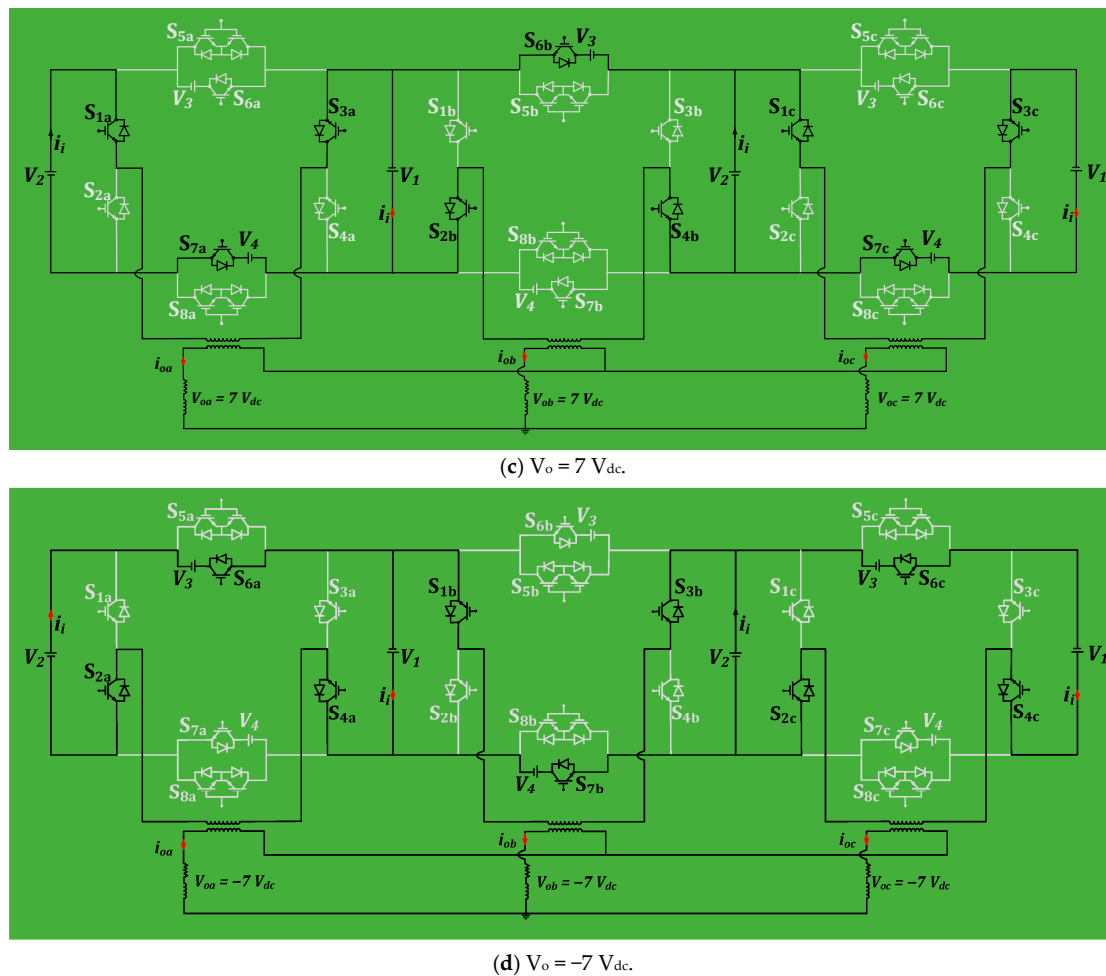


Figure 3. Conducting switches of selected switching modes.

The per-phase switching sequence of the proposed MLI is similar to that of the classical single-phase H-bridge. Positive or negative load voltages are produced by a diagonal switching sequence. The upper and lower switches are gated to provide a path for the generation of these voltages but are noted as gated ON or OFF concurrently. Considering Equations (1)–(5) and acceptable switching sequences, the maximum levels of load voltage that the proposed topology can generate are shown in Table 1. The fundamental frequency control (FFC) method is employed for the safe switching of the proposed MLI because FFC provides the following advantages against conventional PWM techniques in medium- and high-power applications: minimum switching losses, low EMI and dv/dt interference, easy to control and implement, suited for medium-high-voltage and medium-high power applications, reduced harmonic content at high levels, etc. FFC utilizes fewer switching transitions periodically compared to PWM, which operates at a high frequency, thus resulting in a higher number of switching events per cycle. A smaller number of switching events per cycle provides less thermal stress and fewer switching losses in the semiconductor switches. Therefore, these advantages make the proposed DVR reliable and efficient [6,10,12]. The junction temperatures in PWM-controlled MLI are high, culminating in higher losses; the thermal management in these devices is complex [6]. PWM techniques require pinpoint carrier integration [9] and a high-bandwidth controller, but FFC operates with minimal processing necessities [22], unsophisticated control structures, and enhanced durability to noise computation [23].

Table 1. Switching sequence.

State	Active Switches			Output Voltage
	Phase A	Phase B	Phase C	V_A V_B V_C
I	S_{2a}, S_{3a}, S_{8a}	S_{2b}, S_{3b}, S_{5b}	S_{2c}, S_{3c}, S_{8c}	V_{dc}
II	S_{1a}, S_{4a}, S_{8a}	S_{1b}, S_{4b}, S_{5b}	S_{1c}, S_{4c}, S_{8c}	$2 V_{dc}$
III	S_{1a}, S_{3a}, S_{8a}	S_{2b}, S_{4b}, S_{5b}	S_{1c}, S_{3c}, S_{8c}	$3 V_{dc}$
IV	S_{2a}, S_{4a}, S_{7a}	S_{1b}, S_{3b}, S_{6b}	S_{2c}, S_{4c}, S_{7c}	$4 V_{dc}$
V	S_{2a}, S_{3a}, S_{7a}	S_{2b}, S_{3b}, S_{6b}	S_{2c}, S_{3c}, S_{7c}	$5 V_{dc}$
VI	S_{1a}, S_{4a}, S_{7a}	S_{1b}, S_{4b}, S_{6b}	S_{1c}, S_{4c}, S_{7c}	$6 V_{dc}$
VII	S_{1a}, S_{3a}, S_{7a}	S_{2b}, S_{4b}, S_{6b}	S_{1c}, S_{3c}, S_{7c}	$7 V_{dc}$
VIII	S_{2a}, S_{4a}, S_{8a}	S_{2b}, S_{4b}, S_{8b}	S_{2c}, S_{4c}, S_{8c}	0
IX	S_{1a}, S_{4a}, S_{5a}	S_{1b}, S_{4b}, S_{6b}	S_{1c}, S_{4c}, S_{5c}	$-V_{dc}$
X	S_{2a}, S_{3a}, S_{5a}	S_{2b}, S_{3b}, S_{8b}	S_{2c}, S_{3c}, S_{5c}	$-2 V_{dc}$
XI	S_{2a}, S_{4a}, S_{5a}	S_{1b}, S_{3b}, S_{8b}	S_{2c}, S_{4c}, S_{5c}	$-3 V_{dc}$
XII	S_{1a}, S_{3a}, S_{6a}	S_{2b}, S_{4b}, S_{8b}	S_{1c}, S_{3c}, S_{6c}	$-4 V_{dc}$
XIII	S_{1a}, S_{4a}, S_{6a}	S_{1b}, S_{4b}, S_{7b}	S_{1c}, S_{4c}, S_{6c}	$-5 V_{dc}$
XIV	S_{2a}, S_{3a}, S_{6a}	S_{2b}, S_{3b}, S_{7b}	S_{2c}, S_{3c}, S_{6c}	$-6 V_{dc}$
XV	S_{2a}, S_{4a}, S_{6a}	S_{1b}, S_{3b}, S_{7b}	S_{2c}, S_{4c}, S_{6c}	$-7 V_{dc}$

The magnitude of the source voltages is expressed by the following:

$$\begin{cases} V_1 = V_{dc} \\ V_2 = 2V_{dc} \\ V_3 = V_4 = 4V_{dc} \end{cases} \quad (1)$$

The line and phase voltages are related by the following:

$$\begin{cases} V_{AB} = V_{AN} - V_{BN} \\ V_{BC} = V_{BN} - V_{CN} \\ V_{CA} = V_{CN} - V_{AN} \end{cases} \quad (2)$$

Finally, the following is evident from Figure 2:

$$\begin{cases} V_{AN} = V_A \\ V_{BN} = V_B \\ V_{CN} = V_C \end{cases} \quad (3)$$

The per-phase peak voltage for the proposed topology is computed as follows:

$$V_A = V_B = V_C = \pm 7V_{dc} \quad (4)$$

The maximum line-to-line output voltage is expressed as follows:

$$V_{AB} = V_{BC} = V_{CA} = \pm 7V_{dc} * \sqrt{3} \quad (5)$$

3. Proposed Three-Phase MLI-Based DVR

The circuit architecture of the proposed three-phase multilevel inverter-based DVR is shown in Figure 4. The proposed dynamic voltage restorer is composed of the following

parts: three-phase MLI, output filter, bypass switches S_{ba} , S_{bb} , S_{bc} , and an injection transformer. Other parts of the system are the grid voltage and the sensitive load. As depicted by Figure 4, the proposed three-phase DVR uses an external energy source (inverter DC source voltage) to compensate for voltage sag or swell disturbances. Also, each phase of the MLI requires one low-frequency transformer, which also functions as the injection transformer and a galvanic isolator.

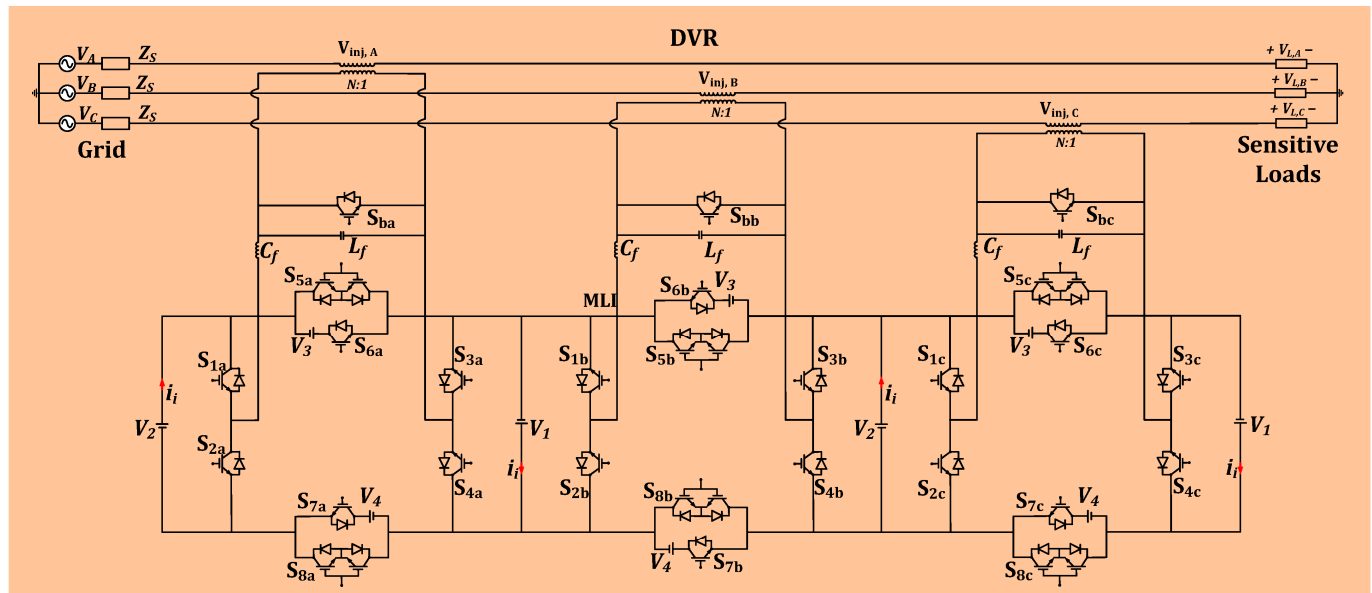


Figure 4. Proposed MLI-based DVR.

3.1. Principle of Operation

The operational principle of the proposed DVR based on a three-phase MLI is categorized into two states: zero voltage-compensating or bypass state and voltage-compensating state.

1. In the bypass or zero-voltage-compensating state, zero voltage is generated by each phase of the three-phase MLI and injected into the grid by turning on the bypass switches S_{ba} , S_{bb} , and S_{bc} . This is because the grid voltage is at its nominal value due to the absence of voltage sag or voltage swell disturbances; hence, compensating voltage is not required.
2. During voltage sag or swell disturbance, the compensation state is activated. Therefore, an opposite polarity voltage of equal magnitude and phase is generated by the three-phase inverter to mitigate voltage sag or swell disturbances.

3.2. Proposed DVR Compensation

In general, DVRs fed by DC sources, such as MLI, are limited by the magnitude and period of compensating voltage. These limitations are no longer major drawbacks, due to the proliferation of photovoltaic systems for power generation. In the proposed DVR, compensating energy is derived from the inverter DC-link (battery); therefore, compensating magnitudes are hugely dependent on the magnitude of the DC-link and the maximum output voltage of the MLI. The generalized compensating magnitude of the proposed dynamic voltage restorer is presented in this section. The maximum inverter output voltage, V_{MLI} , of the proposed DVR is expressed by Equation (6).

$$V_{MLI} = \pm 7V_{dc} \quad (6)$$

The general relationship between the grid voltage, DVR voltage, and load voltage of the proposed DVR of Figure 4 is determined by KVL analysis of Figure 2, which yields Equation (7). Due to the symmetry of the phases, KVL analysis of phase A yields Equation (8), which applies to the other phases.

$$V_G + V_{DVR} = V_L \quad (7)$$

$$\begin{cases} V_{A,G} + V_{A,DVR} = V_{A,L} \\ V_{B,G} + V_{B,DVR} = V_{B,L} \\ V_{C,G} + V_{C,DVR} = V_{C,L} \end{cases} \quad (8)$$

where V_G , V_L , and V_{DVR} represent grid voltage, load voltage, and DVR voltage, accordingly. Respective phase parameters have A, B, and C as initial subscripts. The inverter output voltage, V_{MLI} , and injected DVR voltage, V_{DVR} , of Figure 4 are related by the equation below:

$$V_{DVR} = nV_{MLI} \quad (9)$$

Assuming x is the transfer ratio of the inverter, expressed by Equation (10), then the inverter output voltage V_{MLI} and grid voltage V_G are related by Equation (11).

$$x = \frac{V_o}{V_{in}} \quad (10)$$

$$V_G = \frac{V_{MLI}}{x} \quad (11)$$

Equation (12) shows the needed computation during swell and sag occurrences, where V_{SWELL} and V_{SAG} represent swell and sag voltages, respectively.

$$\begin{cases} V_{SAG} = V_{L,REF} - V_G \\ V_{SWELL} = V_{L,REF} - V_G \end{cases} \quad (12)$$

From Equation (11), $V_{L,REF}$ represents the reference line voltage. Considering the sag phenomenon, $V_{L,REF}$ is greater than V_G ; therefore, V_{SAG} has positive polarity. Likewise, during the swell phenomenon, $V_{L,REF}$ is less than V_G ; therefore, V_{SWELL} has negative polarity. Therefore, the proposed MLI produces the required voltage (V_{DVR}) with positive and negative polarities to offset the sag and swell phenomena, as expressed by Equation (13).

$$\begin{cases} V_{DVR} = +V_{SAG} \\ V_{DVR} = -V_{SWELL} \end{cases} \quad (13)$$

4. Simulation and Experimental Results

In this section, theoretical analysis of the proposed topology is validated by conducting simulations and experimental investigations. The experimental and simulation outcomes showcase the practicality of the proposed DVR, based on a three-phase MLI. This section is segmented into two sections; in the first section, simulation-based results of the proposed MLI topology are provided. The second section provides the experimental results of the proposed DVR, based on three-phase MLI.

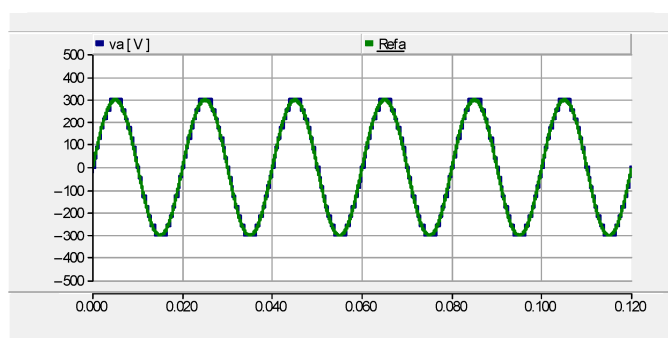
4.1. Simulation Results

Simulation results of the proposed three-phase MLI are derived by modeling its power circuit in PSCAD/EMTDC software. The proposed three-phase MLI has an RL load connected in a Y configuration. The transformers used provide galvanic isolation with a turns ratio of $\frac{N_1}{N_2} = 1$. Relevant control techniques that are capable of producing quality

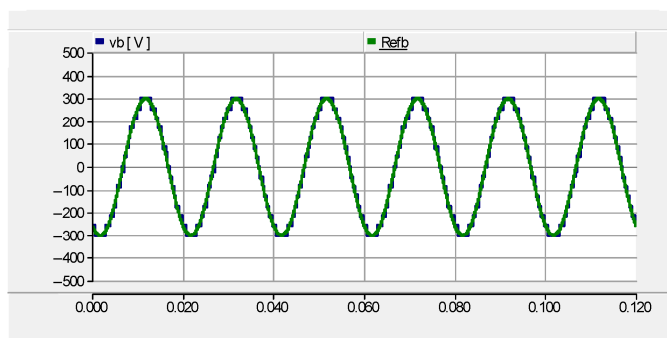
output waveforms, reduced switching losses, and harmonics are essential for enabling the switching sequence of Table 1. Therefore, fundamental frequency modulation, also known as the nearest zero technique, is selected for switching the proposed MLI. Also, its switching losses are comparatively less when juxtaposed with the sinusoidal PWM and other PWM techniques. Using the experimental and simulation parameters of Table 2, the output waveforms of the simulation are illustrated in Figures 5–9. The step (v_a , v_b , and v_c) and reference (Ref_a , Ref_b , and Ref_c) load voltage waveforms of all the phases, having a peak value of 300 V, are shown in Figure 5a–c accordingly. Both waveforms (step and reference) are aligned properly; therefore, the load voltage is a pure sinusoidal waveform.

Table 2. Simulation and experimental parameters.

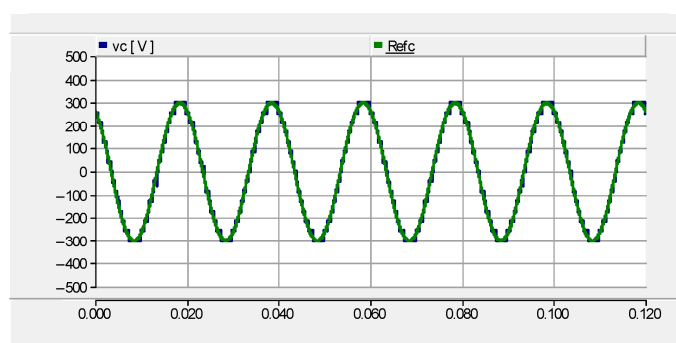
Parameters	Value
Input Voltage V_{dc}	$V_1 = 42.85$ V, $V_2 = 85.70$ V, $V_3 = V_4 = 171.40$ V
Load Resistance R	100 Ω
Load Inductance L	55 mH
Switching Frequency f_s	5 kHz
Load Frequency f_o	50 Hz
Modulation Index	1



(a)



(b)



(c)

Figure 5. Phase voltage waveforms. (a) phase A voltage waveform; (b) phase B voltage waveform; (c) phase C voltage waveform.

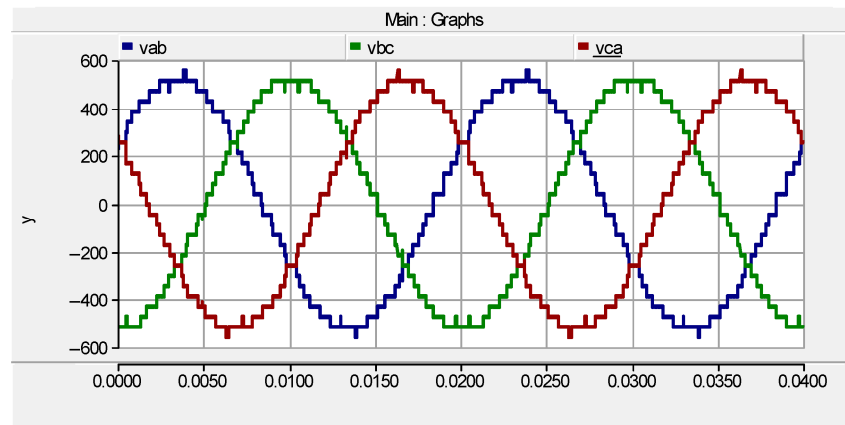


Figure 6. Line-to-line voltage waveform.

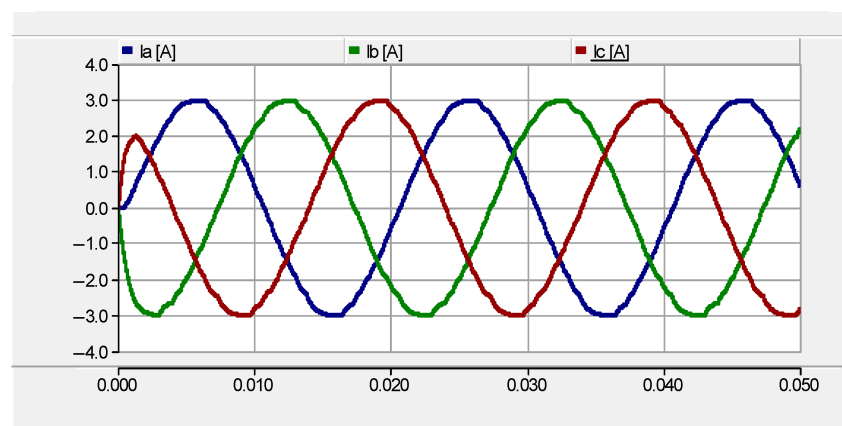
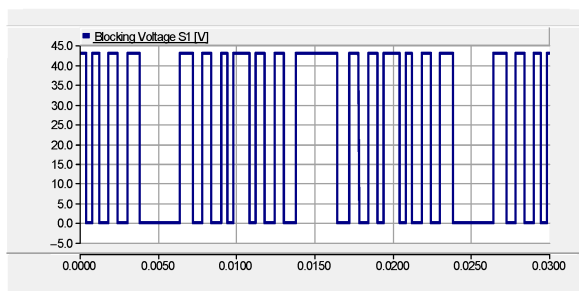
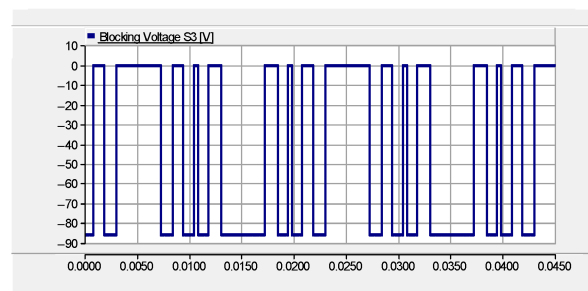


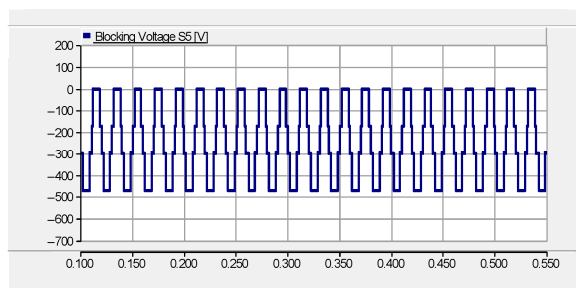
Figure 7. Load current waveform.



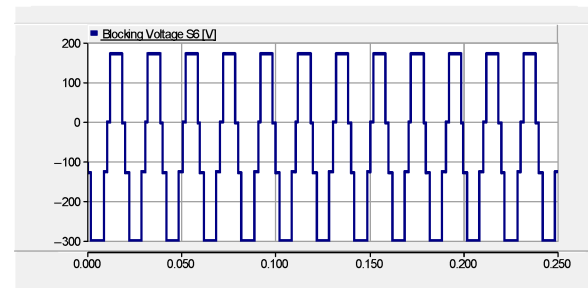
(a)



(b)



(c)



(d)

Figure 8. Blocking voltage waveforms. (a) switch 1; (b) switch 3; (c) switch 5; (d) switch 6.

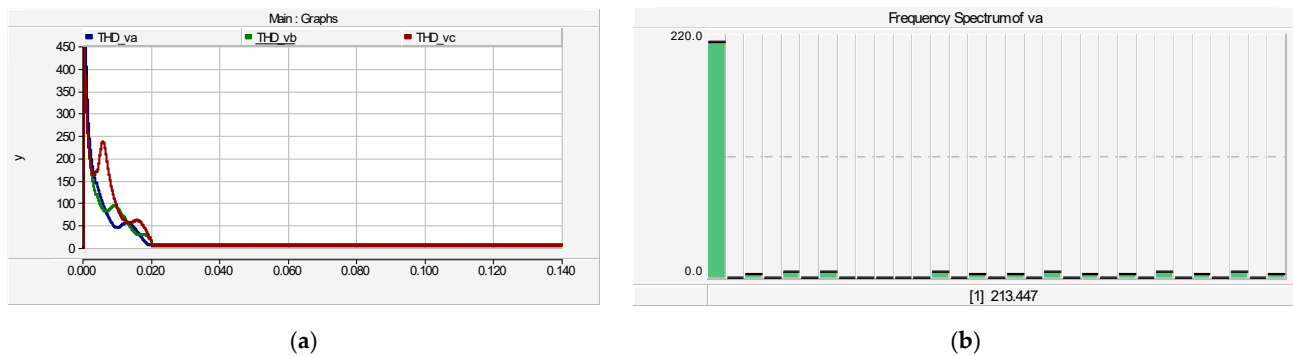


Figure 9. THD and FTT voltage waveforms. (a) THD waveform; (b) FFT waveform.

The line-line load voltage waveforms for phases AB, BC, and CA with an approximate maximum magnitude of 520 V are illustrated in Figure 6. The load current waveforms illustrated in Figure 7 exhibit pure sinusoidal waveform characteristics. Therefore, the proposed topology does not require an output filter; hence, the cost, volume, and weight of the propounded topology are not increased. The peak magnitude of the current waveforms is 3 A. Figure 8 shows the blocking voltages of some selected switches in Phase A. Switches on the same leg of connection or current path have an equal magnitude of blocking voltage, i.e., S_1 and S_2 are equal, S_3 and S_4 are equal, S_5 and S_7 are equal, and S_6 and S_8 are equal.

Figure 9a,b show the voltage THD and frequency spectrum, respectively, of the proposed three-phase multilevel inverter. From Figure 9a, the THD value of approximately 5.8% for each phase is less than the 8% IEEE 519-2022 standard [24] at the PPC (point of common coupling). The THD waveform of Figure 9a is composed of a transient period, 0.00 – 0.020 s, and the steady state period, 0.020 – 0.140 s, and were simulated using the phase load voltages of the three-phase multilevel inverter. Also, the frequency spectrum of Figure 9b shows that the harmonics' magnitude is within acceptable ranges. The even-order harmonics are naturally zero (0), and some of the odd-order harmonics are significantly minimized. The third, fifth, and seventh harmonics are high, but within the IEEE 519-2022 acceptable range of 8% and 1.5% for low and high voltages, respectively.

4.2. Experimental Results

This section provides the experimental results of the proposed DVR topology, considering voltage sag and swell fault states for linear and nonlinear loads. The 20% sag and 30% sag and swell fault conditions are investigated for the linear and nonlinear loads, respectively. The laboratory setup of the proposed DVR, based on a three-phase multilevel inverter, is built using the parameters of Table 2 and source voltages expressed by Equation (14). Due to the operational similarities between the phases of the three-phase MLI, experimental analysis and results are produced for Phase A only. Nonetheless, the source voltage equations are expressed for the three phases, as in the case of Equation (14). Figure 10 illustrates the experimental waveform of the load current (green color) and voltage (blue color) for Phase A of the proposed three-phase MLI. The peak magnitude of the current and voltage waveforms is 3 A and 300 V, respectively.

The proposed DVR's operations under normal, sag, and swell fault conditions are examined in this section. The following assumptions are made for this analysis. The input three-phase voltages (v_{sa} , v_{sb} , and v_{sc}) in the normal condition are as follows:

$$\begin{aligned} v_{sa} &= 300 \sin(100\pi t) \\ v_{sb} &= 300 \sin(100\pi t - 120^\circ) \\ v_{sc} &= 300 \sin(100\pi t - 240^\circ) \end{aligned} \quad (14)$$

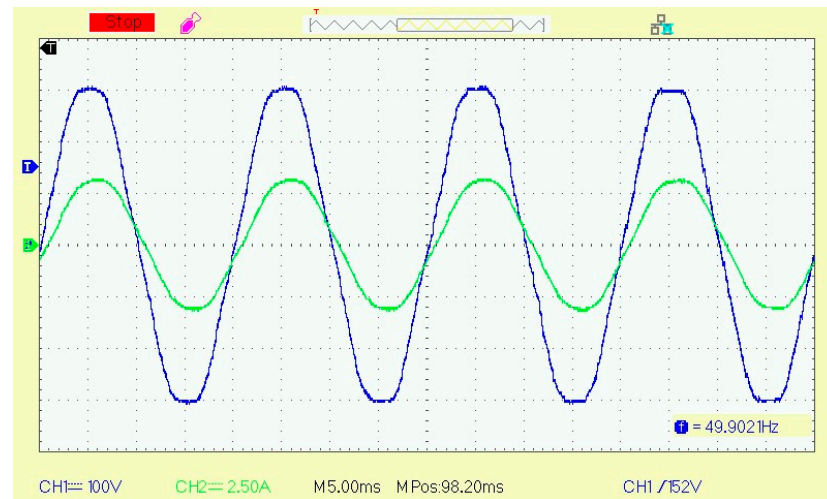
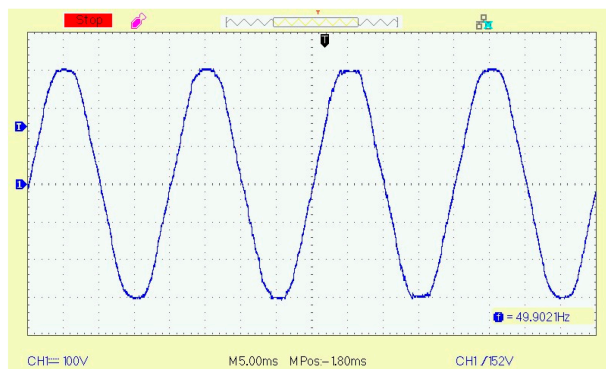


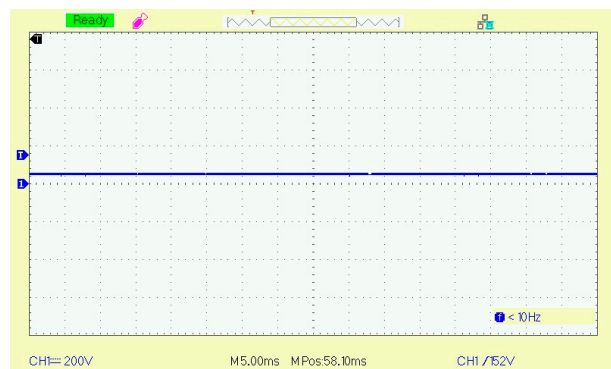
Figure 10. Phase A load voltage and current waveforms.

4.2.1. Normal Operating Condition

The load voltage across Phases A, B, and C is denoted by v_a , v_b , and v_c , accordingly. Figure 11a shows the grid voltage for normal operation, i.e., this period is devoid of any fault condition; therefore, the injected voltage from the DVR is zero voltage (0 V), as illustrated by Figure 11b.



(a)

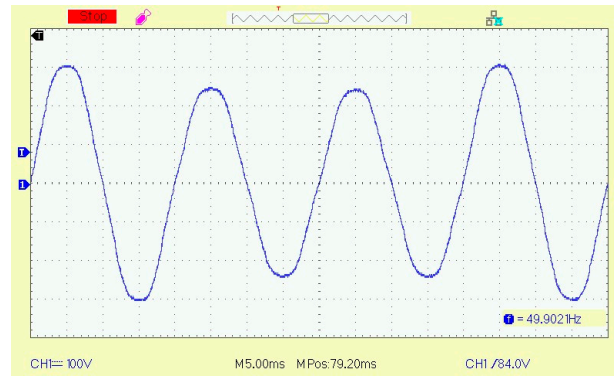


(b)

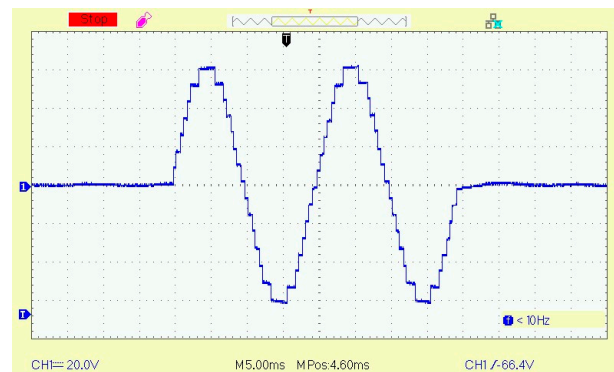
Figure 11. Grid voltage and injected voltage during normal operating mode. (a) grid voltage; (b) injected voltage.

4.2.2. Linear Loads

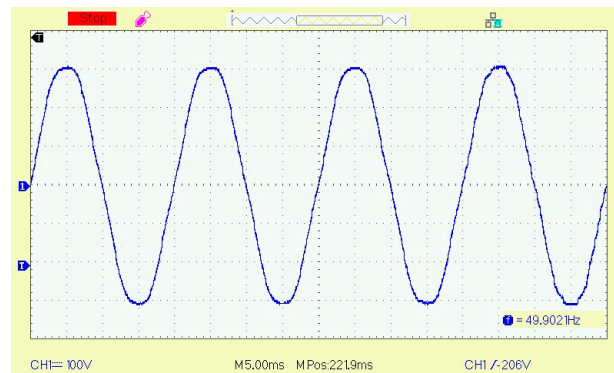
Considering the sag–swell fault conditions under investigation for linear loads, it is expected that under sag conditions, the proposed MLI injects a positive difference voltage to keep the three-phase load voltage constant. However, during swell conditions, the multilevel inverter injects a negative difference voltage with a 180° phase difference to offset the disturbance and restore the load voltage to the nominal value. In this experiment, the grid's voltage is expressed by Equation (14) for rated conditions. During the sag and swell period, the rated voltage reduces and increases by 0.8% and 1.2%, respectively. The sag mode is expressed by Equation (15) for the time interval of 0.02–0.04 s and the swell mode is expressed by Equation (16) for the time interval of 0.04–0.06 s. Also, the faultless period of operation of the proposed DVR occurs during the time intervals of 0.00–0.02 s and 0.06–0.10 s. These faultless and faulty states of operations of the proposed DVR are illustrated in Figures 12 and 13 for the sag and swell states, respectively.



(a)



(b)



(c)

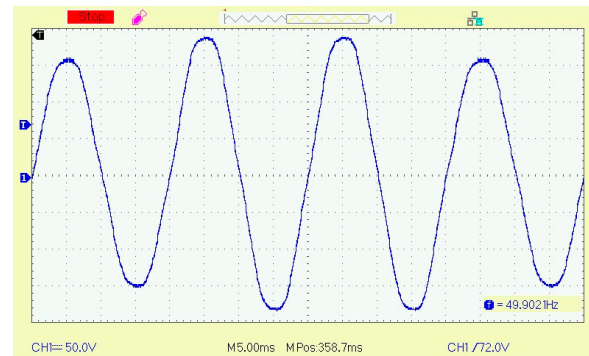
Figure 12. Sag state for linear loads. (a) sag voltage waveform; (b) injected voltage waveform; (c) restored nominal voltage waveform.

$$\begin{aligned} v_{sa} &= 240 \sin(100\pi t) \\ v_{sb} &= 240 \sin(100\pi t - 120^\circ) \quad 0.02 < t < 0.04 \\ v_{sc} &= 240 \sin(100\pi t - 240^\circ) \end{aligned} \quad (15)$$

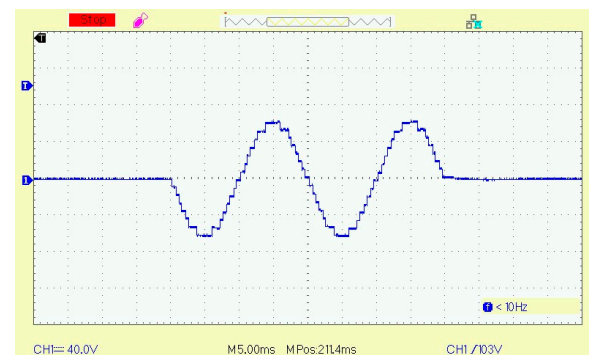
$$\begin{aligned} v_{sa} &= 360 \sin(100\pi t) \\ v_{sb} &= 360 \sin(100\pi t - 120^\circ) \quad 0.04 < t < 0.06 \\ v_{sc} &= 360 \sin(100\pi t - 240^\circ) \end{aligned} \quad (16)$$

$$\begin{aligned} v_{sa} &= 300 \sin(100\pi t) \\ v_{sb} &= 300 \sin(100\pi t - 120^\circ) \quad 0.06 < t < 0.10 \\ v_{sc} &= 300 \sin(100\pi t - 240^\circ) \end{aligned} \quad (17)$$

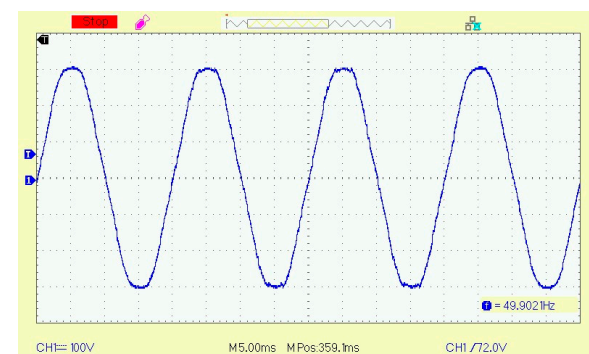
To resolve the above sag–swell issues, the DVR needs to inject the required voltages to offset or compensate for these anomalies. Figures 12a and 13a show the line voltages under faulty conditions. Figures 12b and 13b show the required injected voltage to compensate for the sag–swell faults, respectively. During the time interval of 0.02 – 0.04 s, the DVR injects the required magnitude of voltage in phase with the line voltage to mitigate the decrease in the rated voltage. Similarly, during the time interval of 0.04 – 0.06 s, the DVR injects the required voltage magnitude out of phase with the line voltage to mitigate the increase in the rated voltage. Between 0.00 – 0.02 s and 0.06 – 0.10 s, the DVR injects no voltage, because the sag–swell fault conditions are not present. Figure 13c shows the restored line voltage with a rated peak voltage of 300 V.



(a)



(b)



(c)

Figure 13. Swell state for linear loads. (a) swell voltage waveform; (b) injected voltage waveform; (c) restored nominal voltage waveform.

4.2.3. Nonlinear Loads

Similarly, the proposed DVR-based MLI is investigated for voltage sag and swell conditions for nonlinear loads. During the sag and swell period, the rated voltage reduces

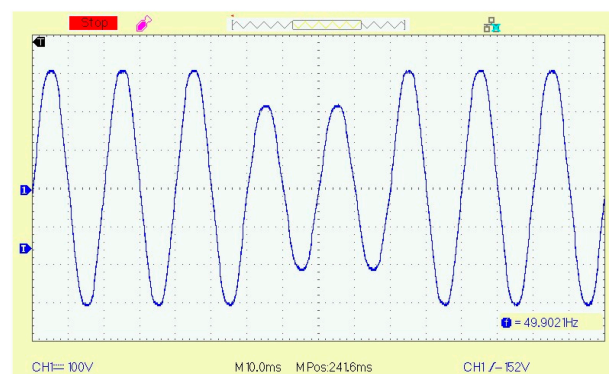
and increases by 0.7% and 1.3%, respectively, for nonlinear loads. Thus, the DVR is required to inject a voltage of 70 V in and out of phase to mitigate the sag and swell fault conditions. However, considering the maximum source voltage of the MLI, the DVR can only compensate for 86% of the sag/swell condition. Considering the sag and swell modes depicted in Figures 14a and 15a, the injected voltages for compensation are shown in Figures 14b and 15b, accordingly. The restored (87%) load voltage for nonlinear loads considering the sag and swell conditions is shown in Figures 14c and 15c, accordingly. Only 86–87% of the load voltage is restored in this case, because of the magnitude of the incremental voltage value (V_{dc}) and the level count of the MLI. The maximum MLI output voltage and the load voltage are equal. Increasing the level count to more than 31 directly reduces the V_{dc} value, thus allowing for compensations at lower V_{dc} magnitudes.

The proposed DVR is also investigated for unbalanced three-phase distortions, considering a load voltage of 310 V. Equations (18)–(20) show the load voltage waveforms during the normal operating period ($0.00 < t < 0.02$ s), faulty period ($0.02 < t < 0.08$ s), and restored (after compensation) period ($0.08 < t < 0.120$ s), respectively. Two sag cases are presented for phases A and C, with sag voltage magnitudes of 280 V and 250 V, respectively. The swell condition is analyzed in phase B, with a swell voltage magnitude of 50 V. Figures 16 and 17 show the simulation results for the faulty conditions (Figure 16) and restored or compensated load voltage (Figure 17). The presence of negative-sequence components (NSC) in three-phase unbalanced loads introduces new challenges, such as complex control (NSC comes in the form of fluctuating AC quantities with double frequency, making it hard for the DVR control technique to track, maintain, and compensate them adequately), reduced performance due to the error in the compensating voltage, and DVR output voltage. Nonetheless, the application of the right control techniques, such as negative-sequence elimination (NSE), multiple DQ transformation, etc., eliminates these limitations.

$$\begin{aligned} v_{sa} &= 310 \sin(100\pi t) \\ v_{sb} &= 310 \sin(100\pi t - 120^\circ) \quad 0.00 < t < 0.02 \\ v_{sc} &= 310 \sin(100\pi t - 240^\circ) \end{aligned} \quad (18)$$

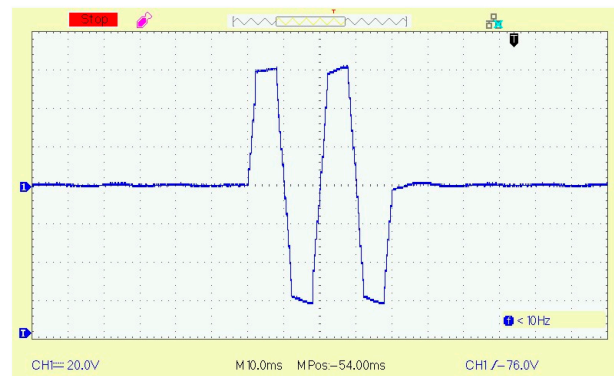
$$\begin{aligned} v_{sa} &= 280 \sin(100\pi t) \\ v_{sb} &= 360 \sin(100\pi t - 120^\circ) \quad 0.02 < t < 0.08 \\ v_{sc} &= 250 \sin(100\pi t - 240^\circ) \end{aligned} \quad (19)$$

$$\begin{aligned} v_{sa} &= 310 \sin(100\pi t) \\ v_{sb} &= 310 \sin(100\pi t - 120^\circ) \quad 0.08 < t < 0.120 \\ v_{sc} &= 310 \sin(100\pi t - 240^\circ) \end{aligned} \quad (20)$$

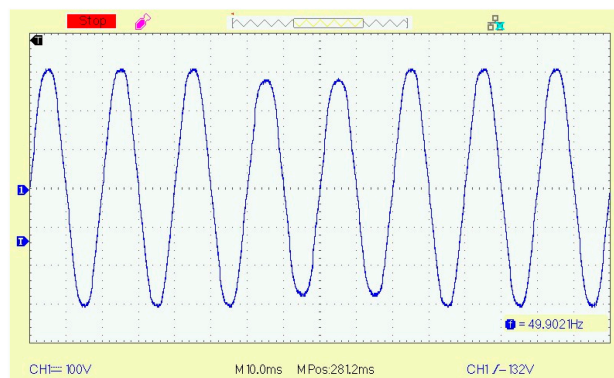


(a)

Figure 14. Cont.

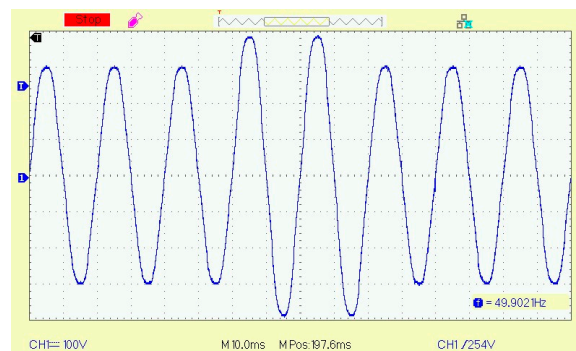


(b)

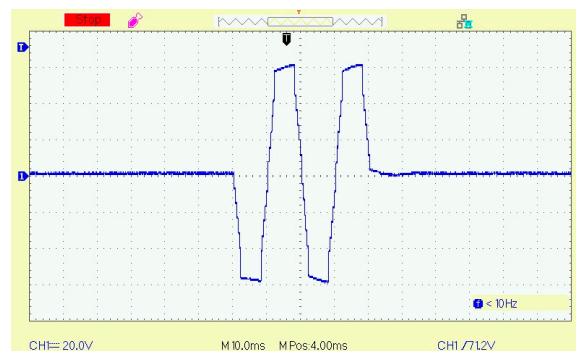


(c)

Figure 14. Sag state for nonlinear loads. (a) sag voltage waveform; (b) injected voltage waveform; (c) restored nominal voltage waveform.

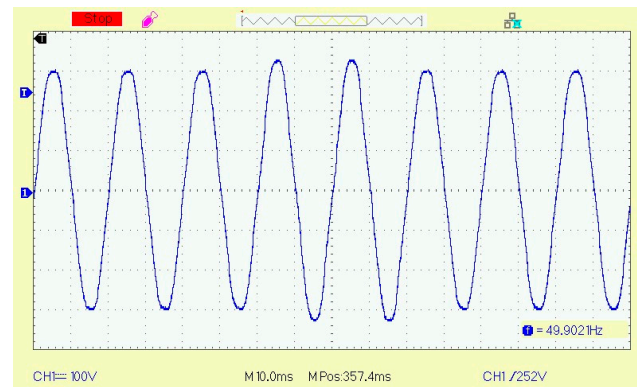


(a)



(b)

Figure 15. Cont.



(c)

Figure 15. Swell state for nonlinear load. (a) swell voltage waveform; (b) injected voltage waveform; (c) restored nominal voltage waveform.

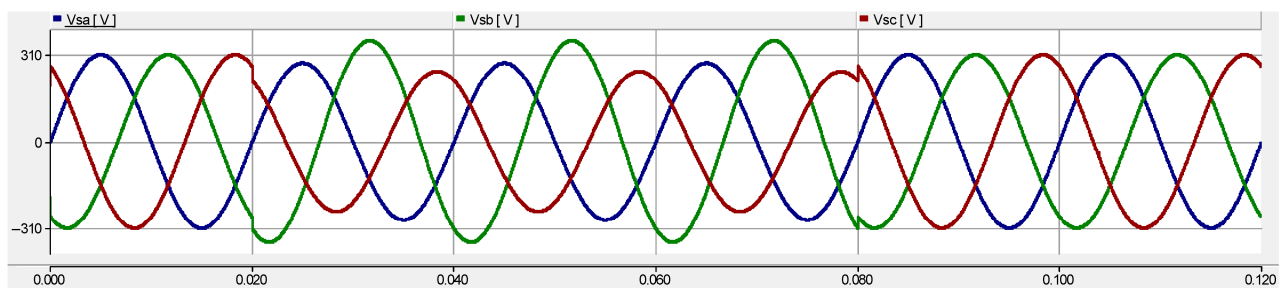


Figure 16. Three-phase unbalanced load voltage waveforms.

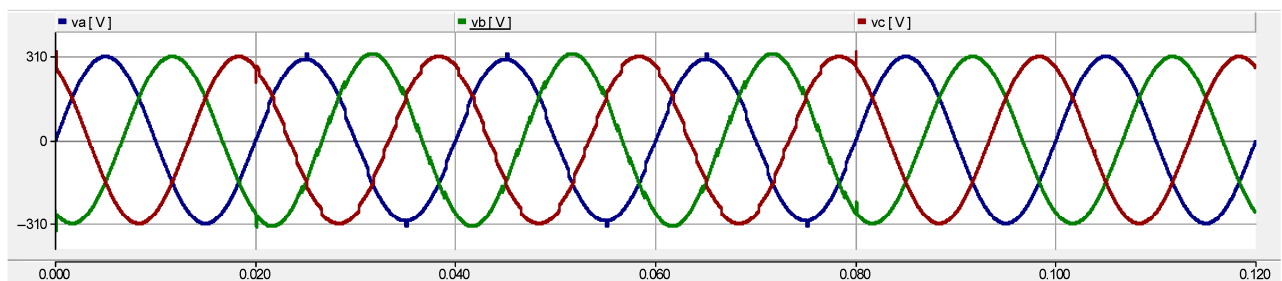


Figure 17. Restored three-phase load voltage waveforms.

4.2.4. Compensation Limitations

The primary function of a DVR is to mitigate power quality issues, such as voltage swell and dip, by injecting voltage of an appropriate magnitude and phase. Therefore, the magnitude of the compensating voltage should be suitable to offset any power disturbance. This section investigates the proposed DVR's compensating capabilities, considering critical DVR parameters such as peak voltages of the DVR, incremental voltage values, compensating percentages, etc., for the varying input voltages provided in Table 3. The major limitations of most DVRs are the magnitude of the compensating voltage and the compensating duration capabilities. From Table 3, it is evident that the proposed DVR can compensate for any voltage sag or swell conditions if the MLI input voltage is varied.

However, because the incremental voltage levels are dependent on the magnitude of V_{dc} , and the DVR voltage output levels are 15, this may impose some limitations on the compensating duration and voltage magnitude. The maximum compensating voltage and compensating percentage that the proposed DVR can deliver at any time are based

on the magnitude of the source voltages V_1 , V_2 , and V_3/V_4 . For example, if $V_1 = 20$ V, $V_2 = 40$ V, and $V_3 = V_4 = 80$ V, and the load voltage is 300 V, the proposed DVR can provide 46.67% of compensation (sag or swell), with an incremental voltage level of 20V. Similarly, if $V_1 = 42.85$ V, $V_2 = 85.70$ V, and $V_3 = V_4 = 171.40$ V, and the load voltage is 300 V, the proposed DVR can provide 46.67% of compensation (sag or swell), with an incremental voltage level of 20V. The compensating duration of the proposed DVR will not be a major limitation when renewable energy sources and/or energy storage systems, such as PV, etc., are applied as the source voltage [25]. Improvements made in large-scale battery production for utility or commercial applications, such as Megapack by Tesla, can interface with PV systems and the DVR to provide compensation for long-duration disturbances. Additionally, a rectifier circuit can be used to provide power directly from the grid, as in the case of AC-DC-AC DVR topologies. The latter methodology introduces double-stage power conversion, which reduces the overall system efficiency due to multiple operations of power switching during the conduction and switching states. In the absence of the above features, the proposed DVR functions better in small-to-medium depth and duration compensation, juxtaposed with deep and prolonged compensation because of the limitation of the battery (DC-link), i.e., voltage capacity and battery life. As shown by the second (case 1) and fifth (case 4) columns of Table 3, where the load voltages far exceed the maximum MLI-DVR output voltage, the compensation capabilities of the proposed DVR are reduced during deep disturbances. Finally, the compensating capabilities of multilevel inverter-based DVRs depend on the peak magnitude of the DVR output voltage, the number of output voltage levels, the voltage's incremental magnitude, and the lifespan of the source voltage. Figure 18 shows a graph of the major compensating parameters.

Table 3. Limitation analysis of the proposed three-phase MLI-based DVR.

Cases	1	2	3	4
MLI Input Voltage	$V_{dc} = V_1 = 20$ V $V_2 = 40$ V $V_3 = V_4 = 80$ V	$V_{dc} = V_1 = 42.85$ V $V_2 = 85.70$ V $V_3 = V_4 = 171.40$ V	$V_{dc} = V_1 = 60$ V $V_2 = 120$ V $V_3 = V_4 = 240$ V	$V_{dc} = V_1 = 80$ V $V_2 = 160$ V $V_3 = V_4 = 320$ V
Peak DVR Output Voltage	140	300	420	560
Voltage Incremental Levels (V_{dc})	20	42.85	60	80
Load Voltage (V)	300	300	600	1 kV
Compensating Percentage (%)	46.67	100	70	56

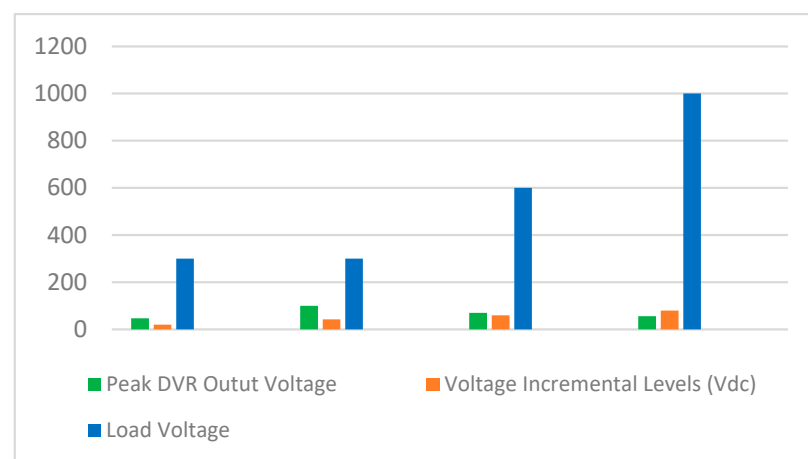


Figure 18. Magnitude of compensating parameters.

4.2.5. Comparative Analysis

Comparative analysis of the proposed three-phase MLI DVR and existing DVRs, considering features such as phase count, control technique, stages of voltage conversion, etc., is presented in this section. The result of this comparative investigation is illustrated in Table 4. It is evident that the proposed three-phase multilevel inverter-based DVR stacks properly against existing DVR topologies. For example, the proposed DVR can adequately compensate for voltage sag and swell, as well as harmonics, in linear and nonlinear three-phase loads and unbalanced loads. Also, the compensating voltage has a single voltage conditioning feature, and the presence of a battery makes it suitable for renewable energy integration.

Table 4. Comparative investigation [13,14,16,22,23,26,27].

Topology	Proposed	[13]	[14]	[16]	[22]	[26]	[27]	[23]
Control Technique	FFM	SRPE—DQ Algorithm	Finite-Control-Set Model Predictive Control MPC	AGPSO Algorithm	Sliding Mode	SVPWM	PWM	ST-SMC
Voltage Boosting	Yes/No	No	No	No	No	Yes	No	No
Number of Voltage Conversion Stages	Single	Single	Single	Single	Single	Multiple	Direct	Single
Phase Count	Three	Three	Three	Three	Three	Three		Single
Converter Topology	MLI	MLI	MLI	MLI	AC-AC	DC-DC, MLI	AC-AC	MLI
Type of Power Issue Mitigation	Sag, Swell, Harmonics, Linear loads, Nonlinear loads	Sag, Swell, Harmonics	Sag, Swell, Harmonics, Nonlinear loads	Harmonics, Sag, Swell	Sag, Swell,	Sag	Sag, Swell	Sag, Swell, Harmonics
Energy Storage Type	Battery	Battery	Battery	Battery, Capacitor	No	Battery, Capacitor	No	Battery

The absence of a direct voltage-boosting feature in the MLI is a drawback, considering the current trajectory of multilevel inverter topologies. Having voltage-boosting capabilities, as in the case of impedance-based topologies (a common example is the Z-source), will provide a longer cycle life for the source voltage (battery) and will also enable the DVR to compensate for deep sag/swell conditions and for longer duration without putting much stress on the battery. Nonetheless, voltage-boosting capabilities can be provided by the low-frequency transformer, which serves as the injection and galvanic isolation device. The inherent features of the low-frequency transformer directly affect the scalability and transient behavior of the proposed MLI-DVR. The winding resistance and leakage inductance are increased because of the bulkiness of the transformer, due to its operations at the fundamental network frequency. Increased winding resistance and leakage inductance cause losses, reduced efficiency, and reduced voltage injection response time during an abrupt grid disruption. Also, thermal limitations and transient magnetic saturation can establish nonlinear characteristics, causing a reduction in the efficacy of the compensations. In the absence of voltage-boosting features, the proposed MLI-DVR is highly suited for applications in grid networks such as distribution systems facing low-to-medium voltage sag/swell challenges (10–30%). Voltage compensation in such networks can be achieved without LDES (long-duration energy storage) or boost DC-DC converters. The inherent advantages of MLIs (better voltage synthesizing and superior quality waveforms) produce voltage waveforms with low THD, thus complying with industry standards such

as IEEE 519. These features make the proposed topology appropriate for applications in low–medium power networks, where the protection of sensitive loads in commercial buildings, industries, and microgrid is desired. Table 5 shows a summarized presentation of the sag and swell for linear and nonlinear and unbalanced loads, considering the dip/swell percentage, the injected voltage, and the fault duration.

Table 5. Summarized experimental DVR compensations.

Fault Type	Linear Loads	Nonlinear Loads	Unbalanced Loads
Sag Percentage (%)	80	70	Phase A: 90.32 Phase C: 69.44
Sag Duration (s)	0.02–0.04	0.02–0.04	0.02–0.08
Swell Percentage (%)	120	130	Phase B: 116.13
Swell Duration (s)	0.04–0.06	0.04–0.06	0.02–0.08

5. Conclusions

A dynamic voltage restorer (DVR) is undoubtedly the most efficient power quality enhancer, considering sensitive loads and proximity to the load. This article proposes a dynamic voltage restorer based on a new three-phase MLI that is suitable for mitigating power quality challenges such as voltage dip, swell, and harmonics in power systems. The capabilities of the proposed MLI-DVR are demonstrated by simulation, using PSCAD/EMTDC software and experimental investigations. The proposed three-phase MLI generates 15 steps of load voltage using fewer components. Symmetric and asymmetric analysis of the proposed MLI source voltages confirms the generation of higher levels of load voltage from the asymmetric topology without increasing the component count or structure. The quality of the inverters' simulated load waveforms juxtaposed with the reference waveforms is high. Similarly, experimental analysis of the proposed three-phase MLI validates the qualities of the simulated waveforms by using the fundamental frequency control technique. Simulated THD and FFT values are within acceptable standards, like IEEE 519-2022. The proposed MLI-DVR is investigated during normal operations and fault conditions, such as voltage dip and voltage swell for linear and nonlinear loads, and unbalanced loads, where the proposed DVR adequately mitigated the power disturbances and restored the voltage magnitude to the nominal value; thus, attesting to the practicality of the proposed DVR topology. Also, a comparative analysis of the proposed DVR and existing DVR topologies is conducted.

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