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Impact of Asymmetrical Leakage Inductance on a 380 V–12 V *LLC* Converter with Synchronous Rectifier for DC Transformer Application †

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Abstract

High-density 380 V–12 V *LLC* resonant converters typically employ planar transformers with integrated leakage inductance. To achieve Zero-Voltage Switching (ZVS), an air gap is introduced to adjust the magnetizing inductance (L_m). However, this gap alters the internal magnetic field (H) distribution. In Center-Tapped (CT) structures, this alteration leads to asymmetric leakage inductances between the positive and negative half-cycles, causing resonant frequency mismatch and performance degradation, particularly under light-load conditions. In this work, the asymmetrical leakage inductance effect in a CT transformer for a 380 V–12 V *LLC* resonant converter is systematically investigated. A mathematical model is derived to quantify the leakage inductance distribution, revealing that the relative position between the air gap and the windings significantly affects the symmetry. Based on this modeling analysis, the centralized assembly method is identified as the optimal solution to ensure impedance symmetry. The accuracy of the proposed model and the effectiveness of this structure are validated through Finite Element Analysis (FEA) simulations and a hardware prototype of a 250-W, 600-kHz *LLC* converter. Results demonstrate that this method eliminates the approximately 11% leakage inductance discrepancy (1.8 µH vs. 1.6 µH), ensuring stable operation across the full load range.

Keywords: asymmetrical effect; center-tapped transformer; leakage inductance; *LLC* resonant converter

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1. Introduction

A data center is regarded as the key infrastructure to support the rapid advancements in emerging technologies such as artificial intelligence (AI), 5G, and cloud computing [1,2]. The accelerated evolution of these technologies has significantly increased the demand for electrical power, emphasizing the need for power architectures with higher power density, efficiency, and current capacity. Currently, the efficiency of the power supply from the grid to the data centers is approximately 85%, revealing substantial potential

for optimization [3–6]. Therefore, optimizing data center power architecture is essential not only to address the increasing energy demands of advancing technologies but also to enhance overall operational efficiency. The 380-V bus architecture directly steps down the input voltage of 380 V to a 12 V load, significantly reducing the number of conversion stages [7–9]. By delivering power from a high-voltage 380-V bus and transferring lower current, more power can be efficiently delivered due to the remarkable reduction in power consumption in i^2R. This makes it a promising solution for future data center power architectures. However, this transition also presents numerous challenges in terms of practical design and implementation.

A traditional 380 V–12 V isolated DC-DC converter, typically based on the *LLC* resonant topology, comprises three main stages: an inverter, a resonant tank, and a rectifier. The *LLC* resonant converter is renowned for its soft-switching capabilities, achieving zero-voltage switching (ZVS) for primary switches and zero-current switching (ZCS) for secondary rectifiers, which makes it highly suitable for high-frequency applications [10–14]. To further enhance performance, Gallium Nitride (GaN) High-Electron-Mobility Transistors (HEMTs) are widely adopted as primary switches, pushing switching frequencies to the MHz level and significantly increasing power density [15–17]. This converter typically operates in DC Transformer (DCX) mode with unity gain, where the switching frequency is fixed at the resonant frequency to minimize circulating energy [18]. The rectifier stage converts the high-frequency AC current into a DC output, commonly utilizing either Full-Bridge (FB) or Center-Tapped (CT) configurations.

The recent literature has extensively investigated the magnetic design within these topologies. As detailed in [19], introducing an air gap in the FB configuration can alter the primary and secondary leakage inductances (L_{lp} and L_{ls}), where a larger L_{ls} provides a broader frequency control bandwidth. Furthermore, ref. [20] proposed a magnetic integration method to reduce L_{ls} in the FB configuration, thereby simplifying the resonant tank design and lowering AC losses. Beyond inductance values, the air gap also induces fringing flux, leading to additional copper losses (fringing loss) that cannot be accurately predicted by traditional one-dimensional (1D) analytical models. To address this, studies such as [21,22] employed Fourier series to model the magnetic field strength (H) distribution within the core window, allowing for the separation and accurate calculation of DC and AC loss components. While these studies have comprehensively optimized magnetic components and analyzed fringing effects, they have predominantly focused on the FB configuration or general loss models. However, in CT transformers, the air gap can induce an asymmetrical H-field distribution, leading to unequal leakage inductances for the positive (L_{l+}) and negative (L_{l-}) half-cycles. This specific phenomenon of leakage inductance asymmetry ($L_{l+} \neq L_{l-}$) and its impact on the converter's operation have not been systematically investigated in the previous literature.

In this work, the impact of asymmetrical leakage inductance distribution on the *LLC* resonant tank of a 380 V–12 V DC-DC converter is investigated. It is revealed that the H-field distribution is dependent on the assembly configuration of the winding, core, and air gap. Specifically, the position of the air gap significantly affects both L_{l+} and L_{l-}. Consequently, unequal L_{l+} and L_{l-} lead to divergent resonant frequencies during the positive and negative half-cycles, resulting in asymmetrical operations, particularly under light load conditions. To address this issue, the centralized assembly method is identified as the optimal configuration to ensure symmetrical L_{l+} and L_{l-} and facilitate balanced *LLC* operation.

The rest of this paper is organized as follows: The transformer design analysis for the 380 V–12 V high step-down DC-DC converter is presented in Section 2. The variations in the H-field distribution within the transformer, caused by the assembly method between

the winding and the core, and the asymmetrical leakage inductances, are investigated in Section 3. Experimental validations are illustrated in Section 4 and the following results and discussion are in Section 5. Finally, Section 6 summarizes the main conclusions of this paper.

2. Transformer Design for *LLC* Resonant High Step-Down Converter

2.1. System Architecture and Operational Principle

The schematic of the investigated 380 V–12 V *LLC* resonant converter is presented in Figure 1. The system comprises three main modules: an inverter, an *LLC* resonant tank, and a rectifier. From a topology perspective, as shown in Figure 1b,c, the rectifier can be configured as either FB or CT. The FB configuration allows each rectifier to withstand half the voltage stress, though it requires twice the number of devices compared to the CT configuration [23].

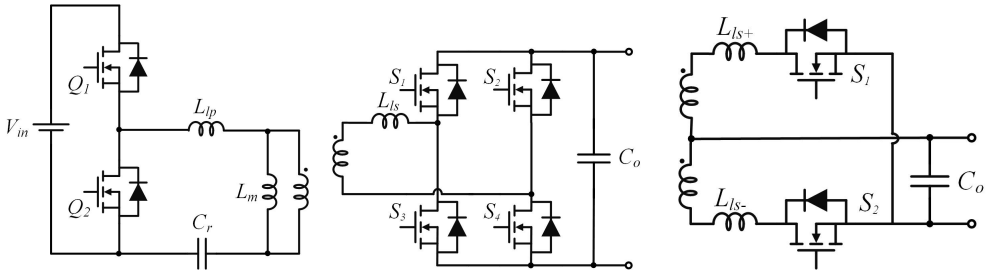


Figure 1. Configurations of the half-bridge *LLC* resonant converter: (**a**) primary side, (**b**) secondary side with FB, (**c**) secondary side with CT.

In the FB configuration, the total leakage inductance L_l is represented as:

$$L_l = L_{lp} + n^2 L_{ls} \tag{1}$$

where L_{lp} is the primary leakage inductance, L_{ls} is the secondary leakage inductance, and n is the turns ratio.

In contrast, for the CT configuration, L_l is divided into L_{l+} and L_{l-} for the positive and negative half-cycles, respectively, as given by:

$$L_{l+} = L_{lp} + n^2 L_{ls+} \tag{2}$$

$$L_{l-} = L_{lp} + n^2 L_{ls-} \tag{3}$$

2.2. Effect of Magnetizing Inductance on Converter Operation

Operating in DCX mode enables the *LLC* resonant converter to achieve optimal efficiency, since it maximizes energy delivery to the output while minimizing recirculation within the resonant tank. In this mode, the *LLC* converter's gain is fixed—independent of the inductance ratio (L_n) and quality factor (Q_e)—thus requiring no frequency regulation. However, L_m must still store sufficient magnetizing energy to discharge the primary switch output capacitance (C_{ds}) and ensure ZVS. The relationship between L_m and C_{ds} can be expressed as [24]:

$$t_{dead} \geq 32 \times C_{ds} \times f_{sw} \times L_m \tag{4}$$

where t_{dead} is the dead-time, f_{sw} is the switching frequency. To ensure ZVS is achieved within the fixed t_{dead}, L_m must be sufficiently small. Since f_{sw} and C_{ds} are constant, as (5)

shows, a smaller L_m generates a larger peak magnetizing current, which is required to fully discharge the C_{ds} before the switch turns on.

$$I_m = \frac{nV_o}{2fL_m} \tag{5}$$

L_m can be estimated using (6):

$$L_m = \frac{{N_p}^2}{R_c} \tag{6}$$

where N_p is the number of primary winding turns, R_c is the magnetic reluctance. According to (6), a higher step-down ratio (which requires a larger N_p for a given N_s) leads to a larger L_m. This presents a design conflict theoretically, as ZVS operation requires a sufficiently small L_m.

Based on the theoretical analysis above, the specific transformer parameters are selected. The target 380 V–12 V half-bridge converter requires a 16:1 transformer ratio. Assuming core PC200 EE 22/12/16 from TDK is selected, with key parameters shown in Table 1, the impact of the air gap is analyzed.

Table 1. Parameters of PC200 EE 22/12/16 core.

Key Parameters	Types or Value
Material	PC200
l_c	65 mm
B_s	530 mT
μ_r	800
A_c	79 mm^2
Window height	7 mm

The relationship between the air gap length l_g and the magnitude of L_m is depicted in Figure 2. When there is no air gap, L_m exceeds 400 µH, while L_l is less than 3 µH. This scenario is unsuitable, as the resulting high L_m is too large to achieve ZVS, and L_n is over 100. Consequently, an air gap is essential to reduce L_m to the required value for ZVS.

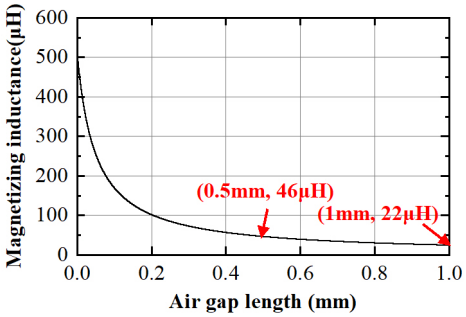


Figure 2. Relationship between air gap length and magnetizing inductance.

2.3. Impact of Leakage Inductance on Input Impedance Under Varying Load Conditions

According to Figure 1, based on the FHA, the input impedance of the *LLC* resonant network, denoted as $Z_{in}(j\omega)$ can be expressed as:

$$Z_{in}(j\omega) = j\omega L_r + \frac{1}{j\omega C_r} + \frac{j\omega L_m R_{ac}}{R_{ac} + j\omega L_m} \tag{7}$$

The equivalent AC resistance R_{ac} is related to the output load resistance R_L by the transformer turns ratio n:

$$R_{ac} = \frac{8n^2}{\pi^2} R_L \tag{8}$$

By combining (7) and (8), the frequency-dependent characteristics of Z_{in} under varying L_r and R_L conditions are illustrated in Figure 3. Here, the R_L range from 0.1 to 1 is selected to represent a comprehensive sweep from heavy load to light load conditions for theoretical analysis, and f_n is the normalized switching frequency defined as the ratio f_{sw}/f_r. As illustrated in this figure, the operation range is divided into two distinct regions. The ZVS region, as labeled in the figure, indicates that the input impedance of the LLC resonant tank exhibits inductive characteristics, which is the prerequisite for achieving ZVS operation. Several key observations can be made from these curves. First, figures indicate that heavier load conditions (e.g., $R_L = 0.1$) present a significantly narrower phase margin for ZVS. In this region, even a slight decrease in inductance or frequency could drive the operating point into the capacitive region, resulting in the loss of ZVS. Conversely, at lighter loads (Figure 3d), the phase rises steeply to highly inductive levels, making ZVS easily achievable.

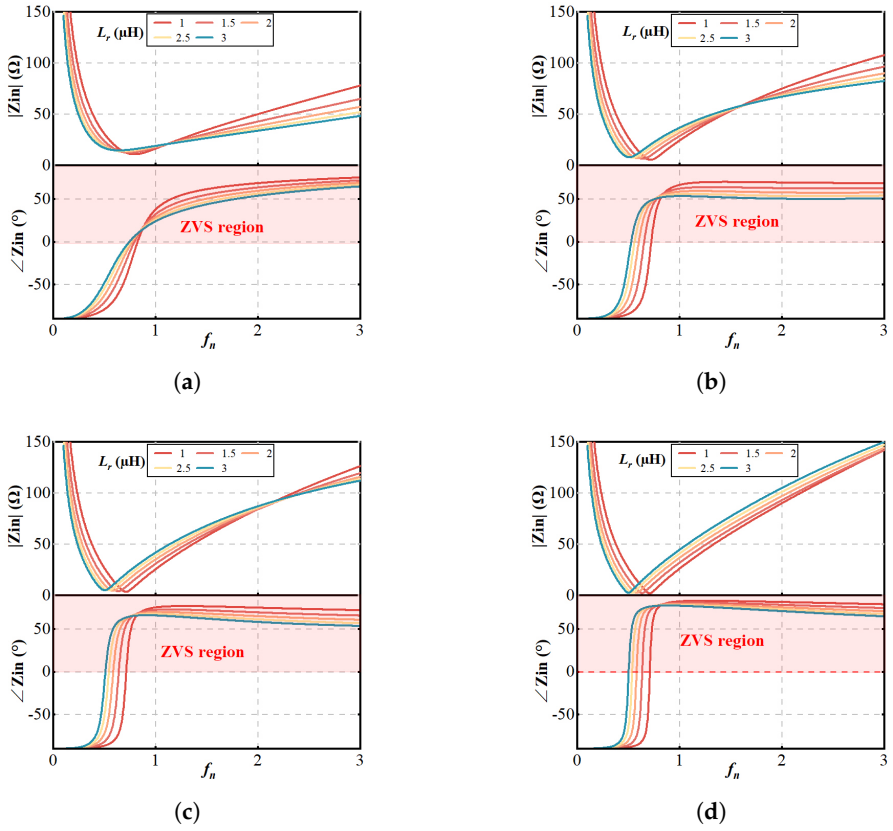


Figure 3. Impact of L_r on Input Impedance Characteristics under Various Load Conditions (R_L): (**a**) $R_L = 0.1$, (**b**) $R_L = 0.3$, (**c**) $R_L = 0.5$, (**d**) $R_L = 1$.

Second, regarding the sensitivity of the input impedance (Z_{in}) to L_r, the variation is notably more pronounced under light load conditions ($R_L = 1$, as shown in Figure 3d). Variations in L_r induce much larger deviations in the impedance magnitude $|Z_{in}|$ compared to the heavy load case. This implies that under light load conditions, the regulation of the converter gain is highly sensitive to the variations in L_r.

2.4. Effect of Winding Design on Leakage Inductance

For the 16:1 center-tapped (CT) transformer, a 4-layer PCB is used to physically separate the secondary windings for the positive and negative half-cycles. As depicted in Figure 4, the windings are arranged as follows:

- Secondary (Layer1 & Layer4): The single-turn positive half-cycle winding is on the top layer, and the single-turn negative half-cycle winding is on the bottom layer.
- Primary (Layer2 & Layer3): The primary winding is split into two 8-turn sections connected in series, placed on the second and third layers.

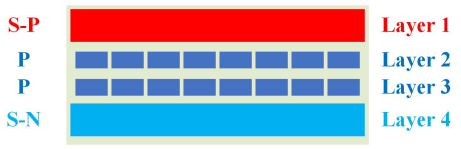


Figure 4. PCB winding arrangement.

This layout allows the secondary winding terminals to be tightly integrated with the synchronous rectifiers (SRs) and output capacitors, which is critical for minimizing the secondary-side commutation loop length.

The 1.6 mm height of the 4-layer PCB is significantly smaller than the 7 mm core window height of the selected EE core. This mismatch means the core window is not fully utilized, leaving substantial vertical space. This extra space permits flexibility in the PCB's placement relative to the core. Considering this, along with the PCB winding structure, three typical assembly methods for the EE core and two for the EI core are presented in Figure 5 and Figure 6, respectively. (Note: The material definitions and color coding labeled in Figure 5b apply to all sub-figures in both Figures 5 and 6).

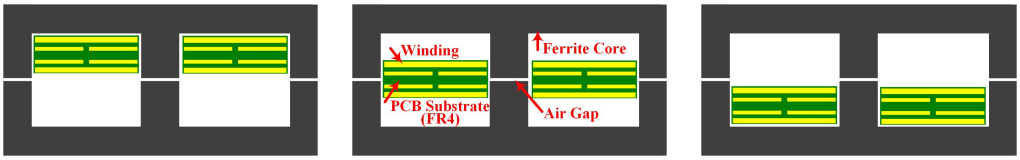


Figure 5. Assembling methods with EE core: (**a**) E core-winding-gap-E core, (**b**) E core-winding-air gap-winding-E core, (**c**) E core-air gap-winding-E core.



Figure 6. Assembling methods with EI core: (**a**) E core- winding-I core, (**b**) I core-winding-E core.

After introducing an air gap, the primary and secondary MMFs no longer fully cancel, as expressed by (9). This MMF imbalance ($\phi_m R_c$) creates an asymmetrical magnetic field (H) distribution within the core window.

$$N_p I_p - N_s I_s = \phi_m R_c \tag{9}$$

For example, in the assembly from Figure 5a, the H-field is zero on the top layer (adjacent to the core) but non-zero on the bottom layer, where the air gap is located. This leads to an MMF distribution that is asymmetrical for the positive and negative half-cycles, resulting in unequal leakage inductances (L_{l+} and L_{l-}). This asymmetry is highly undesirable in the CT configuration, where L_l is directly utilized for resonance, because

it creates two different resonant frequencies (f_{r+} and f_{r-}). This same issue applies to the configurations in Figures 5c and 6. Only the fully symmetrical assembly in Figure 5b ensures a balanced L_l distribution, as will be discussed next.

3. Analysis of MMF and Leakage Inductance

3.1. Theoretical Relationship Between Air Gap and MMF

When an air gap is introduced, a portion of the magnetic energy from the primary side is stored in L_m, resulting in the circulating energy in the *LLC* resonant tank and impacting the energy conversion efficiency. Using the First Harmonic Approximation (FHA) and the key parameters from Table 2, the MMF of the air gap can be derived from Faraday's law of induction as follows:

$$\Phi_m R_c = \frac{V_{Lm}}{4.44 \cdot f \cdot N_P} \cdot \frac{l_g}{\mu_0 A_c} = H_g l_g \tag{10}$$

Table 2. Parameters to calculate $\Phi_m R_c$.

Key Parameters	Types or Value
f	500 kHz
V_{Lm}	190 V
N_P	16
μ_r	800
A_c	79 mm^2

Thus, the direct relationship between l_g and its MMF is illustrated in Figure 7. Using the presented parameters, the calculated MMF across the air gap is 19.2 A·t for a 0.5-mm gap and 38.4 A·t for a 1-mm gap. This calculation reveals that with a 10-A secondary current, only around 21% of the primary current contributes to the power transfer to the output, while the majority circulates as the magnetizing current. These analytical findings were subsequently verified using circuit simulation software, which showed strong agreement.

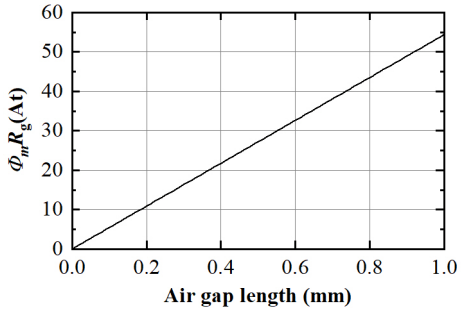


Figure 7. Relationship between the $H_g l_g$ and the l_g.

3.2. Zero Air Gap

When there is no air gap, the magnetic flux originating from the primary and secondary windings cancels completely within the core. As a result, H is considered to be zero throughout the entire magnetic circuit. For the PCB winding, the boundaries of the top and bottom layers, which are adjacent to the core, exhibit zero H.

For a 4-layer FR4 PCB, the core layer is much thicker than the prepreg layers. Thus, any stored leakage energy in the core layer will be the dominant factor in the total leakage inductance. In the zero air gap case, the H-field at the PCB boundaries (adjacent to the magnetic core) is zero. This boundary condition results in a perfectly symmetrical MMF distribution for both the positive and negative half-cycles, as shown in Figure 8. This figure depicts the half cross-sectional structure of the transformer. S_1 and S_2 denote the

secondary windings located on the top and bottom layers, which conduct during the positive and negative half-cycles, respectively. P_1 and P_2 represent the series-connected primary windings placed in the inner layers. By analyzing the MMF distribution across the prepreg and core layers, the internal H-field distribution of the transformer can be effectively derived.

Since this symmetrical MMF distribution exists within the dominant core layers, the stored magnetic energy is identical for both half-cycles. Therefore, equal leakage inductances (L_l+ and L_l-) are achieved.

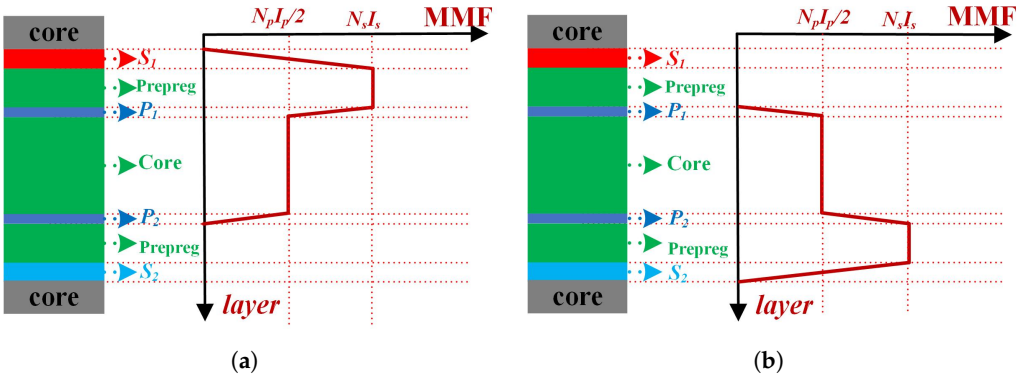


Figure 8. MMF distribution of EE core with zero air gap: (**a**) positive half-cycle, (**b**) negative half-cycle.

3.3. Non-Zero Air Gap

When the length of the air gap is non-zero, there will be a residual magnetic flux within the core. This residual flux signifies that the primary and secondary MMFs no longer cancel, which in turn alters the MMF distribution within the transformer window.

3.3.1. Assembly Method with Top Layer Adjacent to Core

As depicted in Figure 5, there are three types of assembly methods between the PCB windings and the core. If assembled as shown in Figure 5a, the MMF distribution can be derived as shown in Figure 9. The influence brought about by the air gap in (9) has caused a change in the distribution of MMF at the air gap region, leading to a non-zero H on the bottom layer bordering the air gap, and consequently resulting in an asymmetrical MMF distribution. Furthermore, the MMF in the core layer during the negative half-cycle is always greater than that in the positive half-cycle. As a result, the leakage energy during the negative half-cycle is theoretically greater than that during the positive half-cycle, leading to higher L_{l-}.

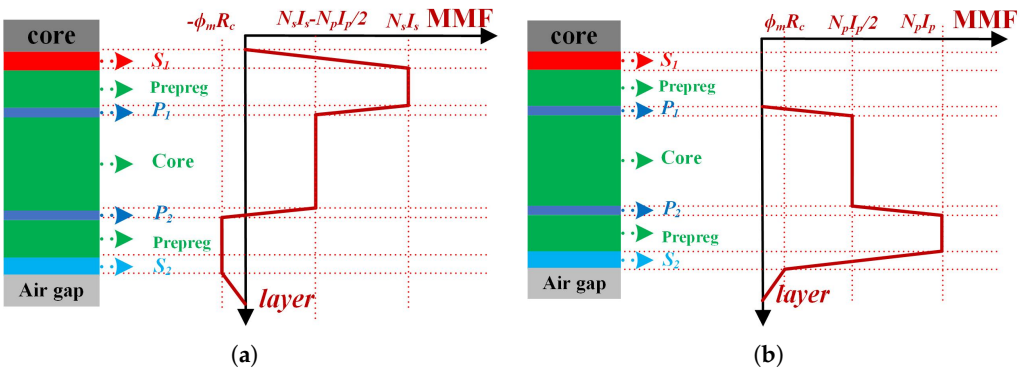


Figure 9. MMF distribution of EE core with non-zero air gap: (**a**) positive half-cycle, (**b**) negative half-cycle.

3.3.2. Assembly Method with Centralized Air Gap

For Figure 5b, the air gap is fully surrounded by the core layer, and its MMF distribution is shown in Figure 10. In the absence of an air gap, the H-field within the core layer is uniform. When an air gap is introduced in this central location, it alters the H-field distribution. However, this change is localized as a fringing field symmetrically around the gap. As a result, the H-field distribution remains symmetrical for both the positive and negative half-cycles. This symmetry is the critical factor that ensures equal leakage inductances (L_{l+} and L_{l-}).

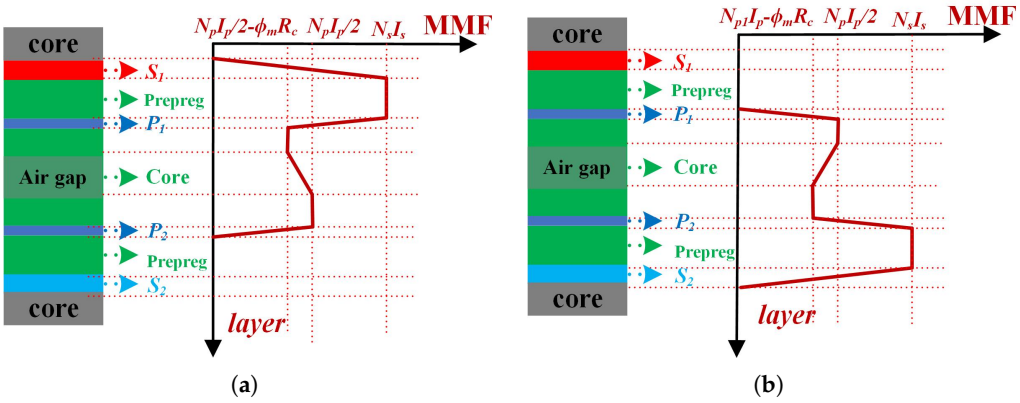


Figure 10. MMF distribution of EE core with centralized air gap: (**a**) positive half-cycle, (**b**) negative half-cycle.

3.3.3. Assembly Method with Bottom Layer Adjacent to Core

When the winding is assembled as shown in Figure 5c, its MMF distribution is a mirror image of the one in Figure 9. This configuration also results in an asymmetrical leakage inductance distribution between the positive and negative half-cycles.

3.4. EI Core

The analysis thus far has focused on EE cores. For an EI core, the air gap inherently creates asymmetrical H-field boundary conditions at the top and bottom layers. As a result, regardless of the PCB assembly method, an asymmetrical MMF distribution is unavoidable. This inevitably leads to unequal leakage inductances ($L_{l+} \neq L_{l-}$). Therefore, a Full-Bridge (FB) topology is required for an EI core with an integrated L_r, as it utilizes the total leakage inductance. The Center-Tapped (CT) configuration is fundamentally unsuitable in this case.

3.5. Analytical Modeling of Air Gap Impact on Leakage Inductance Distribution

Although the presence of the fringing flux increases the total copper loss, as presented in [22], for an EI core with different winding arrangement (e.g., SPP or PPS), only the 1D loss component changes, which means that the 1D loss model is sufficient to evaluate the effect of the winding arrangement on the total copper loss and the leakage inductance. Therefore, the analysis of the leakage inductance difference in this study relies only on the 1D loss model.

Several assumptions need to be made to simplify the modeling: the H-field is one-dimensional, varying only along the height direction (y-direction); the windings are assumed to be infinitely long; the core material has infinite magnetic permeability. Thus, the H-field distribution is constant within the non-source region and can be derived within the source region as follows [25]:

$$H_x(y) = \frac{H_1 \sinh(\gamma(h-y)) + H_2 \sinh(\gamma y)}{\sinh(\gamma h)} \tag{11}$$

where H_1 and H_2 denote the boundary values of the winding, x represents the horizontal coordinate within the cross-sectional area, h is the winding height, and $\gamma = \sqrt{j\omega\mu\sigma}$ is the complex propagation constant.

The stored magnetic energy within the core window can be given as:

$$E = \begin{cases} \int_0^{h_s} \frac{1}{2} \cdot \mu_0 \cdot H_x^2(y) \cdot l_w \cdot w_c \cdot dy & \text{(Source Region)} \\ \\ \frac{1}{2} \cdot \mu_0 \cdot H_x^2 \cdot l_w \cdot w_c \cdot h_{ns} & \text{(Non-source Region)} \end{cases} \tag{12}$$

where l_w and w_c are the length and width of the region; h_s and h_{ns} are the heights of the source and non-source regions, respectively. In the non-source region, H_x is constant.

Applying the boundary condition analysis from Figure 9 and summing all magnetic energy within the core window, the leakage inductance can be calculated from:

$$L_l = \frac{2E_{total}}{I_p^2} \tag{13}$$

where L_l is the leakage inductance referred to the primary side, E_{total} is the total stored magnetic energy in the core window, and I_p is the peak primary current.

Using the parameters from Table 3, the relationship between the secondary current and the leakage inductance difference $|L_{l+} - L_{l-}|$ is plotted in Figure 11. The 1D analytical model exhibits a limitation in this context. It is because this model assumes a constant MMF from the air gap, and the calculated inductance difference undesirably varies with the secondary current. To mitigate this effect, this analysis focuses on the high-current region where I_s is sufficiently large. Under this condition, the difference can be simplified as a constant value of approximately 0.2 µH.

Table 3. Key parameters to Calculate Leakage Inductance.

Parameter	Symbol	Value
Primary turns	N_p	16
Secondary turns	N_s	1
Switching Frequency	f_s	500 kHz
Core window width	w_c	6 mm
Air Gap MMF	$\Phi_m R_c$	25.7
Primary winding length	l_{wp}	504.7 mm
Secondary winding length	l_{ws}	63.3 mm
Core winding length	l_{wc}	63.3 mm
Primary section turns	N_{p1}	8

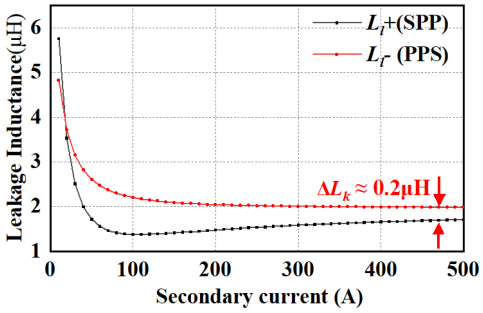


Figure 11. Relationship between the secondary current and the ΔL_l.

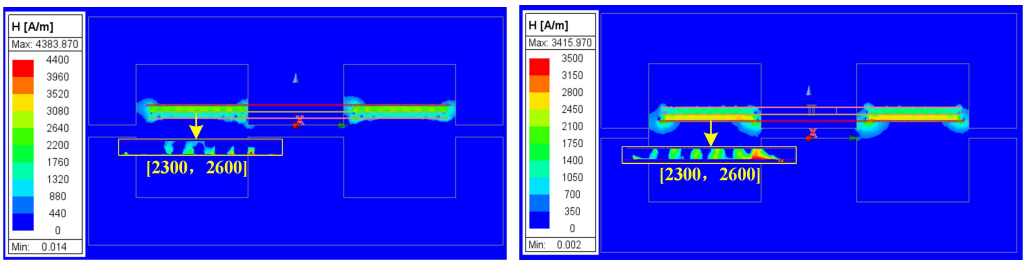
The modeling results show close agreement with the aforementioned MMF analysis. More importantly, as consistent with the previous analysis, this case significantly affects

the *LLC* operation, especially under light load conditions where the sensitivity is highest. Experimental verification of this phenomenon will be presented in the next section.

4. Simulated and Experimental Verification

4.1. Finite Element Analysis Verification

To further validate the analysis of asymmetrical L_{l+} and L_{l-}, a finite element analysis (FEA) simulation is conducted, with the top layer positioned adjacent to the core and the frequency set at 500 kHz. The simulated H distribution is presented in Figure 12. The regions with non-zero H correspond to the interior of the PCB structure. The distribution of the H-field magnitude directly reflects the profile of the stored magnetic field energy, thereby enabling the prediction of the leakage inductance value. As depicted, during the negative half-cycle, H within the range of 2300 to 2600 A/m displays a more uniform and widespread distribution compared to the positive half-cycle, consistent with the analytical findings discussed previously.



(**a**) (**b**)

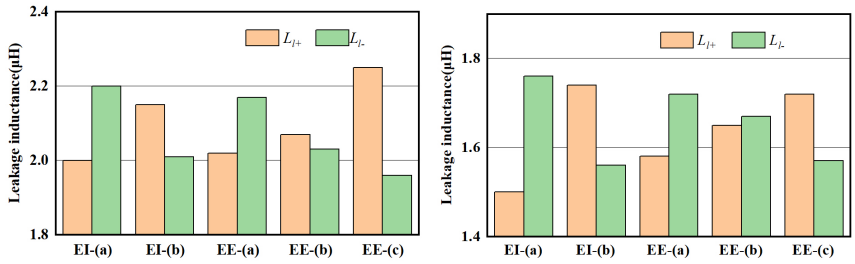
Figure 12. FEA simulation with top layer adjacent to core: (**a**) positive half-cycle, (**b**) negative half-cycle.

Based on theoretical analysis and FEA simulations, it is concluded that introducing an air gap in a CT transformer leads to an asymmetrical leakage inductance distribution. This asymmetry, which arises from improper assembly methods, negatively impacts the efficient operation of the *LLC* resonant converter.

4.2. Measurement Results of L_l with Various Assembly Methods

The FEA simulation has demonstrated that an asymmetrical leakage inductance distribution occurs when an incorrect assembly method is employed. To further investigate this analysis, 5 different assembly structures, as shown in Figures 5 and 6, have been considered. L_{l+} and L_{l-} were measured using the impedance analyzer, with the measured condition that the secondary side winding is shorted, along with the presence of the output filter capacitors.

As shown in Figure 13, the measured results demonstrate that the leakage inductance distribution is highly sensitive to the relative vertical position of the winding within the core window. Specifically, when the PCB winding is positioned adjacent to the top core leg, L_{l+} is observed to be smaller than L_{l-}. Conversely, placing the PCB winding adjacent to the bottom leg results in an opposite distribution. Meanwhile, centering the winding within the window yields nearly balanced values for L_{l+} and L_{l-}. This trend is consistent regardless of the core type (EE or EI), and the experimental data aligns well with the analytical predictions.



(**a**) 400 kHz (**b**) 1 MHz

Figure 13. Measured leakage inductance with 5 different assembly methods: (**a**) 400 kHz, (**b**) 1 MHz.

4.3. LLC Converter Demonstration

To investigate the impact of asymmetrical leakage inductance distribution in practical implementation, a hardware prototype of a 380 V–12 V DC-DC converter is built, as illustrated in Figure 14. The system integrates a high-voltage DC source for the input, a low-voltage DC source for the driver, a micro-controller for generating the driving signals, and a resistive load. Key waveforms are captured using a multi-channel oscilloscope connected to the designated measurement points on the prototype. The key parameters are summarized in Table 4.

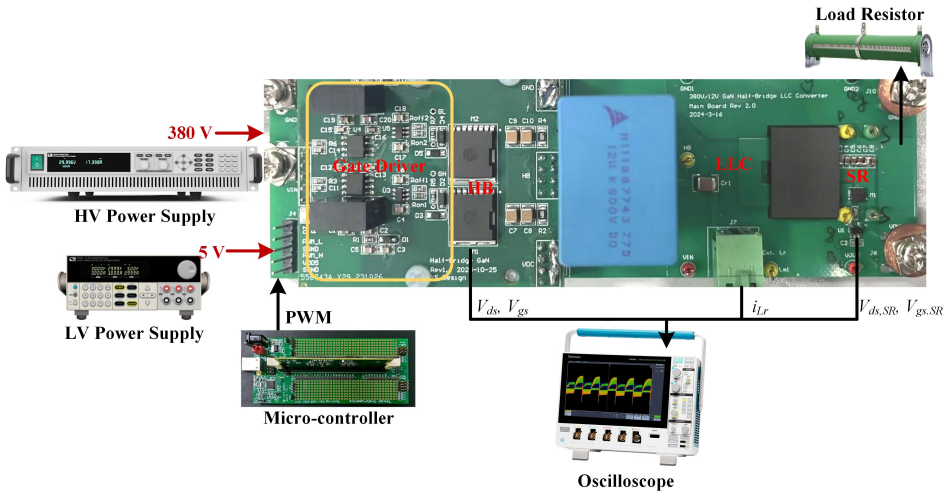


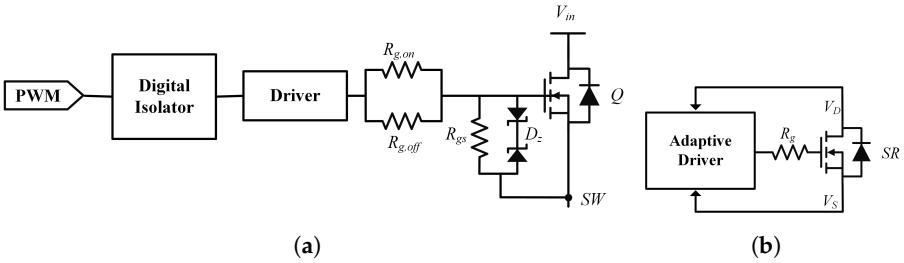
Figure 14. Experimental test bench setup.

Table 4. Key parameters of converter prototype.

Parameter	Symbol	Value
Core	-	PC200EE22/12/16
SR	-	IQE008N03LM5CG
SR driver	S_D	UCC24612
Primary switch	-	INN650D080BS
Primary driver	P_D	UCC27511
Input Voltage	V_{in}	380 V
Output Voltage	V_{out}	12 V
Switching Frequency	f_s	600 kHz
Capacitance	C_r	33 nF
Gap length	l_g	1 mm

The detailed schematic of the isolated gate-driver circuit is presented in Figure 15. The primary side adopts a two-stage driving scheme: a digital isolator (NSI8210) is used to provide galvanic isolation and high common-mode transient immunity, followed by a

high-speed low-side gate driver (UCC27511) to drive the GaN HEMTs. Asymmetrical gate resistors ($R_{g,on}$ and $R_{g,off}$) are employed to optimize the switching speed. On the secondary side, an adaptive driver method utilizing the UCC24612 is employed. It generates the drive signal by directly sensing the drain-source voltage (V_{DS}), which ensures precise ZVS timing and eliminates the need for the SR drive signal to be referenced to the primary ground.



(**a**) (**b**)

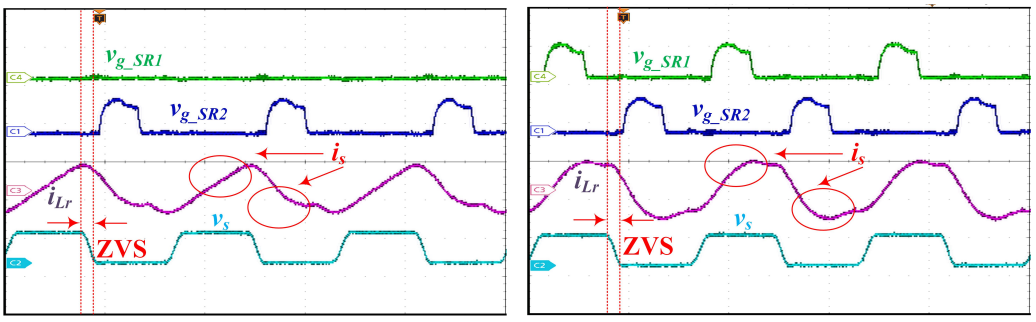
Figure 15. Schematic diagram of the implemented gate driving circuits. (**a**) Primary-side isolated driver circuit. (**b**) Secondary-side adaptive SR driver circuit.

Furthermore, based on the theoretical derivation in (4), the minimum required dead-time is calculated to be 66 ns by substituting the prototype parameters. In the practical implementation, a conservative dead-time of 200 ns is selected. This setting provides a sufficient safety margin to ensure the complete charging and discharging of the junction capacitance (C_{oss}), thereby guaranteeing reliable ZVS operation.

5. Results and Discussion

5.1. Asymmetrical Leakage Inductance

Firstly, the experimental results with the assembly method shown in Figure 5c are presented in Figure 16, with L_l directly serving as the resonant inductance. The leakage inductance is measured at 600 kHz, with the values of 1.8 µH and 1.6 µH for the positive and negative half-cycles, respectively. At light load (50 W), as depicted in Figure 16a, three distinct characteristics are observed: (1) ZVS is achieved for the primary switches; (2) the resonant current is asymmetrical; and (3) the synchronous rectifiers SR1 and SR2 cannot be driven simultaneously, with SR1 failing to turn on successfully during the positive half-cycle. These characteristics show some inconsistency with the previous analysis. When the power increases to 250 W, as shown in Figure 16b, ZVS is achieved, the resonant current i_{Lr} remains asymmetrical, and both SR1 and SR2 can be driven successfully, in contrast to the light load condition.



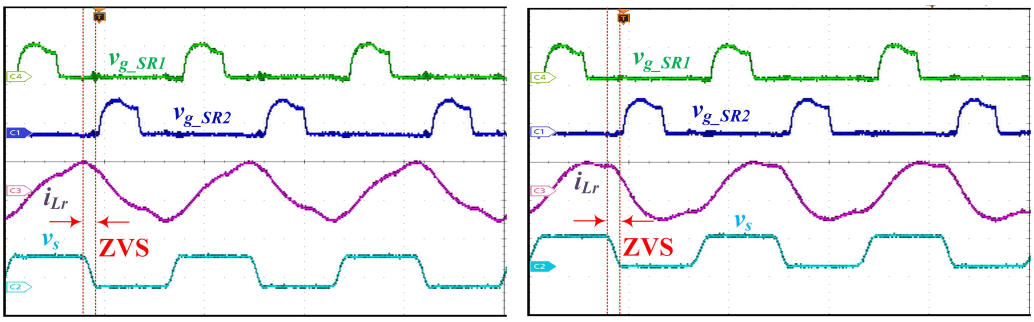
(**a**) 50 W (**b**) 250 W

Figure 16. Measured waveforms with asymmetrical leakage inductances: (**a**) light load, (**b**) heavy load. The time dimension is 1 µs/div. The vertical scales are v_{g_SR1} (10 V/div), v_{g_SR2} (10 V/div), i_{Lr} (1 A/div), and v_s (500 V/div).

Regarding (1), ZVS is primarily determined by sufficient magnetizing energy to discharge the C_{ds} of the switches, and by adjusting L_m, ZVS is achieved. For (2), as proposed in the aforementioned analysis, this assembly method can cause asymmetrical leakage inductance distribution, resulting in a varying input impedance of the *LLC* resonant tank and an asymmetrical i_{Lr}, as confirmed by experimental results. It is worth noting that throughout these tests, the switching frequency was strictly maintained at 600 kHz to ensure the ZVS margin; this confirms that the observed asymmetry is intrinsic to the transformer structure and independent of frequency fluctuations.

5.2. Symmetrical Leakage Inductance

The experimental results for the assembly method shown in Figure 5b are presented in Figure 17. At light load (50 W), as shown in Figure 17a, or at 250 W, as depicted in Figure 17b, ZVS is achieved with symmetrical i_{Lr}, and SR1 and SR2 are driven simultaneously. It can also be inferred that the correct assembly method, in addition to providing a symmetrical leakage inductance distribution to maintain an equal input impedance of the *LLC* resonant tank, also ensures stable operation of the *LLC* resonant converter.



(**a**) 50 W (**b**) 250 W

Figure 17. Measured waveforms with symmetrical leakage inductances: (**a**) light load, (**b**) heavy load. The time dimension is 1 µs/div. The vertical scales are v_{g_SR1} (10 V/div) , v_{g_SR2} (10 V/div), i_{Lr} (1 A/div), and v_s (500 V/div).

According to the analysis above, different assembly methods of the core and winding result in varying leakage inductance distributions, which alter the impedance of the *LLC* resonant tank and lead to different current distributions.

5.3. Analysis of Adaptive SR Misoperation Induced by Asymmetry

In this study, the selected SR has a low on-state resistance $R_{ds,on}$. The SR driver is adaptive, which generates the drive signal by detecting the voltage across the SR, with power supplied through the output terminal. In order to generate the normal drive signal V_{gs}, two necessary conditions must be fulfilled: (1) sufficient power supply, and (2) the attainment of the threshold voltage range, as shown in Table 5. In the experimental setup described above, the output voltage is 12 V, which is sufficient to fulfill (1). For (2), the voltage across the SR should be as given by:

$$V_{ds,on} = R_{ds,on} \cdot I_d \tag{14}$$

where $V_{ds,on}$ is the voltage across SR, I_d is the secondary load current. When the load current is 10 A, the on-state voltage is approximately 8.3 mV, which is close to the typical turn-off threshold voltage of the SR driver and causes the SR to be mistakenly turned off, leading to the body diode conducting instead. When the output current increases, the voltage across the SR becomes larger, enhancing its ability to provide the drive signal. As illustrated in Figure 17b, both SRs are successfully driven under the higher power rating.

To summarize, the symmetrical leakage inductance distribution is essential for the adaptive SR approach.

Table 5. Parameters of SR and SR driver.

Parameter	Symbol	Value
SR on-state resistance	$R_{DS(on),max}$	0.85 mΩ
Driver VG turn-on threshold	V_{THVGON}	−240 mV
Driver VG turn-off threshold	$V_{THVGOFF}$	−9 mV

6. Conclusions

Due to the high number of primary turns in the 380 V–12 V DC–DC converter, an air gap has to be introduced to reduce L_m and achieve ZVS. However, after introducing the air gap, H distribution within the transformer changes if the core window is not fully filled. In a CT configuration, it significantly affects both L_{l+} and L_{l-}, which in turn impacts the resonant frequency. To investigate the impact of different assembly methods for the air gap, core, and PCB winding on the leakage inductance distribution, 5 different assembly configurations are tested, utilizing both EE and EI cores. By investigating the MMF distribution of these assembly methods, the work concludes that only a fully centralized assembly method can ensure a symmetrical leakage inductance distribution. Both FEA simulations and impedance analyzer measured results have shown strong agreement with the theoretical analysis. Finally, a 380 V–12 V *LLC* converter prototype has been demonstrated and tested. The experimental results align closely with the analysis, providing valuable insights into the impact of assembly methods on the transformer parasitic parameters.

It is worth noting that this work primarily focuses on the impact of transformer parasitic parameters on the operation of the *LLC*. Although stable operation at 250 W has been verified, a detailed thermal analysis will be carried out in future work.

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