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Active Damping Control for the Modular Multi-Active-Bridge Converter

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Abstract

The modular multi-active bridge (MMAB) converter—characterized by electrical isolation, modular design, high power density, and high efficiency—can be readily scaled to multiple DC ports through an internal shared high-frequency bus (HFB), establishing it as a viable topology for DC transformer (DCT) applications. However, its interconnection to a DC grid via low-damping inductors may provoke low-frequency oscillations and instability. To mitigate this issue, this paper employs a pole-zero cancellation approach to model the conventional constant-power control (CPC) loop as a second-order system, thereby elucidating the relationship between equivalent line impedance and stability. An active damping control strategy based on virtual impedance is then introduced, supported by systematic design guidelines for the damping compensation stage. Simulation and experimental results confirm that under weak damping conditions, the proposed method raises the damping coefficient to 0.707 and effectively suppresses low-frequency oscillations—all without altering physical line impedance, introducing additional power losses or requiring extra sensing devices—thereby markedly improving grid-connected stability.

Keywords: modular multiple-active bridge; constant-power control; active damping control; stability; low-frequency oscillation suppression

1. Introduction

With the widespread application of distributed renewable energy sources (RESs), energy storage systems (ESSs), and DC loads, the DC microgrid has become a current research hotspot. To achieve interconnection between different DC sub-grids, power conversion is indispensable, where the DC transformer (DCT) can play a pivotal role.

Due to the advantages of high density, fast dynamic response, soft-switching ability, etc., dual-active-bridge (DAB) is considered as a popular base cell for DCT [1]. The series-parallel interconnection of multiple DABs enables the construction of high-voltage or high-power ports, thereby fulfilling the demands for flexible voltage and power scalability. However, DAB faces limitations in interconnecting more than two DC sub-grids, primarily due to the lack of a standardized internal bus architecture for port expansion. The multi-active-bridge (MAB) converter is regarded as a natural extension of the DAB, offering multiple ports to integrate distributed DC sources and loads. However, high operating frequencies increase the design and manufacturing challenges of its key component—the multi-winding high-frequency transformer (HFT) [2]. Additionally, the bulky multi-winding HFT limits the modularity and scalability of this topology. By replacing the multi-winding

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HFT in the MAB with multiple interconnected dual-winding HFTs coupled through a shared high-frequency bus (termed high-frequency-link), the MMAB converter (as shown in Figure 1) achieves not only electrical isolation and bidirectional power flow but also offers flexible submodule reconfiguration and scalable port expansion [3]. These distinctive features establish the MMAB as a front-runner topology for DCT implementation.

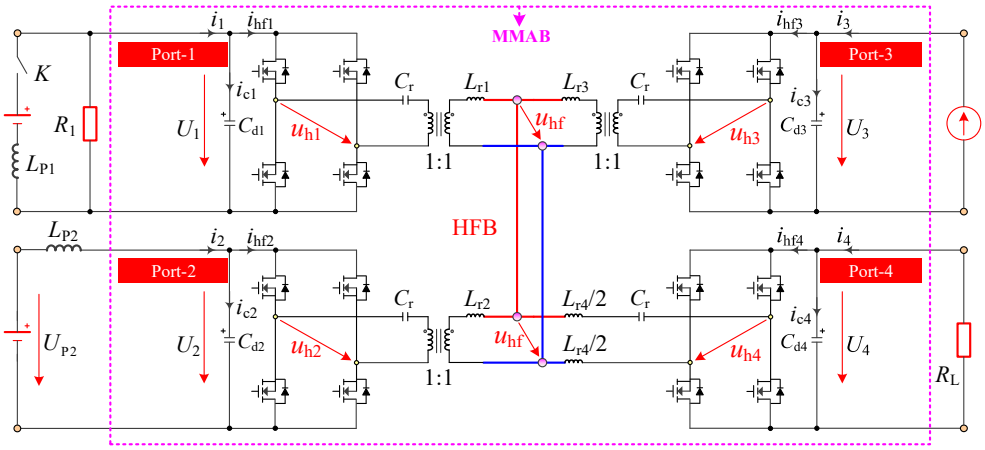


Figure 1. The four-port MMAB converter topology.

The absence of energy buffer capacitors in the MMAB converter results in highly coupled power flow among its ports, which has spurred significant research on decoupling control strategies to improve dynamic performance [4–7]. Although single-phase-shift (SPS) control is widely adopted for its simplicity, it suffers from reduced system efficiency under mismatched port voltage conversion ratios. To address this issue, [8–13] systematically analyzed the soft-switching characteristics of MMAB, and explored coordinated optimization approaches involving reactive power control, inductor peak current suppression, and DC bias elimination in inductor currents. In addition, high-frequency oscillations on the AC side of MMAB significantly increase voltage stress in the HFT, induce electromagnetic interference (EMI) and common-mode noise, and elevate losses due to waveform distortion [14,15]. To eliminate these high-frequency oscillations, an active harmonic elimination phase-shift modulation method was proposed in [15], it demonstrates easier implementation and no additional power losses compared with conventional passive voltage clamping methods.

In terms of stability enhancement, active damping control—as a method to dynamically increase damping without incurring additional real losses—has been extensively studied in DC microgrids and various types of power electronic converters. Common approaches include virtual resistance, capacitor current feedback, and bandpass-filter-based damping injection [16]. The core idea is to introduce virtual impedance within specific frequency bands through control algorithms, thereby suppressing resonance peaks and improving phase margin. However, existing active damping methods are primarily designed for conventional converter topologies, such as two-level voltage source converters (VSCs) [17]. In recent years, the LC-DAB system—a cascaded structure combining an LC filter with a DAB converter—has attracted considerable research interest. For example, Y. Guan et al. [18] augmented the conventional dual-loop control (output voltage and output current loops) with an additional input voltage loop. This not only stabilizes the input voltage but also acts as a parallel virtual resistance, reshaping the DAB-stage input impedance to positive values across the full frequency range and thereby improving system stability. Similarly, Y. Chen et al. [19] proposed a single voltage-loop control scheme for LC-DAB, introducing a series virtual impedance to reshape the DAB-stage input impedance

around the resonant frequency band. This method enhances stability while preserving dynamic performance, without the need for extra sensors. Nevertheless, these approaches mainly address the constant-output-voltage operation of DAB converters and do not fully explore scenarios requiring constant input-side current control. Moreover, the control structure in [18] is relatively complex due to its multiple loops, and the virtual impedance implementation in [19] is intricate and sensitive to model accuracy. The MMAB converter studied in this paper also interfaces with the grid or a DC source through an LC filter on its DC side. Like the LC-DAB system, it exhibits negative impedance behaviour under constant-power operation, leading to low-frequency oscillations and instability. However, because the MMAB features strong inter-port coupling and diverse operating modes across ports, its control strategy should remain simple. Consequently, existing active damping methods developed for LC-DAB systems are not directly suitable for this topology. To address these limitations, this paper proposes a simple and practical active damping strategy for the constant-power control (CPC) loop of the MMAB in grid-connected applications. A systematic parameter design procedure and stability analysis are also provided to ensure reliable operation under practical conditions.

The remainder of this paper is organized as follows. Section 2 presents the MMAB topology configuration and establishes its mathematical model. Section 3 analyzes the oscillation issues and root causes of instability in the conventional CPC loop. An active damping control strategy with a parameter design methodology is proposed in Section 4, and the effectiveness of the proposed strategy is validated through simulations and experiments in Section 5. Finally, the conclusion is drawn in Section 6.

2. Mathematical Model of the MMAB Converter

The four-port MMAB converter topology is illustrated in Figure 1. Each port integrates an MMAB submodule composed of an H-bridge and an HFT. These submodules are coupled through a shared high-frequency bus (HFB) operating above 20 kHz. Port-4 employs inductive coupling to the HFB instead of an HFT, thereby establishing galvanic isolation among all four ports [20]. Port-1 and Port-2 interface with DC voltage sources via filter inductors L_{p1} and L_{p2}, respectively, while Port-3 terminates at a constant-current load and Port-4 connects to resistive load R_L. To prevent HFT saturation, each submodule incorporates a DC-blocking capacitor C_r to eliminate magnetic bias [21]. All ports adhere to a symmetrical design principle: identical 1:1 HFT turn ratios. Port-1 is designated as the slack port to balance active power among all ports [22,23]. Port-2 operates in the constant-power (CP) mode, while Port-3 and Port-4 both function in the constant-voltage (CV) mode.

Using the single-phase-shift (SPS) modulation method [20], the DC side current i_{hfg} of Port-g (g = 2, 3, or 4) can be expressed as

$$i_{hfg} = -\frac{1}{U_g}\left(\frac{U_g U_1 D_{1-g}}{2 f_s L_{1-g}} + \sum_{k\neq 1,g} P_{k-g}\right) \quad g \neq 1 \tag{1}$$

$$P_{k-g} = \frac{U_g U_k \cdot D_{k-g}}{2 f_s \cdot L_{k-g}} \tag{2}$$

$$D_{k-g} = (d_g - d_k)\left(1 - \left|d_g - d_k\right|\right) \tag{3}$$

where f_s denotes the switching frequency, d_k and d_g represent the phase–shift ratios of the H-bridges in Port-k and Port-g, respectively, with $d_1 = 0$. P_{k-g} indicates the active power

transferred from Port-k to Port-g, and $L_{k\text{-}g}$ is the equivalent power transfer inductance between Port-k and Port-g [20].

$$L_{k-g} = L_{rk} L_{rg} \cdot \sum_{R=1}^{4} \frac{1}{L_{rR}} \tag{4}$$

The DC side of Port-2 satisfies

$$\begin{cases} U_{P2} = U_2 + L_{P2} \frac{di_2}{dt} + r_{P2} i_2 \\ i_2 = i_{hf2} + C_{d2} \frac{dU_2}{dt} \end{cases} \tag{5}$$

where r_{P2} is the equivalent series resistance (ESR) of inductor L_{P2}.

The small-signal model of Port-2 can be derived from Equations (1)–(5) as

$$\begin{cases} \hat{i}_{hf2} = -\left(\frac{U_1^* \hat{D}_{1_2}}{2 f_s L_{1_2}} + \sum_{k \neq 2} \frac{D_{k_2}^* \hat{U}_k}{2 f_s L_{k_2}} + \sum_{k \neq 1,2} \frac{U_k^* \hat{D}_{k_2}}{2 f_s L_{k_2}} \right) \\ \hat{i}_2(s) = \hat{i}_{hf2}(s) / \left(C_{d2} L_{P2} s^2 + C_{d2} r_{P2} s + 1 \right) \end{cases} \tag{6}$$

where the superscripts * and ˆ indicate the steady-state value and the deviation value, respectively.

3. Instability of the Conventional CPC Loop in the MMAB Converter

Based on Equation (6), a PI regulator is adopted for closed-loop control of the power flow through Port-2, with the implementation illustrated in Figure 2. The loop coefficient K_2 satisfies

$$K_2 = \frac{U_1^* U_2}{2 f_s L_{1_2}} \tag{7}$$

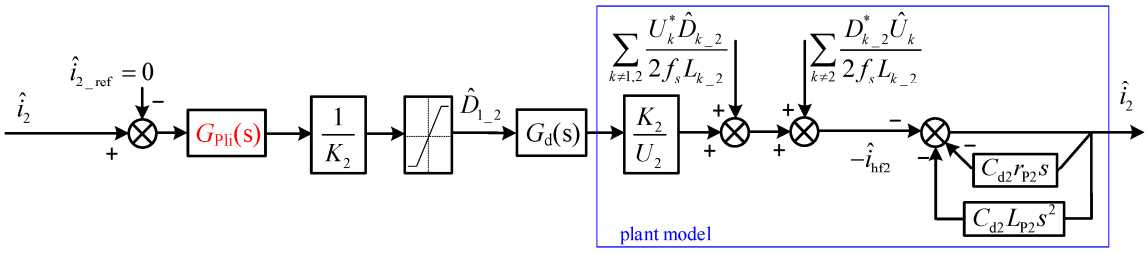


Figure 2. Block diagram of the conventional CPC loop for the four-port MMAB converter.

$G_{PIi}(s)$ and $G_d(s)$ are the transfer functions of the current regulator and delay element, respectively, expressed as

$$G_{PIi}(s) = K_{Pi} + K_{Ii}/s \tag{8}$$

$$G_d(s) = \frac{1}{1 + (T_{sd} + 0.5 T_{hd}) s} \tag{9}$$

where T_{sd} and T_{hd} represent the delay time and the hold time, respectively.

Then, the open-loop transfer function of the CPC loop can be derived as

$$\begin{cases} G_i(s) = \left(K_{Pi} + \frac{K_{Ii}}{s} \right) \frac{1}{1 + (T_{sd} + 0.5 T_{hd}) s} \frac{1}{K_2} \cdot G_{plant}(s) \\ G_{plant}(s) = \frac{K_2}{U_2} \frac{1}{C_{d2} L_{P2} s^2 + C_{d2} r_{P2} s + 1} \end{cases} \tag{10}$$

where $G_{plant}(s)$ is the transfer function of the plant.

When significant time delay exists in the control system, the delay element $G_d(s)$ must be taken into account [20]. To reduce the order of $G_i(s)$, a pole-zero cancellation method is

adopted in designing the current regulator, such that the zero of $G_{\mathrm{PIi}}(s)$ coincides with the pole of $G_{\mathrm{d}}(s)$, thereby ensuring the PI parameters satisfy

$$K_{\mathrm{Pi}}/K_{\mathrm{Ii}} = T_{\mathrm{sd}} + 0.5T_{\mathrm{hd}} \tag{11}$$

Consequently, the open-loop transfer function reduces to

$$G_{\mathrm{i}}(s) = \frac{K_{\mathrm{Ii}}}{s}\left(\frac{1}{U_2}\frac{1}{C_{\mathrm{d2}}L_{\mathrm{P2}}s^2 + C_{\mathrm{d2}}r_{\mathrm{P2}}s + 1}\right) \tag{12}$$

According to Equation (12), the phase crossover frequency of $G_{\mathrm{i}}(s)$ (corresponding to a phase of -180°), as illustrated in Figure 3, coincides with the resonant frequency of the plant, i.e.,

$$\omega_{-\pi} = \omega_{\mathrm{n}} = \frac{1}{\sqrt{L_{\mathrm{P2}}C_{\mathrm{d2}}}} \tag{13}$$

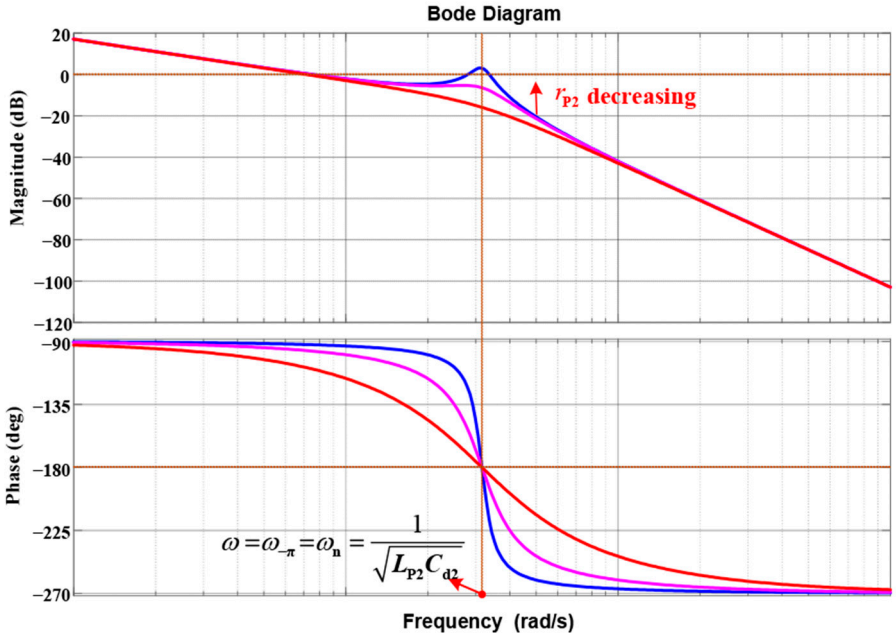


Figure 3. Bode plot of the open-loop transfer function of the conventional CPC loop.

Substituting Equation (13) into Equation (12) yields the gain margin of the control loop as

$$\gamma_{\mathrm{m}} = 20\lg\left(\frac{U_2}{K_{\mathrm{Ii}}} \cdot \frac{r_{\mathrm{P2}}}{L_{\mathrm{P2}}}\right) \tag{14}$$

From the Bode plot shown in Figure 3 and Equation (14), we observed that when the equivalent series resistance r_{P2} approaches zero or is small, the gain margin of the system decreases, and is prone to low-frequency oscillations near the natural resonant frequency of the LC network, potentially leading to control instability.

4. Active Damping Control of the MMAB Converter

To enhance the stability margin, r_{P2} should be increased to R_{P2} as follows:

$$R_{\mathrm{P2}} = r_{\mathrm{P2}} + r_{\mathrm{vir}} \tag{15}$$

where r_{vir} denotes the added damping resistance.

With the introduction of r_{vir}, the CPC loop is modified as shown in Figure 4. Compared with the conventional CPC loop in Figure 2, this is equivalent to adding a component $\Delta\hat{i}_{hf2}(s)$ to the current $\hat{i}_{hf2}(s)$, given by

$$\Delta\hat{i}_{hf2}(s) = C_{d2} r_{vir} s \cdot \hat{i}_2(s) \tag{16}$$

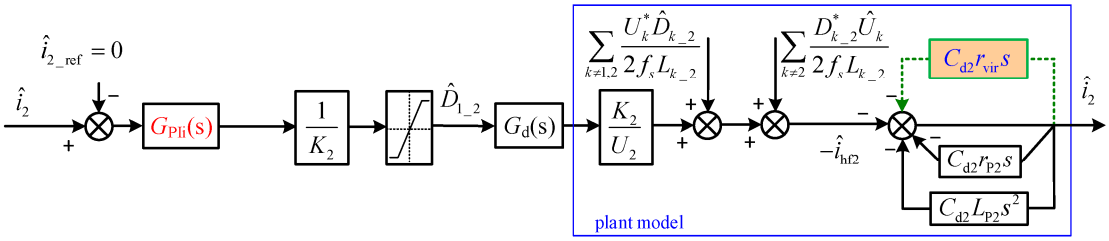


Figure 4. Block diagram of the CPC loop for the four-port MMAB converter with added damping resistance.

The added term $\Delta\hat{i}_{hf2}(s)$ can further be replaced by a feedforward compensation term $y_c(s)$, which satisfies

$$y_c(s) = C_{d2} U_2 r_{vir} s \cdot \hat{i}_2(s) \tag{17}$$

or, expressed in discrete form:

$$y_c = C_{d2} U_2 r_{vir} \cdot \frac{di_2}{dt} = C_{d2} U_2 f_s r_{vir} \cdot (i_2(k) - i_2(k-1)) \tag{18}$$

where $i_2(k)$ denotes the sampled dc-side current at the k-th control cycle.

This results in an active-damping CPC loop of the MMAB converter, illustrated in Figure 5. We observed that introducing the feedforward term y_c equivalently adds a virtual resistance into the control loop, thereby increasing the loop damping resistance and effectively improving system stability.

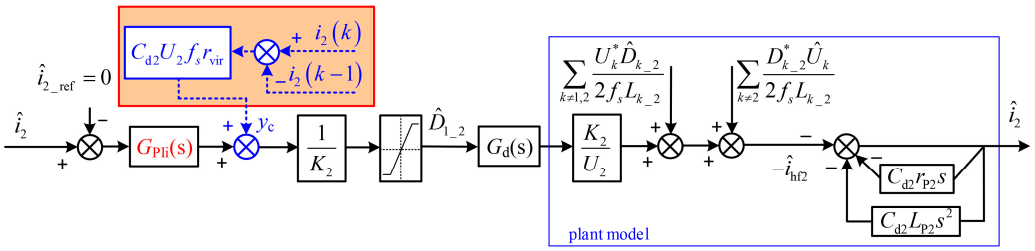


Figure 5. Block diagram of the proposed active-damping CPC loop for the four-port MMAB converter.

According to Figure 5, the open-loop transfer function of the active-damping CPC loop can be derived as

$$G_i(s) = \left(K_{Pi} + \frac{K_{Ii}}{s}\right) \frac{1}{1 + (T_{sd} + 0.5T_{hd})s} \left(\frac{1}{U_2} \frac{1}{C_{d2} L_{P2} s^2 + C_{d2} R_{P2} s + 1}\right) \tag{19}$$

Furthermore, by applying Equation (11) for zero-pole cancellation, it can be simplified as

$$G_i(s) = \frac{K_{Ii}}{s} \left(\frac{1}{U_2} \frac{1}{C_{d2} L_{P2} s^2 + C_{d2} R_{P2} s + 1}\right) \tag{20}$$

Figure 3 and Equation (20) demonstrate that under a constant DC-side voltage U_2, the integral gain coefficient K_{Ii} determines the gain crossover frequency of the open-loop transfer function, thereby directly influencing the system's dynamic response time.

Meanwhile, the gain margin is predominantly governed by the second-order term of the plant, i.e.,

$$G'_{\text{plant}}(s) = \frac{1}{C_{\text{d2}}L_{\text{P2}}s^2 + C_{\text{d2}}R_{\text{P2}}s + 1} \tag{21}$$

Therefore, stability design can be primarily addressed based on this second-order system, where the damping ratio ξ is defined as

$$\xi = \frac{R_{\text{P2}}}{2}\sqrt{\frac{C_{\text{d2}}}{L_{\text{P2}}}} \tag{22}$$

Setting $\xi = 0.707$ yields the virtual resistance r_{vir} as

$$r_{\text{vir}} = R_{\text{P2}} - r_{\text{P2}} = \sqrt{\frac{2L_{\text{P2}}}{C_{\text{d2}}}} - r_{\text{P2}} \tag{23}$$

As specified by Equation (14), the system's gain margin must satisfy

$$\gamma_{\text{m}} = 20\text{lg}\left(\frac{U_2}{K_{\text{Ii}}} \cdot \sqrt{\frac{2}{L_{\text{P2}}C_{\text{d2}}}}\right) > 6\text{dB} \tag{24}$$

Based on the parameter ranges defined by Equations (20), (23) and (24), combined with the key parameters specified in Table 1, the root locus, magnitude-frequency response, and phase-frequency response of the control loop are derived, as illustrated in Figure 6.

Table 1. Power circuit parameters.

Parameter	Value
DC side voltage reference U_{h_ref}	700 V
DC support capacitor $C_{\text{d1}}/C_{\text{d2}}/C_{\text{d3}}/C_{\text{d4}}$	2 mF
DC-blocking capacitor C_{r}	100 uF
Turn ratio of high-frequency transformer	1:1
Power transmission inductance $L_{\text{r1}}/L_{\text{r2}}/L_{\text{r3}}/L_{\text{r4}}$	3.2 μH
Port-2 DC side inductance L_{P2}, r_{P2}	100 μH, 50 mΩ
Port-1 DC side inductance L_{P1}, r_{P1}	300 μH, 3 mΩ
Switching frequency f_{s}	20 kHz
Control frequency f_{MMAB}	20 kHz

Figure 6a demonstrates the magnitude-frequency and phase-frequency responses of G_i(s) with $K_{Ii} = 2 \times 10^5$. When the series equivalent resistance $R_{P2} = 0$ or 0.02 Ω, the control loop's gain margin becomes negative, resulting in system instability. Increasing R_{P2} enhances relative stability, but persistent overshoot indicates insufficient damping. If a virtual resistor is introduced according to Equation (23), and an active damping compensation module is added as shown in Figure 5, the amplitude margin will be significantly increased.

Figure 6b–d demonstrate the control loop performance under varying parameters with virtual resistance integration. Figure 6b presents the root locus diagram of the control loop, it reveals that virtual impedance significantly increases the number of poles residing in the left-half plane (LHP), demonstrating enhanced closed-loop stability. According to Figure 6c, reducing K_{Ii} leads to increases in both gain margin and phase margin, thereby achieving enhanced closed-loop stability. Figure 6d demonstrates that a higher K_{Ii} leads to a bigger control loop bandwidth and faster dynamic response. However, as K_{Ii} rises, the system overshoot also increases correspondingly. Through comprehensive trade-offs between the relative stability of the control loop and the response speed, $K_{Ii} = 2 \times 10^5$ is ultimately selected, yielding a step response settling time of 12 ms.

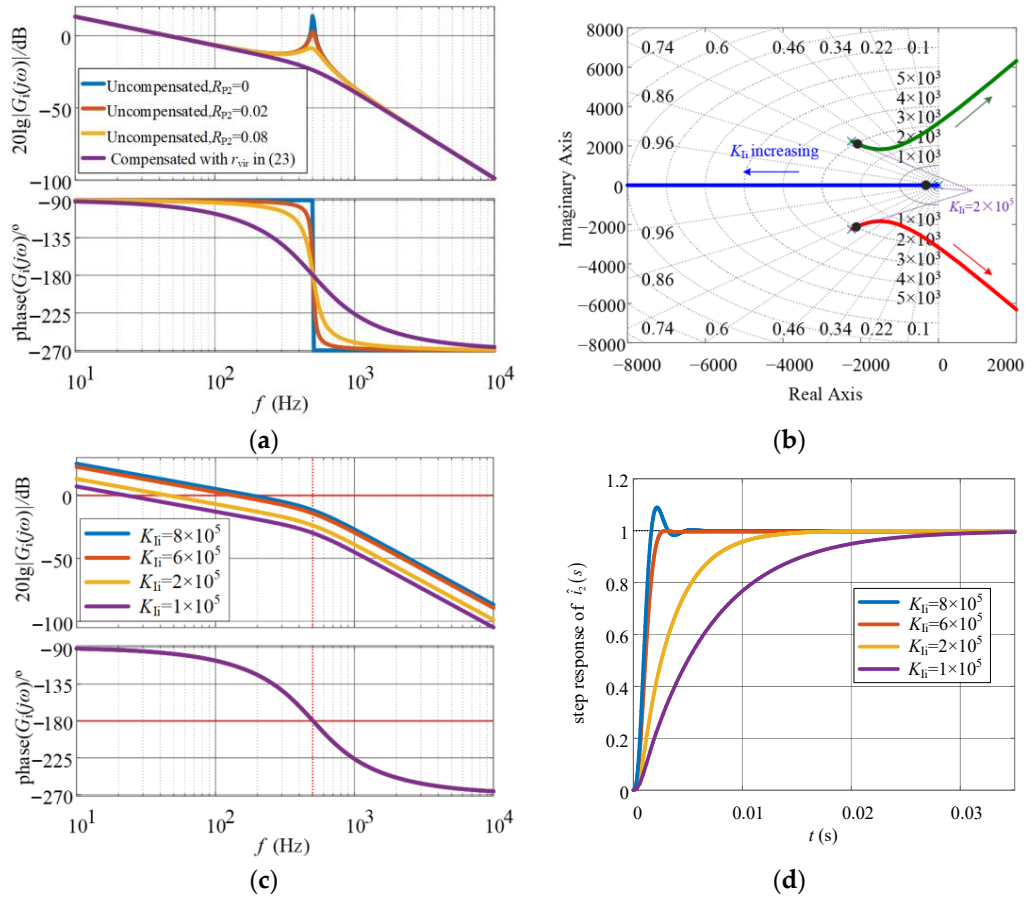


Figure 6. The active-damping CPC Loop performance characteristics under varying control parameters. (**a**) Bode plots of G_i(s) under varying damping resistance conditions. (**b**) Root locus of G_i(s)/(1 + G_i(s)) poles vs. K_{Ii}. (**c**) Bode plots of G_i(s) under varying values of K_{Ii}. (**d**) Step response curve of $\hat{i}_2(s)$.

5. Results

5.1. Simulation Results

Taking sudden load increase/decrease conditions as an example, the performance of the proposed control strategy is validated via simulation. The simulation settings are as follows: the input power of Port-3 and Port-4 remains constant at $P_3 = P_4 = -49$ kW. Prior to t = 0.1 s, the input power of Port-2 is P_2 = 98 kW (corresponding to i_2 = 140 A). At t = 0.1 s, the value of P_2 is abruptly reduced to 0 kW, and at t = 0.2 s, Port-2 is restored to P_2 = 98 kW.

As shown in Figure 7a, during the abrupt load increase/decrease at Port-2, the currents i_3 and i_4 remain constant, with i_4 being slightly lower than i_3. Since the DC voltage waveforms of Port-3 and Port-4 are nearly identical, only the voltage U_4 of Port-4 is displayed in Figure 7b, and the maximum fluctuation of U_4 is 3 V. Figure 7c illustrates a minor oscillation in i_2 during the sudden load changes, with a transition time of approximately 12 ms and a peak current fluctuation of 26 A, which closely match the design specification. The simulation results demonstrate that the proposed control strategy exhibits favourable dynamic performance under abrupt load variation conditions.

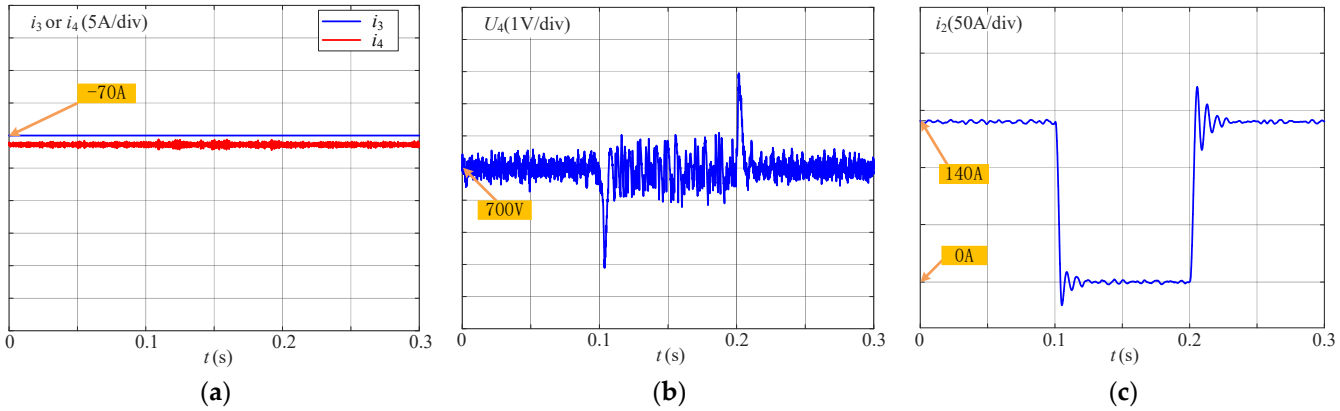


Figure 7. Dynamic performance simulation results of the proposed active-damping CPC strategy. (**a**) input currents of Port-3 and Port-4. (**b**) DC side voltage of Port-4. (**c**) input current of Port-2.

Figure 8 presents comparative simulation results under varying ESR conditions, and the current i_2 and voltage U_4 are illustrated in Figure 8a,b, respectively. The ESR r_{p2} is set successively to 0.02 Ω and 0.05 Ω, both corresponding to low damping coefficients. As observed from Figure 8, after introducing virtual impedance and adjusting the damping coefficient uniformly to 0.707, the control performance remains nearly identical despite the differences in the value of r_{p2}, and the system maintains stability. In contrast, when the virtual impedance is omitted, the control loop becomes unstable, and due to the limiter incorporated in the control loop, both voltage and current exhibit sustained constant amplitude oscillations.

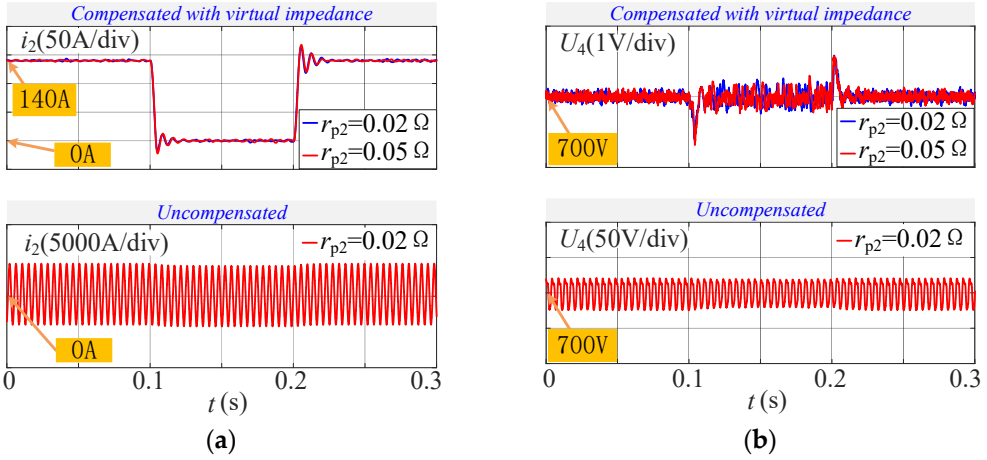


Figure 8. Comparative simulation results between the proposed active-damping CPC strategy (shown as "compensated with virtual impedance") and conventional CPC strategy (shown as "uncompensated") under low-ESR conditions. (**a**) Input current of Port-2. (**b**) DC side voltage of Port-4.

5.2. Experimental Results

The feasibility of the proposed control strategy is also validated using a hardware-in-the-loop (HIL) system. As shown in Figure 9, the power circuit model is implemented in the NI PXIe-7868R real-time simulator, while the controller is designed on a DSP-FPGA co-processing platform. Analogue and digital signal exchanges between the real-time simulator and the controller are facilitated by an I/O interface board, whose signals can be simultaneously monitored via a scopecorder. Key experimental parameters are listed in Table 1. Specifically, r_{p2} = 0.02 Ω, indicating that Port-2 exhibits weak damping characteristics, and the local load at Port-1 is R_1 = 19.6 Ω. The initial experimental conditions are

defined as: Port-1 and Port-2 are normally grid-connected, with Port-2, Port-3, and Port-4 having input powers of P_3 = 105 kW, $P_2 = P_4$ = 0 kW, respectively.

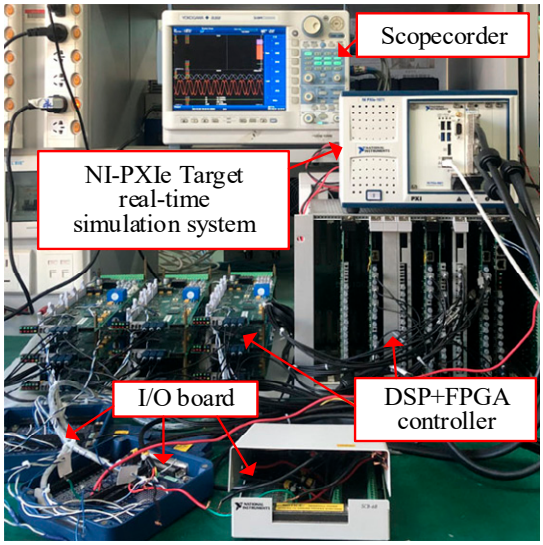


Figure 9. HIL experimental platform.

As shown in Figure 10, current i_2 and voltage U_4 exhibit significant oscillations under the conventional CPC strategy, attributed to the weak damping characteristic of Port-2, which closely matches the simulation results illustrated in Figure 8.

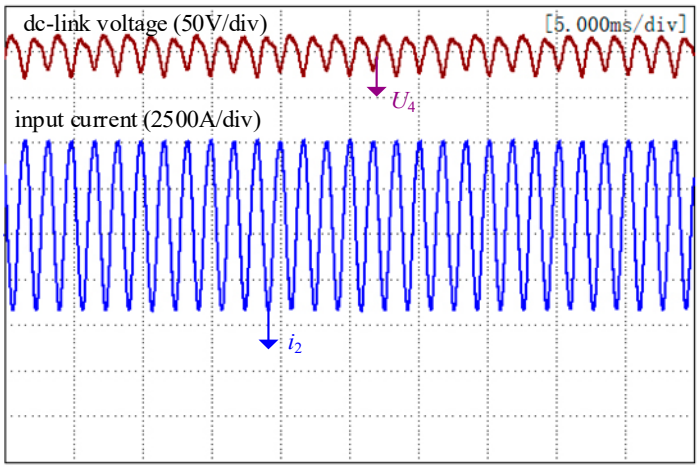


Figure 10. Experimental results of the conventional CPC strategy under low-ESR conditions.

Figure 11 presents experimental results of the proposed active-damping CPC strategy. As shown in Figure 11a, prior to time t_1, all four ports are able to operate stably at their preset power points under low-ESR conditions—a capability unattainable with the conventional CPC strategy. At t_1, the breaker of Port-1 is opened, causing the slack port (i.e., the port operating in power-following mode) of the MMAB to shift from Port-1 to Port-2. Consequently, Port-1 only supplies its local load R_1, while Port-2 switches from constant-power mode to power-following mode to balance the real-time active power among all ports. The experimental results show that the input power of Port-2 abruptly changes from 0 kW to −80 kW, the transition lasts about 8 ms, the current i_2 exhibits an overshoot of approximately 35 A, and the voltage U_4 fluctuates by about 10 V.

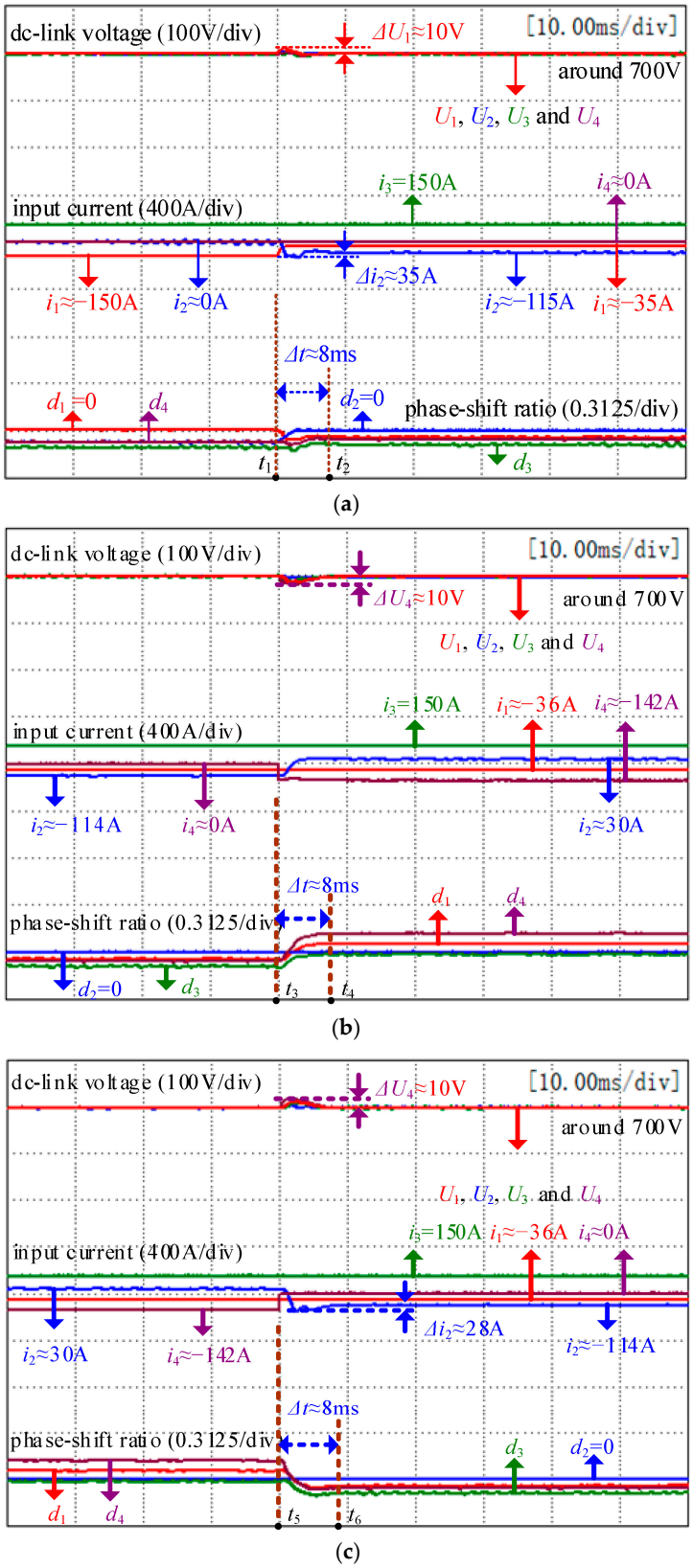


Figure 11. Experimental results of the proposed active-damping CPC strategy under low-ESR conditions. (**a**) Slack port switching from Port-1 to Port-2. (**b**) P_4 step changing from 0 kW to −100 kW. (**c**) P_4 step changing from −100 kW to 0 kW.

Furthermore, a step load-change test is performed on Port-4. Figure 11b shows the case when P_4 steps from 0 kW to −100 kW, and Figure 11c shows the case when P_4 steps

back from −100 kW to 0 kW. In both scenarios, the transition duration is around 8 ms, with an i_2 overshoot of about 28 A and a U_4 fluctuation of about 10 V.

We observed that the experimental results demonstrate good agreement with the simulations, confirming that the proposed active-damping CPC strategy exhibits significantly enhanced performance over the conventional CPC strategy.

6. Conclusions

This paper presents an active damping-based constant power control strategy for the MMAB converter interfacing with DC grids or other DC sources. A comprehensive analysis and systematic design methodology are developed for both controller parameters and active damping networks. Simulation and experimental results demonstrate that the proposed control strategy exhibits superior dynamic performance, featuring fast transient response during load steps with minimal voltage/current overshoot. The introduced active damping effectively suppresses low-frequency oscillations and stabilizes system dynamics, successfully addressing instability issues caused by insufficient port damping. However, the study still has certain limitations that require further investigation. Firstly, the design of the virtual damping relies on the parameters of the plant model and currently lacks adaptive capability. Secondly, the adaptability of the method under severe multi-port power transients or asymmetric parameter conditions, as well as the overall stability of the MMAB, still need to be further verified.

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