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An Enhanced CDSC-Based Grid Parameter Estimation Method for Distorted Grids

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Abstract

In modern power systems, DC offset and odd-order harmonics degrade grid phase and frequency estimation accuracy. To address this problem, this paper proposes an enhanced grid parameter estimation scheme based on cascaded delayed signal cancellation (CDSC). Unlike the conventional CDSC, the proposed method introduces a redesigned delay configuration, significantly reducing the inherent filtering delay while preserving the rejection capability for the DC component and targeted odd-order harmonics. Meanwhile, an amplitude-phase compensation strategy is developed to correct the magnitude attenuation and phase distortion introduced by the CDSC filter, which allows accurate extraction of the fundamental grid component. Furthermore, a frequency-adaptive module is integrated to maintain stable grid synchronization under off-nominal frequency deviations. Finally, experimental results verify the effectiveness of the proposed method.

Keywords: cascaded delayed signal cancellation; harmonic rejection; DC offset suppression; phase-locked loop

1. Introduction

In single-phase grid-connected converter systems, grid voltages at the point of common coupling are often distorted by low-order odd harmonics caused by nonlinear loads, converter switching actions, and grid disturbances. Moreover, measurement imperfections such as sensor bias, signal acquisition errors, and non-ideal analog-to-digital conversion processes may introduce DC offset into the measured voltage signals [1–4]. The presence of such disturbances can significantly affect the accuracy of grid synchronization and degrade the overall control performance of grid-connected converters.

As a result, the practical input signal used for control and synchronization often contains both a DC offset and dominant odd-order harmonics. The coexistence of these distortions poses significant challenges to accurate fundamental component extraction, which is essential for reliable phase tracking and frequency estimation [5,6]. Existing methods for fundamental and harmonic detection in single-phase systems can be broadly classified into frequency-domain and time-domain approaches.

Frequency-domain techniques, such as the discrete Fourier transform (DFT) and recursive DFT (RDFT) [7,8], provide high steady-state accuracy in harmonic analysis. However, the conventional DFT is limited to periodic steady-state signals and is susceptible to spectral leakage and the picket-fence effect under non-ideal conditions, such as grid

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Academic Editors: Pavlos S. Georgilakis and Jianyu Zhou

Received: 30 June 2026
Revised: 26 July 2026
Accepted: 17 August 2026
Published: 18 August 2026

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voltage distortion and frequency deviations. In addition, these methods require at least one fundamental cycle of data, resulting in inherent detection delay. When multiple harmonic components are extracted simultaneously, the computational burden further increases, limiting their applicability in real-time grid-connected control [9,10].

Beyond frequency-domain methods, alternative techniques such as wavelet transform [11–14], Kalman filtering [15,16], and the Hilbert transform [17,18] have also been applied to harmonic analysis. Although these methods can achieve satisfactory estimation performance under certain conditions, they generally involve relatively high computational complexity, challenging parameter tuning, or limited dynamic response.

Time-domain detection methods mainly include zero-crossing detection, adaptive notch filtering, and phase-locked loop (PLL) techniques [19–21]. Zero-crossing detection features a simple structure but suffers from slow dynamic response and high sensitivity to grid harmonics and high-frequency noise. Adaptive notch filtering can track grid frequency variations; however, it is limited by its relatively slow convergence and complex parameter tuning [22–24]. PLLs are widely recognized as the core technique for phase detection in single-phase systems. Due to the availability of only a single input signal, a quadrature signal generator (QSG) is required to construct orthogonal components for vector decoupling and PLL operation. Existing QSG implementations include both closed-loop and open-loop approaches, such as transport delay, Hilbert transform, and the second-order generalized integrator (SOGI) [25–28]. However, under severe harmonic distortion, the generated quadrature signal may exhibit waveform distortion, which degrades PLL performance. To mitigate this issue, auxiliary filters are often cascaded with the QSG; nevertheless, conventional fixed-parameter filters generally lack adaptability to complex and time-varying harmonic conditions.

The delayed signal cancellation (DSC) method enables selective harmonic filtering [29–32]. Originally developed for three-phase systems, the DSC method requires prior signal vectorization when applied to single-phase systems. To address this, ref. [32] proposed an anti-conjugate decomposition (ACD)-based cascaded DSC (CDSC) method, in which the single-phase signal is reformulated as an $\alpha\beta$-frame vector. By cascading multiple DSC stages, harmonic components can be effectively eliminated.

Compared with conventional PLLs relying on quadrature signal generation, the ACD-CDSC operates in an open-loop manner, achieving fast convergence within one fundamental cycle and zero steady-state error. However, the conventional CDSC design (CDSC-I) employs five DSC stages, resulting in a relatively large delay of 0.97 cycles. To reduce this delay, a second configuration (CDSC-II) was proposed in [32], which shortens the delay to 0.47 cycles but sacrifices DC offset suppression, making it unsuitable for grid conditions with DC components.

To address these challenges, this paper develops an enhanced CDSC-based method for distorted grid parameter estimation. By redesigning the delay configuration of the conventional CDSC, the proposed method reduces the detection delay from 0.97 cycles to 0.5 cycles while maintaining effective suppression of DC offset and dominant odd-order harmonics. In addition, an amplitude and phase compensation scheme is introduced based on the redesigned CDSC structure to ensure accurate fundamental estimation, and a frequency-adaptive mechanism is incorporated to enhance robustness under grid frequency deviations. Experimental results validate the effectiveness of the proposed method.

The rest of the paper is organized as follows: Section 2 introduces the signal vectorization method and the principle of the CDSC operator. Section 3 presents the proposed enhanced CDSC-based detection system. Section 4 provides experimental validation results. Finally, Section 5 concludes the paper.

2. Signal Vectorization and CDSC Principle

In this section, the signal vectorization method based on ACD is first introduced for distorted single-phase grid signals. Then, the definition and frequency characteristics of the DSC operator are presented in detail. Finally, the CDSC structure is described for selective harmonic extraction and forms the basis for the proposed detection scheme.

In practical single-phase grid-connected applications, the grid voltage at the point of common coupling is often affected by DC offset and low-order odd harmonics. Such a voltage can be generally expressed as

$$v(t) = V_0 + \sum_{h=1}^{H} v_h(t) = V_0 + \sum_{h=1}^{H} V_h \sin(h\omega t + \phi_h) \tag{1}$$

where V_0 denotes the DC offset component, h is the harmonic order, $\omega = 2\pi f$ is the angular frequency, V_h and ϕ_h are the amplitude and initial phase of the h-th harmonic, respectively, and H is the highest harmonic order considered.

In practical grid-connected converter systems, the harmonic spectrum is typically dominated by low-order odd harmonics due to converter switching actions and nonlinear loads; among them, the 5th, 7th, 11th, and 13th harmonic components are usually the most significant.

To enable the application of three-phase vector filtering techniques to single-phase systems, the signal is reformulated using a complex exponential representation. For a single harmonic component

$$v_h(t) = V_h \sin(h\omega t + \phi_h)$$

its decomposition based on Euler's formula is given by

$$v_h(t) = \frac{V_h}{2j}\left(e^{j(h\omega t+\phi_h)} - e^{-j(h\omega t+\phi_h)}\right) \tag{2}$$

where j denotes the imaginary unit.

Based on the ACD concept, a vector in the $\alpha\beta$-stationary frame is constructed as

$$\mathbf{v}_{\alpha\beta}(t) = \begin{bmatrix} 0 \\ v_h(t) \end{bmatrix} \tag{3}$$

which can be equivalently expressed in complex form as $0 + jv_h(t)$. Substituting (2) into this formulation yields

$$\mathbf{v}_{\alpha\beta}(t) = \underbrace{\frac{V_h}{2}e^{j(h\omega t+\phi_h)}}_{\mathbf{v}_{\alpha\beta}^{+h}(t)} + \underbrace{\left(-\frac{V_h}{2}e^{-j(h\omega t+\phi_h)}\right)}_{\mathbf{v}_{\alpha\beta}^{-h}(t)} \tag{4}$$

where $\mathbf{v}_{\alpha\beta}^{+h}(t)$ and $\mathbf{v}_{\alpha\beta}^{-h}(t)$ denote a pair of oppositely rotating components in the $\alpha\beta$ frame, corresponding to counterclockwise and clockwise rotations, respectively. It should be noted that these components do not represent symmetrical sequence components as defined in three-phase systems, but are mathematical constructs obtained via the ACD process.

Expanding the complex exponentials into trigonometric form, the $\alpha\beta$-frame representation of the two rotating components can be explicitly written as

$$\mathbf{v}_{\alpha\beta}^{+h}(t) = \frac{V_h}{2}\begin{bmatrix} \cos(h\omega t + \phi_h) \\ \sin(h\omega t + \phi_h) \end{bmatrix} \tag{5}$$

$$\mathbf{v}_{\alpha\beta}^{-h}(t) = -\frac{V_h}{2}\begin{bmatrix}\cos(h\omega t + \phi_h)\\ -\sin(h\omega t + \phi_h)\end{bmatrix} \tag{6}$$

The superposition of these two components yields

$$\mathbf{v}_{\alpha\beta}^{+h}(t) + \mathbf{v}_{\alpha\beta}^{-h}(t) = \begin{bmatrix}0\\ V_h\sin(h\omega t + \phi_h)\end{bmatrix} = \begin{bmatrix}0\\ v_h(t)\end{bmatrix} \tag{7}$$

which confirms that the ACD-based vectorization reconstructs the original single-phase signal without information loss.

The DSC operator is employed to extract the fundamental component from the vectorized signal. It is a linear vector filter defined in the $\alpha\beta$-frame. For ACD-based vectors, the DSC operator with delay factor n targeting harmonic order h^* is defined as

$$\mathrm{DSC}_n^{h^*}\left[\mathbf{v}_{\alpha\beta}(t)\right] = \frac{1}{2}\left[\mathbf{v}_{\alpha\beta}(t) + \mathbf{R}(\theta_r)\,\mathbf{v}_{\alpha\beta}\left(t - \frac{T}{n}\right)\right] \tag{8}$$

where T is the fundamental period, and $\mathbf{R}(\theta_r)$ is the rotation matrix given by

$$\mathbf{R}(\theta_r) = \begin{bmatrix}\cos\theta_r & \sin\theta_r\\ -\sin\theta_r & \cos\theta_r\end{bmatrix}, \quad \theta_r = -\frac{2\pi h^*}{n} \tag{9}$$

To analyze its filtering characteristics, a unity-amplitude forward-rotating harmonic vector is considered

$$\mathbf{v}_{\alpha\beta}^{(h)}(t) = \begin{bmatrix}\cos(h\omega t + \phi_h)\\ \sin(h\omega t + \phi_h)\end{bmatrix} \tag{10}$$

After substitution and simplification, the output becomes

$$\mathrm{DSC}_n^{h^*}\left[\mathbf{v}_{\alpha\beta}^{(h)}(t)\right] = \cos\left(\pi\frac{h-h^*}{n}\right)\begin{bmatrix}\cos\left(h\omega t + \phi_h + \pi\frac{h^*-h}{n}\right)\\ \sin\left(h\omega t + \phi_h + \pi\frac{h^*-h}{n}\right)\end{bmatrix} \tag{11}$$

Thus, the magnitude gain and phase shift are obtained as

$$G_n^{h^*}(h) = \left|\cos\left(\pi\frac{h-h^*}{n}\right)\right| \tag{12}$$

$$\Delta\phi_n^{h^*}(h) = -\pi\frac{h-h^*}{n} \tag{13}$$

From (12), the magnitude gain becomes zero when $\cos(\pi(h-h^*)/n) = 0$, i.e., $h = h^* + \left(k+\frac{1}{2}\right)n$, and unity when $h = h^* + kn$, where k is an integer. Accordingly, parameters n and h^* can be properly designed to retain the target harmonic and eliminate unwanted harmonics.

In distorted grid conditions, where multiple odd-order harmonics and DC offset coexist, a single DSC stage is insufficient to achieve satisfactory filtering performance. Therefore, multiple DSC stages are cascaded to form the CDSC, which enhances the overall harmonic rejection capability through the combined effect of individual stages:

$$\mathrm{CDSC}\left[\mathbf{v}_{\alpha\beta}(t)\right] = \mathrm{DSC}_{n_1}^{h_1^*} \circ \mathrm{DSC}_{n_2}^{h_2^*} \circ \cdots \circ \mathrm{DSC}_{n_m}^{h_m^*}\left[\mathbf{v}_{\alpha\beta}(t)\right] \tag{14}$$

where ∘ denotes series composition. Since the DSC operator is linear and time-invariant, the overall magnitude gain and phase shift are given by

$$G_{\text{total}}(h) = \prod_{i=1}^{m} \left| \cos\left(\pi \frac{h - h_i^*}{n_i} \right) \right| \tag{15}$$

$$\Delta\phi_{\text{total}}(h) = -\sum_{i=1}^{m} \pi \frac{h - h_i^*}{n_i} \tag{16}$$

By properly designing the parameter set $\{(n_i, h_i^*)\}$, the CDSC can effectively retain the target harmonic while significantly attenuating other harmonics and the DC offset. This formulation lays the theoretical foundation for the proposed CDSC-based fundamental detection method.

3. Proposed Enhanced CDSC-Based PLL System

This section presents the proposed enhanced CDSC-based single-phase grid fundamental detection system. The overall system architecture is first introduced, followed by a detailed description of the proposed CDSC structure, the dqPLL-based fundamental estimation, and the magnitude and phase compensation strategy. In addition, a frequency-adaptive delay mechanism is incorporated to ensure robust harmonic cancellation under grid frequency deviations. The inherent filtering delay, harmonic rejection capability, and frequency adaptability of the proposed system are also analyzed.

Figure 1 shows the overall block diagram of the proposed detection system, which consists of three core functional modules: the enhanced CDSC, the dqPLL, and the magnitude recovery & phase compensation block.

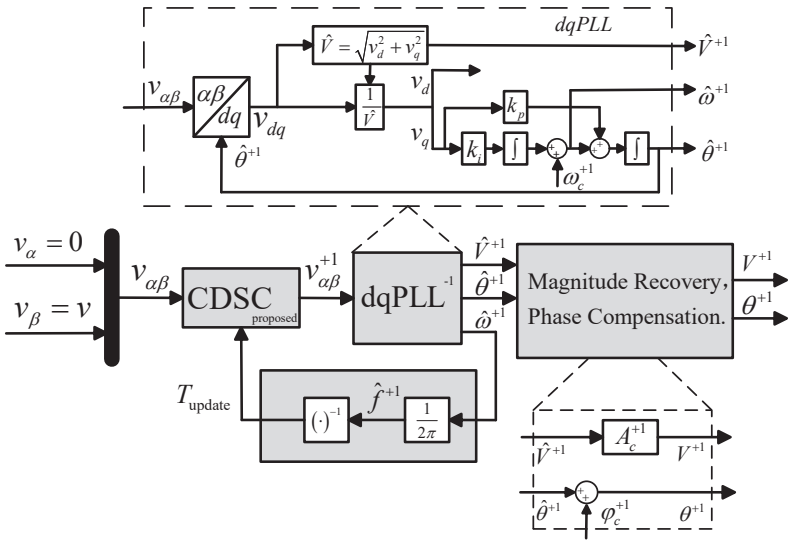


Figure 1. Overall structure of the proposed single-phase enhanced CDSC-PLL system.

Using the ACD principle, the single-phase grid voltage v is combined with a zero signal to construct a vector in the $\alpha\beta$-stationary reference frame. This vectorized signal is then processed by the enhanced CDSC module to suppress DC offset and harmonic components.

3.1. Enhanced CDSC Structure and Delay Analysis

The conventional CDSC adopts multiple DSC stages with identical target harmonic order $h^* = 1$ and delay factors arranged in a power-of-two sequence. Its structure is shown in Figure 2. The overall magnitude response is obtained by cascading individual DSC units, as illustrated in Figure 3. Each DSC stage behaves as a comb filter with periodic

nulls, and their cascade achieves near-zero gain for most harmonic components except the fundamental.

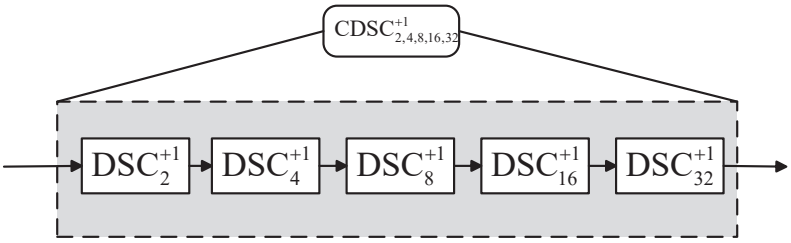


Figure 2. Structure of the conventional CDSC.

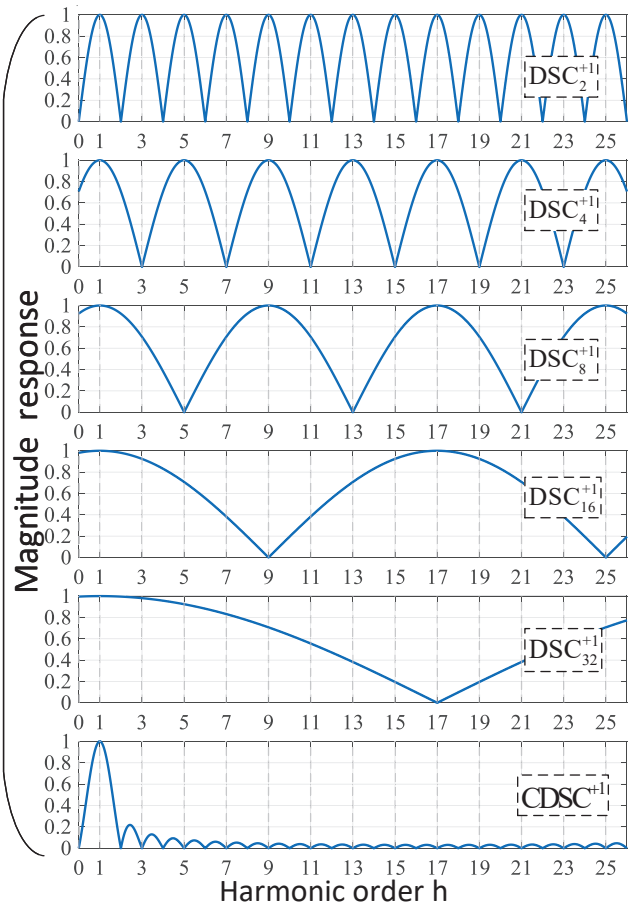


Figure 3. Individual and total magnitude responses of the conventional CDSC.

However, the use of a high-delay DSC stage leads to a total detection delay close to one fundamental cycle. To address this limitation, the proposed CDSC redesigns the delay factor configuration and introduces a DSC stage with a different target harmonic order. According to the magnitude gain characteristic given in (12), the parameters n_i and h_i^* are selected according to a null-placement rule based on the desired attenuation frequencies, where the null condition "$h = h_i^* + (k + \frac{1}{2})n_i$" determines the attenuation locations. Accordingly, the proposed CDSC adopts the parameter set $\{(4,1),(8,1),(16,1),(32,16)\}$. The first three stages are cascaded to provide attenuation at the dominant odd-order harmonics (5th, 7th, 11th, and 13th), while the final DSC_{32}^{16} stage is introduced to provide DC offset rejection. This configuration effectively reduces the overall inherent filtering delay. The resulting structure is shown in Figure 4, and its corresponding frequency response is plotted in Figure 5.

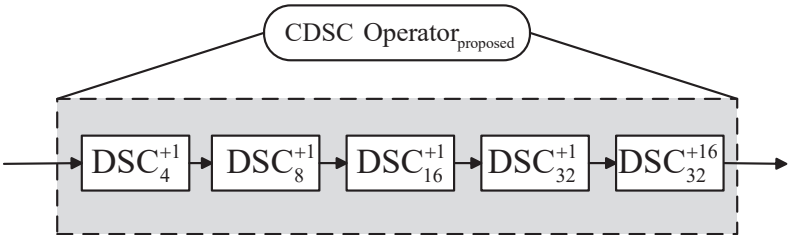


Figure 4. Structure of the proposed CDSC.

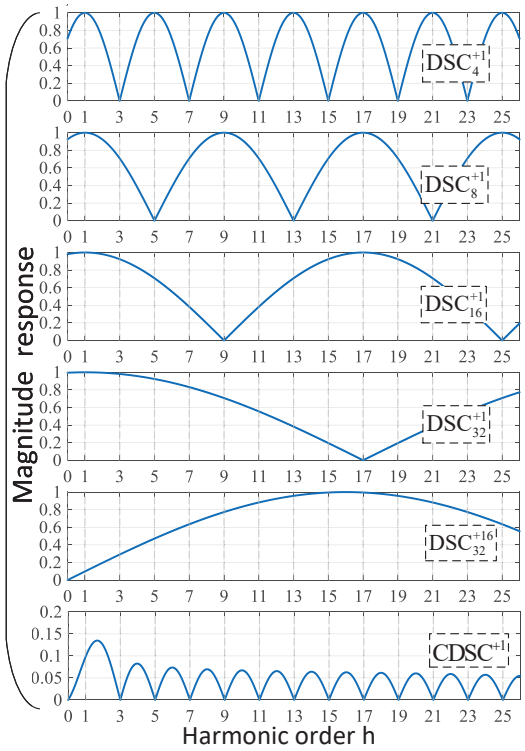


Figure 5. Individual and total magnitude responses of the proposed CDSC.

As shown in Figure 5, the individual DSC stages provide complementary frequency-selective characteristics, while the overall magnitude response of the proposed CDSC effectively rejects the DC component and the targeted odd-order harmonics. This verifies the rationality of the proposed parameter configuration.

The total time delay introduced by the CDSC is the sum of the delays of all DSC stages:

$$T_{\text{delay}} = \sum_{i=1}^{m} \frac{T}{n_i} \tag{17}$$

For the conventional CDSC, the total inherent filtering delay is approximately $0.97T$, whereas the proposed CDSC reduces this delay to $0.5T$, corresponding to nearly a 50% reduction. It should be noted that the inherent filtering delay discussed in this paper denotes the theoretical delay introduced by the cascaded delayed-signal operators. It is not intended to represent the group delay of the overall compensated filtering system.

3.2. dqPLL-Based Fundamental Estimation

After CDSC filtering, the signal is fed into the dqPLL to estimate the fundamental magnitude, phase angle, and frequency. A Park transformation is performed using the estimated phase angle $\hat{\theta}^{+1}$ to obtain the d- and q-axis components v_d and v_q. The fundamental magnitude is calculated as

$$\hat{V}^{+1} = \sqrt{v_d^2 + v_q^2} \tag{18}$$

The normalized q-axis component is regulated to zero by a proportional–integral (PI) controller to track the grid phase and frequency. The controller employs proportional and integral gains k_p and k_i, where k_p determines the dynamic response speed and k_i eliminates the steady-state phase error. Based on the PI output, the estimated angular frequency $\hat{\omega}^{+1}$ is obtained and subsequently integrated to yield the phase angle $\hat{\theta}^{+1}$.

3.3. Magnitude Recovery, Phase Compensation, and Frequency Adaptation

Due to the inherent attenuation and phase delay introduced by the CDSC filtering process, magnitude and phase compensation are required. For the fundamental component ($h = 1$), the total gain and phase shift introduced by the CDSC are given by

$$G_{\text{total}} = \prod_{i=1}^{m} \left| \cos\left(\pi \frac{1 - h_i^*}{n_i} \right) \right| \tag{19}$$

$$\Delta\phi_{\text{total}} = -\sum_{i=1}^{m} \pi \frac{1 - h_i^*}{n_i} \tag{20}$$

Accordingly, the amplitude recovery coefficient and phase compensation angle are defined as

$$A_c^{+1} = \frac{1}{G_{\text{total}}}, \qquad \varphi_c^{+1} = -\Delta\phi_{\text{total}} \tag{21}$$

The compensated fundamental magnitude and phase angle are obtained as

$$V^{+1} = A_c^{+1} \cdot \hat{V}^{+1}, \qquad \theta^{+1} = \hat{\theta}^{+1} + \varphi_c^{+1} \tag{22}$$

Moreover, the effectiveness of the CDSC relies on accurate knowledge of the fundamental period T. When the grid frequency deviates from its nominal value, the delay times must be updated accordingly. In the proposed system, the estimated frequency $\hat{\omega}^{+1}$ from the dqPLL is directly used to update the delay as

$$T_{\text{update}} = \frac{2\pi}{\hat{\omega}^{+1}} \tag{23}$$

forming a frequency-adaptive delay update mechanism that maintains consistent harmonic suppression under frequency variations.

Since the adaptive mechanism only updates the delay parameter of the CDSC operator according to the estimated grid frequency and does not modify the internal control structure of the PLL itself, its influence on the overall synchronization dynamics is mainly reflected through the variation in the filtering characteristics. Under normal operating conditions, the frequency estimation error remains bounded, and the resulting delay mismatch is limited. Therefore, the adaptive delay mainly affects the transient filtering performance rather than significantly affecting the stability characteristics of the PLL dynamics.

In summary, the proposed CDSC-based detection system achieves a significant reduction in inherent filtering delay while maintaining equivalent harmonic rejection capability. With the introduced magnitude recovery, phase compensation, and frequency-adaptive delay mechanism, accurate fundamental estimation can be achieved under DC offset, harmonic distortion, and frequency variations.

4. Experimental Results

To validate the effectiveness of the proposed method, experimental tests are conducted on the YXSPACE-SP2000 platform with a sampling frequency of 10 kHz. For a fair comparison, both the proposed method and the conventional CDSC adopt frequency-adaptive delay mechanisms, and linear interpolation is employed to handle non-integer

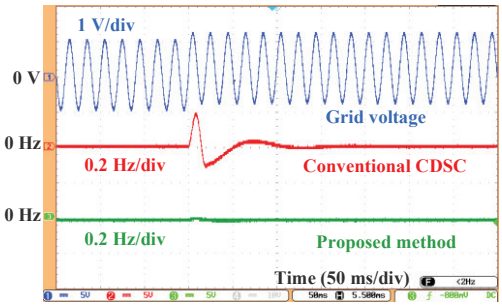
delay samples. The controller parameters are set to $k_p = 92$ and $k_i = 4232$ for both methods. The experimental conditions are summarized in Table 1.

Table 1. Experimental conditions.

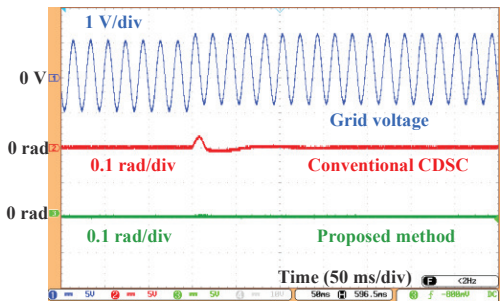
Cases	Conditions
A	Grid voltage with 0.2 p.u. DC offset.
B	Grid voltage with 0.1 p.u. 3rd, 0.05 p.u. 5th, 0.03 p.u. 7th, 0.01 p.u. 9th, 0.01 p.u. 11th, 0.01 p.u. 13th harmonics and 0.2 p.u. DC offset.
C	Frequency deviation from 50 Hz to 51 Hz, with the same conditions as Case B.
D	Frequency jump from 50 Hz to 55 Hz, with the same conditions as Case B.
E	Phase angle jump from 0 rad to $\pi/12$ rad, with the same conditions as Case B.

Note: The experimental voltages are generated by a grid simulator with a nominal fundamental voltage amplitude of 1 V. All quantities expressed in per-unit (p.u.) are normalized with respect to the nominal fundamental voltage amplitude.

Figure 6 presents the experimental results for Case A, where a 0.2 p.u. DC offset is injected into the grid voltage. Compared with the conventional CDSC design, the proposed method exhibits smaller transient oscillations, shorter settling time, and lower frequency and phase estimation errors. This demonstrates the improved dynamic performance of the proposed method under DC offset conditions.



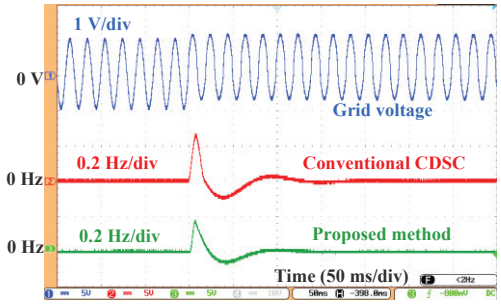
(**a**) Frequency estimation errors



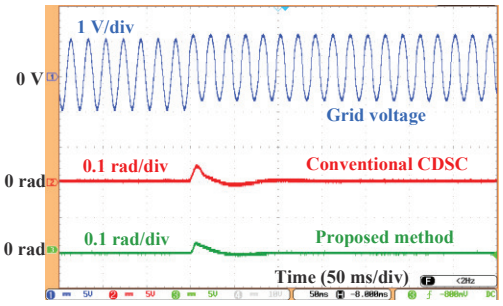
(**b**) Phase estimation errors

Figure 6. Experimental results under Case A: DC offset injection.

Figure 7 presents the experimental results for Case B, where the grid voltage contains 0.1 p.u. 3rd, 0.05 p.u. 5th, 0.03 p.u. 7th, 0.01 p.u. 9th, 0.01 p.u. 11th, and 0.01 p.u. 13th harmonics, along with a 0.2 p.u. DC offset. It can be observed that the proposed method effectively eliminates the injected odd-order harmonics and DC offset, resulting in zero steady-state error in both frequency and phase estimation. Moreover, during the transient process, the proposed method exhibits reduced overshoot compared to the conventional CDSC design. These results demonstrate the strong disturbance rejection capability and improved dynamic performance of the proposed method.



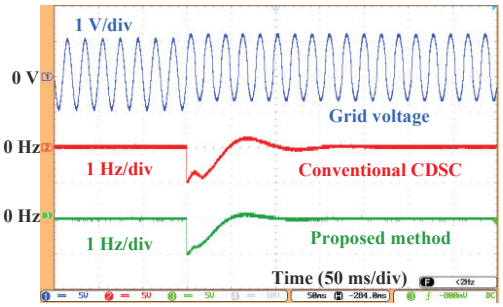
(**a**) Frequency estimation errors



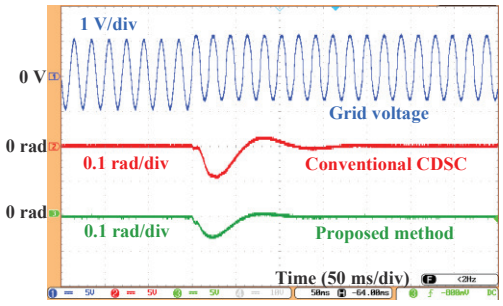
(**b**) Phase estimation errors

Figure 7. Experimental results under Case B: Harmonic and DC offset injection.

Figure 8 presents the experimental results for Case C, where the grid frequency varies from 50 Hz to 51 Hz while maintaining the same harmonic and DC offset conditions as in Case B. By employing frequency-adaptive delay times updated from the estimated frequency, the proposed method is able to track frequency variations in real time, achieving fast convergence and accurate frequency and phase estimation during the variation process. These results validate the effectiveness of the adaptive delay mechanism under small frequency deviations.



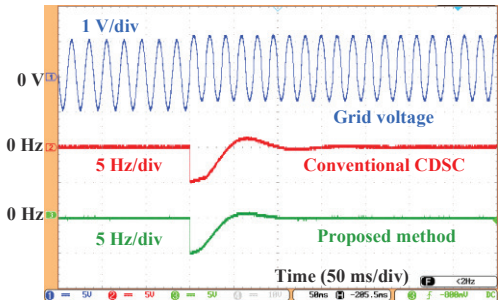
(**a**) Frequency estimation errors



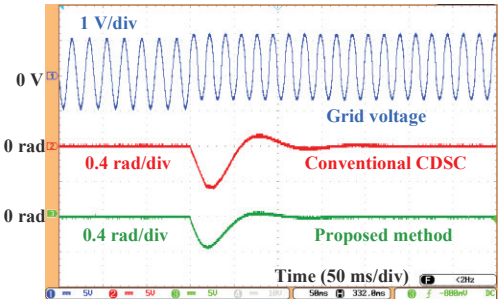
(**b**) Phase estimation errors

Figure 8. Experimental results under Case C: Small frequency deviation.

Figure 9 presents the experimental results for Case D, where the grid frequency undergoes a step change from 50 Hz to 55 Hz under the same harmonic and DC offset conditions as in Case B. Despite the large frequency step, the proposed method maintains accurate frequency and phase tracking. It can be observed that the proposed method achieves rapid convergence after the frequency step, with a shorter settling time and smaller overshoot compared to the conventional CDSC design. These results demonstrate that the proposed method retains excellent performance under large frequency deviations, confirming its robustness against severe grid transients.



(**a**) Frequency estimation errors



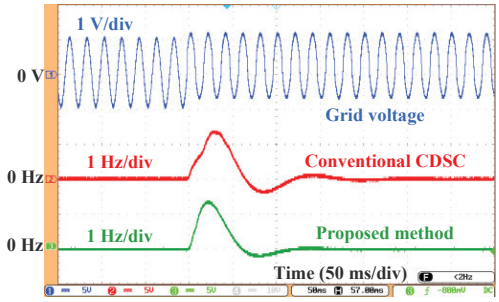
(**b**) Phase estimation errors

Figure 9. Experimental results under Case D: Large frequency jump.

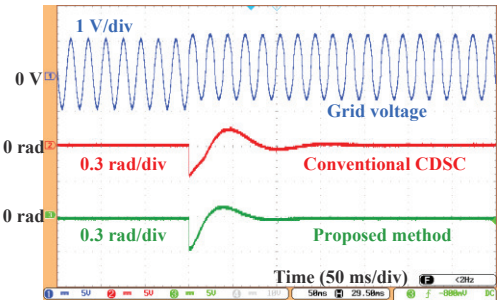
Figure 10 presents the experimental results for Case E, where the grid voltage phase angle undergoes a step change from 0 rad to $\pi/12$ rad under the same harmonic and DC offset conditions as in Case B. In this case, both the proposed method and the conventional CDSC design exhibit larger transient estimation errors than in the previous test cases. Nevertheless, both methods achieve accurate steady-state estimation. These results indicate that the proposed method maintains stable phase tracking performance under sudden phase disturbances.

To provide a quantitative comparison, the maximum absolute errors (MAEs) of the frequency and phase estimations are summarized in Table 2. The proposed CDSC achieves smaller MAEs than the conventional CDSC in most test cases, demonstrating its improved dynamic performance and disturbance rejection capability. For Cases C and D, both methods have the same frequency MAE due to the imposed frequency step, while the proposed method exhibits smaller phase MAEs. In Case E, both methods show comparable MAEs.

Overall, the experimental results demonstrate that the proposed method achieves faster dynamic response and smaller transient estimation errors than the conventional CDSC. With the frequency-adaptive delay mechanism, accurate frequency and phase tracking are maintained under various grid disturbances. These results confirm that the proposed method effectively reduces the inherent filtering delay while maintaining excellent disturbance rejection capability and high steady-state accuracy.



(**a**) Frequency estimation errors



(**b**) Phase estimation errors

Figure 10. Experimental results under Case E: Phase angle jump.

Table 2. Maximum Absolute Error (MAE) Comparison under Different Test Cases.

Case	Frequency MAE (Hz)		Phase MAE (rad)	
	Conv.	Prop.	Conv.	Prop.
A	0.185	0.008	0.031	0.001
B	0.262	0.172	0.044	0.026
C	1.000	1.000	0.090	0.059
D	5.000	5.000	0.471	0.346
E	1.371	1.376	0.262	0.262

Note: Conv. and Prop. denote Conventional CDSC and Proposed CDSC, respectively.

5. Conclusions

This paper proposes an enhanced CDSC-based method for distorted grid parameter estimation. By redesigning the CDSC structure, the proposed method achieves a 50% reduction in detection delay while preserving DC offset and odd-order harmonic rejection capability. To compensate for the magnitude attenuation and phase shift introduced by the CDSC, an amplitude and phase compensation scheme is developed to ensure accurate fundamental estimation. In addition, a frequency-adaptive feedback mechanism is incorporated to maintain effective harmonic cancellation under grid frequency variations. Experimental results across multiple test scenarios demonstrate that the proposed method improves dynamic performance while maintaining zero steady-state error under various distorted grid conditions, including DC offset, odd-order harmonics, frequency variations, and phase-angle jumps.

Future work will investigate the performance of the proposed method under more complex grid conditions, including measurement noise, interharmonics, and time-varying harmonic disturbances, and further improve its robustness for practical applications.

Author Contributions: Conceptualization, Y.Z. (Yihua Zhu), X.W. and C.L.; methodology, Y.Z. (Youfeng Zhou), X.W. and J.Y.; validation, C.L., J.Y. and Y.Z. (Yihua Zhu); writing—original draft preparation, Y.Z. (Youfeng Zhou) and Y.Z. (Yihua Zhu); writing—review and editing, X.W., G.L. and

Z.D.; visualization, C.L.; supervision, Y.Z. (Yihua Zhu) and Z.D.; project administration, G.L.; funding acquisition, Z.D. All authors have read and agreed to the published version of the manuscript.

Funding: The authors declare that this study received funding from the National Key Research and Development Program of China under Grant 2023YFB4203200 and the Natural Science Foundation of Shaanxi Province under Grant 2025JC-YBMS-482. The funder was not involved in the study design, collection, analysis, interpretation of data, the writing of this article or the decision to submit it for publication.

Data Availability Statement: The original contributions presented in this study are included in the article. Further inquiries can be directed at the corresponding author.

Conflicts of Interest: Authors Yihua Zhu, Jiawei Yu and Chao Luo were employed by the Electric Power Research Institute, China Southern Power Grid. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

PLL	phase-locked loop
DSC	delayed signal cancellation
CDSC	cascaded delayed signal cancellation
DFT	discrete Fourier transform
RDFT	recursive DFT
QSG	quadrature signal generator
SOGI	second-order generalized integrator
ACD	anti-conjugate decomposition
MAE	maximum absolute error

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