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A Four-Switch Single-Stage Common-Ground Buck–Boost Inverter with Series-Capacitor Compensation

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Abstract

This paper proposes a single-stage common-ground series-capacitor-compensated buck–boost inverter (CG-SCC-BBI) for wide-input DC–AC applications. Featuring a common-ground neutral and a series-blocking film capacitor, the topology inherently suppresses high-frequency common-mode leakage-current excitation and blocks the structural DC offset. To counteract frequency-dependent voltage attenuation caused by the output network, a fundamental-frequency equivalent model is derived to pre-scale the modulation reference and fully restore output voltage amplitude. The four-switch power stage operates with single-active-leg PWM, confining high-frequency switching to a single half-bridge at any instant to significantly reduce the switching-loss budget. Furthermore, by eliminating the conventional line-frequency output filter choke and utilizing film capacitors exclusively, the topology completely avoids electrolytic capacitors, thereby enhancing long-term operational reliability and lifespan. The proposed inverter supports seamless transition between boost and buck operating modes across the entire input-voltage range. Its operating principles are validated through time-domain simulations, and these were experimentally verified on a 300 W SiC MOSFET standalone laboratory prototype. Experimental results confirm correct operation from 95 V to 400 V DC input, achieving maximum measured efficiencies of 96.79% at the rated 300 W under low-input operation and 97.66% at the rated 300 W under high-input operation, while maintaining an output-current total harmonic distortion (THD) below 2.5%.

Keywords: buck–boost inverter; non-isolated inverter; series-blocking capacitor; model-based voltage compensation; common-ground inverter; single-phase inverter



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1. Introduction

Over the last two decades, renewable-energy sources and distributed DC power systems have become increasingly important for residential and commercial electricity applications [1]. In these systems, low-power single-phase DC–AC inverters, typically rated below 1 kW, constitute the key power-conditioning stage that converts a variable DC source into a regulated AC supply for diverse AC power systems and standalone loads [2–4]. A fundamental challenge in many DC-powered AC conversion systems is the wide variation in input voltage, which may originate from renewable-energy sources, battery-storage systems, or other variable DC supplies. Ratios exceeding 2:1 between

the minimum and the maximum operating voltage are common in such sources [1,2]. Conventional full-bridge voltage-source inverters (VSIs) are intrinsically buck converters whose AC output amplitude cannot exceed the DC-bus voltage, leaving them unable to exploit the full operating range of a wide-range DC source. This constraint motivates the search for single-phase inverter topologies with intrinsic voltage-boosting capability [3].

A well-established route to buck–boost inversion cascades a front-end boost DC–DC converter with a conventional VSI, forming a two-stage conversion chain [2]. While this architecture separates front-end voltage conditioning from DC–AC conversion, it requires an additional energy-storage inductor and a bulk interstage capacitor and subjects the power to two successive conversion events, each introducing switching and conduction losses [5,6]. The resulting system is larger, costlier, and less efficient than an equivalent single-stage design. These penalties have driven extensive research into single-stage topologies that provide voltage boosting and AC synthesis within one power-processing stage [2,5].

Several single-stage buck–boost families, surveyed comprehensively in [7], eliminate the two-stage cascade penalty. The Z-source inverter [5] exploits the otherwise-forbidden shoot-through state to boost the DC link, but at the cost of significant device current stress and a carefully designed impedance network. Switched-boost [8] and diode-assisted [9] inverters reduce the passive count at the expense of an additional active switch. Split-inductor differential-boost topology [10] achieves single-stage buck–boost through bimodal operation, yet suffers circulating-current paths that complicate control and reduce high-gain efficiency. The quasi-switched-boost inverter [11] references its output to the positive DC rail to suppress common-mode swings, but it is restricted to boost-only mode and cannot synthesize output voltages below the DC input. Differential and electrolytic-capacitor-less buck–boost families originally developed for wide-input-voltage power-conditioning applications [12,13] broaden this design space further, yet each retains either a large magnetic count or a boost-only gain characteristic.

A significant milestone in single-stage buck–boost conversion is the three-phase GaN Y-inverter reported by Antivachis et al. [14], which delivers high-quality sinusoidal output over a wide DC range through a compact four-switch-per-phase topology at high switching frequency. A return-path-inductor variant [15] further reduces device current stress while extending the input range, and related three-phase architectures based on coupled inductors [6] and Z-source networks [16] have also been reported to have high-performance power conversion. Their common-mode behavior has been systematically reviewed in [17]. However, all of these topologies are inherently three-phase, requiring three independent LC filter sets and three coordinated modulation channels, making them less suitable for compact single-phase AC power systems, where reduced hardware complexity, lower cost, and high power density are primary design objectives. Developing a single-phase inverter that preserves the wide-input-voltage capability and compact switching architecture of the Y-inverter family while operating from a conventional two-terminal AC output therefore remains an important research challenge.

In transformerless single-phase inverters, common-mode (CM) leakage current remains an important design concern because high-frequency variations of the common-mode voltage (CMV) across parasitic capacitances may generate unwanted leakage current, electromagnetic interference, and additional system losses [18–20]. Galvanic isolation effectively suppresses this phenomenon, but increases converter size, weight, and cost [21]. Among transformerless solutions, the H6 [21] and HERIC [22] topologies reduce leakage current by decoupling the DC and AC sides during the zero state, while improved modulation and clamping techniques further suppress the residual leakage current [23,24]. Nevertheless, these converters cannot completely eliminate the leakage associated with

device parasitic capacitances, and NPC- and T-type converters [25] require a split DC-link structure that increases capacitor count and hardware complexity. Comparative studies of transformerless single-phase and multilevel inverter topologies have reached similar conclusions [26]. However, these existing topologies generally remain limited to either buck or boost operation or require additional power-conversion stages, making it difficult to simultaneously achieve wide-input-voltage operation, compact structure, and common-ground capability within a single-stage inverter.

An elegant way to suppress leakage current is the common-ground (CG) inverter, in which one terminal of the DC source is permanently bonded to the AC neutral so that the CMV is clamped to a constant value by design rather than by modulation. The traditional CG family introduced by Siwakoti and Blaabjerg [27] establishes this principle with a low component count, but its members operate in buck mode only and therefore inherit the limited-voltage-range drawback of the conventional VSI. To add boosting, a second class of topologies references the AC output to the positive DC rail (V^+) by tying the output neutral to the source positive terminal. Huang et al. [28] realize a four-switch CG inverter with dual-mode (buck–boost/buck) operation and a DC-link requirement only slightly higher than the required AC output amplitude; however, its asymmetric per-half-cycle operation produces uneven thermal stress and requires floating gate drivers. Boost-oriented positive-rail designs built from standard half-bridge modules [29], systematically derived single-stage boost families [30], and single-source nine-level boost inverters with a low switch count [31]—together with the more recent common-ground stages built from four [32] and five [33] switches—further raise the voltage gain and output quality, yet they remain confined to boost-only operation and demand high duty cycles that elevate inductor current and switch voltage stress. Across this evolution, a single-phase positive-rail topology that simultaneously delivers true buck-and-boost gain and inherent leakage elimination is still missing.

Because positive-rail power stages generate a unipolar intermediate voltage containing both a DC offset and the desired AC component, a series-blocking film capacitor C_s is inserted between the power stage and the load to remove the offset before delivery. Nguyen and Tran [34] adopt exactly this principle in a four-switch single-stage switched-boost inverter, where a series DC-blocking capacitor isolates the offset at the output. While conceptually simple, this capacitor carries the full AC load current, so its equivalent series resistance raises conduction losses at high load. Moreover, that work cannot recover the load-dependent voltage attenuation the capacitor introduces. The same reactive impedance appears in positive-rail topologies that reference the output to V^+ [11,28] and in virtual-ground buck–boost inverters that clamp the reference node through an auxiliary branch [35,36], yet these either operate in a single gain mode, rely solely on an outer regulator, or omit a physically motivated compensation model. To the best of the authors' knowledge, no reported single-phase common-ground inverter simultaneously provides genuine buck–boost capability together with an analytically derived model that compensates for the voltage attenuation introduced by the mandatory series-blocking capacitor.

To bridge this gap, this paper proposes the CG-SCC-BBI topology for wide-input DC–AC power conditioning. By employing a model-based compensation that pre-adjusts the modulation reference based on the known load, the proposed system turns the reactive attenuation of the blocking network into a precisely managed design parameter. The specific contributions are as follows. (1) The proposed topology permanently bonds the AC neutral to the positive terminal of the DC source, inherently fixing the common-mode voltage and eliminating high-frequency leakage current without relying on modulation techniques, while a series-blocking film capacitor isolates the structural DC offset. (2) Unlike traditional inverters, the proposed topology requires no bulky output filter inductor, achieving high-

quality output voltage filtering using only a single parallel capacitor, which significantly reduces the system's total volume, weight, and hardware cost. (3) A steady-state analytical model rigorously characterizes the frequency-dependent voltage-divider effect among the series capacitor, output capacitor, and load. Based on this model, a straightforward open-loop compensation scales the modulation reference beforehand to compensate for the voltage drop without requiring output-voltage feedback. (4) Practical component-selection guidelines are established for the energy-storage inductor, intermediate buffer capacitor, series-blocking capacitor, and output capacitor based on boundary-conduction operation, capacitor-ripple, and voltage-retention criteria.

2. The Proposed CG-SCC-BBI

2.1. Circuit Topology and Operating Principle

The proposed CG-SCC-BBI is a single-phase, non-isolated, single-stage buck–boost topology that synthesizes an AC output from a DC source without a bulky, lossy isolation transformer. As illustrated in Figure 1, it integrates two functional blocks: a four-switch buck–boost power stage and a passive three-element output-coupling network. To establish an unambiguous framework for steady-state analysis, four circuit nodes are designated throughout. Node “a” is the primary switching node, where the midpoint of the boost half-bridge, the intermediate capacitor C_p , and the series-blocking capacitor C_s meet. Node “b” is the negative terminal (V^-) of the DC input source. Node “o” is the active terminal of the AC output, formed at the junction of C_s , the output filter capacitor C_o , and the load. Node “n” is the AC output neutral. With this convention, the three core element voltages are written compactly as the internode potentials:

$$v_{Cp} = v_{ab}, \quad v_{Cs} = v_{ao}, \quad v_{Co} = v_{on} = v_o \quad (1)$$

where v_{ab} is the unipolar node “a” potential referred to the negative DC rail, v_{ao} is the instantaneous voltage across the series-blocking capacitor, and v_{on} is the inverter AC output voltage v_o across the filter capacitor C_o . Referred to the output neutral, the total synthesized output-side voltage is $v_{an} = v_a - v_n = v_{Cs} + v_o$, which comprises a DC offset $V_{an,DC}$ and a sinusoidal AC component $v_{an,AC}$.

The power stage uses four active switches, S_1 – S_4 , arranged as two complementary half-bridge legs. The upper (buck) half-bridge is formed by S_1 and S_2 , with its midpoint tied to one terminal of the energy-storage inductor L_1 . The lower (boost) half-bridge consists of S_3 and S_4 , whose midpoint forms the primary switching node “a”. Bridging node “a” and the negative rail, the intermediate capacitor C_p acts purely as a local energy buffer and high-frequency ripple filter for the switching cell. As a high-frequency decoupling element, it carries no fundamental-frequency load current and plays no role in the output model of Section 3.

A defining feature of this topology is the placement of the AC output neutral “n”. Rather than referencing it to the negative DC rail as in conventional systems, it is permanently bonded to the positive rail (V^+) of the input source. This direct bonding establishes a true common-ground topology that clamps the common-mode voltage to a constant value independently of high-frequency switching, suppressing parasitic ground leakage current at its origin.

The resulting structural DC offset is isolated from the load by the three-element coupling network. Specifically, the series-blocking film capacitor C_s , inserted between node “a” and output terminal “o,” withstands the DC bias so that only the fundamental AC component is delivered downstream. The output filter capacitor C_o , connected in parallel with the load between nodes “o” and “n,” attenuates high-frequency switching harmonics to ensure output waveform quality and a transformerless single-phase power-processing cell.

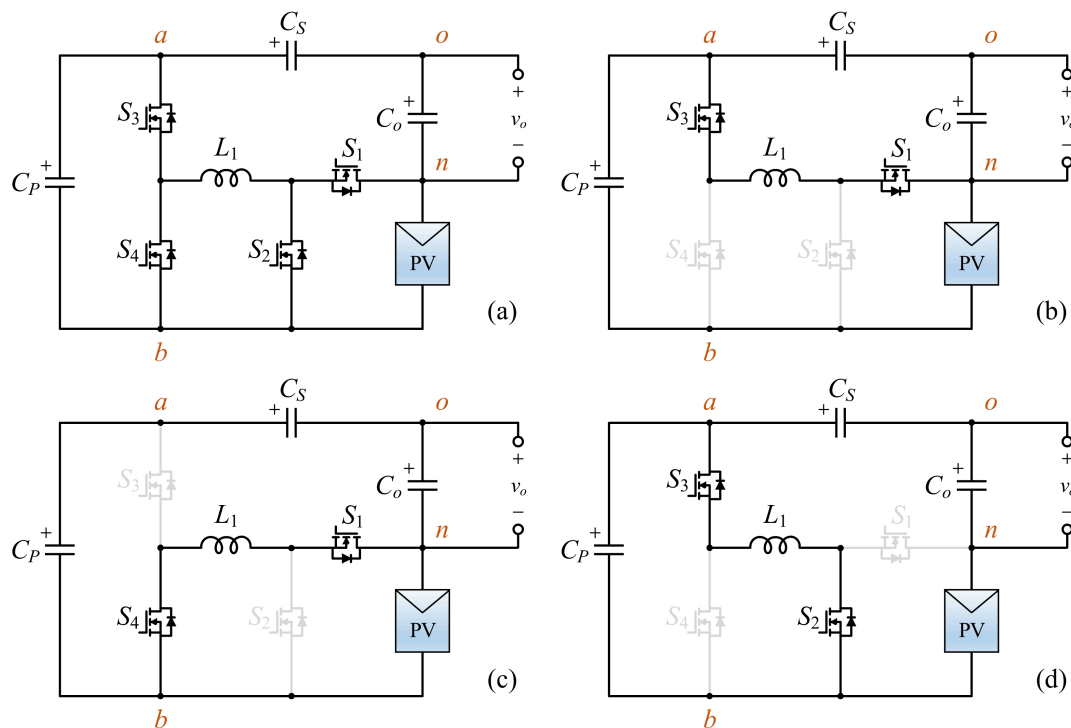


Figure 1. Proposed common-ground non-isolated buck-boost inverter: (a) complete topology with labeled nodes a, b, o, n; (b) buck-regime interval with S_3 and S_1 conducting; (c) boost-regime interval with S_4 and S_1 conducting; (d) buck-regime freewheeling interval with S_3 and S_2 conducting.

2.2. Topological Switching States

Within each high-frequency switching period, the converter operates in one of two regimes—buck or boost—depending on whether the instantaneous target output voltage is lower or higher than the input voltage V_{in} . In both regimes, high-frequency pulse-width modulation (PWM) is confined to a single half-bridge leg while the other leg is clamped, which limits the switching-loss budget relative to a conventional four-switch full-bridge inverter.

Buck regime ($V_o \leq V_{in}$). The left half-bridge is clamped by keeping S_3 permanently ON and S_4 OFF. High-frequency switching is executed entirely by the right half-bridge (S_1 and S_2). When S_1 is ON (Figure 1b), the inductor L_1 is connected between node “a” (via S_3) and the neutral node “n” (via S_1), and energy is transferred through the reactive network. When S_1 turns OFF (Figure 1d), S_2 provides a freewheeling path and the inductor current circulates through S_3 , L_1 , and S_2 back to node “b,” releasing stored energy to the intermediate capacitor C_P .

Boost regime ($V_o > V_{in}$). The right half-bridge is clamped by holding S_1 permanently ON and S_2 OFF. High-frequency modulation is transferred to the left half-bridge (S_3 and S_4). When S_4 is ON (Figure 1c), the inductor L_1 is connected between node “b” and node “n” (the positive rail via S_1), so the source energizes L_1 and its current ramps up. When S_4 turns OFF, S_3 turns ON and steers the inductor current into node “a,” boosting the potential across C_P and driving energy through C_S to the load.

Because high-frequency commutation is confined to a single leg at any instant, the circuit operates as an integrated single-stage non-inverting buck-boost cell with a seamless buck-to-boost transition. Crucial to the modeling in Section 3, the series capacitor C_S is the only series element between node “a” and output node “o,” forcing the total load current i_o to flow through it across all switching states. Consequently, the fundamental load current induces a notable reactive voltage drop across C_S , directly shaping the output voltage delivered to the load.

3. Mathematical Modeling of Series-Capacitor and Output-Voltage Interdependence

This section derives the fundamental-frequency amplitude attenuation and phase shift imposed by the series coupling network.

3.1. Fundamental-Frequency Equivalent Circuit

To analyze the steady-state behavior at the fundamental line frequency (ω_o), the superposition principle is applied to decouple the DC and AC components. Because the intermediate capacitor C_p operates entirely within the switching cell to buffer high-frequency switching ripples, it carries no fundamental load current. Consequently, the fundamental-frequency output model simplifies to the series-blocking capacitor C_s , the output filter capacitor C_o , and the load.

The modulation employs a unipolar reference voltage at node “a,” $v_a(t) = V_{a,pk}(\sin \omega_o t + 1)$, whose amplitude is denoted by $V_{a,pk}$. Its implementation is described in Section 4. Under the adopted carrier-based strategy, the carrier-averaged voltage across C_p follows this reference in both the buck and the boost regime, so its average DC value over one fundamental period is $V_{Cp,DC} = V_{a,pk}$.

Referring to the AC output neutral “n”—which is permanently bonded to the positive DC rail (V_{in})—the structural DC offset voltage $V_{an,DC}$ is derived as:

$$V_{an,DC} = V_{Cp,DC} - V_{in} = V_{a,pk} - V_{in} \quad (2)$$

and C_s , being a capacitor, blocks this offset, so that $V_{Cs,DC} = V_{an,DC}$, no DC current reaches the load, and only the AC component $v_{an,AC}(t) = V_{a,pk} \sin \omega_o t$ is delivered.

At the fundamental frequency the filter-capacitor current and the resistive load current are related by $|I_{C_o}| / |I_R| = \omega_o C_o R = R / X_{C_o}$. With $C_o = 6.8 \mu\text{F}$ and $f_o = 60 \text{ Hz}$, $X_{C_o} \approx 390 \Omega$, so this ratio reaches approximately 1.03 at the 400Ω light-load condition of Table 1, where the filter-capacitor current slightly exceeds the resistive-load current. The output branch is therefore represented by the parallel combination:

$$Z_o = R \parallel \frac{1}{j\omega_o C_o} = \left(\frac{1}{R} + j\omega_o C_o \right)^{-1} = \frac{R}{1 + j\omega_o R C_o} \quad (3)$$

fed through the series-blocking capacitor of impedance:

$$Z_{C_s} = \frac{1}{j\omega_o C_s} = -jX_{C_s}, \quad X_{C_s} = \frac{1}{2\pi f_o C_s} \quad (4)$$

with $X_{C_s} \approx 12.06 \Omega$ for $C_s = 220 \mu\text{F}$.

Table 1. Fundamental-frequency model quantities and the error introduced by neglecting C_o ($C_s = 220 \mu\text{F}$, $C_o = 6.8 \mu\text{F}$, $f_o = 60 \text{ Hz}$, $V_o = 110 V_{rms}$).

Load Condition	$R (\Omega)$	R/X_{C_o}	$\varphi (^{\circ})$, Equation (7)	$I_{C_s,rms} (\text{A})$, Equation (9)	$V_{C_s,AC,rms} (\text{V})$, Equation (10)	$k_{v,0}$, Equation (11)	$k_{v,r}$, Equation (6)	$\varepsilon_{kv} (\%)$, Equation (12)	$\varepsilon_V (\%)$, Equation (12)
Full load (300 W, 100%)	40	0.103	16.30	2.764	33.33	0.957	0.931	2.84	−2.76
Light load (30 W, 10%)	400	1.025	1.67	0.394	4.75	0.999	0.969	3.09	−3.00

3.2. Voltage-Transfer Function and Voltage-Retention Factor

Apply the voltage divider formed by Equations (3) and (4):

$$H(j\omega_o) = \frac{V_o}{V_{an,AC}} = \frac{Z_o}{Z_o + Z_{C_s}} = \frac{1}{1 + \frac{C_o}{C_s} - j\frac{X_{C_s}}{R}} \quad (5)$$

The first denominator term, $1 + C_o/C_s$, is the load-independent capacitive divider between C_s and C_o , and the second, X_{C_s}/R , is the reactive drop across C_s and vanishes as the load is lightened. The magnitude of Equation (5) gives the voltage-retention factor and the uncompensated output voltage:

$$k_v = |H(j\omega_o)| = \frac{1}{\sqrt{\left(1 + \frac{C_o}{C_s}\right)^2 + \left(\frac{X_{C_s}}{R}\right)^2}}, \quad V_{o,actual} = \frac{k_v V_{a,pk}}{\sqrt{2}} \quad (6)$$

and the angle by which the load voltage leads the synthesized source:

$$\varphi = \angle H(j\omega_o) = \arctan\left(\frac{1}{\omega_o R(C_s + C_o)}\right) \quad (7)$$

which is governed by the sum $C_s + C_o$ rather than by C_s alone. At no load does the attenuation vanish:

$$\lim_{R \rightarrow \infty} k_v = \frac{C_s}{C_s + C_o} \quad (8)$$

which equals 0.970 for the prototype. This load-independent residue bounds the open-circuit output, so the modulator never has to synthesize an unbounded reference. Figure 2 plots k_v against C_s from Equation (6). Each curve saturates at the ceiling given by Equation (8) rather than at unity.

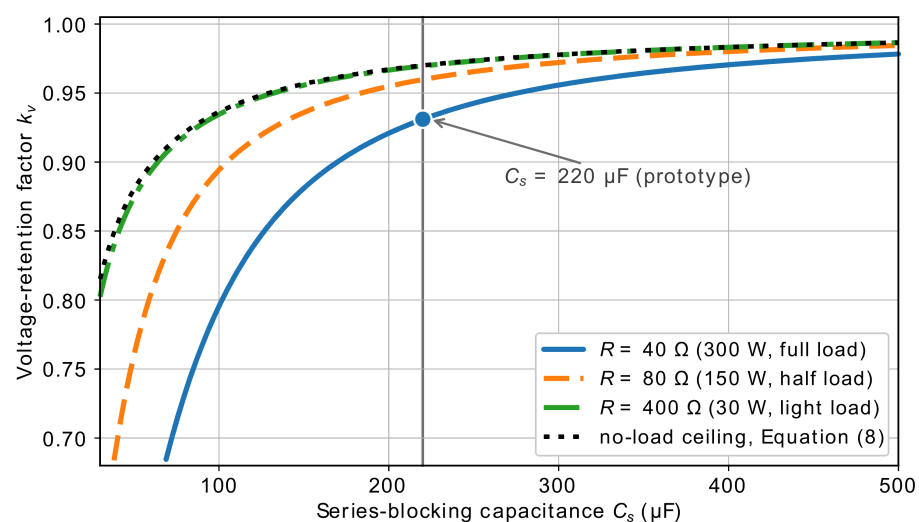


Figure 2. Voltage-retention factor k_v of Equation (6) versus the series-blocking capacitance C_s ($C_o = 6.8 \mu\text{F}$, $f_o = 60 \text{ Hz}$) for the three load conditions of Table 1. The dotted curve is the load-independent no-load ceiling of Equation (8), which the retention factor approaches as the load is lightened.

3.3. Series-Capacitor Current, Voltage, and Sensitivity to the Filter Capacitance

The current forced through C_s is the sum of the resistive and the capacitive branch currents:

$$I_{C_s} = I_R + I_{C_o} = V_o \left(\frac{1}{R} + j\omega_o C_o \right), \quad I_{C_s,rms} = V_o \sqrt{\frac{1}{R^2} + (\omega_o C_o)^2} \quad (9)$$

and the fundamental voltage it develops across the series capacitor is:

$$V_{C_s,AC,rms} = |Z_{C_s}| I_{C_s,rms} = V_o \sqrt{\left(\frac{C_o}{C_s}\right)^2 + \left(\frac{X_{C_s}}{R}\right)^2} \quad (10)$$

Setting $C_o = 0$ in (6) gives the first-order approximation:

$$k_{v,0} = \frac{1}{\sqrt{1 + \left(\frac{X_{C_s}}{R}\right)^2}} = \frac{R}{\sqrt{R^2 + X_{C_s}^2}} \quad (11)$$

whose relative error, together with the output-voltage deficit incurred when the gain $k_{comp,0} = 1/k_{v,0}$ is used in place of $k_{comp} = 1/k_v$, is:

$$\varepsilon_{k_v} = \frac{k_{v,0} - k_v}{k_v} \times 100\%, \quad \varepsilon_V = \left(\frac{k_{comp,0}}{k_{comp}} - 1 \right) \times 100\% \quad (12)$$

Table 1 evaluates Equations (6)–(12) over the complete operating range for $C_s = 220 \mu\text{F}$, $C_o = 6.8 \mu\text{F}$, and $f_o = 60 \text{ Hz}$.

The error stays between 2.8% and 3.1% and grows as the load is lightened, because the load-independent divider of Equation (8) becomes the dominant attenuation mechanism once the reactive drop across C_s has decayed. At 400Ω , the filter-capacitor current, 0.282 A irrespective of load, exceeds the resistive one and raises $I_{C_s,rms}$ by 43% above V_o/R . Since the compensation is open-loop and no feedback path removes a residual gain error, the full model—Equations (5)–(10)—is used for the compensation law of Section 4 and for the component stresses of Section 5.

4. Modulation and Model-Based Voltage Compensation

The modulation strategy uses the factor k_v of Equation (6) to pre-adjust its reference so that the target output is obtained for the known load. This section presents the DC-offset scheme that guarantees a unipolar reference, the dual duty-cycle generation, the model-based compensation, and the operating limits and load sensitivity that the compensation implies.

4.1. DC-Offset Sinusoidal Modulation

A non-inverting buck–boost converter cannot produce a negative node “a” voltage, so a plain sinusoidal reference is unrealizable. Adding a DC offset equal to the peak output voltage gives node “a” reference to the negative rail:

$$v_a(t) = \sqrt{2} V_o (\sin(\omega_o t) + 1) \quad (13)$$

where V_o is the target RMS output voltage, $\omega_o = 2\pi f_o$, and the unity offset ensures $v_a(t) \geq 0$ for all t . Referred to the output neutral, this equals the synthesized voltage $v_{an}(t) = v_a(t) - V_{in}$ analyzed in Section 3, where $V_{a,pk}$ denotes the peak value of the AC component of the node “a” reference and equals $\sqrt{2}V_o$ before compensation. The peak of the unipolar node “a” potential itself is therefore $V_{a,max} = 2V_{a,pk}$. The normalized modulation index and its span are:

$$m_a(t) = \frac{v_a(t)}{V_{in}}, \quad m_{a,min} = 0, \quad m_{a,max} = \frac{2\sqrt{2} V_o}{V_{in}} \quad (14)$$

4.2. Dual Duty-Cycle Control Law Derivation

At each sampling instant, the controller computes $m_a(t)$, selects the operating state, and forms the dual duty cycles for the two switch pairs. In the buck state ($m_a < 1$), the upper half-bridge (S_1 and S_2) chops while S_3 is clamped ON and S_4 OFF, so $d_{\alpha 1} = m_a(t)$ and $d_{\alpha 2} = 1$. Averaging the switched node over one carrier period gives:

$$v_{Cp,avg} = d_{\alpha 1} V_{in} = m_a(t) V_{in} = v_a(t) \quad (15)$$

In the boost state ($m_a \geq 1$), the lower half-bridge (S_3 and S_4) chops while S_1 is clamped ON and S_2 OFF. Volt-second balance on L_1 over one switching period, with $D_4 = 1 - d_{\alpha 2}$ the fraction for which S_4 conducts, gives:

$$V_{in} D_4 = (v_{Cp,avg} - V_{in}) d_{\alpha 2} \Rightarrow v_{Cp,avg} = \frac{V_{in}}{d_{\alpha 2}} = V_{in} m_a(t) = v_a(t) \quad (16)$$

so that $d_{\alpha 1} = 1$ and $d_{\alpha 2} = 1/m_a(t)$. Equations (15) and (16) also justify Equation (2), since in both states the carrier-averaged node voltage equals the reference. Collecting both states, the dual duty-cycle control law executed by the modulator is:

$$\begin{cases} d_{\alpha 1} = m_a(t), d_{\alpha 2} = 1, & m_a(t) < 1 \text{ (buck)} \\ d_{\alpha 1} = 1, d_{\alpha 2} = 1/m_a(t), & m_a(t) \geq 1 \text{ (boost)} \end{cases} \quad (17)$$

Gate signals G_1 and G_2 are complementary and so are G_3 and G_4 , so only one switch pair switches at high frequency at any instant, which reduces the switching-loss budget relative to full-bridge operation. The boundary $m_a = 1$ is crossed twice per fundamental period, at:

$$\varphi_t = \arcsin\left(\frac{V_{in}}{V_{a,pk}} - 1\right) \quad (18)$$

which has a solution only for $0 \leq V_{in} \leq 2V_{a,pk}$. Above that, the converter stays in the buck regime over the whole period. These relationships are illustrated in Figure 3.

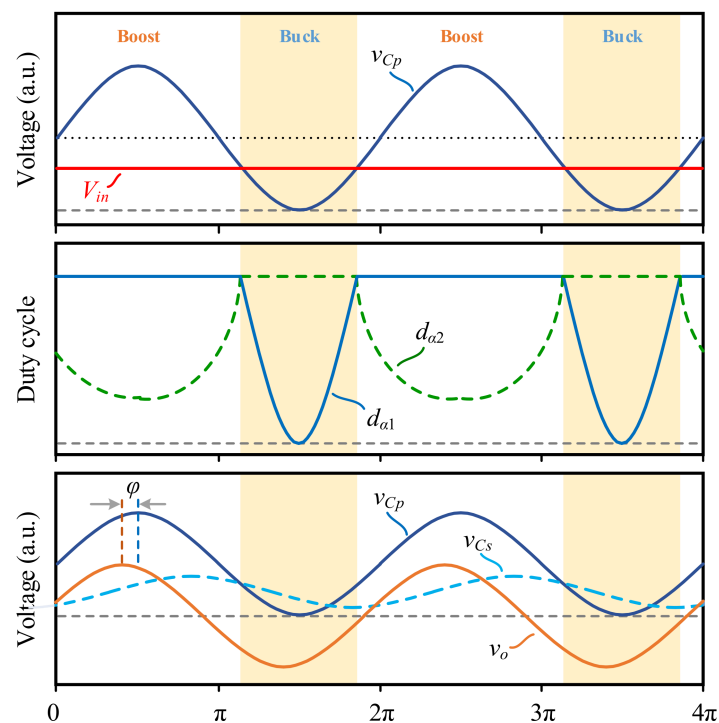


Figure 3. Modulation waveforms illustrating the buck-to-boost transition and dual duty-cycle generation.

4.3. Model-Based Compensation of the Series-Capacitor Voltage Drop

Because Equation (6) gives k_v in closed form for the known C_s , C_o , and R , the reference is scaled before operation by the compensation factor:

$$k_{comp} = \frac{1}{k_v} = \sqrt{\left(1 + \frac{C_o}{C_s}\right)^2 + \left(\frac{X_{C_s}}{R}\right)^2} \quad (19)$$

so that the compensated reference and its amplitude become:

$$v_{a,comp}(t) = \sqrt{2} V_o k_{comp} (\sin(\omega_o t) + 1), \quad V_{a,pk} = \sqrt{2} V_o k_{comp} \quad (20)$$

Substituting this amplitude into Equation (6) gives:

$$V_{o,actual,comp} = k_v \frac{\sqrt{2} V_o k_{comp}}{\sqrt{2}} = V_o k_{comp} k_v = V_o \quad (21)$$

that is, the target output is restored exactly, because by construction $k_{comp} = 1/k_v$. The compensated modulation index is:

$$m_{a,comp}(t) = \frac{\sqrt{2} V_o k_{comp} (\sin(\omega_o t) + 1)}{V_{in}} \quad (22)$$

and Equation (17) applies unchanged, with m_a replaced by $m_{a,comp}$.

Since the proposed compensation is open-loop, the compensation factor is calculated only once for each intended operating condition and stored in the digital signal processor (DSP) as a constant coefficient. Three values, listed in Table 2, cover the 10–100% load range of the prototype. No online estimation, adaptive update or output-voltage measurement is performed during operation. Note also that Equation (19) contains no V_{in} , so a given load resistance yields the same k_{comp} at every input voltage. The input voltage acts only on the modulation index through Equation (22), and hence on the buck or boost regime.

Table 2. Series-blocking capacitance sizing at the two tested load conditions ($V_{in} = 95$ V, $m_{a,lim} = 4$).

Load Condition	R (Ω)	k_v , Equation (6)	$C_{s,min}$ (μ F), Equation (29)
Full load	40	0.9310	110
Light load	400	0.9696	33.2

4.4. Operating Limits and Load Sensitivity

Because the reference amplitude in Equation (20) is scaled by k_{comp} , so is the modulation index. The peak value reached by Equation (22) is:

$$m_{a,pk} = \frac{2\sqrt{2} V_o k_{comp}}{V_{in}} = k_{comp} m_{a,max} \quad (23)$$

which supersedes the uncompensated limit of Equation (14): the maximum modulation index does include the compensation scaling. Its realizable upper bound is not $m_a = 1$, since the converter is deliberately operated with $m_a > 1$ throughout the boost regime, but the smallest boost duty ratio $d_{\alpha 2,min} = 1/m_{a,lim}$ that the modulator can produce, which is set by the dead time and the minimum switch on-time at f_s . Hence:

$$m_{a,pk} \leq m_{a,lim} = \frac{1}{d_{\alpha 2,min}} \Leftrightarrow V_{in} \geq V_{in,min} = 2\sqrt{2} k_{comp} V_o d_{\alpha 2,min} \quad (24)$$

A conservative controller-imposed minimum duty ratio $d_{\alpha 2,min} = 0.25$ is adopted for the prototype to leave sufficient margin for digital pulse resolution, transient operation, parasitic voltage drops, and current ripple. This constraint is not dictated by the converter topology itself, but is selected as a conservative control limit that guarantees adequate PWM pulse width at the 50 kHz switching frequency within the resolution of the digital signal processor. This choice yields $m_{a,lim} = 4$, corresponding to a minimum allowable input voltage of $V_{in,min} = 83.5$ V at full load, whereas the experimental operating point $V_{in} = 95$ V operates at $m_{a,pk} = 3.52$.

The accuracy of an open-loop gain depends on how closely the actual load matches the design value. Differentiating Equation (19) gives the normalized sensitivity:

$$S_R = \frac{R}{k_{comp}} \frac{\partial k_{comp}}{\partial R} = -\frac{(X_{C_s}/R)^2}{k_{comp}^2} \quad (25)$$

For the prototype ($C_s = 220$ μ F, $f_o = 60$ Hz, $X_{C_s} = 12.06$ Ω), the normalized sensitivity equals -0.0788 at the rated (40 Ω) and -0.0009 at the light-load (400 Ω) condition, respectively. Therefore, if the actual load resistance differs from the design value by $\pm 10\%$, the resulting steady-state output-voltage deviation remains below 0.8%.

Since the proposed compensation is purely open-loop, the compensation factor remains unchanged during load transients until a new coefficient is selected. Consequently,

temporary steady-state voltage deviations may appear under abrupt load changes. If tighter voltage regulation is required, Equation (19) can be incorporated as the feedforward term of a conventional outer voltage-control loop.

5. Design Guidelines

The component values follow from the steady-state model of Sections 3 and 4. Each criterion is expressed in closed form and evaluated for the prototype in Tables 2 and 3.

Table 3. Compensation factor and compensated peak modulation index (23) versus input voltage ($V_o = 110 \text{ V}_{rms}$); k_{comp} is independent of V_{in} .

Load Condition	k_{comp} , Equation (19)	$m_{a,pk}$, $V_{in} = 95 \text{ V}$	$m_{a,pk}$, $V_{in} = 400 \text{ V}$
Full load, 40 Ω	1.0741	3.518	0.835
Light load, 400 Ω	1.0313	3.378	0.802

5.1. Energy-Storage Inductor

The inductor L_1 is dimensioned to limit the high-frequency ripple to a fraction γ of the maximum inductor current. In the boost regime, which governs that maximum:

$$\Delta i_{L_1} = \frac{V_{in} D_4}{L_1 f_s}, \quad D_4 = 1 - d_{a2} = 1 - \frac{1}{m_a} \quad (26)$$

where D_4 is largest at the peak of the reference. Imposing $\Delta i_{L_1} \leq \gamma I_{L_1,max}$ gives:

$$L_1 \geq \frac{V_{in} D_{4,max}}{f_s \gamma I_{L_1,max}} \quad (27)$$

The maximum inductor current is not obtained from a closed-form estimate, because the instantaneous power of a single-phase stage pulsates at twice the line frequency and the conduction intervals depend on the duty ratio. It is instead taken as the largest time-domain value over the operating range.

5.2. Intermediate Capacitor

The intermediate capacitor C_p buffers the boost half-bridge and attenuates the high-frequency ripple at node “a”. It is sized to keep Δv_{C_p} within 1–2% of the maximum node voltage $V_{a,max}$ of Equation (30):

$$C_p \geq \frac{I_{L_1,max} D_{4,max}}{f_s \Delta v_{C_p,max}} \quad (28)$$

A polypropylene or ceramic capacitor with a low equivalent series resistance (ESR) is recommended. With the switching-cell passives fixed, the remaining degree of freedom is the series-blocking capacitance, which sets the retention factor and hence the compensation gain.

5.3. Series-Blocking Capacitor

The series-blocking capacitor is the most critical passive component: through Equations (6) and (19), it sets the retention factor and the compensation gain, and through Equation (32) its own voltage rating. It influences Equation (6) through two distinct parameters: the load-independent capacitive-divider ratio C_o/C_s and the load-dependent reactive term X_{C_s}/R . Consequently, the two attenuation mechanisms respond differently to a change in capacitance: at the prototype ratio $C_s/C_o \approx 32$, a further 10% increase in capacitance improves k_v by 0.95% at full load, but by only 0.28% at light load where the fixed divider dominates. Beyond this point, the volume and cost penalties outweigh the marginal gain.

A lower bound on C_s follows directly from the modulation limit in Equation (24). Substituting the largest admissible compensation factor into Equation (19) yields a quadratic equation in $1/C_s$ whose positive root is:

$$C_{s,\min} = \frac{a}{\sqrt{C_o^2 + a(k_{comp,\max}^2 - 1) - C_o}}, \quad a = C_o^2 + \frac{1}{(\omega_o R)^2}, \quad k_{comp,\max} = \frac{m_{a,\lim} V_{in}}{2\sqrt{2} V_o} \quad (29)$$

Table 2 lists the resulting design coefficients: the selected $C_s = 220 \mu\text{F}$ provides a factor-of-two margin over Equation (29) at full load, and the reduced-capacitance case examined in Section 6 sits exactly on that bound, which is consistent with the loss of regulation observed there.

5.4. Operating Region and Input-Voltage Range

The admissible input-voltage range is bounded below by Equation (24) and unbounded above: for $V_{in} \geq 2V_{a,pk}$. The reference never crosses the input level and the converter operates purely in the buck region. Table 3 evaluates Equation (23) for two load conditions at the minimum (95 V) and maximum (400 V) input voltages considered in Section 6.

The compensation factor k_{comp} depends solely on the output network and is independent of V_{in} , whereas the compensated peak modulation index $m_{a,pk}$ decreases as V_{in} increases. Consequently, the 95 V case requires mixed buck–boost operation ($m_{a,pk} > 1$), whereas the 400 V case operates entirely in the buck region ($m_{a,pk} < 1$).

All entries satisfy Equation (24) with $m_{a,\lim} = 4$. The resulting compensated reference amplitude $V_{a,pk}$ serves as the baseline for deriving all device voltage and current stresses.

5.5. Component Voltage and Current Stress

The compensation raises the synthesized reference by k_{comp} , so every voltage stress derived from the node “a” potential scales accordingly. From Equation (20):

$$V_{a,\max} = 2V_{a,pk} = 2\sqrt{2} V_o k_{comp} \quad (30)$$

The upper half-bridge is clamped to V_{in} under all conditions, whereas S_3 and S_4 are tied to the switching node “a”:

$$V_{S1,\max} = V_{S2,\max} = V_{in}, \quad V_{S3,\max} = V_{S4,\max} = V_{a,\max} \quad (31)$$

Equation (30) gives 334.2 V at full load and 320.9 V at light load for $V_{a,\max}$, against the 311.1 V predicted by the uncompensated expression $2\sqrt{2}V_o$. The compensated values agree with the peak of approximately 331 V observed in Section 6, confirming that the k_{comp} scaling must be retained in the device rating. The blocking stress on S_3 falls to zero during buck operation, where it is clamped permanently ON. The series capacitor must withstand the DC bias of Equation (2) plus the peak of Equation (10):

$$V_{C_s,\max} = \left| \sqrt{2} V_o k_{comp} - V_{in} \right| + \sqrt{2} V_{C_s,AC,rms} \quad (32)$$

which yields 119.2 V at full load and 72.2 V at light load for $V_{in} = 95$ V, so a film capacitor rated to roughly twice $V_{C_s,\max}$ provides adequate margin. The RMS current of a device is set by its own conduction interval:

$$I_{S_k,rms} = \sqrt{\frac{1}{T_o} \int_0^{T_o} g_k(t) i_{L_1}^2(t) dt} \quad (33)$$

where $g_k(t)$ is the conduction function of S_k , equal to unity while the device conducts and zero otherwise. Because the conduction intervals are set by the operating regime, the most heavily loaded device changes with the input voltage: S_1 under low-input-voltage operation and S_3 under pure-buck operation. The individual device RMS currents used in the loss calculation are therefore extracted from the time-domain switching waveforms. Since

Equations (6), (19), (29), and (30) depend only on the passive output-network parameters and the target output, the same procedure scales directly to other power ratings and output voltages.

6. Simulation and Experimental Results

6.1. Validation of the Analytical Model by Simulation

The proposed CG-SCC-BBI and its model-based compensation were verified by time-domain simulation in PLECS, covering both boost and buck operation to confirm the full buck–boost capability. The power stage operates at a switching frequency of $f_s = 50$ kHz with a 250 ns dead time to synthesize a 60 Hz, 110 V_{rms} AC output. To evaluate parameter sensitivity and validate the operating limits predicted by Equations (24) and (29), two series capacitance values were tested: the nominal design value ($C_s = 220$ μ F) and a halved capacitance ($C_s = 110$ μ F). Furthermore, testing under two distinct DC input voltages—95 V for low-input-voltage operation and 400 V for high-input-voltage, pure-buck operation—demonstrates the wide-input capabilities of the converter. The evaluation spans the full operating power range from 10% (30 W, $R = 400$ Ω) to 100% (300 W, $R = 40$ Ω) of the rated load. All simulation waveforms were recorded from $t = 0.4$ s to 0.5 s to ensure that steady-state conditions were reached. The simulation parameters are summarized in Table 4, matching those of the experimental prototype in Section 6.2 for direct consistency.

Table 4. Simulation and prototype parameters.

Parameter	Symbol	Value
DC input voltage	V_{in}	95 V, 400 V
Target RMS output voltage	V_o	110 V_{rms}
Output frequency	f_o	60 Hz
Switching frequency	f_s	50 kHz
Dead time	t_d	250 ns
Energy-storage inductor	L_1	250 μ H, measured ESR 0.11 Ω
Intermediate capacitor	C_p	6.8 μ F/400 V film (WCAP-FTBE)
Output filter capacitor	C_o	6.8 μ F/400 V film (WCAP-FTBE)
Series-blocking capacitor	C_s	220 μ F nominal; 110 μ F reduced
Full load (100%)	R, P_o	40 Ω , 300 W
Light load (10%)	R, P_o	400 Ω , 30 W
Power devices	S_1 – S_4	C2M0080120D SiC MOSFET (1200 V, 36 A, 80 m Ω)

6.1.1. Steady-State Operation at Low Input Voltage

At $C_s = 220$ μ F, the compensated reference from Equation (20) successfully maintains the output close to the 110 V_{rms} target across both load conditions. Figure 4 illustrates the full-load operation (300 W) at $V_{in} = 95$ V, where the output is a clean 108.6 V_{rms} sinusoid. As required by Equation (13), the node “a” voltage remains strictly non-negative throughout the fundamental period, while the series capacitor carries a positive DC bias of $V_{C_s,DC} = 72.1$ V, consistent with Equations (2) and (20). The switch-stress profile in Figure 5 is dictated by the topology rather than the load: S_1 and S_2 are clamped to the 95 V input, whereas S_3 and S_4 block approximately 331 V.

Figure 6 repeats this test at 30 W light load using the same reference law, adjusting only k_{comp} , which directly confirms Equation (9) in the time domain. Here, the total current forced through C_s is 0.394 A_{rms} , whereas the resistive load branch draws only $V_o/R = 0.275$ A_{rms} . The remaining 0.282 A_{rms} represents the current through the filter capacitor C_o . Because this filter current is load-independent, it becomes dominant as the load lightens. This behavior clearly demonstrates why omitting C_o from the compensation model is untenable: a phenomenon masked at 300 W full load where the same 0.282 A constitutes less than 10% of the resistive load current.

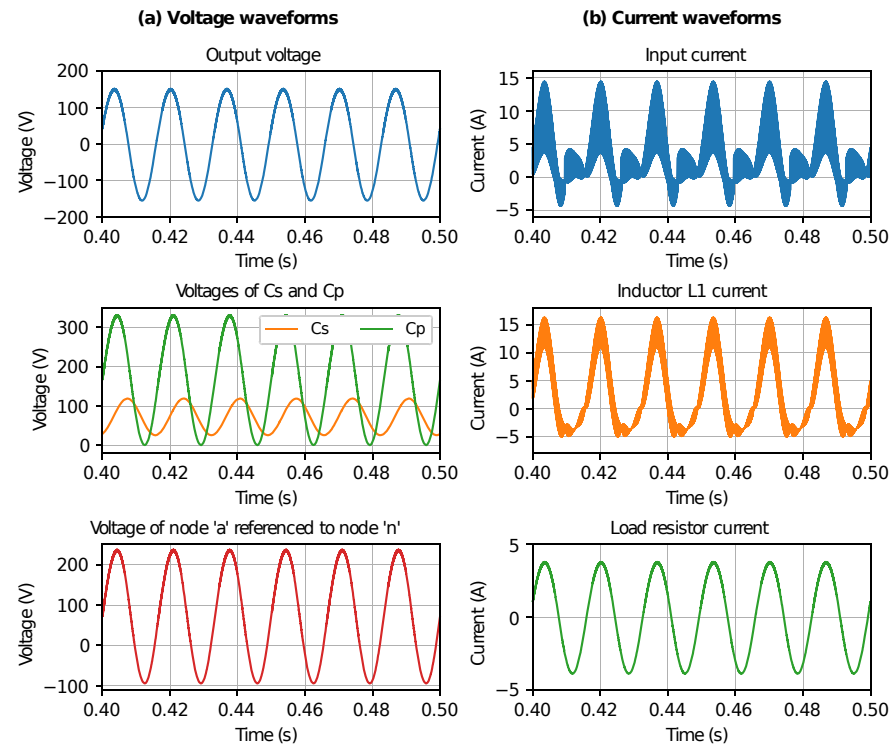


Figure 4. Full-load steady-state waveforms at low input voltage (300 W, $V_{in} = 95$ V, $C_s = 220$ μ F): (a) voltages v_o , v_a , v_{Cp} , v_{Cs} ; (b) currents i_{L1} , i_R , i_{Cs} .

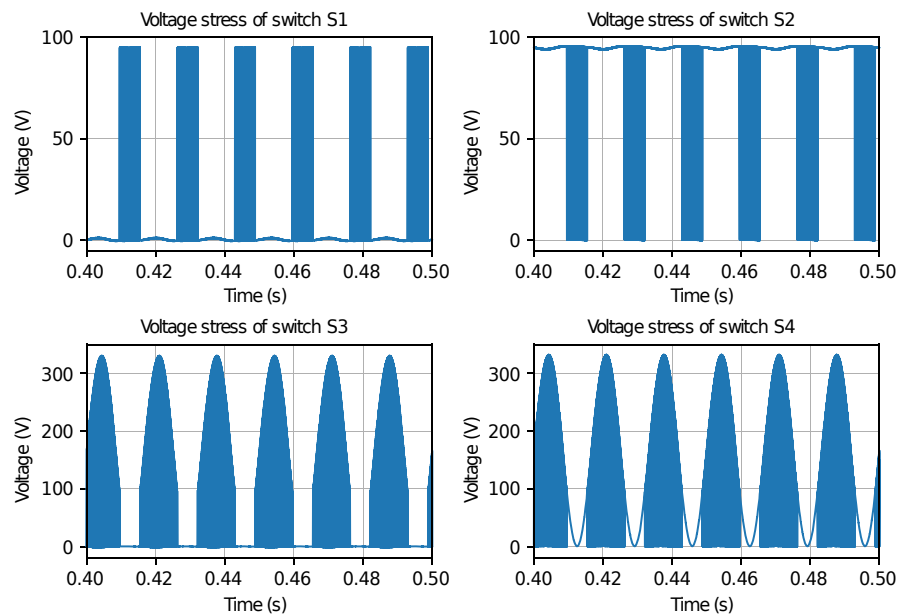


Figure 5. Switch voltage-stress waveforms at low input voltage (300 W, $V_{in} = 95$ V, $C_s = 220$ μ F).

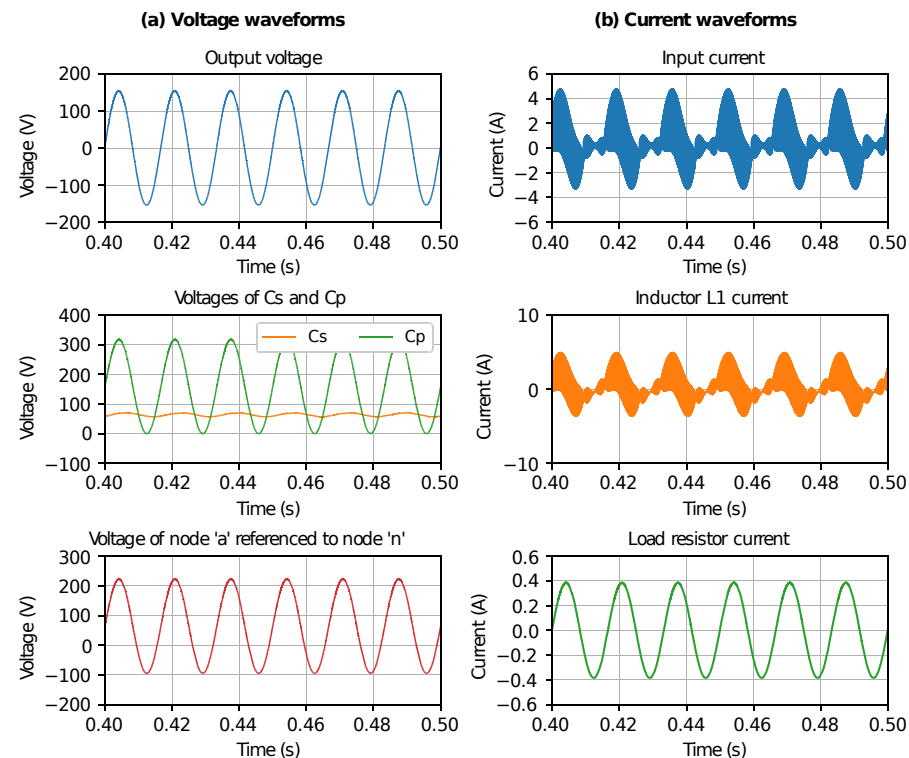


Figure 6. Light-load steady-state waveforms at low input voltage (30 W, 10% of rated power, $V_{in} = 95$ V, $C_s = 220$ μ F): (a) voltages; (b) currents.

6.1.2. Steady-State Operation at High Input Voltage

Raising the input voltage to 400 V while maintaining the same 110 V_{rms} target demonstrates the converter's buck capability, confirming true buck–boost operation alongside the low-input results. Figure 7 illustrates the inverter stepping 400 V down to 110 V_{rms} . From Equation (23), the peak modulation index is $m_{a,pk} = 0.835$. Since $m_{a,pk} < 1$ throughout the fundamental period, the boundary condition Equation (18) has no solution, and hence the converter never enters the boost region and operates with $d_{a2} = 1$ continuously. The corresponding switch voltage-stress profiles under high input voltage are presented in Figure 8.

Varying V_{in} introduces two fundamental operating changes predicted by the steady-state model in Section 3: As V_{in} increases, the DC bias across C_s ($V_{Cs,DC} = \sqrt{2} k_{comp} V_o - V_{in}$) reverses polarity, shifting from +72.1 V at $V_{in} = 95$ V to −232.9 V at $V_{in} = 400$ V. Because the fundamental AC voltage across C_s remains constant at 33.3 V_{rms} , the peak voltage stress $V_{Cs,max}$ reaches its worst-case maximum (280.1 V) during high-input buck operation, establishing $V_{in} = 400$ V as the critical design point for dimensioning C_s . At low input voltage ($V_{in} = 95$ V), S_3 and S_4 withstand the peak node “a” potential of 334 V, while S_1 and S_2 are clamped to the 95 V DC rail. Conversely, at high input voltage ($V_{in} = 400$ V), S_1 and S_2 execute high-frequency PWM and block the full 400 V DC bus, whereas S_4 withstands the peak node “a” potential (334 V) and S_3 remains clamped permanently ON with virtually zero blocking stress.

Figure 9 completes the experimental matrix under the light-load condition (30 W) at high input voltage. The output voltage is held at 109.9 V_{rms} using the same compensation coefficient as at 95 V. The series-capacitor DC bias settles at −240.0 V with a fundamental AC ripple of 4.74 V_{rms} , closely matching the values predicted by Equations (2) and (10). Figure 10 shows the corresponding light-load switch stress waveforms.

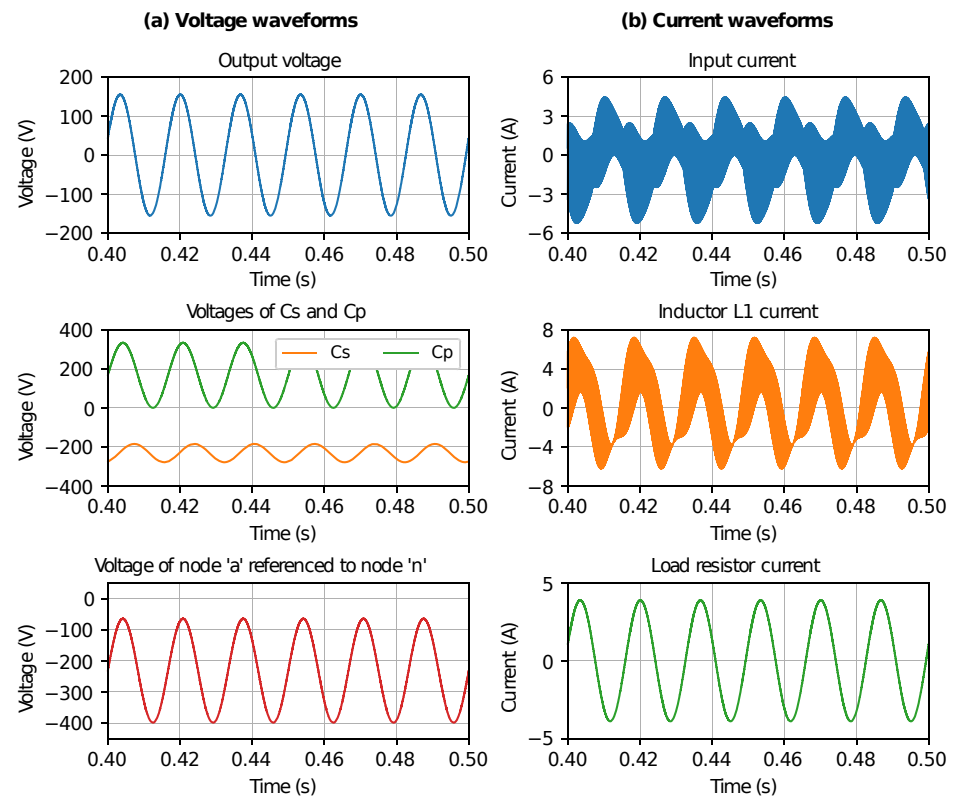


Figure 7. Full-load steady-state waveforms at high input voltage (300 W, $V_{in} = 400$ V, $C_s = 220$ μ F): (a) voltages; (b) currents.

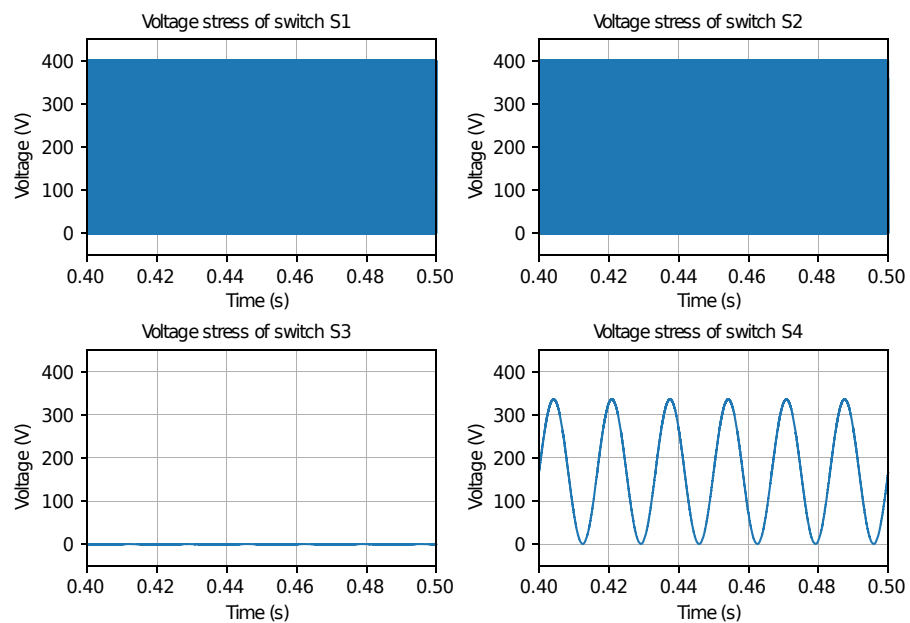


Figure 8. Switch voltage-stress waveforms at high input voltage (300 W, $V_{in} = 400$ V, $C_s = 220$ μ F).

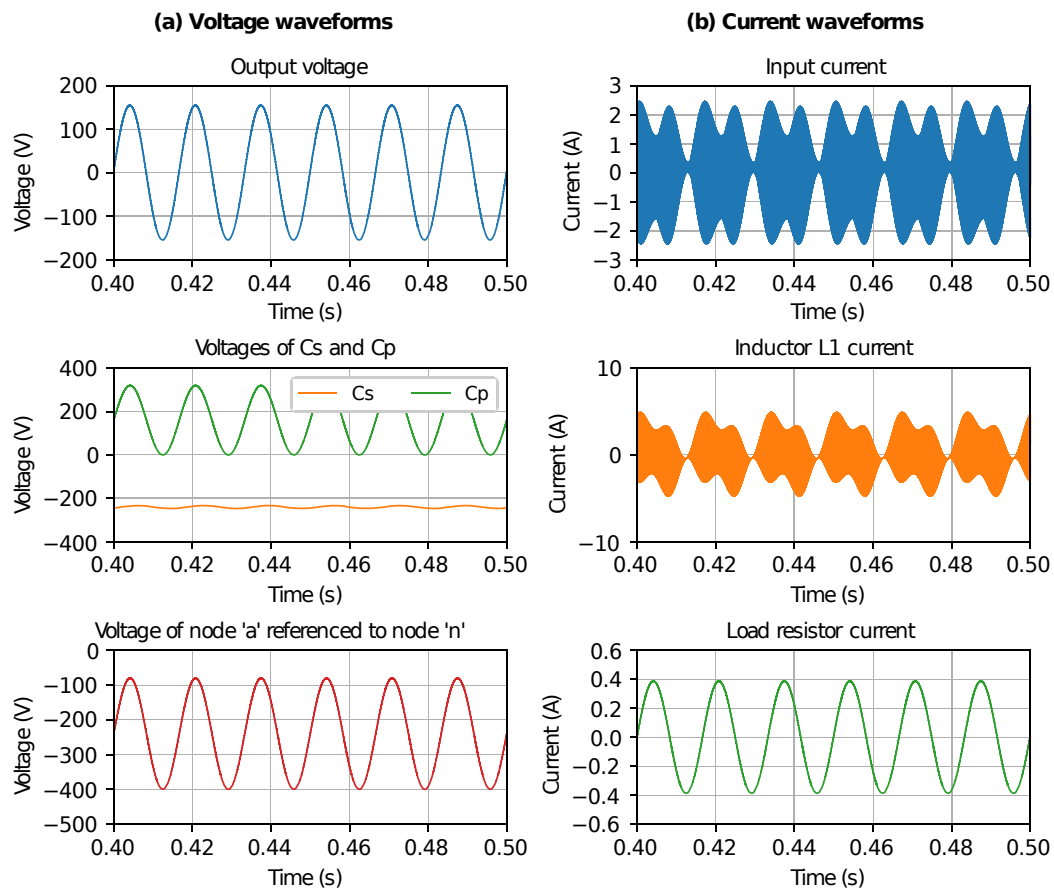


Figure 9. Light-load steady-state waveforms at high input voltage (30 W, 10% of rated power, $V_{in} = 400$ V, $C_s = 220$ μ F): (a) voltages; (b) currents.

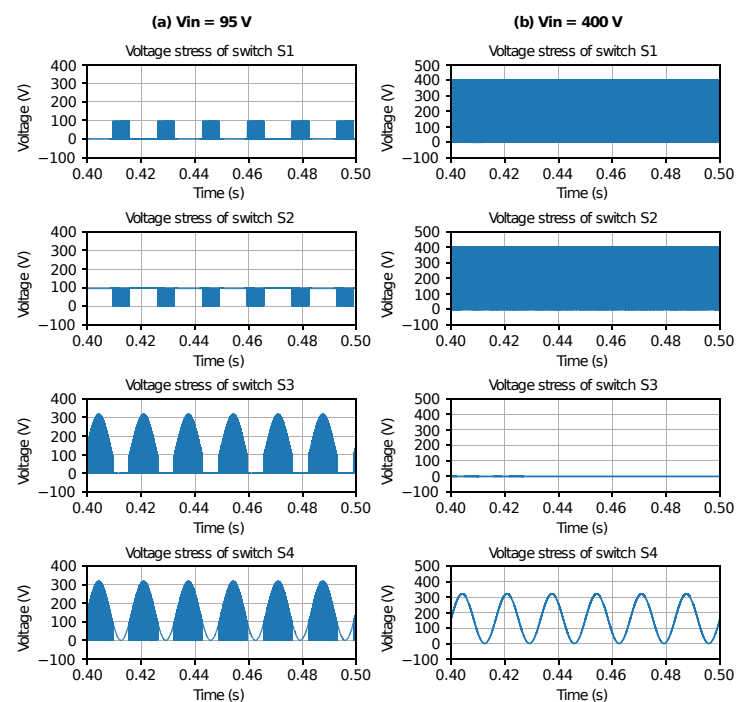


Figure 10. Simulated switch voltage-stress waveforms at the light-load condition (30 W, $C_s = 220$ μ F): (a) $V_{in} = 95$ V; (b) $V_{in} = 400$ V.

6.1.3. Verification of the Voltage-Retention Factor and of the Compensation Law

The primary objective of the simulation was to quantitatively verify the voltage-retention factor derived in Equation (6) and the model-based compensation strategy proposed in Equation (19). From the simulated output RMS voltage $V_{o,sim}$, the realized retention factor $k_{v,sim}$ is extracted as:

$$k_{v,sim} = \frac{V_{o,sim}}{k_{comp} V_o} \quad (34)$$

and the corresponding residual voltage-regulation error ε_V is defined as:

$$\varepsilon_V = \frac{V_{o,sim} - V_o}{V_o} \times 100\% \quad (35)$$

where $V_o = 110 V_{rms}$ is the target of Equation (13) and k_{comp} the coefficient of Equation (19) evaluated for the load under test. Table 5 compares Equation (34) with the analytical value Equation (6).

Table 5. Analytical prediction versus simulation of the output-network model and of the compensated output voltage ($C_s = 220 \mu\text{F}$).

Operating Point	$R (\Omega)$	k_{comp} , Equation (19)	k_v , Equation (6)	$k_{v,sim}$, Equation (34)	$V_{o,sim} (V_{rms})$	$\varepsilon_V (\%)$, Equation (35)
Full load, $V_{in} = 95 \text{ V}$ (300 W)	40	1.0741	0.9310	0.9188	108.56	−1.31
Light load, $V_{in} = 95 \text{ V}$ (30 W)	400	1.0314	0.9696	0.9596	108.87	−1.03
Full load, $V_{in} = 400 \text{ V}$ (300 W)	40	1.0741	0.9310	0.9327	110.20	+0.18
Light load, $V_{in} = 400 \text{ V}$ (30 W)	400	1.0314	0.9696	0.9683	109.85	−0.14

Table 5 compares the analytical predictions with the simulation results across all four extreme operating corners (full/light load under 95 V and 400 V inputs). The circuit-level retention factor $k_{v,sim}$ agrees with the analytical value k_v from Equation (6) to within 1.3%, while the residual output-regulation error ε_V stays well below 1.31% in all tested cases.

The minor deviation observed at $V_{in} = 95 \text{ V}$ (−1.31% at full load and −1.03% at light load) stems primarily from the higher current stress inherent to boost operation. At low input voltage, the converter processes significantly higher inductor and switch currents, which magnify the fundamental-frequency voltage ripple across the energy-buffer capacitors (C_p and C_s) and induce slight parasitic conduction drops across the power stage. Conversely, at $V_{in} = 400 \text{ V}$, the system operates entirely in the buck regime with substantially lower operating currents, minimizing these secondary effects and improving the analytical-to-simulation agreement to +0.18% and −0.14%.

6.1.4. Component Voltage and Current Evaluation

Table 6 compares the analytically predicted component-voltage stresses with the simulation results at the four operating corners. These points cover the minimum and maximum input voltages as well as 10% and 100% of rated power. The analytical predictions agree closely with the simulation results, confirming that the revised model provides sufficiently accurate estimates for semiconductor and capacitor voltage ratings. In particular, the model correctly predicts the polarity reversal of the series-capacitor dc bias between the 95 V and 400 V operating conditions. The small discrepancies are mainly attributed to switching ripple, dead time, and nonideal circuit elements included in the simulation.

Table 7 summarizes the RMS currents of the energy-storage inductor and the power switches at the rated output power (300 W) under the two extreme input-voltage conditions. At 95 V, the energy-storage inductor and switch S_1 carry the highest RMS currents because the converter operates in the buck–boost mode with a large input current. At 400 V, the higher input voltage leads to a substantial reduction in the input current, resulting in lower

RMS currents in L_1 and S_1 . In this pure buck operating regime, S_3 conducts the main inductor current, while the current through S_4 becomes negligible.. These results provide useful guidance for component current ratings and thermal design.

Table 6. Component voltage stress: analytical prediction versus simulation at the four operating corners ($C_s = 220 \mu\text{F}$).

Quantity	30 W, 95 V (ana./sim.)	300 W, 95 V (ana./sim.)	30 W, 400 V (ana./sim.)	300 W, 400 V (ana./sim.)
Peak node "a" voltage $V_{a,max}$ (V)	320.9/318.0	334.2/331.6	320.9/320.2	334.2/333.8
S_3 blocking voltage (V)	320.9/318.0	334.2/330.6	0/ ≈ 0	0/ ≈ 0
S_4 blocking voltage (V)	320.9/318.1	334.2/332.3	320.9/320.4	334.2/331.1
Series-capacitor DC bias $V_{C_s,DC}$ (V)	+65.4/+63.9	+72.1/+72.3	−239.6/−238.0	−232.9/−231.0
Series-capacitor AC voltage $V_{C_s,AC}$ (V_{rms})	4.75/4.70	33.33/32.90	4.75/4.74	33.33/33.34
Peak absolute series-capacitor voltage $V_{C_s,max}$ (V)	72.2/70.6	119.2/118.7	246.3/245.7	280.1/279.2

Table 7. Simulated RMS currents of the energy-storage inductor and of the power switches at the rated output power of 300 W under low- and high-input-voltage operation.

Operating Regime	$I_{L1,rms}$	$I_{S1,rms}$	$I_{S2,rms}$	$I_{S3,rms}$	$I_{S4,rms}$
Boost/mixed, $V_{in} = 95 \text{ V}$	7.557	7.403	1.516	4.511	6.063
Pure buck, $V_{in} = 400 \text{ V}$	4.013	2.826	2.850	4.013	≈ 0

6.1.5. Sensitivity to Series Capacitance

To evaluate the parameter robustness of the proposed model-based compensation and validate the theoretical lower capacitance bound $C_{s,min}$ derived in Equation (29), a deliberate parameter mismatch scenario was simulated. The series capacitance C_s was halved to 110 μF while the open-loop compensation factor k_{comp} was held fixed at the nominal 220 μF design value. This tests the ability of the analytical expression Equation (6) to accurately predict off-design system performance under uncompensated impedance variations.

Table 8 compares the analytically predicted output voltages with the circuit simulation results, and Figure 11 overlays the corresponding output voltage waveforms at full load (300 W) for both $V_{in} = 95 \text{ V}$ and $V_{in} = 400 \text{ V}$.

Table 8. Output voltage when C_s is halved to 110 μF while k_{comp} is held at its 220 μF value.

Operating Point	k_v at 110 μF , Equation (6)	V_o predicted (V_{rms})	V_o simulated (V_{rms})	Deviation from Target (%)
Full load, $V_{in} = 95 \text{ V}$ (300 W)	0.8190	96.8	96.38	−12.4
Full load, $V_{in} = 400 \text{ V}$ (300 W)	0.8190	96.8	97.10	−11.7

The simulation results agree with the analytical predictions derived from Equation (6) to within 0.42 V across both input voltage extremes. Halving C_s increases the uncompensated series reactance X_{C_s} , resulting in an output voltage drop of approximately 12.4% at 95 V (96.38 V_{rms}) and 11.7% at 400 V (97.10 V_{rms}). The close agreement with the predicted value of 96.8 V_{rms} quantitatively confirms the accuracy of the retention model in Equation (6) under off-design operating conditions.

Furthermore, as illustrated in Figure 11, the output voltage maintains a clean sinusoidal waveform without harmonic degradation, which shows that a parameter mismatch produces purely an amplitude regulation error rather than waveform distortion. It should be emphasized that the 110 μF case is not a compensated design evaluated at the theoretical boundary, because k_{comp} is deliberately retained at its nominal 220 μF value. It

is a 50% parameter-mismatch test. Recomputing the coefficient for $C_s = 110 \mu\text{F}$ would give $k_{\text{comp}} \approx 1.221$ and would restore the $110 V_{\text{rms}}$ target, at the cost of a compensated peak modulation index approaching the limit set by Equation (24). This is the practical significance of $C_{s,\text{min}}$, and it is why a nominal $220 \mu\text{F}$ is selected for the prototype: the resulting factor-of-two margin absorbs component manufacturing tolerances and ageing while keeping the required compensation gain far from the modulation limit.

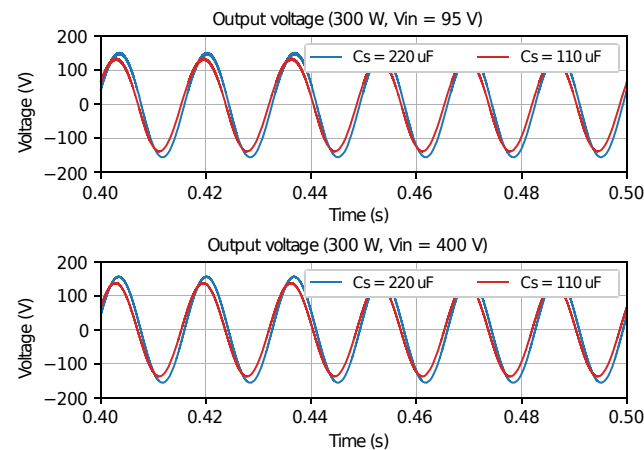


Figure 11. Output-voltage comparison at 300 W for $C_s = 220 \mu\text{F}$ and $C_s = 110 \mu\text{F}$, with the compensation factor fixed at its $220 \mu\text{F}$ value: (a) $V_{\text{in}} = 95 \text{ V}$; (b) $V_{\text{in}} = 400 \text{ V}$.

6.1.6. Operation with a Nonlinear Load

Rectifier-fed equipment represents a common load class for standalone AC supplies, drawing current in short pulses near the peak of the output voltage. To evaluate performance under nonlinear loading, the converter was simulated with the circuit shown in Figure 12, comprising a single-phase diode-bridge rectifier, a $560 \mu\text{F}$ smoothing capacitor, and an 80Ω load resistor. Because the series-blocking capacitor C_s carries the full pulsed rectifier current, this configuration imposes the most demanding steady-state operating condition on the coupling network analyzed in Section 3.

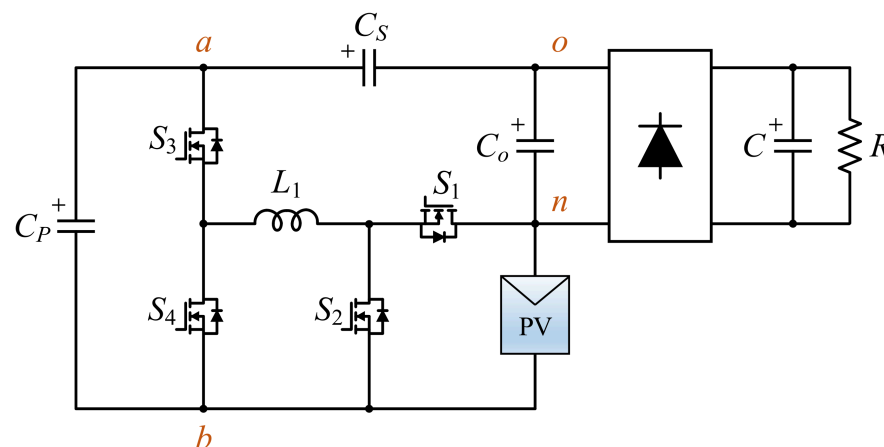


Figure 12. Nonlinear load configuration: a single-phase diode-bridge rectifier with a capacitive filter ($C = 560 \mu\text{F}$) and a resistive load ($R = 80 \Omega$).

Figures 13 and 14 present the steady-state waveforms under low-input and high-input conditions. In both cases, the output voltage exhibits the flat-topped waveform characteristic of capacitive rectifier loads, yielding RMS values of 107.6 V and 103.4 V while delivering 216 W and 204 W to the DC load, respectively. The rectified DC output voltage settles at 131.6 V (95 V input) and 127.7 V (400 V input) with a double-line-

frequency ripple of approximately 14 V, while the load resistor draws continuous currents of 1.64 A and 1.60 A. Driven by the pulsed current, the voltage across C_s experiences peak-to-peak excursions of 71 V and 69 V, both well within the film capacitor ratings established in Section 5.5.

Low-input-voltage operation, $V_{in} = 95 \text{ V}$

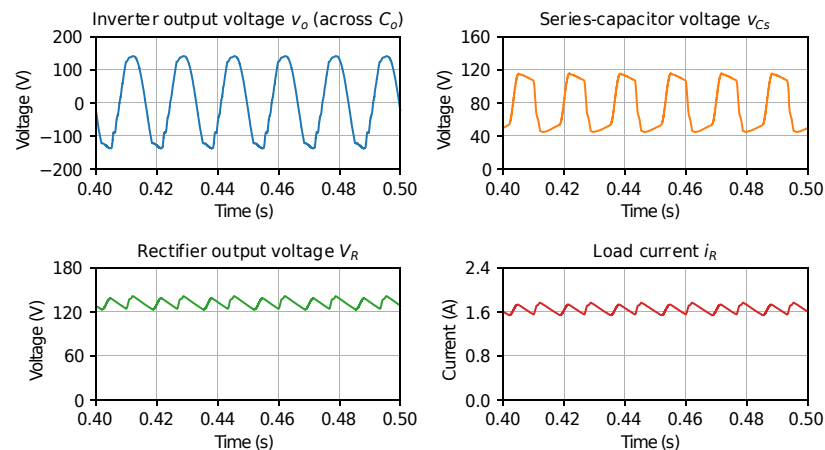


Figure 13. Simulated steady-state waveforms with the nonlinear load under low-input-voltage operation ($V_{in} = 95 \text{ V}$, $C = 560 \mu\text{F}$, $R = 80 \Omega$): output voltage v_o , series-capacitor voltage v_{Cs} , rectifier output voltage V_R , and load current i_R .

High-input-voltage operation, $V_{in} = 400 \text{ V}$

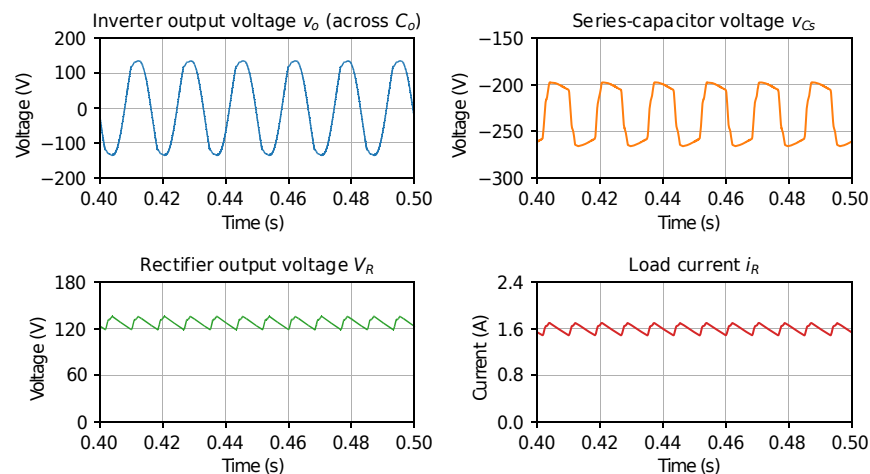


Figure 14. Simulated steady-state waveforms with the nonlinear load under high-input-voltage operation ($V_{in} = 400 \text{ V}$, $C = 560 \mu\text{F}$, $R = 80 \Omega$): output voltage v_o , series-capacitor voltage v_{Cs} , rectifier output voltage V_R , and load current i_R .

These results confirm that the converter maintains stability under nonlinear loads. The residual output RMS deviations (-2.2% at 95 V and -6.0% at 400 V relative to the $110 V_{rms}$ target) occur because the open-loop compensation factor is calculated from a resistive fundamental-frequency equivalent rather than the complex nonlinear input impedance. To fully restore the target voltage amplitude under such loads, either the equivalent fundamental resistance at the delivered active power must be substituted into Equation (3), or the open-loop compensation factor should serve as the feedforward term in an outer closed-loop voltage controller.

6.2. Experimental Validation

A laboratory prototype was constructed and evaluated to verify the analysis experimentally (Figure 15). The power stage uses C2M0080120D SiC MOSFETs (1200 V, 36 A, 80 m Ω , Wolfspeed, Durham, NC, USA) switching at 50 kHz. The energy-storage inductor L_1 has a nominal value of 250 μ H with a measured ESR of 0.11 Ω . WCAP-FTBE film capacitors (6.8 μ F, 400 V, Würth Elektronik, Waldenburg, Germany) are used for both the intermediate capacitor C_p and the output filter capacitor C_o for their low ESR, and the series-blocking capacitor C_s is implemented as two PILKOR PCPW-245 film capacitors (110 μ F, 450 V, PILKOR Electronics, Ansan, Republic of Korea) in parallel for an effective 220 μ F. The remaining parameters are those of Table 4.

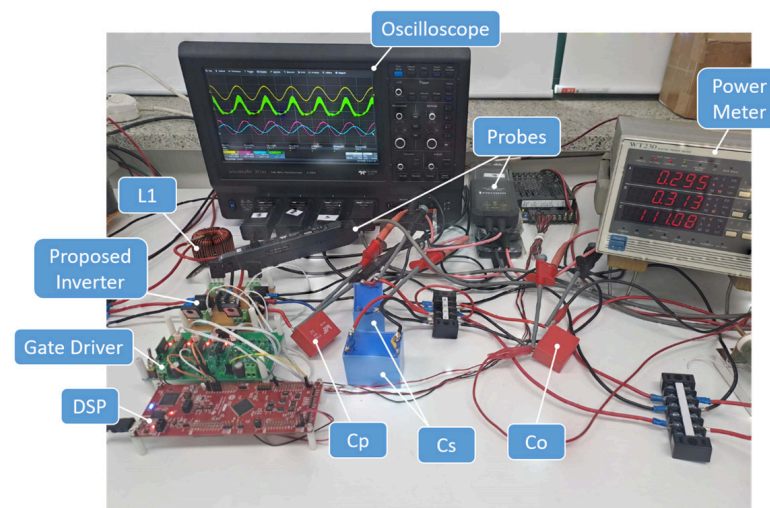


Figure 15. Experimental laboratory prototype of the proposed CG-SCC-BBI.

To evaluate performance across the 10–100% power range (40 Ω to 400 Ω), open-loop compensation scaling factors derived from Equation (19) were preloaded into the DSP. Under full-load operation (300 W), the prototype maintains precise output voltage regulation in both operating regimes using the fixed open-loop compensation. Under low-input-voltage operation ($V_{in} = 95$ V), the measured output voltage reaches 109.5 V_{rms} , representing a minor deviation of -0.45% relative to the 110 V_{rms} target. Under high-input-voltage operation ($V_{in} = 400$ V), the output voltage settles at 111.7 V_{rms} , corresponding to a residual regulation error of $+1.55\%$. These residual positive biases stem from component manufacturing tolerances (film capacitors and load resistors), finite DSP reference resolution, and sensor calibration accuracy, remaining well within the sensitivity limits predicted in Section 6.2.10.

6.2.1. Steady-State Operation at Low Input Voltage

Figure 16 illustrates the experimental steady-state performance at the rated output power of 300 W under low input voltage conditions. By applying the model-based voltage compensation factor derived from the analytical parameters and validated in simulation, the prototype synthesizes a clean sinusoidal output voltage of 109.5 V_{rms} . The small voltage error relative to the 110 V_{rms} target confirms both the single-stage voltage-boosting capability and the effectiveness of the proposed compensation scheme in counteracting the voltage drop across the series capacitor.

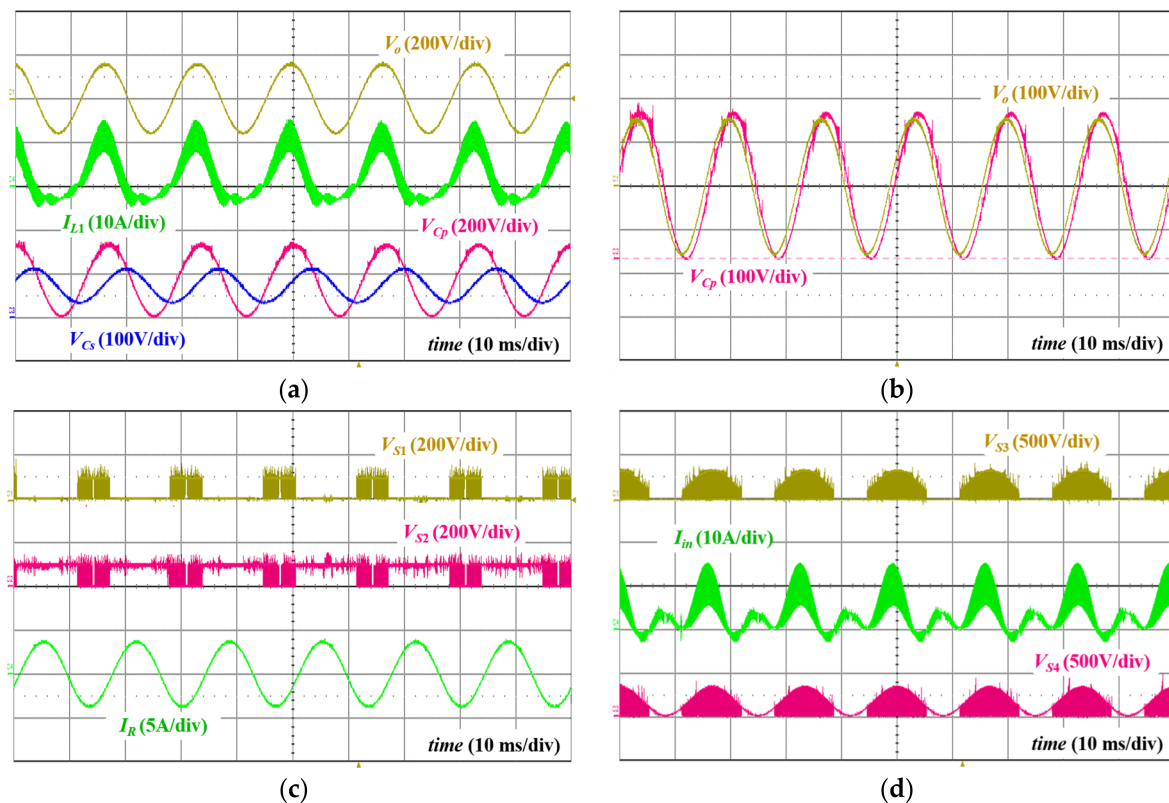


Figure 16. Experimental steady-state waveforms under full load at low input voltage (300 W, $V_{in} = 95$ V): (a) v_o , i_{L1} , v_{Cp} , v_{Cs} ; (b) v_o , v_{Cp} ; (c) v_{S1} , v_{S2} , i_R ; (d) v_{S3} , i_{in} , v_{S4} .

Regarding semiconductor stress, the off-state voltage across S_1 and S_2 is clamped at the 95 V input, confirming that high-frequency PWM switching is confined to a single half-bridge leg. S_3 and S_4 block the peak potential at node “a,” which aligns with the theoretical stress model presented in Section 5.

The measured displacement between the fundamental components of the output voltage v_o and the node potential v_{Cp} is approximately 13.4° compared with the 16.3° predicted by Equation (7) for an ideal network at full load. This small discrepancy is accounted for by the parasitic ESR of the capacitor bank and the winding resistance of inductor L_1 , which introduce a resistive component to the series branch and reduce the reactive angle. Nevertheless, the empirical load trend remains entirely consistent with the model: as the load resistance R increases and the reactance-to-resistance ratio X_{Cs}/R decays, the phase displacement collapses to 1.7° at high resistance levels.

6.2.2. Steady-State Operation at High Input Voltage

Experimental verification of pure-buck operation ($V_{in} = 400$ V) at rated power is shown in Figure 17, matching the simulation setup in Section 6.1.2. The inverter maintains a stable sinusoidal output with S_3 clamped fully ON while high-frequency PWM is executed exclusively by S_1 and S_2 , validating the predicted switching sequence, voltage-stress distribution, and wide-input-voltage capability.

Figure 17 also confirms the predicted DC-bias polarity reversal across C_s : as V_{in} exceeds the peak compensated output voltage, V_{Cs} transitions from positive to negative bias while its fundamental AC voltage ripple remains constant. These measured waveforms directly validate the theoretical model.

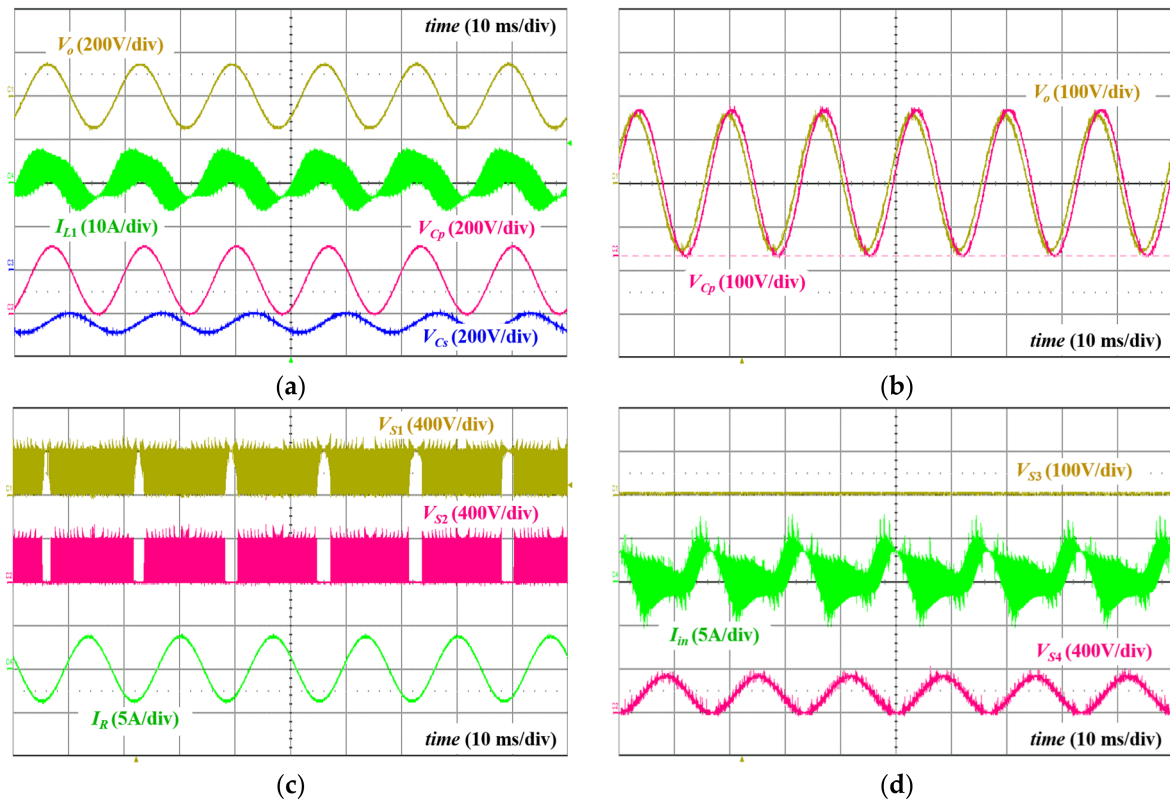


Figure 17. Experimental steady-state waveforms under full load at high input voltage (300 W, $V_{in} = 400$ V), where the converter remains in the buck region throughout the fundamental period: (a) v_o , i_{L1} , v_{Cp} , v_{Cs} ; (b) v_o , v_{Cp} ; (c) v_{S1} , v_{S2} , i_R ; (d) v_{S3} , i_{in} , v_{S4} .

6.2.3. Steady-State Operation Under Light-Load Condition

Figure 18 compares the experimental steady-state waveforms at 30 W, corresponding to 10% of the rated output power, for $V_{in} = 95$ V and $V_{in} = 400$ V. In both cases, the inverter maintains a stable sinusoidal output voltage. Because the load current is small, the fundamental-frequency voltage variation across the series capacitor C_s is also reduced. Consequently, the phase difference between the output voltage v_o and the intermediate-node voltage v_{Cp} becomes less pronounced than at rated load. The measured dc bias of C_s also follows the predicted operating behavior: it is positive at $V_{in} = 95$ V and negative at $V_{in} = 400$ V.

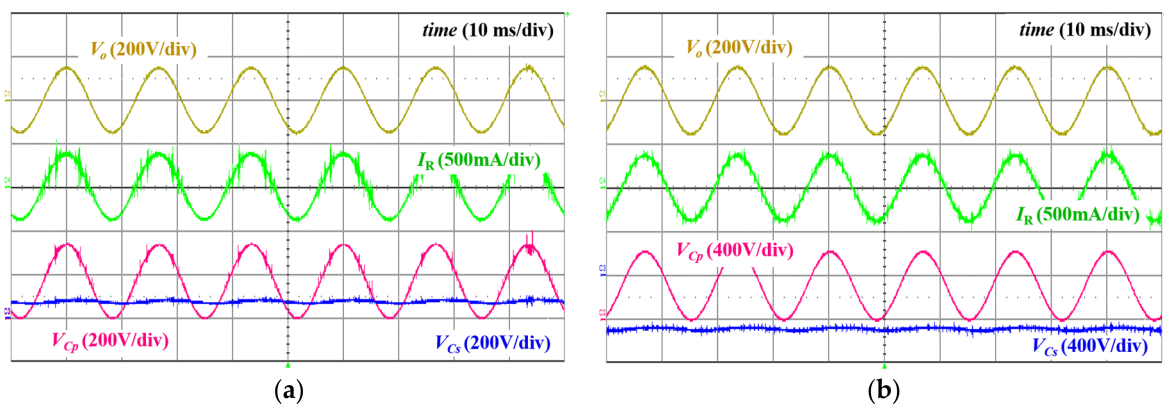


Figure 18. Experimental steady-state waveforms at the light-load condition (30 W, $R = 400 \Omega$, 10% of rated power): (a) low input voltage; (b) high input voltage.

6.2.4. Operation with a Reactive Load

To verify system performance under a reactive load, an inductive RL load with $R = 40\ \Omega$ and $L = 30\ \text{mH}$ was applied as shown in Figure 19, introducing a distinct phase shift between the voltages across the inductor (v_L) and the resistor (v_R). Despite this, v_R preserves its high-quality sinusoidal profile. Furthermore, v_{CS} and v_L exhibit stable steady-state waveforms, confirming stable operation of the proposed topology under a non-resistive load. The compensation coefficient used in this test remains based on the nominal resistive-load model. Extending the analytical compensation to a general complex load requires the load resistance in Equation (3) to be replaced by the corresponding load impedance, which changes both k_v and the phase angle of Equation (7).

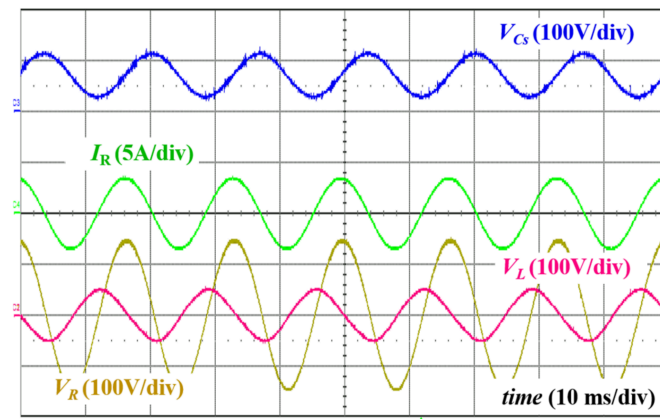


Figure 19. Experimental steady-state waveforms with an inductive (RL) load ($R = 40\ \Omega$, $L = 30\ \text{mH}$): series-capacitor voltage v_{CS} , load current i_R , load-resistor voltage v_R and inductor voltage v_L .

6.2.5. Operation with a Nonlinear Load

To evaluate performance under nonlinear loading, a single-phase diode-bridge rectifier with a $560\ \mu\text{F}$ DC-link capacitor and an $80\ \Omega$ DC load was connected to the inverter output (Figure 20). Despite the high-crest-factor pulsed current drawn by the rectifier, the inverter operates stably, preserving its output-voltage envelope with the typical flat-topping characteristics associated with capacitor-input rectifier loads.

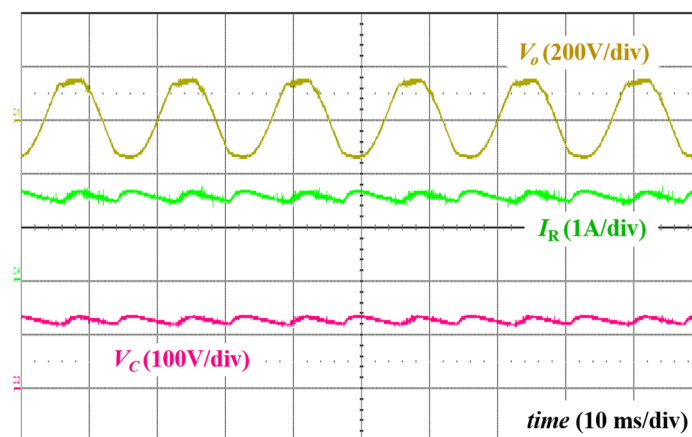


Figure 20. Experimental waveforms feeding a single-phase diode-bridge rectifier with a $560\ \mu\text{F}$ DC-link capacitor and a resistive DC load: output voltage v_o , output current i_o and rectified DC-link voltage.

6.2.6. Load-Step Transients

Figure 21 illustrates the transient performance during an abrupt transition from no-load to full-load conditions under both low and high input voltages. With the compen-

sation coefficient held fixed at its full-load value throughout the step, the test evaluates open-loop stability under an unannounced load change. The inverter exhibits a seamless dynamic response, settling rapidly to steady state without overshoot, ringing, or mode-transition instability. The slight voltage shift observed before the step corresponds to the difference between the no-load and full-load voltage-retention factors, as predicted by Equations (6) and (8).

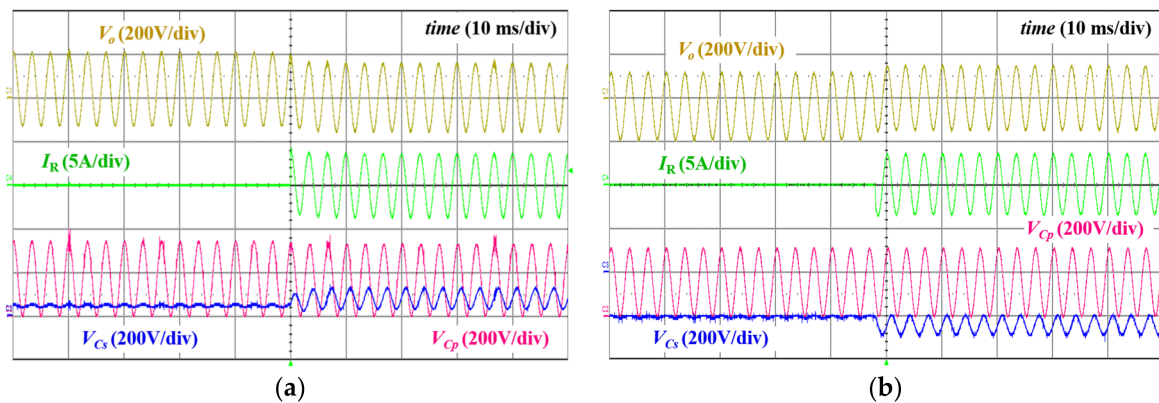


Figure 21. Experimental transient waveforms during the transition from no load to rated load: (a) low input voltage; (b) high input voltage.

Figure 22 further evaluates open-loop behavior during a load step from $100\ \Omega$ (121 W) to $50\ \Omega$ (242 W) while retaining the initial $100\ \Omega$ compensation factor. As expected for an unadjusted feedforward scheme, doubling the load current introduces a minor, predictable steady-state voltage drop (-2.0% deviation, yielding $107.8\ V_{rms}$). Nevertheless, the output voltage settles quickly without severe transient overshoot or sustained oscillation, governed by the passive output network. These results confirm that the open-loop compensation scheme remains inherently stable under severe load steps, producing a bounded and calculable regulation error that can be eliminated by updating the compensation gain.

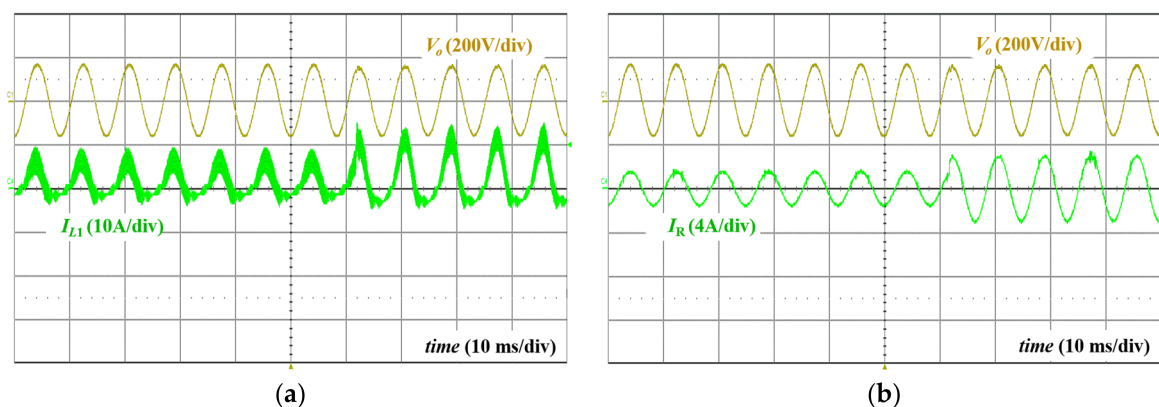


Figure 22. Experimental output behavior during a load step from $100\ \Omega$ (121 W) to $50\ \Omega$ (242 W): (a) v_o , i_{L1} ; (b) v_o , i_R .

6.2.7. Output-Current Harmonic Content

To evaluate the output power quality, the output-current THD was analyzed across the operating load range at the low input voltage $V_{in} = 95\ V$. Table 9 summarizes the measured and simulated THD values together with the relative error defined as:

$$\varepsilon_{THD} = \frac{|\text{THD}_{\text{exp}} - \text{THD}_{\text{sim}}|}{\text{THD}_{\text{exp}}} \times 100\% \quad (36)$$

Table 9. Experimental and simulated output-current THD versus output power, with the relative deviation of Equation (36).

Output Power (W)	% of Rated	Experimental THD (%)	Simulated THD (%)	ε_{THD} (%), Equation (36)
30	10	—	0.45	—
100	33	0.9	0.85	5.6
200	67	1.6	1.55	3.1
300	100	2.4	2.36	1.7

The experimental THD remains slightly higher than the simulated value, with an absolute difference of approximately 0.04–0.05 percentage points and a relative deviation ε_{THD} of 1.7–5.6%. The small discrepancy is mainly attributed to practical nonidealities not fully represented in the simulation, including semiconductor voltage drops, passive-component parasitics, interconnection effects, and uncertainty in the current-probe and FFT measurements. Nevertheless, both the simulated and experimental THD values remain below 2.5% over the measured load range.

Table 10 presents the simulated output-current harmonic components at rated power under the two extreme input-voltage conditions. At $V_{in} = 95$ V, the second-order harmonic is dominant at 2.24%, followed by the third-order harmonic at 0.74%, while the fifth- to eleventh-order harmonics remain below 0.05% of the fundamental. At $V_{in} = 400$ V, all reported low-order harmonics remain below 0.03%, indicating substantially lower current distortion in pure-buck operation.

Table 10. Simulated output-current harmonic magnitudes normalized to the fundamental at rated power (%).

Harmonic Order	Boost ($V_{in} = 95$ V, 300 W)	Buck ($V_{in} = 400$ V, 300 W)
2nd	2.24	0.03
3rd	0.74	0.02
5th	0.04	<0.01
7th	0.03	<0.01
9th	0.02	<0.01
11th	0.01	<0.01
Total THD (%)	2.36	0.04

6.2.8. Common-Mode Voltage and Leakage Current

Figure 23 presents the measured common-mode voltage (v_{CM}) and ground leakage current (i_{lk}) across an emulated parasitic capacitance connected between the negative DC rail and earth, in accordance with the test procedure commonly adopted for common-ground topologies [31,33]. Because the AC output neutral is directly bonded to the positive DC rail, high-frequency common-mode voltage fluctuations across the parasitic capacitance are structurally eliminated, confining v_{CM} to a DC offset with a minor low-frequency component.

Consequently, the measured RMS leakage current is 38 mA under low input voltage ($V_{in} = 95$ V) and 25 mA under high input voltage ($V_{in} = 400$ V). These values correspond to only 12.7% and 8.3% of the 300 mA safety threshold dictated by the DIN VDE 0126-1-1 standard [37], respectively. These experimental results confirm that the common-ground structure effectively suppresses common-mode leakage current well within regulatory safety limits while maintaining stable sinusoidal output operation.

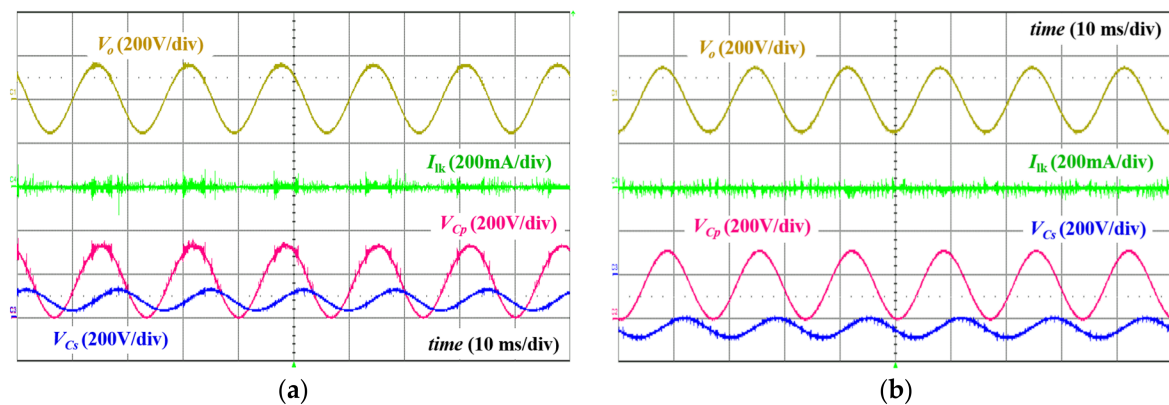


Figure 23. Measured common-mode voltage v_{CM} and leakage current i_{lk} through an emulated parasitic capacitance: (a) low input voltage; (b) high input voltage.

6.2.9. Loss Breakdown and Efficiency

To analyze power-dissipation mechanisms and evaluate switching-loss reduction, a comprehensive loss model was developed using device datasheet parameters for the C2M0080120D SiC MOSFETs. Semiconductor dissipation includes $R_{DS(on)}$ -based conduction losses and switching losses derived from turn-on/turn-off energy profiles. Passive losses encompass inductor copper losses from the measured L_1 ESR, core losses, and capacitor conduction losses from the equivalent series resistances of C_p , C_s , and C_o . Table 11 details the resulting loss breakdown and calculated efficiency across four power levels under both input voltage regimes.

Table 11. Computed loss breakdown (W) and simulated efficiency at both input voltages.

Loss Component	$V_{in} = 95 \text{ V}$				$V_{in} = 400 \text{ V}$			
	30 W	100 W	200 W	300 W	30 W	100 W	200 W	300 W
MOSFET conduction, S_1 – S_4	0.30	0.85	2.73	6.16	0.40	0.49	0.81	1.37
MOSFET switching, S_1 – S_4	0.22	0.37	0.75	1.10	0.67	0.75	0.90	1.14
Inductor L_1 (copper + core)	0.35	0.94	2.86	6.18	0.43	0.53	0.88	1.46
Capacitor ESR, $C_p + C_s + C_o$	0.02	0.03	0.09	0.18	0.06	0.08	0.13	0.21
Total loss	0.89	2.20	6.43	13.62	1.56	1.85	2.71	4.18
Simulated efficiency (%)	97.12	97.85	96.89	95.66	95.07	98.19	98.66	98.62

Figure 24 illustrates the loss breakdown versus output power at low input voltage, $V_{in} = 95 \text{ V}$. At the rated 300 W load, MOSFET conduction loss (6.16 W) and inductor loss (6.18 W) constitute 90.6% of the total power dissipation (13.62 W), whereas switching loss accounts for only 8.1% (1.10 W). Scaling power from 30 W to 300 W causes conduction and copper losses to increase quadratically. In contrast, switching loss increases only fivefold because high-frequency PWM commutation is confined to a single half-bridge leg. This confirms that full-load efficiency reduction is driven predominantly by conduction dissipation rather than switching penalties, validating the low switching-loss characteristic of the single-active-leg modulation strategy.

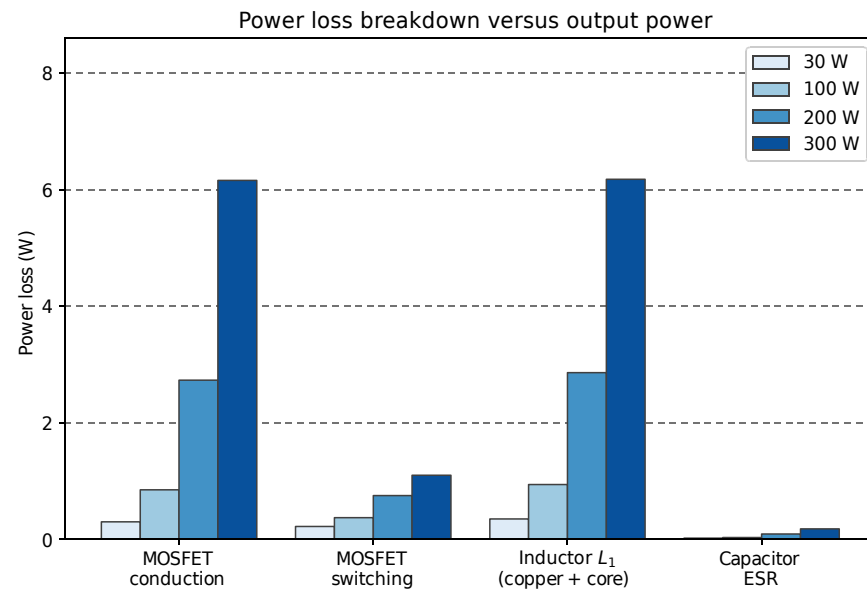


Figure 24. Computed loss breakdown versus output power at low input voltage: MOSFET conduction, MOSFET switching, inductor (copper plus core) and capacitor ESR losses.

Figure 25 compares the loss distribution between input voltage extremes at rated power. At $V_{in} = 400$ V, total power loss drops significantly to 4.18 W (98.62% efficiency) compared to 13.62 W (95.66%) at 95 V. This efficiency improvement stems from a fourfold reduction in inductor and device RMS currents at elevated input voltage. Consequently, minimizing semiconductor $R_{DS(on)}$ and inductor winding resistance represents the primary path for further efficiency optimization and power scaling.

$V_{in} = 95$ V @ 300 W (total = 13.62 W)

$V_{in} = 400$ V @ 300 W (total = 4.18 W)

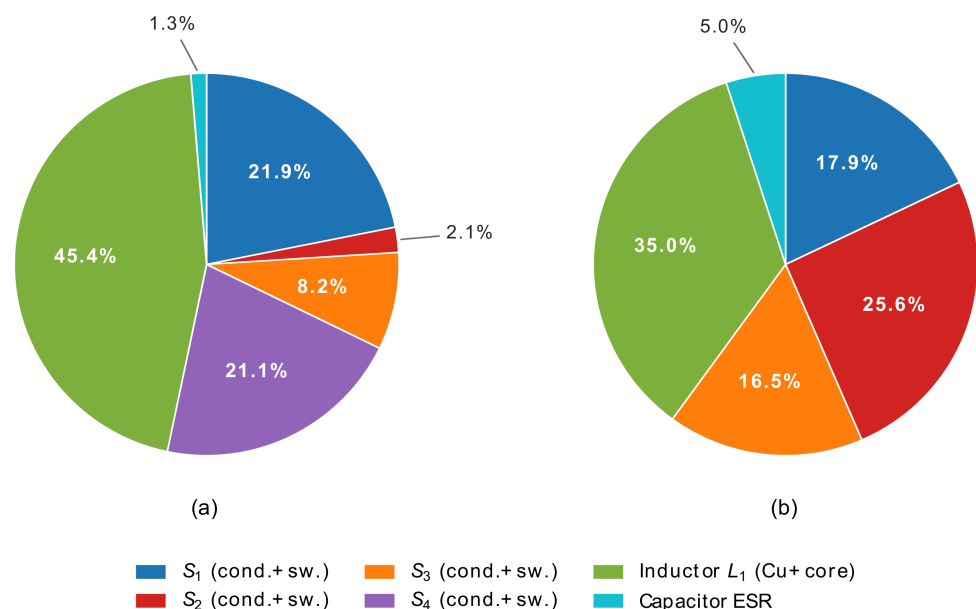


Figure 25. Distribution of the total loss among the circuit components at the rated output power of 300 W: (a) $V_{in} = 95$ V, 13.62 W total; (b) $V_{in} = 400$ V, 4.18 W total.

Figure 26 compares the measured and calculated converter efficiency across the entire load range (30–300 W, corresponding to 10–100% of the rated power) under both input-voltage conditions. At $V_{in} = 95$ V, the measured efficiency reaches a maximum of 96.79% at 100 W and gradually decreases to 94.41% at the rated output power of 300 W. The

experimental efficiency closely follows the analytical prediction, with the measured values remaining approximately one percentage point lower over the entire operating range. This difference is mainly attributed to practical nonidealities that are not fully represented in the analytical model, including semiconductor switching and conduction losses, passive-component parasitics, and parameter tolerances.

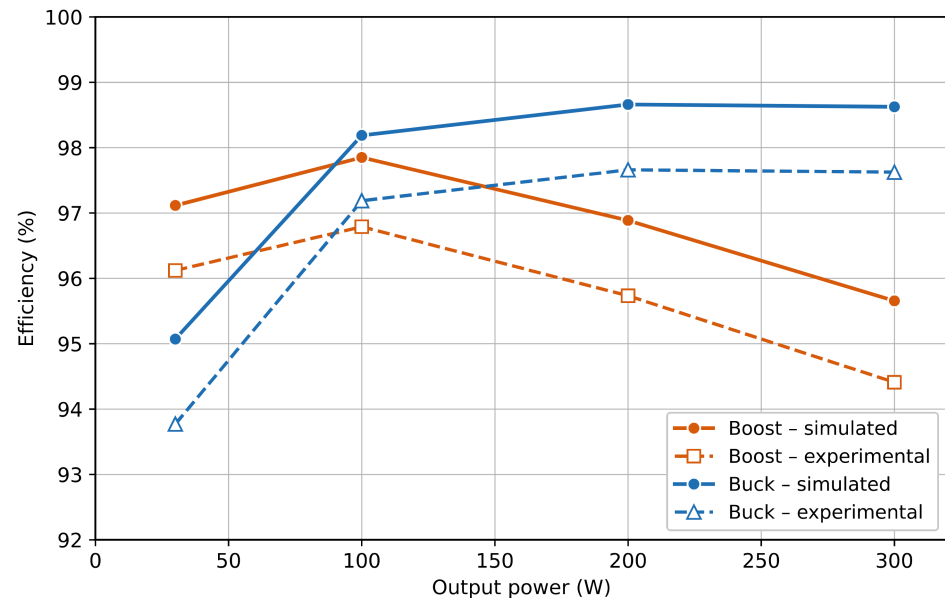


Figure 26. Measured and simulated efficiency versus output power over the 10–100% load range at low and high input voltage.

6.2.10. Measurement Uncertainty and Parameter Sensitivity

To evaluate the repeatability of the experimental results, statistical processing was performed using five consecutive measurements for each operating condition. Table 12 summarizes the sample size, mean values, standard deviations, and instrument accuracies for the key performance parameters at the rated output power of 300 W. The low standard deviations confirm good measurement repeatability, while the remaining differences between the analytical, simulated, and experimental results are consistent with the practical nonidealities discussed in the preceding sections.

Table 12. Statistical evaluation of the measured performance at the rated output power of 300 W (five consecutive trials per operating condition).

Quantity	Number of Measurements	Mean	Std. Dev.	Instrument Accuracy
Output voltage	5	109.5 V	0.32 V	±0.5%
Efficiency	5	94.41%	0.18%	±0.2%
THD	5	2.4%	0.09%	±0.1%

6.3. Thermal Behavior and Long-Term Reliability

Table 11 also provides the basis for the thermal assessment. At the rated operating point (300 W, $V_{in} = 95\text{V}$), the calculated total losses are 7.26 W in the four SiC MOSFETs and 6.18 W in the inductor. Using the specified thermal resistances, the worst-case junction-temperature rise is approximately 14 °C above ambient, indicating that all semiconductor devices operate with a comfortable margin below their 150 °C junction-temperature rating. The inductor therefore represents the dominant thermal design constraint. As device temperature increases, the SiC MOSFET on-state resistance and the inductor copper resistance also increase, leading to a moderate reduction in efficiency. Under a 100 °C temperature

rise, the calculated efficiency decreases from 95.66% to approximately 94.3%, while the voltage-transfer relationships derived in Section 3 remain unaffected because they depend only on the passive-network parameters.

Regarding long-term reliability, the proposed converter employs only polypropylene film capacitors, eliminating the electrolyte dry-out mechanism associated with electrolytic capacitors. The sensitivity analysis in Section 5.3 shows that a 5% capacitance reduction produces less than a 0.5% change in the open-loop output voltage, indicating good tolerance to capacitor ageing. A comprehensive lifetime evaluation based on accelerated thermal-cycling and endurance testing is beyond the scope of this work and is left for future study.

6.4. Discussion on Power Scaling and Prospects

The design methodology presented in Section 5 is not restricted to the 300 W prototype. Because the voltage-retention factor and compensation characteristics are determined by the output-network parameters, the same design procedure can be applied to higher power ratings by appropriately selecting the passive components according to the scaling relationships established in Section 5. Similar buck–boost converter cells have been reported in multi-kilowatt applications, supporting the applicability of the underlying operating principle [38].

Three practical approaches may be considered for higher-power implementations. The first is interleaving multiple converter cells, which reduces the current stress of each phase, improves ripple cancellation, and facilitates thermal management. The second is increasing the switching frequency to reduce the required inductance and capacitance, thereby improving power density when wide-bandgap semiconductor devices are employed. The third is increasing the series capacitance C_s , which increases the voltage-retention factor, reduces the required compensation gain, and improves the operating margin over a wide input-voltage range. The appropriate scaling strategy depends on the target power level, efficiency, thermal constraints, and passive-component size.

For higher-power single-phase applications, the inherent twice-line-frequency power pulsation at the DC port should also be considered. This issue can be mitigated by incorporating an active power-decoupling circuit without modifying the proposed modulation strategy or compensation method [39–41]. In addition, previous studies have shown that smooth transition between the buck and boost operating modes requires appropriate coordination by the outer voltage controller under dynamic operating conditions [42]. Experimental validation of kilowatt-level prototypes and long-term reliability evaluation remain subjects for future work.

7. Comparative Evaluation

Table 13 compares the proposed converter with representative single-phase transformerless topologies, including buck-only common-ground inverters, boost inverters, and single-stage buck–boost converters. The comparison considers the semiconductor count, passive components, presence of a dedicated output filter inductor, input-voltage capability, common-ground implementation, and reported maximum efficiency.

Since buck-only inverters cannot generate the required AC voltage from low input voltages, the H6 topology [21] and the traditional common-ground inverter [27] are additionally listed together with a front-end boost stage to provide an input-voltage capability comparable to that of the proposed converter.

The comparison highlights the trade-offs among the three topology families. Buck-only common-ground converters, such as the H6 topology [21] and the traditional common-ground inverter [27], achieve very high inverter efficiencies. However, their operating range is limited by the input voltage, and a front-end boost converter becomes necessary when a

wide DC-input range is required. Although the additional boost stage extends the operating range, it also increases the number of semiconductor devices, passive components, and overall conversion stages, reducing the achievable system efficiency.

Table 13. Comparison of representative inverter topologies.

Topology	Ref.	SW	D	L	C	Output Filter L_f	V_{in} (V)	V_o (V_{rms})	Common Ground	Max. Eff. (%)
Split-inductor DBI	[10]	4	2	4	2	No	70–200	110	No	97.7
Quasi-switched boost	[11]	5	6	1	1	Yes	30	35	No	83.7
H6 transformerless	[21]	6	2	0	0	Yes	380–700	230	No	97.1
Two-stage: boost + H6	[21] +boost	7	3	1	1	Yes	wide	220	No	93.2 *
Traditional CG (Type I)	[27]	4	1	0	1	Yes	340	230	Yes	99.3
Two-stage: boost + CG (Type I)	[27] +boost	5	2	1	2	Yes	wide	230	Yes	95.3 *
Dual-mode 4-SW CG BB	[28]	4	4	1	1	No	200	120	Yes	—
Half-bridge boost	[29]	6	0	1	2	Yes	40	110	Yes	95.9
Single-stage boost family	[30]	5	0	1	1	Yes	22	120	Yes	—
Nine-level boost	[31]	9	4	0	4	Yes	100	283	Yes	96.3
Switched-boost 4-SW (series-cap)	[34]	4	2	1	2	No	96	110	No	95.5
Virtual-ground BB	[35]	5	2	1	2	No	84–200	110	Virtual	97.2
Proposed	—	4	0	1	3	No	95–400	110	Yes	96.8

* Overall efficiency of the cascade, obtained by multiplying the reported inverter efficiency by an assumed 96% front-end boost-stage efficiency.

Single-stage boost-capable converters avoid the need for a front-end DC–DC converter, but generally require additional circuit complexity. The split-inductor differential boost inverter [10] employs multiple magnetic components, while the nine-level boost inverter [31] relies on a significantly larger number of active switches and capacitors. Other boost-capable topologies, including the half-bridge boost inverter [29] and the virtual-ground buck–boost inverter [35], reduce the number of magnetic components, but require five or more active switches. The dual-mode common-ground buck–boost inverter [28] achieves a four-switch configuration, although it relies on asymmetric modulation and floating gate drivers. The switched-boost topology in [34] also employs four switches, but incorporates additional passive components and does not include a compensation mechanism for the series-capacitor voltage drop.

Compared with these representative topologies, the proposed converter combines a wide input-voltage range of 95–400 V with a single-stage four-switch structure requiring no external diodes. It also eliminates the dedicated output filter inductor while maintaining common-ground operation throughout the entire operating range. The only magnetic component is the energy-storage inductor used for buck–boost power conversion, rather than a line-frequency output filter choke. Consequently, the proposed topology achieves a reduced semiconductor count while maintaining a measured peak efficiency of 96.79%.

Overall, the proposed converter does not aim to maximize inverter-only efficiency, as achieved by buck-only common-ground structures. Instead, it provides a balanced compromise among wide-input-voltage capability, reduced component count, common-ground operation, elimination of the dedicated output filter inductor, and competitive efficiency within a single-stage architecture. These characteristics make it particularly suitable for standalone power-conversion systems supplied by wide-range DC sources.

8. Conclusions

This paper presented the CG-SCC-BBI, a single-stage non-isolated buck–boost inverter for wide-input DC applications. The proposed topology combines common-ground operation, a series-blocking capacitor, and a model-based compensation method to achieve wide-range voltage conversion while eliminating the dedicated output filter inductor.

It also employs only four active switches and no external diodes, resulting in a simple single-stage power-conversion structure.

A fundamental-frequency analytical model including the output capacitor was developed to predict the voltage-retention factor, component stresses, and operating limits. Based on this model, closed-form design guidelines were derived for the passive components and the modulation range. The analysis was verified by simulation and experimentally validated using a 300 W SiC MOSFET prototype under resistive, inductive, nonlinear, and transient operating conditions. The prototype achieved measured peak efficiencies of 96.79% at $V_{in} = 95$ V and 97.66% at $V_{in} = 400$ V, while maintaining an output-current THD below 2.5%.

The proposed converter represents a practical compromise between wide-input-voltage capability, common-ground operation, reduced semiconductor count, and competitive efficiency. Nevertheless, the present implementation employs an open-loop compensation method, exchanges the twice-line-frequency power ripple directly with the DC source, and has not yet been validated through long-term thermal-cycling or endurance testing. Future work will therefore focus on adaptive closed-loop voltage regulation, active power decoupling, and experimental validation of higher-power prototypes together with long-term reliability evaluation.

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