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Dynamic Thermal Network Parameter Updating Strategy for IGBT Full-Bridge Modules in Digital Twin Applications

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Abstract

To meet the conflicting demands of real-time simulation and high fidelity for thermal modeling of IGBT modules in digital twin applications, this paper presents a dynamic thermal network parameter updating strategy. A hybrid thermal model is constructed by combining a high-fidelity finite-element-method reference model with a 3-D compact network. Initial thermal resistance and capacitance parameters are obtained via offline calibration and validated against the transient thermal impedance curve. A dynamic identification method based on recursive least squares with precomputed sensitivity matrices is then proposed. It dynamically updates each independent thermal branch using only real-time chip junction temperature measurements. The Vincotech full-bridge IGBT module is used for simulation validation. The proposed method achieves steady-state identification errors of 3.2% for the IGBT chip thermal resistance and 4.5% for the freewheeling diode chip thermal resistance, outperforming particle swarm optimization and dual Kalman filter in both convergence speed and steady-state accuracy. Thus, it satisfies the requirements of real-time tracking and dynamic evolution for thermal models in digital twin systems.

Keywords: IGBT full-bridge module; digital twin; 3-D compact model; dynamic parameter updating; recursive least squares

1. Introduction

Power semiconductor devices, represented by insulated gate bipolar transistors (IGBTs), are the core components of power electronic equipment and are widely used in renewable energy generation, electric vehicles, rail transportation, aerospace, and other fields [1,2]. During operation, IGBT modules withstand repeated power shocks, and the amplitude and fluctuation of their junction temperature are key factors affecting device reliability, lifetime, and safe system operation [3,4]. Studies have shown that about 60% of IGBT module failures are related to thermal stress, and accurate thermal modeling and junction temperature monitoring are the foundations for life prediction, health management, and intelligent maintenance [5,6]. Therefore, establishing an IGBT thermal model that balances accuracy and efficiency, and dynamically tracking the evolution of device thermal characteristics during actual operation, has become a research hotspot in the field of power electronics reliability [7,8].

In terms of IGBT thermal modeling, existing methods are mainly divided into three categories: the finite element method (FEM) [9,10], the equivalent thermal network

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method [11,12], and the Foster behavioral model from data manuals [13]. FEM, by establishing the 3-D geometric structure and material properties of the device, can accurately simulate the internal temperature field distribution and is currently the most accurate thermal modeling method [9]. However, FEM models have high computational complexity and long simulation times, making it difficult to meet the requirements of real-time applications. The Foster model has a simple structure and high computational efficiency, and is widely used for junction temperature estimation, but its parameters lack physical meaning and cannot reflect the influence of aging and fatigue of various internal material layers (such as solder layers, substrates, and thermal interface materials) on the thermal characteristics [13]. Between these two lies the equivalent thermal network model based on the Cauer network, whose thermal resistance and thermal capacitance parameters correspond to the physical structure, offering a certain degree of interpretability and moderate computational cost [11]. As a further development, the 3-D compact thermal model [14] bridges the gap between the Cauer model and the FEM model by accounting for 3-D heat diffusion effects while maintaining a model order that represents a reasonable trade-off between accuracy and computational efficiency.

In recent years, the emergence of digital twin (DT) technology has provided a new paradigm for the construction and updating of thermal models [15–17]. Digital twins emphasize "virtual–real mapping, real-time synchronization, and closed-loop optimization" between physical entities and virtual models [18,19]. Within this framework, the thermal model must not only have high computational efficiency to support real-time simulation but also possess the ability to dynamically update parameters, i.e., to adjust its internal parameters based on measured data so that it remains consistent with the actual device at all times. Traditional offline calibration methods (such as transient thermal impedance curve fitting) can only obtain fixed parameters and cannot track parameter drift during device aging [20,21]. To address this, researchers have attempted to use particle swarm optimization (PSO) [15], Extended Kalman filtering (EKF), and its improved forms (such as dual-extended Kalman filtering, DEKF) [17] for dynamic parameter identification. However, the PSO algorithm has slow convergence speed and high computational cost, making it difficult to embed in real-time control systems. Although DEKF has good dynamic tracking capability, it requires simultaneous filtering of both state and parameter quantities, resulting in still high algorithm complexity. The corresponding comparisons are shown in Figure 1. Moreover, most existing studies simplify the IGBT module into a thermal network model with a single branch or only a few branches, ignoring the thermal coupling effects among multiple chips within the full-bridge module and the influence of 3-D heat diffusion [22]. Their model fidelity is insufficient to meet the high-fidelity requirements of digital twins. Furthermore, the cooling system plays a critical role in determining the thermal performance of power devices [23]. The thermal resistance of a semiconductor device can vary by up to twenty times depending on the cooling system design, dissipated power level, heat pipe dimensions, heatsink size, and airflow velocity. This underscores that thermal model accuracy cannot be evaluated in isolation from the actual cooling conditions.

To address the above issues, this paper takes the Vincotech full-bridge IGBT module as the research object and proposes a dynamic thermal network parameter updating strategy for digital twin applications. The rest of this paper is organized as follows. Section 2 introduces the heat transfer model of the IGBT module and the principles of thermal parameter acquisition, including the establishment of the FEM reference model and the 3-D compact model. Section 3 describes the dynamic parameter updating strategy for the thermal model oriented to digital twins and the details of the RLS algorithm. Section 4 verifies the effectiveness of the model and method through simulations. Section 5 presents the summary and conclusions.

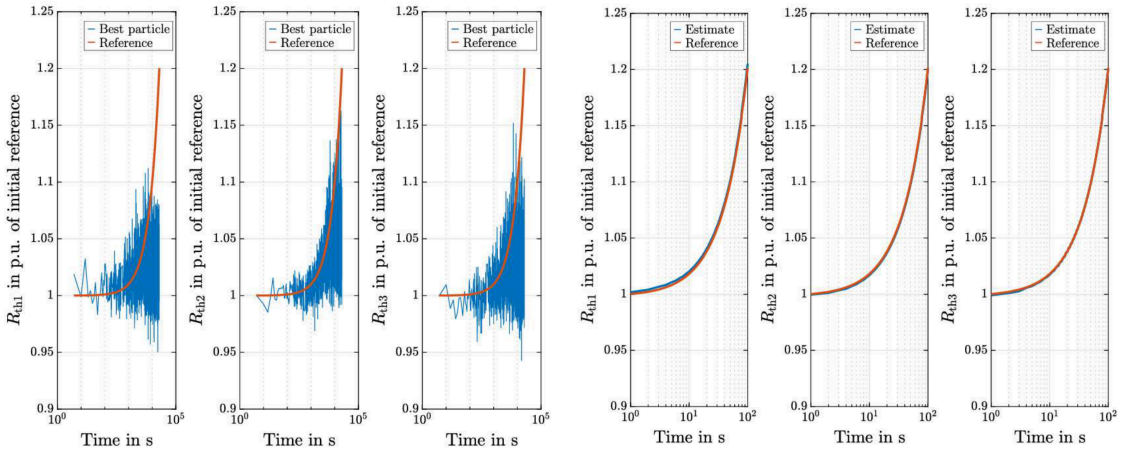


Figure 1. Thermal parameter tracking capabilities under different approaches [17]. (**a**) PSO; (**b**) DEKF.

2. Heat Transfer Model of IGBT Modules and Thermal Parameter Acquisition Principles

The essential requirements of a digital twin are "virtual–real mapping, real-time synchronization, and closed-loop optimization." At present, a single traditional heat transfer model cannot simultaneously meet the real-time and high-fidelity requirements of digital twins. Therefore, it is necessary to construct a quasi-real-time, high-precision, and evolvable hybrid thermal model.

2.1. Finite Element Method Thermal Reference Model

Commercial simulation software such as ANSYS 2022R1 and COMSOL 6.3 can accurately simulate complex geometries and thermal boundary conditions based on the device's geometry and material properties, ensuring high fidelity between the model and the real system. The modeling steps mainly include constructing the 3-D physical model, importing material parameters, and determining thermal boundary conditions.

In this paper, the Vincotech 10-FZ074PA050SM-L624F08 full-bridge IGBT module is taken as the object of study, and its 3-D model is established. The internal structure is shown in Figure 2. T_1, T_2, T_3, and T_4 are IGBT chips; D_1, D_2, D_3, and D_4 are freewheeling diodes (FWD) connected in parallel with each IGBT chip; C_A and C_B are internal DC-link capacitors; and R_t is the thermistor. It should be noted that the modeling shown in Figure 1 was obtained by accurately measuring the physical IGBT module after removing the housing and internal silicone gel; only some manufacturers provide 3-D housing models of the module.

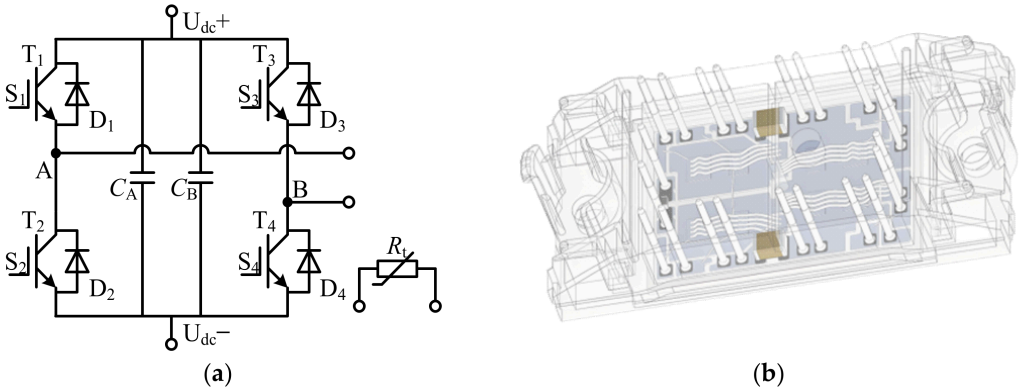


Figure 2. Overview of full-bridge IGBT module (with NTC point). (**a**) Topology; (**b**) 3-D structure.

Figure 3 shows the spatial arrangement of the chips inside the IGBT module and the material layers. The same color corresponds to the same material. The spatial positions of the components in Figure 1a are shown in Figure 2a. The material parameters of each layer are based on parameters given in the literature, fully considering the influence of temperature on thermal conductivity and heat capacity. In addition, the thermal interface material (TIM) and its thermal conductivity can be obtained from the "thermal" section of each manufacturer's datasheet to match the manufacturer's test environment. The heatsink test environment shown in Figure 3a is forced air cooling, and the heatsink material is Cu. In practice, manufacturers measure the Foster model of the semiconductor module based on a specific heatsink, including both forced air cooling and water-cooling environments. The difference is that in forced air cooling, the heat flow in the module spreads over a wider range, so the measured junction-to-case thermal resistance $R_{th(j\text{-}c)}$ is lower; in water cooling, the heat diffusion is not as extensive, so the measured $R_{th(j\text{-}c)}$ value is higher. In most cases, manufacturers use the measurement results from water-cooled heatsinks, which provide a Foster model representing more severe operating conditions, meaning a larger safety margin in applications.

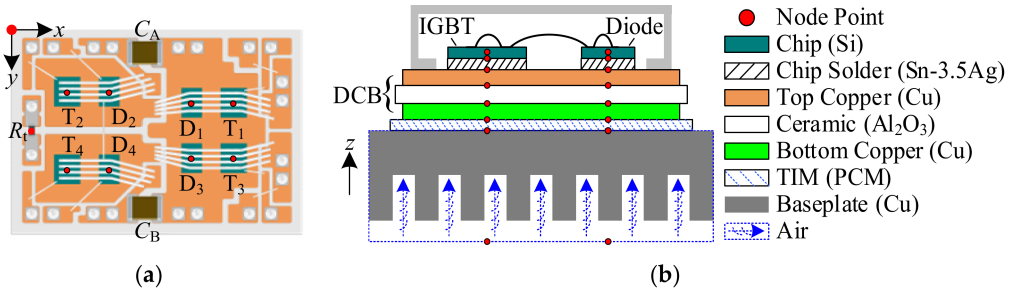


Figure 3. Internal structure of IGBT module. (**a**) Top view of DCB plane. (**b**) Vertical layer structure.

The heatsink model established in this paper is shown in Figure 4. When the test condition is water cooling, the water-cooling test environment can be restored by simply setting the M1 interface in COMSOL; by setting the M2 interface and the N2 region, the forced air-cooling test environment can be simulated. Correspondingly, the thermal boundary conditions are set according to test standards such as IEC 60747-9 [24], with water-cooling and forced air-cooling convective heat transfer coefficients h_w and h_a, forced air velocity v_a, and other parameters.

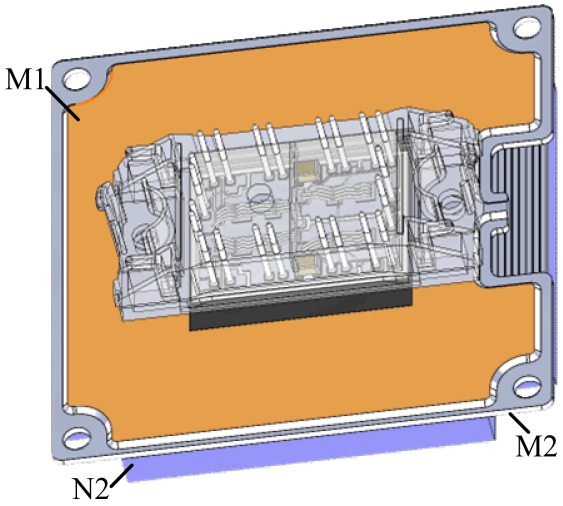


Figure 4. Overview of heatsink.

2.2. 3-D Compact Thermal Model Based on Cauer Network

It should be noted that the Foster model used in data manuals is more of a behavioral model; it does not care about the internal physical structure of the IGBT, only the relationship between input (power loss) and output (junction temperature). Although the FEM model has extremely high accuracy, for digital twin applications, an overly complex model is not conducive to parameter updating and tracking. In view of this, this paper constructs a 3-D compact thermal model based on the Cauer network, as shown in Figure 5. Here, node 0 is the NTC temperature sensor node. Although packaging structures such as silicone gel and housing exist physically (as shown in Figure 3), because their thermal resistance is much larger than that of the main heat dissipation path, only a very small amount of heat (estimated <5%) is dissipated through this path. To simplify the model and focus on the key physical processes affecting junction temperature, the reduced-order model neglects the upward heat transfer path and its associated structures.

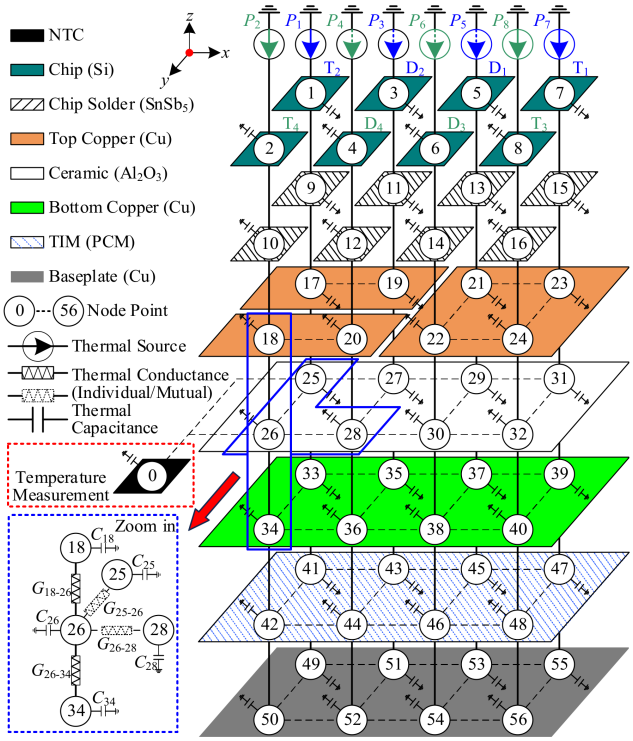


Figure 5. 3-D compact thermal network topology of IGBT module (with NTC point).

In the 3-D compact thermal network model shown in Figure 5, the parameters to be identified include thermal capacitances and thermal conductances. Identifying all thermal capacitance and thermal conductance parameters simultaneously is a difficult task. Therefore, for any non-reference node i in the 3-D compact thermal network model, denoting its temperature as T_i, according to Kirchhoff's current law, the following expression can be obtained:

$$C_i \frac{dT_i}{dt} = P_i - \sum_{m \in M_i} G_{i-m}(T_i - T_m) \tag{1}$$

where M_i is the set of all nodes adjacent to node i. For example, $M_{26} = \{18, 25, 28, 34\}$. P_i is the heat source, which is the power loss injected into node i in the form of a current source. For example, P_1 represents the loss injected into node 1 (chip T_2). For nodes on the chip layer, $P_i \neq 0$; otherwise, $P_i = 0$. C_i is the thermal capacitance to ground of node i, and $G_{i\text{-}m}$ represents the reciprocal of the thermal resistance between node i and node m, i.e., $1/R_{i\text{-}m}$.

Equation (1) can be further expanded as

$$C_i \frac{dT_i}{dt} = P_i - \left(\sum_{m \in M_i} G_{i-m} \right) T_i - \sum_{m \in M_i} (-G_{i-m}) T_m \tag{2}$$

where $\sum_{m \in M_i} G_{i-m}$ is the self-thermal conductance of node i, and -$G_{i\text{-}m}$ is the mutual thermal conductance between node i and node m.

Equation (2) can be further expanded in matrix form:

$$C_{57\times57} \frac{dT_{57\times1}}{dt} = P_{57\times1} + G_{57\times57} T_{57\times1} \tag{3}$$

where T, C, G, and P are the temperature matrix, thermal capacitance matrix, thermal conductance matrix, and loss-input matrix of the 3-D compact thermal network model, respectively. The expressions of these matrices are as follows:

$$T_{57\times1} = \begin{bmatrix} T_1 & T_2 & \cdots & T_{56} & T_0 \end{bmatrix}^{\mathrm{T}} \tag{4}$$

$$C_{57\times57} = \begin{bmatrix} C_1 & 0 & 0 & \cdots & 0 \\ 0 & C_2 & 0 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots & \vdots \\ 0 & 0 & 0 & C_{56} & 0 \\ 0 & 0 & 0 & 0 & C_0 \end{bmatrix} \tag{5}$$

$$G_{57\times57} = \left[\begin{array}{ccccccc:c} -G_{8\times8}^{z1} & G_{8\times8}^{z1} & & & & & & \\ G_{8\times8}^{z1} & G_{8\times8}^{xy1} & G_{8\times8}^{z2} & & & O & & \\ & & \ddots & & & & & (G_{1\times8}^{0})^{T} \\ & & & & G_{8\times8}^{z5} & G_{8\times8}^{xy5} & G_{8\times8}^{z6} & \\ \hdashline & O & & & & G_{8\times8}^{z6} & G_{8\times8}^{xy6} & \\ \hdashline & & & G_{1\times8}^{0} & & & & -G'_0 \end{array}\right] \tag{6}$$

$$P_{57\times1} = \begin{bmatrix} P_1 & P_2 & P_3 & P_4 & P_5 & P_6 & P_7 & P_8 & 0 & \cdots & 0 \end{bmatrix}^{\mathrm{T}} \tag{7}$$

where $G_{1\times8}^{0}$ = [$G_{0\text{-}25}$ $G_{0\text{-}26}$ 0 $\cdots$ 0], G'_0 = $G_{0\text{-}25}$ + $G_{0\text{-}26}$, and $G_{8\times8}^{z}$ and $G_{8\times8}^{xy}$ are the thermal conductance matrices in the z-axis and xy-plane, respectively. In (6), the first row represents the top-layer thermal conductance (chip layer), the second row represents the middle-layer thermal conductance (solder, copper, etc.), the third row represents the bottom-layer thermal conductance (heatsink layer), and the fourth row represents the thermal conductance of the NTC sensor.

In these equations, the 3-D compact thermal network model is considered a low-order approximation of the finite element simulation, meaning that the temperatures at the nodes of the thermal network model are essentially consistent with the simulation results at the corresponding positions of the finite element model.

2.3. Principles of Thermal Parameter Acquisition

Both the FEM reference model and the reduced-order compact model need to be matched to the actual device through some medium. This medium is the transient thermal resistance curve, or the cooling curve. To match the cooling curve of the actual device, during the offline calibration stage, it is necessary to adjust parameters such as material thermal conductivity and specific heat capacity, and in some cases, adjust the thickness of material layers.

For the 3-D compact thermal network model, the thermal resistance and thermal capacitance parameters need to be adjusted. The transient thermal impedance curves of the proposed model can be obtained through simulation, while the measurement of the transient thermal impedance of the actual device must be carried out according to standards such as IEC 60747-9 [24] and JEDEC JESD51-1 [25].

The measurement of transient thermal impedance usually adopts the turn-off method [26,27]. In Figure 6, the device is first heated to steady state by a constant power P_L. As shown in the left part of Figure 6, T_j, T_c, and T_s/T_h are the junction temperature, case temperature, and heatsink temperature (without base plate/with base plate), respectively. The T_j after stabilization is recorded as $T_j(\infty)$. Then, at $t = 0$, the heating current is turned off, and the junction temperature T_j cooling curve is recorded. According to the superposition principle, the response during the heating phase can be obtained by flipping the cooling curve, as shown in the right part of Figure 6. The expression for the transient thermal impedance is

$$Z_{th}(t) = \frac{T_j(\infty) - T_j(t)}{P_L} \tag{8}$$

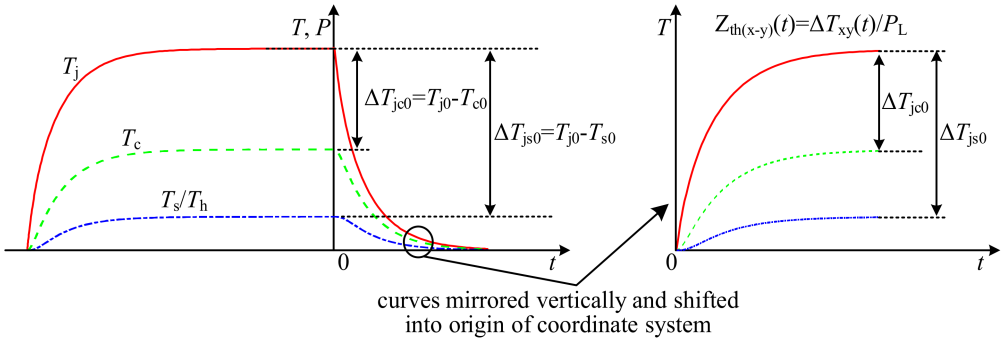


Figure 6. Thermal impedance measurement method.

The junction temperature during the cooling phase is obtained by the temperature-sensitive electrical parameter method [28]. The heating power P_L should be selected such that the junction temperature rise ΔT_j reaches 30–80 °C to avoid measurement errors caused by insufficient temperature rise at low currents. Thus, an accurate transient thermal impedance curve of the actual IGBT can be obtained.

To acquire the model parameters, the Foster model in the manufacturer's datasheet is usually fitted to the measured $Z_{th}(t)$ curve using the nonlinear least squares method, thereby extracting the thermal resistances R_i and time constants τ_i. The objective function is

$$\min \sum_{k=1}^{m} \left[Z_{th,meas}(t_k) - \sum_{i=1}^{n} R_i (1 - e^{-t/\tau_i}) \right]^2 \tag{9}$$

where $Z_{th,meas}(t_k)$ is the measured impedance at time t_k, m is the number of measurement points, and n is the order of the Foster model, with constraints $R_i > 0$ and $\tau_i > 0$.

Since the FEM model already establishes a high-precision 3-D model, the parameters that need to be calibrated offline through the transient thermal impedance are mainly the thermal conductivity and specific heat capacity of the materials. If the physical model has some deviation, geometric dimensions may need adjustment. The error between the final FEM model transient thermal response curve and the measured curve should be less than the tolerance considered in FEM studies.

It should be pointed out that, considering the complexity of the FEM model, a more suitable approach for digital twin applications is to use the reduced-order 3-D compact

thermal network model to achieve dynamic parameter updating, thereby meeting the real-time requirements of digital twins. For longer-term operation and maintenance and health management tasks, the parameters of the FEM model can be updated based on the 3-D compact thermal network model parameters, providing a more intuitive representation of the thermal parameter changes in the actual IGBT module.

The thermal conductances and thermal capacitances of the 3-D compact thermal network model can be solved by the following methods:

1. Solution for thermal conductance: When the 3-D compact thermal network model reaches steady state, differential equation (3) can be rearranged into the following linear equation:

$$T^{0^*(\infty)}_{57\times 96} G^*_{96\times 1} = P^{(\infty)}_{57\times 1} \tag{10}$$

where T^{0^*} is the temperature matrix transformed from temperature T, and the thermal conductance matrix G^* is

$$G^*_{96\times 1} = [\underbrace{G_{1-9}\ G_{2-10}\ \cdots\ ;G_{48-56}}_{1\times 48}\ \underbrace{G_{21-22}\ G_{23-24}\ \cdots\ G_{55-56}}_{1\times 18}\ \underbrace{G_{17-19}\ G_{18-20}\ \cdots\ G_{54-56}}_{1\times 28}\ \underbrace{G_{0-25}\ G_{0-26}}_{1\times 2}]^{\mathrm{T}} \tag{11}$$

It can be seen that the linear system shown in (10) consists of 57 effective equations. When multiple sets of simulation/experimental data are imported, the number of equations must exceed the number of unknowns, making it essentially an overdetermined system. The overdetermined system is usually solved using the non-negative least squares method to identify all unknown parameters. The objective function is

$$G^* = \underset{G^*}{\operatorname{argmin}} \left\| T'^{0^*(\infty)} G^* - P'^{(\infty)} \right\|_2 \tag{12}$$

2. Solution for thermal capacitance: Similar to the solution for thermal conductance, (3) can be rearranged into the following linear ordinary differential equation:

$$\frac{dT^{1*}_{57\times 57}}{dt} C^*_{57\times 1} = P_{57\times 1} - T^*_{57\times 96} G^*_{96\times 1} \tag{13}$$

where $T_1{}^*$ is the temperature matrix transformed from temperature T, and the thermal capacitance matrix C^* is

$$C^*_{57\times 1} = \begin{bmatrix} C_1 & C_2 & C_3 & \cdots & C_{56} & C_0 \end{bmatrix}^{\mathrm{T}} \tag{14}$$

The objective function is

$$C^* = \underset{C^*}{\operatorname{argmin}} \left\| \frac{dT''^{1^*}}{dt} C^* - P'' + T''^* G^* \right\|_2 \tag{15}$$

It should be noted that the above scheme is the basic idea for offline calibration of model thermal resistance and thermal capacitance, achieved under the premise of obtaining a large amount of node temperature data through FEM simulation and actual experiments. Dynamic updating of thermal model parameters requires higher standards.

3. Data-Driven Dynamic Parameter Updating Strategy for Digital Twin Applications

Under the five-dimensional DT framework shown in Figure 7 [18], the thermal model parameter updating process in this paper involves three parts: PE, VE, and DD. PE and VE represent the physical entity and the virtual entity, respectively, which, according to

functional structure, generally include unit level, system level, and complex system level. DD represents various types of DT data stored in the cloud. Section 2.3 has pointed out that the transient thermal resistance curve is the key link between the physical entity and the proposed model, but this is mainly for the offline calibration stage. During actual IGBT module operation, a more feasible method is to observe the junction temperature change curve to dynamically adjust the model parameters, which is essentially the same as relying on the transient thermal resistance curve in the offline calibration stage.

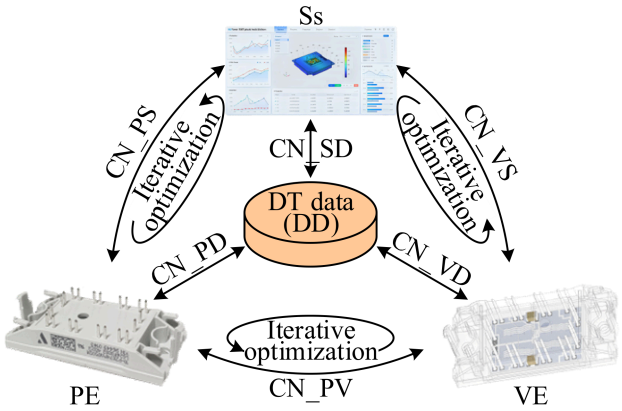


Figure 7. 5-D overview of thermal model under DT framework.

3.1. Thermal Network Model Parameter Updating Strategy

Figure 8 shows the thermal model parameter updating framework proposed in this paper. During the operation of the IGBT module, the chip currents i_1 and voltages v_1 are dynamically collected, and the chip loss P_{loss} is obtained from a loss lookup table [17]. The chip junction temperature T_{j1} and ambient temperature T_{a1} can be obtained through the preset Foster model in the datasheet and sensor acquisition, respectively. In particular, if an NTC sensor as shown in Figure 2 is arranged inside the IGBT module, monitoring the junction temperature of the IGBT module can theoretically be achieved without the need for additional sensors.

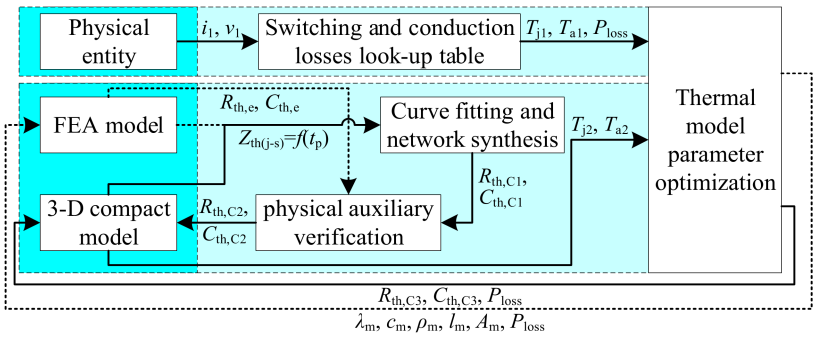


Figure 8. Thermal model parameter update strategy.

The thermal model proposed in this paper adopts a hybrid approach combining the FEA model and the 3-D compact model. During the dynamic updating process, priority is given to updating the parameters of the 3-D compact model, as shown in Figure 9. The dynamic updating strategy consists of static and dynamic parts. In the static part, during offline calibration, the junction-to-heatsink transient thermal resistance curve $Z_{th(j\text{-}s)}$ of the 3-D compact model is fitted to that of the FEM reference model or the physical entity, yielding the initial thermal resistance $R_{th,C1}$ and thermal capacitance $C_{th,C1}$. Then, through the physical constraints of the FEM model on geometric dimensions, the thermal network parameters of the corresponding layer in the 3-D compact model are calibrated, obtaining

the calibrated $R_{th,C2}$ and $C_{th,C2}$. These parameters serve as the initial parameters for the 3-D compact model in the dynamic part.

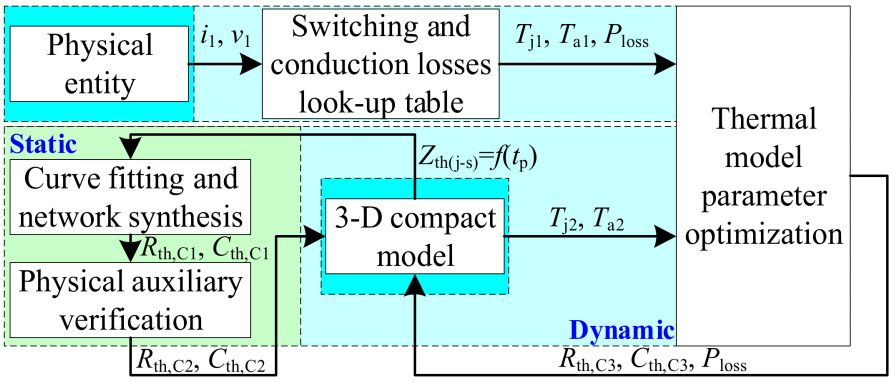


Figure 9. Dynamic update process of thermal model parameters.

The dynamic updating process of the 3-D compact model is as follows: under the input of P_{loss}, the 3-D compact model outputs chip junction temperature T_{j2} and ambient temperature T_{a2}, which are compared with those of the physical entity model. Through the thermal model parameter optimization method, updated thermal resistance $R_{th,C3}$ and thermal capacitance $C_{th,C3}$ are obtained, and the cycle continues to track the changes in the thermal parameters of the physical entity.

The FEA model serves more as a reference model, providing physical constraints for the Cauer model parameters. Its greatest advantage compared to the physical entity is that it can accurately observe the temperature changes in all nodes of the 3-D compact model.

3.2. Optimization Method for Thermal Model Parameters

As described in Section 2.2, the 3-D compact model shown in Figure 5 contains a total of 57 nodes, which are coupled by thermal conductances and thermal capacitances. During the actual operation of the IGBT module, usually only the chip junction temperature T_j or the single-point temperature of the internal NTC thermistor R_t can be measured in real time. The temperatures of other nodes (such as the DCB layer, substrate, interior of the heatsink, etc.) cannot be directly observed. Therefore, it is impractical to update all these parameters dynamically; the model needs a simpler representation.

From the conclusion, the model shown in Figure 4 can be reduced to eight independent Cauer branches because the structure–function method is expressed through the Cauer model [20]. Therefore, the dynamic parameter updating problem can be simplified to the dynamic updating of the parameters of these eight independent branches. That is, for each branch, the real-time junction temperature and the model-predicted junction temperature residual are used to update the thermal resistance and thermal capacitance parameters of that branch in real time.

This paper proposes a dynamic identification strategy based on recursive least squares (RLS) with precomputed sensitivity matrices. The strategy precomputes the sensitivity of each parameter to the junction temperature in the offline stage, and during dynamic operation uses the temperature residual to recursively correct the parameters. It has low computational cost and fast convergence, making it suitable for embedded real-time applications.

Taking the IGBT chip T_1 as an example, the state-space model of a single-branch Cauer model is

$$T(k+1) = A(\gamma)T(k) + BP_{loss}(k) + B_aT_a(k) \tag{16}$$

$$T_j(k) = CT(k) \tag{17}$$

where $T(k)$ and $T(k+1)$ are the node temperature vectors at time k and the next time instant, $T_a(k)$ is the ambient temperature at time k, $P_{\text{loss}}(k)$ is the power loss injected into the chip of this branch at time k, $\gamma = [G_{1\text{-}9}, C_1, G_{9\text{-}17}, C_9, G_{17\text{-}25}, C_{17}, G_{25\text{-}33}, C_{25}, G_{33\text{-}41}, C_{33}, G_{41\text{-}49}, C_{49}]^{\mathrm{T}}$ is the vector of parameters to be identified, and $T_j(k)$ is the chip junction temperature at time k.

Since the relationship between the input T_{j} and γ is nonlinear, to apply linear RLS, a first-order Taylor expansion is performed around the current parameter estimate $\hat{\gamma}(k-1)$:

$$T_{\mathrm{j}}(k) \approx T_{\mathrm{j}}^{(0)}(k) + S(k)^{\mathrm{T}} \Delta\gamma(k-1) \tag{18}$$

where $T_{\mathrm{j}}^{(0)}(k)$ is the model prediction computed using $\hat{\gamma}(k-1)$; $\Delta\gamma = \gamma - \hat{\gamma}$ is the parameter increment; and $S(k) = \left.\frac{\partial T_{\mathrm{j}}}{\partial \gamma}\right|_{\hat{\gamma}(k-1)}$ is the sensitivity vector.

The calculation of $S(k)$ uses the offline finite-difference method, which is based on the already offline-calibrated FEM model and a 3-D compact model. The steps are as follows:

1. With the offline-calibrated parameters γ, a small perturbation $\delta\gamma_{\mathrm{j}}$ is applied to each parameter individually.
2. A step power excitation is applied, and the junction temperature response curve $T_{\mathrm{j}}(t, \gamma_{\mathrm{j}} + \delta\gamma_{\mathrm{j}})$ is recorded.
3. The sensitivity is calculated using a finite-difference approximation:

$$S_{\mathrm{j}}(k) \approx \frac{T_{\mathrm{j}}(t; \gamma_{\mathrm{j}} + \delta\gamma_{\mathrm{j}}) - T_{\mathrm{j}}(t; \gamma_{\mathrm{j}})}{\delta\gamma_{\mathrm{j}}} \tag{19}$$

All sensitivity curves are discretized and stored as a lookup table. During dynamic operation, $S(k)$ is obtained by looking up the table according to the current time instant. It is particularly noteworthy that since all branches have the same structure, only one branch needs to be precomputed, and the eight branches share the same sensitivity table.

The schematic of the RLS recursive update algorithm is as follows. At each sampling time k, the following steps are executed for each branch:

Using the parameters from the previous time instant and the current inputs $P_{\text{loss}}(k)$ and $T_{\mathrm{a}}(k)$, the junction temperature prediction $T_{\mathrm{j}}^{(0)}(k)$ is calculated by (16) and (17). The temperature residual is expressed as

$$e_{\mathrm{T}}(k) = T_{\mathrm{j}}^{\text{meas}}(k) - T_{\mathrm{j}}^{(0)}(k) \tag{20}$$

The RLS recursive expressions are as follows:

$$K(k) = \frac{P(k-1)S(k)}{\lambda + S(k)^{\mathrm{T}} P(k-1) S(k)} \tag{21}$$

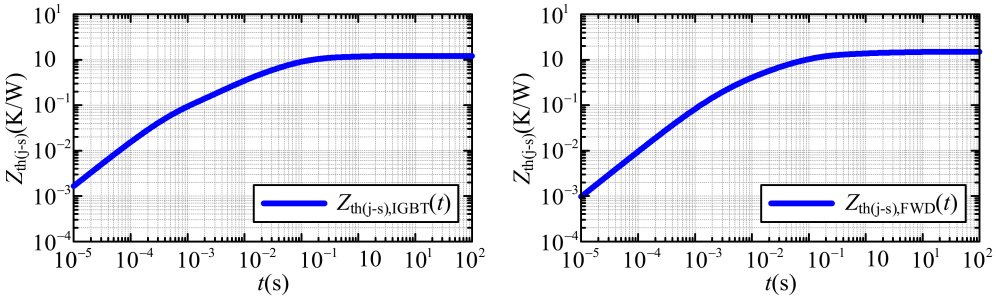
$$\hat{\gamma}(k) = \hat{\gamma}(k-1) + K(k)[e(k) - S(k)^{\mathrm{T}} \Delta\hat{\gamma}(k-1)] \tag{22}$$

$$P(k) = \frac{1}{\lambda}[I - K(k)S(k)^{\mathrm{T}}]P(k-1) \tag{23}$$

where λ is the forgetting factor, controlling the weight of historical data; $P(k)$ is the covariance matrix. According to (22), the dynamic updating results for the thermal model parameters are obtained.

4. Model Validation and Analysis

The IGBT employed in this paper is the Vincotech 10-FZ074PA050SM-L624F08 full-bridge IGBT module. The relevant transient thermal resistance curves and thermal model parameters are shown in Figure 10 and Tables 1 and 2.



(**a**) (**b**)

Figure 10. Transient thermal impedance curves. (**a**) IGBT; (**b**) FWD.

Table 1. Thermal model values of IGBT chip (Foster).

	1	**2**	**3**	**4**	**5**	**6**
R/K·W^{-1}	0.128	0.4402	0.3964	0.1752	0.03439	0.04802
τ/s	0.875	0.1117	0.0356	0.007549	0.001966	0.0004333

Table 2. Thermal model values of FWD chip (Foster).

	1	**2**	**3**	**4**	**5**	**6**
R/K·W^{-1}	0.1032	0.2051	0.6391	0.3387	0.1705	0.04446
τ/s	4.733	0.5533	0.08308	0.02015	0.004421	0.001299

4.1. Offline Calibration Results of the Thermal Model

According to the thermal parameter acquisition method in Section 2.3, offline parameter calibration was performed for both the FEM model and the 3-D compact model. The initial material properties of the FEM model are shown in Table 3.

Table 3. Material parameters of FEM [5].

Material	**Temperature/°C**	**Thermal Conductivity/Wm^{-1}·°C^{-1}**	**Specific Heat Capacity/J·kg^{-1}·°C^{-1}**	**Density/kg·m^{-3}**
Si	50 100 150	131 109 88	700	2329
Sn96.5/Ag3.5	100	53	230	7440
Cu	50 100 150	398 391 389	385	8960
Al_2O_3	\	27	900	3900
Ag	50 100 150	421 409 387	235	10,500
Air	50 100 150	0.028 0.032 0.036	1005 1008 1011	1.092 0.946 0.835

According to the thermal parameter acquisition method in Section 2.3, offline parameter calibration was performed for both the FEM model and the 3-D compact model. The initial material properties and results of the FEM model are shown in Table 3 and Figure 11.

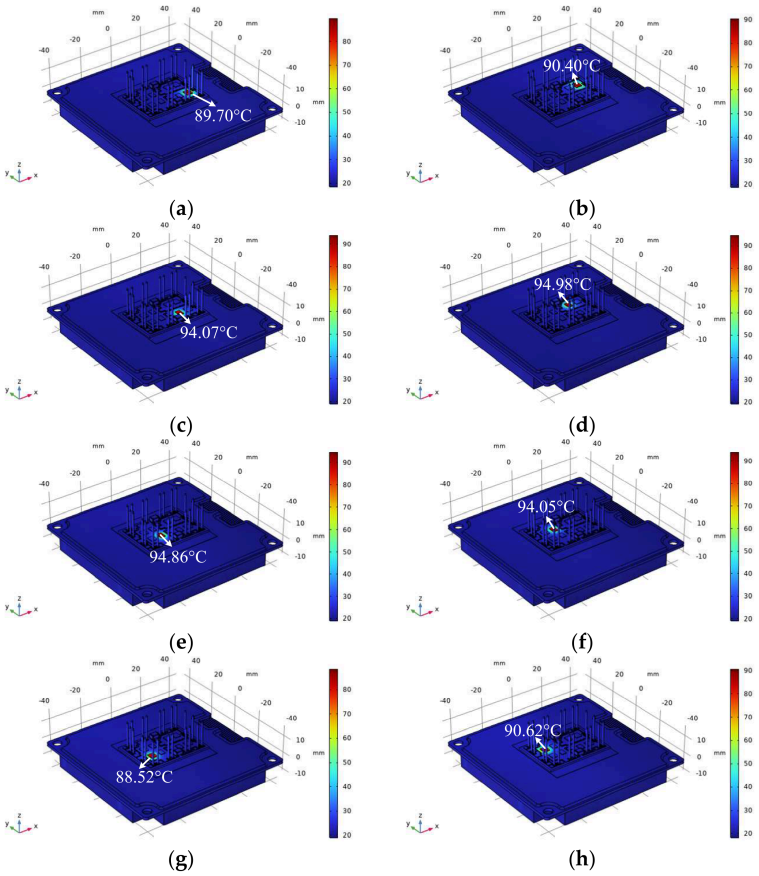


Figure 11. FEA Results. (**a**) P_1 = 50 W; (**b**) P_2 = 50 W; (**c**) P_3 = 50 W; (**d**) P_4 = 50 W; (**e**) P_5 = 50 W; (**f**) P_6 = 50 W; (**g**) P_7 = 50 W; (**h**) P_8 = 50 W.

Through transient thermal simulation and fine-tuning of model parameters to fit the cooling curve of the actual IGBT module, the parameters of the 3-D compact model were obtained through eight steady-state thermal simulations and one transient thermal simulation, completing the offline calibration of all parameters. Figure 11 shows the simulation results when a power of 50 W is injected individually into each of the eight chip nodes. It can be seen that the maximum ΔT_j is 74.98 °C (@T_a = 20 °C) within the range of 30–80 °C.

The model matching results are shown in Figure 12. It can be seen that both the FEM model and the 3-D Cauer model match the actual model well, thus verifying the validity of the model and the feasibility of the proposed strategy.

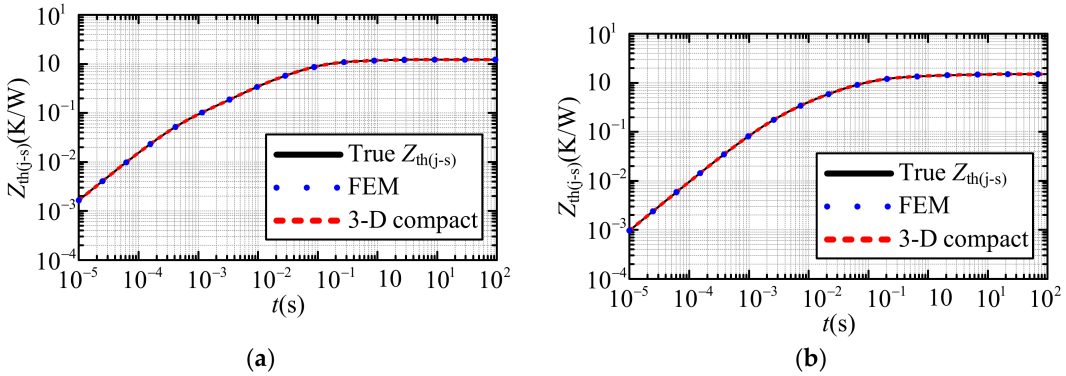


Figure 12. Comparison of transient thermal impedance curves. (**a**) IGBT; (**b**) FWD.

4.2. Dynamic Tracking Results of Thermal Parameter Changes

The dynamic identification strategy decomposes the model into parameter identification of eight independent Cauer branches. The offline-calibrated Cauer model parameters are shown in Tables 4 and 5. To simulate the dynamic tracking effect of parameters, it is assumed that solder layer fatigue occurs, leading to reduced material thermal conductivity and a significant increase in thermal resistance. Figure 13 shows the comparison results of the proposed dynamic strategy and the PSO and DEKF schemes in references [15] and [17], respectively, when thermal parameters change.

Table 4. Thermal model values of IGBT chip (Cauer).

	1	**2**	**3**	**4**	**5**	**6**
$R/\mathrm{K{\cdot}W^{-1}}$	0.1037	0.242	0.2431	0.3766	0.1702	0.08665
$C/\mathrm{J{\cdot}K^{-1}}$	0.005997	0.01574	0.02148	0.06608	0.5263	9.365

Table 5. Thermal model values of FWD chip (Cauer).

	1	**2**	**3**	**4**	**5**	**6**
$R/\mathrm{K{\cdot}W^{-1}}$	0.2651	0.267	0.4182	0.3195	0.1551	0.076607
$C/\mathrm{J{\cdot}K^{-1}}$	0.01024	0.01503	0.0388	0.1872	3.542	57.88

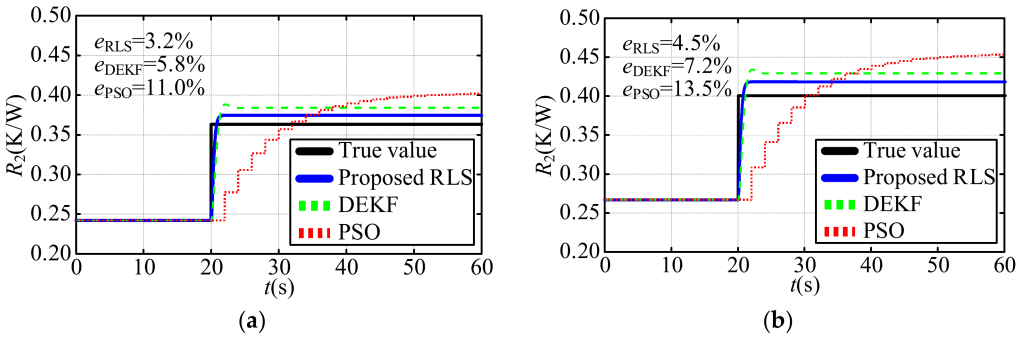


Figure 13. Comparison of tracing R_2. (**a**) IGBT; (**b**) FWD.

At time t = 20 s, the thermal resistance of the chip solder layer increases by 50%, simulating a fatigue issue. Figures 13a and 13b show the tracking results for the IGBT chip and the FWD chip, respectively. The steady-state errors for IGBT chip parameter identification are e_{RLS} = 3.2%, e_{DEKF} = 5.8%, and e_{PSO} = 11.0%. For the FWD chip, the steady-state errors are e_{RLS} = 4.5%, e_{DEKF} = 7.2%, and e_{PSO} = 13.5%. It can be seen that the iterative convergence speed of the PSO algorithm is much worse than that of the proposed RLS and DEKF. Compared with DEKF, the proposed RLS strategy has better steady-state accuracy and comparable response speed.

5. Discussion

In future power electronic systems for digital twin applications, the proposed combination of an FEM thermal reference model and a 3-D compact thermal model will be the optimal choice for solving the thermal effects of devices and equipment. Table 6 compares its performance with the FEM model and the traditional Foster model. This comparison shows that the proposed hybrid thermal model achieves a trade-off between computational efficiency and accuracy while retaining the physical meaning of parameters, thus offering greater flexibility.

Table 6. Performance comparisons among different thermal models.

	FEM	Foster	Proposed Hybrid Thermal Model
Computational efficiency	Extremely low (hours to hundreds of hours per simulation)	Extremely high (millisecond-level computation, can be intensively invoked)	Static phase: similar to FEM; Dynamic phase: millisecond level
Physical interpretability	Strong (directly corresponds to geometric structure and material layers; node temperatures have clear physical meaning)	Weak (purely mathematical fitting; RC stages have no corresponding physical structure)	Relatively strong (based on Cauer network; each stage corresponds to specific material layers; parameters have physical meaning)
Dynamic response capability and hardware requirements	Weak (requires high-performance workstation; difficult to embed in dynamic monitoring systems)	Strong (can run on a microcontroller; fast response)	Relatively strong (can run on edge devices such as ARM Cortex M; meets quasi-dynamic requirements)
Applicable scenarios	Static thermal design, benchmark validation, root cause analysis of failures	Short-term junction temperature monitoring, dynamic thermal estimation under healthy conditions	Full life cycle digital twin, engineering applications with periodic shutdowns

On the other hand, the proposed hybrid model also offers good adaptability for deployment in practical simulation software. The FEM part is essentially a physical geometry model, which is compatible with FEA software such as Ansys and COMSOL. Meanwhile, the dynamic updating strategy of the 3-D compact model ultimately updates the single-branch Cauer model for each chip. The Cauer model can be uniquely converted into a Foster model, whose parameters can be written into an XML file and are compatible with power electronics simulation software like PLECS 4.82. This further demonstrates the flexibility of the proposed model and its practicality for integration into actual simulation software.

6. Conclusions

This paper systematically investigates the dynamic updating problem of the thermal model of an IGBT full-bridge module for digital twin applications. The main conclusions are as follows.

The proposed hybrid FEM and 3-D compact thermal model ensures physical accuracy during offline calibration through the FEM model and meets the real-time requirements for computation through the reduced-order compact network. Offline calibration results show that the transient thermal impedance curves output by the proposed model agree well with the measured curves of the actual device.

To address the challenge of dynamic identification of compact thermal network parameters, an updating strategy based on recursive least squares (RLS) with precomputed sensitivity is designed. This strategy decouples the 57-node 3-D network into eight independent Cauer branches, precomputes the sensitivity curves using the offline finite-difference method, and stores them as a lookup table. During dynamic operation, only a small number of multiplication and addition operations are required to complete the recursive parameter update, with significantly higher computational efficiency than PSO and DEKF.

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Conflicts of Interest: The authors declare no conflict of interest.

Abbreviations

The following abbreviations are used in this manuscript:

IGBT	Insulated Gate Bipolar Transistor
FEM/FEA	Finite Element Method/Finite Element Analysis
RLS	Recursive Least Squares
PSO	Particle Swarm Optimization
DKF	Dual Kalman Filter
FWD	Freewheeling Diode
DT/PE/VE/DD	Digital Twin/Physical Entity/Virtual Entity/Digital Data
NTC	Negative Temperature Coefficient (thermistor)
DCB	Direct Bonded Copper
TIM	Thermal Interface Material

References

1. Lawal, I.O.; Schulte, H.; Salman, A. Virtual Synchronous Machine Testing and System Split Resilience: A Comparative Analysis with Grid-Following PV Inverters. *Energies* **2026**, *19*, 1027. [CrossRef]
2. Qiu, Y.; Li, Z.; Tian, S. GA-LSTM-Based Degradation Prediction for IGBTs in Power Electronic Systems. *Energies* **2025**, *18*, 5574. [CrossRef]
3. Guo, W.; Ma, M.; Wang, H.; Wang, H.; Song, Q.; Chen, W. A Partition Decoupling Algorithm for Compact Thermal Model in Multichip IGBT Modules. *IEEE Trans. Power Electron.* **2023**, *38*, 66–72. [CrossRef]
4. Jeftenić, I.; Štatkić, S.; Aleksandrović, S.; Mitrović, N. Comparative Damage Analysis of Critical Sub-Profiles in Random Mission Profile of Electric Drive Power Converters Under Controlled Thermal Conditions. *Energies* **2026**, *19*, 1193. [CrossRef]
5. Ma, M.; Zhang, Q.; Guo, W.; Song, Q. Dynamic IGBT Compact Thermal Network Model over Long Time Scales. *IEEE Trans. Compon. Packag. Manuf. Technol.* **2025**, *15*, 123–130. [CrossRef]
6. Okilly, A.H.; Lee, W.; Lee, I.; Kim, D.; Baek, J. Thermal-Stress-Induced Degradation Monitoring and Deep-Neural-Network-Driven Lifetime Prediction of IGBT Modules in a Two-Level SVPWM Inverter. *Electronics* **2026**, *15*, 1678. [CrossRef]
7. Lu, Y.; Xiang, E.; Jin, Y.; Luo, H.; Yang, H.; Li, W.; Zhao, R. A 3-D Temperature-Dependent Thermal Model of IGBT Modules for Electric Vehicle Application Considering Various Boundary Conditions. *IEEE J. Emerg. Sel. Top. Power Electron.* **2024**, *12*, 5463–5475. [CrossRef]
8. Zhang, J.; Shen, H.; Sun, H.; Wang, Z. Review on the Thermal Models Applications in the Reliability of Power Semiconductor Device. *IET Power Electron.* **2025**, *18*, e70065. [CrossRef]
9. Wang, Y.; Deng, E.; Wu, T.; Zhang, Y.; Xie, L.; Huang, Y. Thermo-Hygroscopic-Mechanical Coupling Simulation Method for Power Electronics Under Power Cycling Test. *IEEE Trans. Power Electron.* **2023**, *38*, 11521–11530. [CrossRef]
10. Okilly, A.H.; Choi, S.; Kwak, S.; Kim, N.; Lee, J.; Moon, H.; Baek, J. Estimation Technique for IGBT Module Junction Temperature in a High-Power Density Inverter. *Machines* **2023**, *11*, 990. [CrossRef]
11. Wang, H.; Zhou, Z.; Xu, Z.; Ge, X.; Yang, Y.; Zhang, Y.; Yao, B.; Xie, D. A Thermal Network Model for Multichip Power Modules Enabling to Characterize the Thermal Coupling Effects. *IEEE Trans. Power Electron.* **2024**, *39*, 6225–6245. [CrossRef]
12. Okilly, A.H.; Kim, C.; Kim, D.-W.; Baek, J. Control and Modeling Framework for Balanced Operation and Electro-Thermal Analysis in Three-Level T-Type Neutral Point Clamped Inverters. *Energies* **2025**, *18*, 5587. [CrossRef]
13. Shi, Y.; Liu, J.; Ai, Y.; Chen, S.; Bai, Y. Dynamic IGBT Three-Dimensional Thermal Network Model Considering Base Solder Degradation and Thermal Coupling between IGBT Chips. *IEEE Trans. Transp. Electrif.* **2023**, *9*, 2994–3011. [CrossRef]
14. Górecki, K.; Zarebski, J.; Górecki, P.; Ptak, P. Compact Thermal Models of Semiconductor Devices—A Review. *Int. J. Electron. Telecommun.* **2019**, *65*, 151–158. [CrossRef]
15. Torchio, R.; Conte, F.; Scarpa, M.; Filippini, M.; Pase, F.; Toso, F.; Nasab, P.S.; Marson, E.; Viroli, A.; Posa, P.; et al. Digital Twins in Power Electronics: A Comprehensive Approach to Enhance Virtual Thermal Sensing. *IEEE Trans. Power Electron.* **2025**, *40*, 6977–6987. [CrossRef]
16. Ali, A.; Gharehbaghi, R.; Chandrappan, J. Digital Twin-Driven Sustainability in Semiconductor Packaging. *Eng. Proc.* **2026**, *127*, 23. [CrossRef]

17. Kuprat, J.; Debbadi, K.; Schaumburg, J.; Liserre, M.; Langwasser, M. Thermal Digital Twin of Power Electronics Modules for Online Thermal Parameter Identification. *IEEE J. Emerg. Sel. Top. Power Electron.* **2024**, *12*, 1020–1029. [CrossRef]
18. Tao, F.; Xiao, B.; Qi, Q.; Cheng, J.; Ji, P. Digital Twin Modeling. *J. Manuf. Syst.* **2022**, *64*, 372–389. [CrossRef]
19. Zhang, S.; Song, W.; Cao, H.; Tang, T.; Zou, Y. A Digital-Twin-Based Health Status Monitoring Method for Single-Phase PWM Rectifiers. *IEEE Trans. Power Electron.* **2023**, *38*, 14075–14087. [CrossRef]
20. Farkas, G.; Schweitzer, D.; Sarkany, Z.; Rencz, M. On the Reproducibility of Thermal Measurements and of Related Thermal Metrics in Static and Transient Tests of Power Devices. *Energies* **2020**, *13*, 557. [CrossRef]
21. Hegedüs, J.; Szabó, P.G.; Pohl, L.; Hantos, G.; Lipák, G.; Reolon, A.; Ender, F. Thermal Characterization Methods of Novel Substrate Materials Utilized in IGBT Modules. *Electron. Mater.* **2025**, *6*, 9. [CrossRef]
22. Chang, Y.; Li, W.; Luo, H.; He, X.; Iannuzzo, F.; Blaabjerg, F.; Lin, W. A 3D Thermal Network Model for Monitoring Imbalanced Thermal Distribution of Press-Pack IGBT Modules in MMC-HVDC Applications. *Energies* **2019**, *12*, 1319. [CrossRef]
23. Górecki, K.; Posobkiewicz, K. Cooling Systems of Power Semiconductor Devices—A Review. *Energies* **2022**, *15*, 4566. [CrossRef]
24. *IEC 60747-9:2019*; Semiconductor Devices—Part 9: Discrete Devices—Insulated-Gate Bipolar Transistors (IGBTs). IEC: Geneva, Switzerland, 2019.
25. *JEDEC JESD51-1*; Integrated Circuit Thermal Measurement Method—Electrical Test Method (Single Semiconductor Device). JEDEC Solid State Technology Association: Arlington, VA, USA, 1995.
26. Zhang, R.; Li, X.; Ding, J.; Chen, S.; Yang, H.; Guo, H. Review of IGBT Intelligent Gate Drive and Protection Strategies. *IEEE Trans. Power Electron.* **2024**, *39*, 7392–7403. [CrossRef]
27. Funaki, T.; Fukunaga, S.; Hara, T.; Ibuchi, T. Difficulty and Solution in Transient Thermal Resistance Measurement for Wide Band Gap Power Semiconductor Device. In *Proceedings of the 2022 International Power Electronics Conference (IPEC-Himeji 2022- ECCE Asia), Himeji, Japan, 15–19 May 2022*; IEEE: Piscataway, NJ, USA, 2022; pp. 1959–1963. [CrossRef]
28. Alauzet, L.; Tounsi, P.; Fradin, J.-P. Sensorless Dual TSEP (Vth, Rdson) Implementation for Junction Temperature Measurement in Parallelized SiC MOSFETs. *Energies* **2025**, *18*, 3470. [CrossRef]

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