

Review

Load Mismatch Compensation of Load-Modulated Power Amplifiers: A Comprehensive Review

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Abstract: With the diversification, acceleration, and arraying of wireless communication systems, power amplifiers (PAs) face stricter demands in terms of RF operation bandwidth, high-efficiency power range, and load mismatch compensation. After years of development, load-modulated PAs (LMPAs) can maintain high efficiency over a wide bandwidth and a larger output back-off (OBO) range. However, there is obvious performance degradation when the load impedance of the current LMPAs is mismatched. To ensure the perfect application of power amplifiers in wireless communication systems, load mismatch compensation methods should be developed for LMPAs. Therefore, this paper gives a comprehensive review on the load mismatch compensation techniques of LMPAs, including the Doherty power amplifier and load-modulated balanced amplifier.

Keywords: power amplifier; load mismatch; load modulation; high efficiency



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1. Introduction

The radio frequency (RF) power amplifier (PA) serves as a core component in wireless communication transmitter systems. Therefore, it plays a vital role in wireless communication fields such as base stations, terminal devices, satellites, and so on. The performances of the PA directly impact the transmission quality, transmission distance, and system power consumption of the entire communication system [1,2], as shown in Figure 1. Therefore, it is of great significance to research on the RF PAs for enhancing communication quality, responding to user growth, driving technological advancements, expanding application areas, and boosting national competitiveness. With the continuous advancement of wireless communication systems, tremendous changes are taking place across the entire industry [3]. Firstly, the bandwidth and number of communication frequency bands are constantly increasing, necessitating further expansion of the operating bandwidth of communication equipment. Secondly, modulation methods of the communication signals are becoming complex and making it hard to achieve ultra-high-speed data transmission, leading to a constant rise in the peak-to-average power ratio (PAPR) of the communication signals [4]. Thirdly, multi-antenna deployment is gradually becoming a conventional technology, increasing the interactions among multiple wireless communication channels [5]. These changes pose new design requirements for RF PAs, which can be summarized as follows: the ability to expand RF bandwidth, extend high efficiency power range, and improve mismatch tolerance.

In recent years, researchers have conducted a series of studies focusing on the RF bandwidth and high-efficiency power range of PAs, aiming to enhance their capability of processing broadband complex modulated signals. Among various technologies, load

modulation techniques have gained significant attention due to their high efficiency characteristics. The representative load modulation architectures include Doherty PA (DPA) [6–9], Outphasing PA (OPA) [10,11], and load-modulated balanced amplifier (LMBA) [12–15].

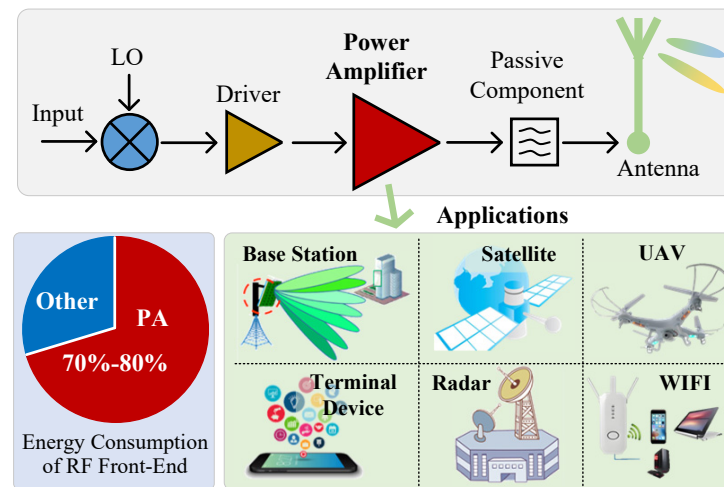


Figure 1. Applications of a power amplifier.

However, the existing LMPAs are always designed based on the standard $50\ \Omega$ load impedance. In multi-channel communication systems, load mismatch can always be observed by the PA, leading to significantly degradation in conversion efficiency and output power, as shown in Figure 2. However, there is relatively little research on the load mismatch compensation of the LMPAs.

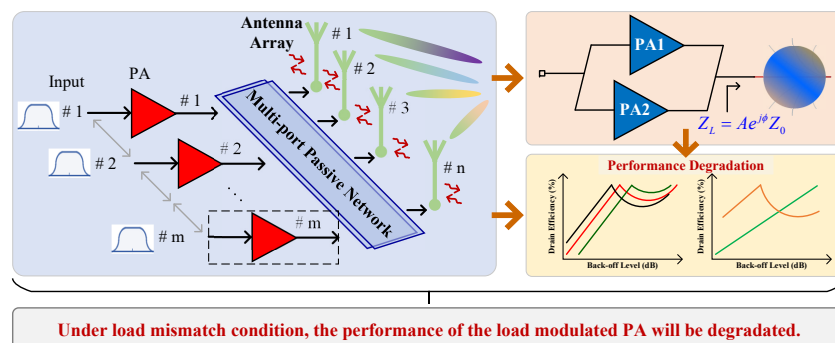


Figure 2. Performance degradation of LMPAs under load mismatch conditions.

Traditionally, to enhance the performances of a single-ended PA under load mismatch conditions, impedance variation sensors were often integrated at the output ports of the PA. Based on the impedance variation information, the operation state of the PA was adjusted to compensate for performance degradation caused by load mismatch [16–21]. In the 5G/6G communication systems, complex modulated signals are widely used, which has enabled LMPAs to become the most popular PA architecture. Consequently, the load mismatch caused by antenna arrays has a significant impact on the performances of the LMPAs [22–27]. Although traditional load mismatch compensation techniques for single-ended PAs could still be applied to LMPAs, developing unique methods to compensate for the load mismatch of the LMPA becomes more and more important. Therefore, this paper focuses on the the load mismatch compensation techniques for two main LMPA architectures, DPA and LMBA.

2. Review on Doherty Power Amplifier

For efficiently amplifying high PAPR signals, DPA is the most popular PA architecture due to its simple circuit topology. The DPA is first introduced in this part. Then, the load mismatch compensation techniques for DPAs are reviewed.

2.1. Introduction on Doherty Power Amplifier

The DPA was invented by William H. Doherty in 1930s [28]. It has two operation modes named parallel and serial DPA, as shown in Figure 3. This figure shows the generalized block diagram of the DPA. It has a carrier PA D1 and a peaking PA D2. These two sub-amplifiers are connected to transmission lines (TL) TL1 and TL2, respectively. Then, TL1 and TL2 are combined by a post-matching network (PMN). The PMN matches $50\ \Omega$ to the combining load Z_L , where Z_L is the combining load of the DPA. For the parallel DPA, the electrical lengths of TL1 and TL2 are 90° and 0° [29]. On the other hand, for the serial DPA, the electrical lengths of TL1 and TL2 are 90° and 180° [29].

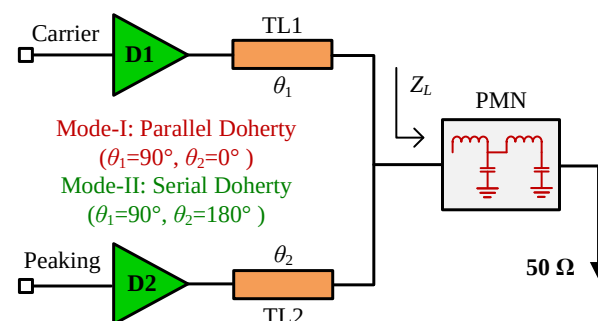


Figure 3. Simplified block diagram of a Doherty power amplifier.

Under the matched load condition, the parallel and serial DPAs have the same performances. The peaking PA is in the off-state until the normalized input reaches 0.5. After the peaking PA is turned on, it will modulate the load impedance of the carrier PA. Due to the active load modulation, the carrier PA maintains voltage saturation when the normalized input is larger than 0.5, leading to a high conversion efficiency. Based on the active load modulation, Figure 4 shows the drain efficiency of the parallel and serial DPAs versus normalized input [29]. The load impedance trajectories of the carrier and peaking PAs are also illustrated in Figure 4. The DPA has a drain efficiency same as the class-B PA at the half and maximum input levels. However, the efficiency response shown in Figure 4 will collapse if the DPA sees a mismatched load impedance, as shown in Figure 5. In the following subsection, the load mismatch compensation techniques of the DPA will be reviewed.

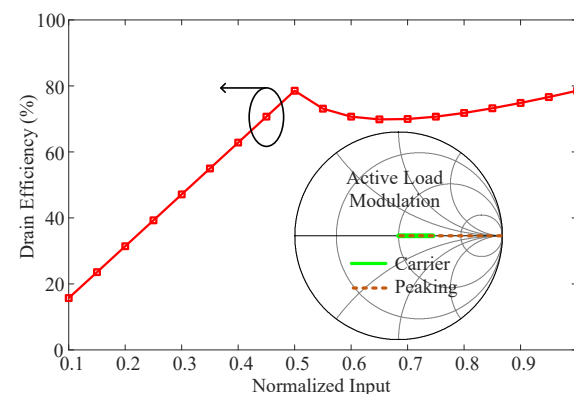


Figure 4. Theoretical drain efficiency of a Doherty power amplifier.

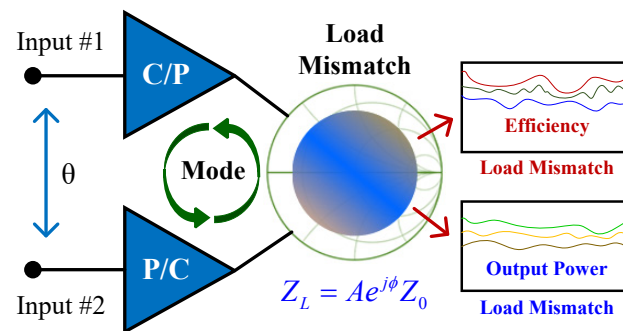


Figure 5. Doherty power amplifier under load mismatch conditions.

2.2. Load Mismatch Compensation of Doherty Power Amplifier

Normally, the RF PA is matched to the optimal load impedance Z_0 , achieving the best performances. However, in antenna array systems, there is a strong interaction between different antennas, leading to a varied load impedance for the PAs. As a result, the performance of the RF PA will be deteriorate, especially for the DPAs, as shown in Figure 5. Though DPA and OPA can be realized by utilizing the interaction between two antennas [30–32], they suffer from poor reliability, making them difficult to be widely applied in antenna array systems. Therefore, some advanced PA architectures and design methods were proposed for LMPAs to against load mismatch.

Some published works have demonstrated that the performance of a mismatched DPA can be improved by tuning the input conditions and DC supply voltages [33–37], as shown in Figure 6. To act against load mismatch, the DC supply voltage of the carrier and peaking PA should be adjusted according to the mismatched load impedance. Additionally, the input amplitude and phase of the carrier and peaking PAs should also be adjusted to achieve optimal load modulation.

In [34], the authors proposed a quasi-load-insensitive (QLI) DPA, which significantly reduces the impact of load variations on the output power by dynamically adjusting the DC supply voltage (V_{DD}) of the carrier and peak transistors as well as the input drive signals. To ensure constant output power, the optimal DC supply voltage and input signals for the carrier and peak PAs under different load conditions were derived based on the load line theory. The experimental results of the DPA in [34] indicated that the output power is improved by 1.3 to 1.7 dB and the back-off efficiency is increased by 15% to 20% when the load impedance is within a 2:1 voltage standing wave ratio (VSWR) circle.

In [35], the authors presented an inverted DPA (IDPA) which is load-insensitive within a 2:1 VSWR circle across an 11% fractional bandwidth. The proposed IDPA integrates a compact wideband impedance sensor within its output power-combining network. Based on the load variation, the IDPA maintains output power and efficiency profiles using load-dependent DC supply voltage and input signal adaptation. The fabricated IDPA achieves constant output power (± 0.2 dB) and improved efficiency (up to 15% at back-off) across a 2:1 VSWR circle.

The above two articles verify that the performance of a mismatched DPA can be restored by adjusting the DC supply voltages and input status through a board-level circuit. This method was also validated by integrated DPAs in [36,37]. In [36], the authors proposed a dual-adaptive bias (DAB) scheme for DPAs to enhance robustness against load variations, gain fluctuations, and supply voltage changes in 5G handsets. The proposed dual-adaptive bias scheme combines feedforward (fast response to input signals) and feedback (robustness to environmental variations) to optimize the DC voltage of the peaking PA. In [37], the authors presented an ultra-broadband load-insensitive dual-input MMIC DPA that is capable of mitigating performance degradation due to load mismatch by

adjusting the supply voltages and input settings of the main and auxiliary PAs. With mismatch compensation, the losses in PAE and output power of the dual-input MMIC DPA are constrained to 11% and 1.4 dB, respectively, over the entire 2.5:1 VSWR circle.

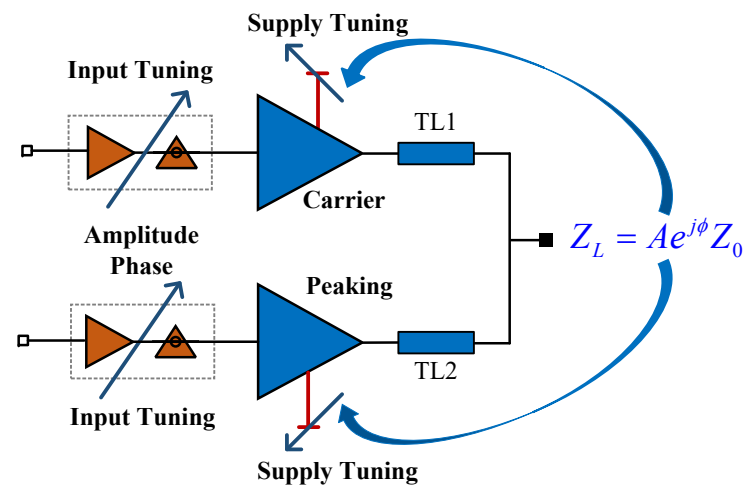


Figure 6. DPA with input tuning and DC supply tuning for compensating load mismatch.

On the other hand, the performance degradation of the DPA caused by load mismatch can also be compensated using mode reconfiguration [38–41]. It should be noted that mode reconfiguration often requires the adaption of DC supply voltages or input conditions. In [39], the authors proposed a balanced-to-Doherty (B2D) PA to compensate load mismatch. The B2D PA can reconfigure between Doherty and balanced modes using a silicon-on-insulator (SOI)-based single-pole double-throw (SPDT) switch. Through Doherty and balanced mode reconfiguration, the B2D PA can recover the performance degradation caused by load mismatch. However, the balanced mode itself lacks the ability to enhance back-off efficiency.

As stated in the above subsection, the DPA has two operation modes: the parallel Doherty mode and the serial Doherty mode. The theoretical analysis in [38] indicated that the parallel and serial DPA modes have opposite load impedance mismatch responses, as shown in Figure 7. The parallel DPA maintains high saturation efficiency when $|Z_L| < Z_0$, but experiences significant degradation in back-off efficiency. Conversely, when $|Z_L| > Z_0$, the parallel DPA has high back-off efficiency and low saturation efficiency. In contrast, the serial DPA maintains high back-off efficiency when $|Z_L| < Z_0$ and high saturation efficiency when $|Z_L| > Z_0$, as illustrated in Figure 7. Therefore, by employing parallel/serial mode reconfiguration, it is possible to simultaneously maintain high saturation and back-off efficiencies under mismatched load condition. Based on the parallel/serial DPA mode reconfiguration, several scholars have proposed advanced design methods to compensate for load mismatch of DPAs [40–43].

It should be noted that parallel/serial mode reconfigurable DPAs are all realized using a quadrature coupler as the combiner, as shown in Figure 8. The DPA is in the parallel mode when the isolation port of the coupler is short-circuited and in the serial mode when the isolation port of the coupler is open-circuited. Therefore, when $|Z_L| > Z_0$, the isolation port of the coupler should be short-circuited. In this situation, PA1 and PA2 in Figure 8 work as the carrier and peaking PAs, respectively. On the other hand, when $|Z_L| < Z_0$, the isolation port of the coupler should be open-circuited. In this situation, PA1 and PA2 work as the peaking and carrier PAs, respectively.

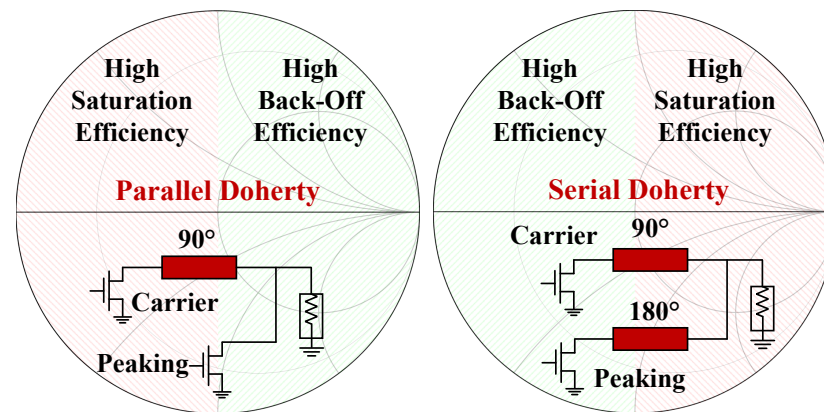


Figure 7. Parallel and serial DPAs under different load mismatch conditions.

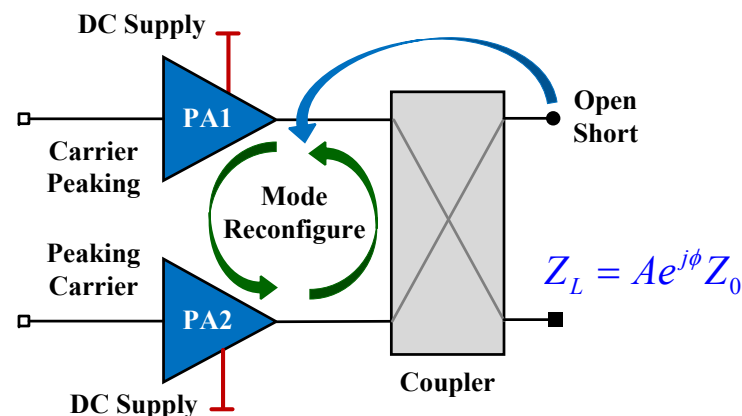


Figure 8. Mode reconfigurable DPA for compensating load mismatch.

In [40], the authors designed a 39 GHz DPA which can mitigate performance degradation under antenna VSWR variations in 5G mm-wave MIMO arrays through a reconfigurable parallel/serial Doherty architecture. The 39 GHz PA achieved an efficiency of 33.2% at OP_{1B} of 20.8 dBm. Under 3:1 VSWR load variation condition, the DPA recovers OP_{1B} to 18.5–19.12 dBm with an efficiency of 20.6–25.3%.

In [41], the authors proposed a quasi-balanced DPA (QB-DPA) with parallel and serial mode reconfiguration to improve load mismatch resilience. The QB-DPA is derived from an ideal balanced amplifier and can be reconfigured between parallel and serial Doherty modes by adjusting the loading of the isolation port and exchanging the roles of the carrier and peaking amplifiers. A 3.5 GHz QB-DPA was realized in [41], maintaining high linearity (<4% EVM) and efficiency (>31%) up to 2.5:1 VSWR. To extend the bandwidth of the QB-DPA, nominal/exchanged biasing and control of phase dispersion were adopted in [42]. A broadband QB-DPA working over 1.7–2.7 GHz was implemented in [42], exhibiting high efficiency (56–78% at OP_{1B}) and linearity under both matched and mismatched load conditions.

All the above mode reconfigurable DPAs have symmetrical configuration, leading to a limited high efficiency power range (6 dB). To solve this problem, a three-way mode reconfigurable DPA was proposed in [43] to maintain high efficiency over an output back-off range of 9 dB under both matched and mismatched load conditions. The proposed DPA employs three sub-amplifiers and a novel output combiner, enabling dual-mode reconfiguration by switching the impedance condition at the combiner control port and the gate biases of the sub-amplifiers. A 2.0 GHz dual-mode three-way DPA was constructed in [43] to validate the proposed theory. The three-way DPA in [43] achieved an efficiency

of 47.8–56.7% at 9 dB output back-off power level under load mismatch conditions up to 2:1 VSWR.

3. Load-Modulated Balanced Amplifier

DPA can maintain high efficiency over 6–10 dB output back-off power range. Therefore, it has been widely adopted in telecommunication systems. However, the DPA has a limited bandwidth due to the frequency dispersion of its combiner. To break the bandwidth limitation of the DPA, LMBA was proposed in 2016 by Professor Steve C. Cripps from Cardiff University [44].

3.1. Introduction on LMBA

The block diagram of the LMBA is depicted in Figure 9. In the LMBA, a balanced PA (D1 and D2 in Figure 9) works as the main amplifier. And a separate amplifier (D3 in Figure 9) injects control signal into the isolated port of the output coupler [44]. At the output back-off power level, the control amplifier is turned off, and the balanced PA operate near peak efficiency. In the high power region, the control signal dynamically adjusts the load impedance of the balanced PA by varying its amplitude and phase. Unlike conventional DPAs, the LMBA employs active load modulation through an external control signal (amplitude and phase adjustments) to modify the impedance seen by the balanced PA. This enables bidirectional (resistive and reactive) impedance tuning without relying on impedance inverter that has a limited bandwidth. Theoretical analysis demonstrated that the bandwidth of the LMBA is only limited by the 90° hybrid coupler. Therefore, it is easy to implement LMBA with octave bandwidth [45].

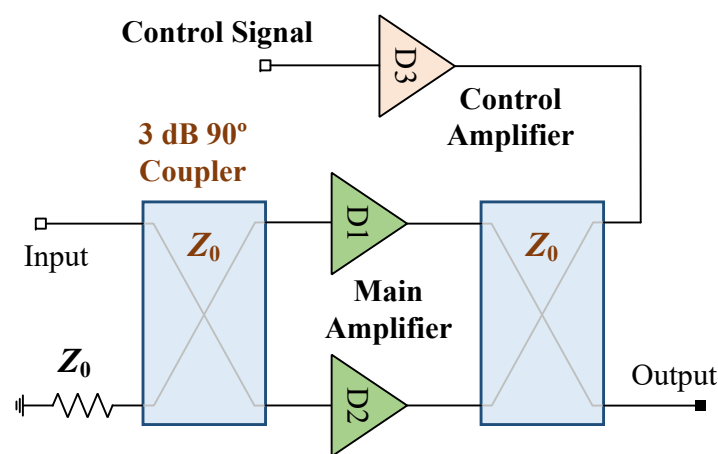


Figure 9. Block diagram of a LMBA.

While the LMBA achieves high efficiency across wide bandwidths, its high efficiency power range remains limited [46–48]. To address this, advanced LMBA variants, such as the pseudo-Doherty LMBA (PD-LMBA) and sequential LMBA (SLMBA), have been proposed to enhance efficiency at deep output power back-off (OBO) levels while maintaining broadband performance. As illustrated in Figure 10, these architectures employ a class-B biased control amplifier (CA) as the main PA and a class-C biased balanced PA pair as the auxiliary stage. For instance, a 3.05–3.55 GHz SLMBA demonstrated 42.3–43.7 dBm peak output power, 60.8–74.8% saturation drain efficiency (DE), and 43.2–51.4% DE at 10 dB OBO [47].

However, conventional PD-LMBA/SLMBA exhibit a critical limitation: the load impedance of the control amplifier remains constant across the entire power range. This forces the control amplifier into over-saturation once the auxiliary BPA activates, po-

tentially compromising stability and long-term reliability [48]. To mitigate this issue, asymmetric PD-LMBA (PD-ALMBA) and asymmetric SLMBA (ASLMBA) topologies were introduced [48,49], as shown in Figure 10. These variants ensure load modulation across all sub-amplifiers, preventing over-saturation. In [48], a 1.7–3.0 GHz PD-ALMBA was realized, achieving >50% DE over a 10 dB output back-off power range [48].

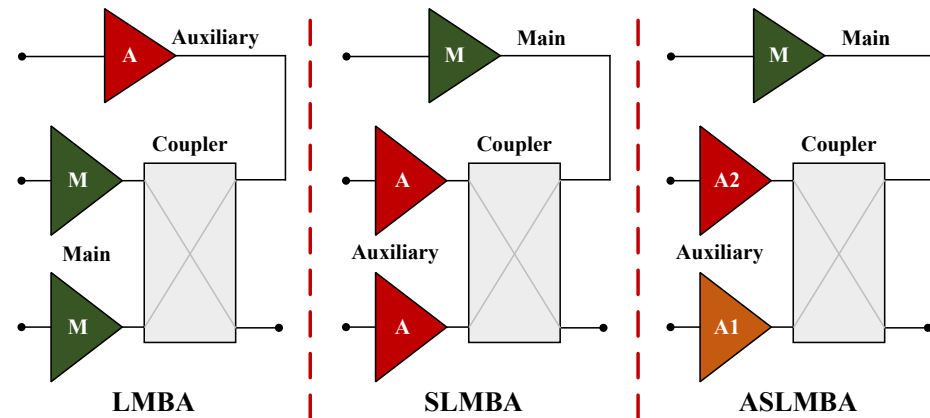


Figure 10. Simplified block diagram of LMBA and its variations.

3.2. Load Mismatch Compensation of LMBA

Similar to the DPA, the LMBA and its variations also undergo performance degradation when load impedance deviates from the optimal value. Therefore, this subsection gives a review of the load mismatch compensation of the LMBA. It is worth mentioning that there are currently very few papers that focus on the load mismatch compensation of the LMBA and its variations [50–52].

In [50], the authors proposed an orthogonal load-modulated balanced amplifier (OLMBA) to mitigate the effects of load mismatch on efficiency and output power of a PA. Figure 11 shows the block diagram of the proposed OLMBA, which has a control signal at the isolation port of the input coupler of a balanced PA and a variant impedance (jX) at the isolation port of the input coupler. The proposed OLMBA architecture utilizes an orthogonal load modulation technique, where the complex ratio between the main and control signals as well as the port impedance of the output coupler can be controlled electronically. This allows for readjusting the matching at the balanced devices and bringing the device impedances closer to the optimum, thereby mitigating the effects of load mismatch. The fabricated OLMBA in [50] achieved 45% power-added efficiency over 1.6–3.2 GHz under a load mismatch of $|\Gamma_L| = 0.6$.

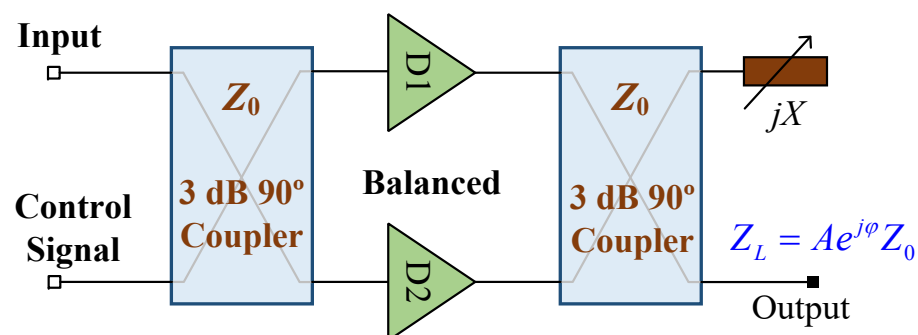


Figure 11. Orthogonal load-modulated balanced amplifier for compensating load mismatch.

In [51], the authors proposed a novel 1-D reconfigurable PD-LMBA to act against load mismatch across a wide bandwidth. The proposed architecture increases the load

mismatch resilience of the PD-LMBA only through the reconfiguration of the DC bias voltage of the control amplifier. Theoretical analysis reveals that when the control amplifier is driven into saturation, it exhibits a duality between a current source and a voltage source, enabling the balanced PA to have complementary load modulation trajectories for the two sub-amplifiers under the load mismatch condition. The proposed 1-D reconfigurable PD-LMBA minimizes the degree of freedom for PA reconfiguration and load sensing. As a validation, a broadband 1.7–2.9 GHz 1-D reconfigurable PD-LMBA was implemented in [51]. Under load mismatch conditions (2:1 VSWR), the fabricated PD-LMBA maintained excellent performance, with a maximum DE of 72.8% at peak power and up to 65.4% at 10 dB back-off power level.

Furthermore, in [52], the authors proposed a novel linear hybrid asymmetrical LMBA (H-ALMBA) with multiband reconfigurability and antenna-VSWR resilience, as shown in Figure 12. The H-ALMBA topology consists of a carrier amplifier (CA) and two peaking balanced amplifiers (BA1 and BA2). It has been demonstrated in [52] that the linearity and efficiency profiles of the H-ALMBA can be maintained against arbitrary load mismatch through the Z_L -dependent reconfiguration of the CA supply voltage and turning-on sequence of BA1 and BA2. The H-ALMBA DPA in [52] operated in the frequency range of 1.7–2.9 GHz, and achieved an efficiency of 47.1–64.8% at the maximum power level and an efficiency of 43.8–57.2% at 10 dB output back-off power level under load mismatch conditions of 2:1 VSWR.

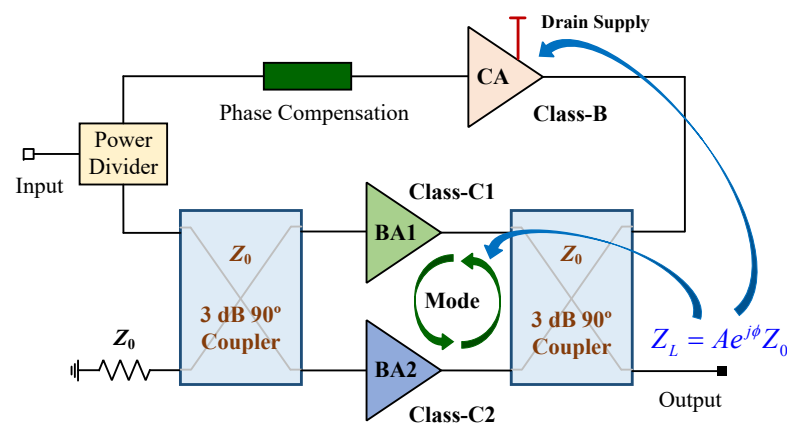


Figure 12. Hybrid asymmetrical LMBA for compensating load mismatch.

4. Potential Solutions

The aforementioned studies suggest that the investigation into mismatch-insensitive LMPAs is still in its preliminary stages of development, lacking systematic design approaches. As a summary and comparison, Table 1 lists several typical mismatch insensitive LMPAs and their measurement results under load mismatch conditions. It can be observed that the performance degradation of a PA caused by load mismatch can be compensated by input tuning, supply tuning, and mode reconfiguration. However, the performance of load-insensitive LMPA still has room for improvement. For example, the lowest back-off drain efficiencies of most of the load-insensitive DPAs are less than 40%. Therefore, it is of great importance to research load mismatch compensation techniques to improve the performances of the LMPAs under load mismatch conditions.

Furthermore, Table 1 indicates that broadband symmetrical two-way Doherty PAs can only maintain excellent conversion efficiency within a 6 dB output back-off power range [34,35,38,41,42], making them difficult to apply in modern wireless communication systems. To address this issue, three-way DPAs and LMBAs have become mainstream solutions. They can maintain high efficiency over a back-off range of 9–10 dB [43,51,52]. However, three-way DPA and LMBA have complex circuit structures, making them hard to

design. Therefore, it is highly beneficial to develop new design techniques aimed at expanding the back-off range of a broadband symmetrical DPA while ensuring load insensitivity.

Table 1. Measurement results of the fabricated concurrent class- F_2 and other state-of-the-art concurrent PAs.

Ref.	Architecture	Frequency (GHz)	Mismatch	Power (dBm)	η_{Sat} (%)	η_{BO} (%)	Technique
[34]	Symmetrical DPA	3.6	2:1 VSWR	42.6–43.8	49–63	35–50@6dB	Input Tuning; Supply Tuning
[35]	Symmetrical DPA	0.9	2:1 VSWR	30.7–31.1	57.8–67.2	N/A	Supply Tuning
[38]	Symmetrical DPA	2.4	2:1 VSWR	42.4–44.3	54.2–66.7	50.7–62.5@6dB	Mode Reconfiguration
[41]	Symmetrical DPA	3.5	2.5:1 VSWR	38.8–40.4	50–60 *	33–43@6dB *	Mode Reconfiguration
[42]	Symmetrical DPA	1.7–2.7	2:1 VSWR	39.1–40.2	49–62	38.1–42.9@6dB	Mode Reconfiguration
[43]	Three-way DPA	2.0	2:1 VSWR	44.8–46.3	50.2–65.8	47.8–56.7@9dB	Mode Reconfiguration
[51]	PD-LMBA	1.7–2.9	2:1 VSWR	39.1–41.4	51.9–72.8	38.6–65.4@10dB	Supply Tuning
[52]	HALMBA	1.7–2.9	2:1 VSWR	40–42.9	47.1–64.8	43.8–57.2@10dB	Mode Reconfiguration

η_{Sat} : Saturation drain efficiency. η_{BO} : Back-off drain efficiency. *: Graphically estimated. N/A: Not Available.

In addition, the aforementioned papers indicate that although existing mismatch insensitive LMPAs can maintain excellent saturation and back-off performances under mismatch conditions, they rely on external control circuits, such as input tuning, DC supply tuning, and mode reconfiguration, as shown in Figure 13. These external control circuits not only increase the complexity of the PA implementation but also introduce additional energy consumption. In [53], the authors proposed a load-modulated double-balanced amplifier that does not require any external control circuits and can maintain excellent performance against load impedance mismatch within a 2:1 VSWR circle. This novel LMPA architecture provides us with a direction for researching load mismatch compensation techniques. That is, it is of great significance to develop new PA architectures that eliminate the need for external control circuits and maintain excellent performance under load mismatch conditions.

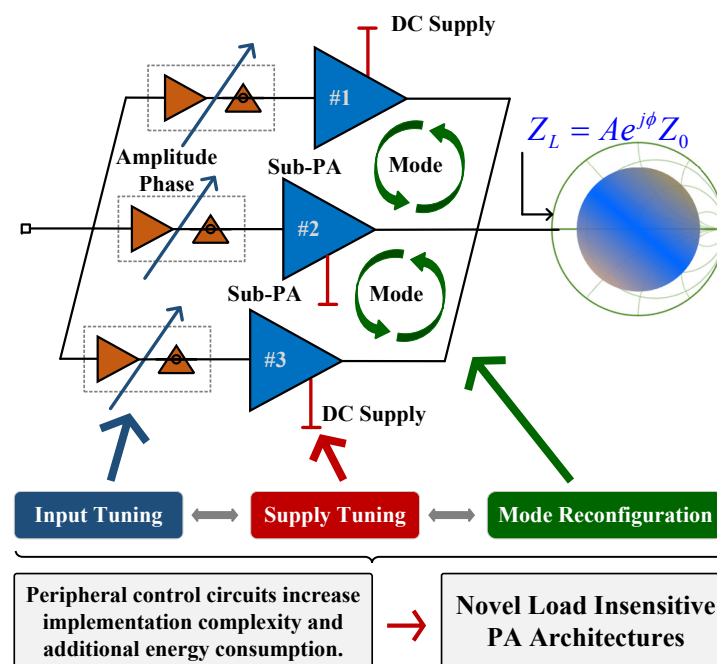


Figure 13. Load mismatch compensation techniques for LMPAs.

5. Conclusions

The article provides a comprehensive review on load mismatch compensation techniques for LMPAs, mainly focusing on DPAs and LMBAs. In modern wireless communication systems, mutual coupling between antennas causes load variation on PAs, leading to significant performance degradation. Therefore, various methods were developed to mitigate performance degradation caused by load mismatch. These methods can be summarized into three categories: DC supply voltage tuning, input signal adaptation, and mode reconfiguration. These three methods were widely by DPAs and LMBAs to act against load mismatch. This article also gives future research directions based on the review results. In the future, new load mismatch compensation techniques are expected to further improve the performances of a mismatched LMPA. And it is also of great significance to develop novel PA architectures that can maintain excellent performance under mismatched load conditions without relying on external control circuits.

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