energies

MDPI

Article

Performance Comparison of Asymmetrical Multilevel Inverter with Different Switching Techniques

Ashish Srivastava [1], Anurag Chauhan [1,*] and Anurag Tripathi [2]

[1] Rajkiya Engineering College Banda, AKTU Lucknow, Banda 210201, Uttar Pradesh, India; ashishsrivastava@recbanda.ac.in
[2] Institute of Engineering and Technology Lucknow, Lucknow 226021, Uttar Pradesh, India; anurag.tripathi@ietlucknow.ac.in
* Correspondence: anurag@recbanda.ac.in; Tel.: +91-8171015620

Abstract: In the present context, the asymmetrical multilevel inverter (AMLI) with minimal switches is extensively used to achieve high power quality across a load. The conventional inverter suffers from the disadvantages of large system components, low efficiency, high THD, high losses, etc. The asymmetrical multilevel inverter therefore offers an appropriate alternative to address the key issues of conventional inverters. The present paper aims to analyze the performance comparison of the proposed 15-level AMLI structure with different switching techniques, i.e., NLC, SHEPWM and SPWM. Moreover, loss analysis of the considered AMLI has been performed for different switching techniques. Furthermore, different performance parameters such as conduction losses, switching losses, total losses, THD, efficiency and power delivery of the inverter have been evaluated. It has been observed that the considered inverter topology offers the superior performance with the SHEPWM modulation technique at a modulation index of 0.8. Finally, hardware arrangement of the inverter has also been developed in the laboratory with a real-time Opal-RT 4510 simulator to verify the accuracy of simulation results.

Keywords: Opal-RT 4510; multilevel inverter; THD; NLC; SHEPWM; SPWM

Academic Editor: Miguel Castilla

Received: 29 September 2024
Revised: 25 October 2024
Accepted: 28 October 2024
Published: 5 February 2025

Citation: Srivastava, A.; Chauhan, A.; Tripathi, A. Performance Comparison of Asymmetrical Multilevel Inverter with Different Switching Techniques. *Energies* **2025**, *18*, 715. https://doi.org/10.3390/en18030715

1. Introduction

In the present context, the multilevel inverter (MLI) is widely used in the industry in order to obtain a power output with low THD. Generally, configuration of the MLI can be classified as symmetrical or asymmetrical. Symmetrical configuration of the MLI has many disadvantages, i.e., requirement of a large number of switches, low voltage levels, high THD, high conversion loss and low efficiency. However, asymmetrical MLI structure offers high efficiency, low conversion loss and low THD, with fewer switches to make more steps in the output voltage [1–6].

Foti et al. [7] proposed an asymmetric hybrid multilevel inverter (AHMLI) used for motor drives, and photo voltaic (PV) for fast and precise regulation. They obtained low-order current harmonic in grid current lower than 2%. THD in the primary voltage of transformer and grid current without harmonics compensation was estimated as 5.2% and 10.9%, respectively. These values are reduced to 2.9% and 11.9%, respectively, with power filter function.

Sarwer et al. [8] proposed a new design of the asymmetrical MLI to make 15 steps in the load voltage using NLC. Different losses of the inverter were also investigated by using PLECS software, and thermal modeling of the IGBT switch was performed. They proposed an MLI using simulation parameters, i.e., an output frequency of 50 Hz, R load

of 50 Ω and 100 Ω and L load of 250 mH. The THD in the load voltage was evaluated as 5.5% for the RL circuit. The maximum efficiency of the converter was calculated to be 98.6%. Thakre et al. [9] tested the performance of a 15-level inverter for different ranges of switching frequency. The inverter consisted of 12 MOSFET switches, and an 18 Ω + 25 mH load was considered. The voltage THD was measured as 4.25%, 3.45%, 2.59% and 2.15% for 15, 17, 23 and 31 voltage steps, respectively.

Chattopadhyay and Chakraborty [10] introduced an asymmetrical cascade topology with the aim of increasing the number of levels in a power system. They achieved this through the level doubling method, which incorporated floating capacitors. The result of this topology reduced the auxiliary source nearly 66% and obtained a 65-level inverter, with 12 switches required per phase to achieve high-resolution output voltage.

Karri et al. [11] proposed a symmetrical and asymmetrical configuration to obtain seven steps, nine steps and eleven steps in the load voltage. They compared the blocking voltage and cost function of the MLI with the latest topologies in this area. They tested the developed hardware for various operating conditions. Singh et al. [12] analyzed a reduced-switch nine-level MLI with a single source to generate all levels of voltage. They employed the carrier PWM method in the MLI to estimate the harmonics using a MATLAB/Simulink environment.

Kurdkandi [13] developed a transformer-less inverter to supply the unity and non-unity power factor loads. A controller was designed to produce the different pulses and to control active and reactive power between inverter and load. Percentage harmonic in the load voltage and output current were estimated to be 25.65% and 1.51%, respectively, for a load of 0.77 kW. Choudhary et al. [14] designed a 17-level inverter using a switched capacitor to obtain high gain. They employed the series and parallel combination of capacitors for the automatic balance of voltage with input voltage source. They minimized the inrush current of the capacitor by using soft switching. THD values in the voltage without and with induction were estimated as 4.73% and 4.03%, respectively.

Bana et al. [15] investigated the performance evaluation of a 3.9 kW solar-PV-coupled 17-level inverter using carrier-based PWM and SHE modulation schemes. They tested the inverter for step variation in solar radiation, rapid changes in load, frequency variation and changes in modulation index. The harmonic spectrum in the output voltage was estimated as 3.88% and 2.18% for the PWM and SHE modulation schemes, respectively.

Hussain et al. [16] developed a 15-level switched-capacitor-based MLI with self-balancing property of capacitor. The designed inverter offered the maximum efficiency of 96.33% with THD of 7.82%. They tested the waveform of load voltage and current under sudden change in the load from 0 to 150 ohm + 120 mH to a load of 75 ohms and 150 ohm + 120 mH to a load of 150 ohms, respectively. Fahad et al. [17] demonstrated the working of the 15-level MLI to minimize the THD and cost with the increase in system efficiency. The harmonic spectrum of load voltage and load current were determined to be 5.50% and 3.26%, respectively. They tested the different output waveforms of the MLI for the modulation indexes of 0.2 to 1.

Based on the review of papers, it is noticed that most of the researchers have not compared the performance parameters of the AMLI with different modulation techniques. Further, the effect of changes of modulation index, frequency and load change on the levels in the load voltage was not analyzed. Also, efficiency and losses of AMLI were not estimated for the variation in modulation indexes [11–20].

This paper proposes an asymmetrical MLI structure with minimum switches to produce seven and fifteen steps in the load voltage. As per the requirement, expansion of the considered MLI configuration can be made to obtain more levels of voltage with the built-in capability to obtain both positive and negative levels. Further, different modulation

techniques, i.e., SPWM, SHEPWM and NLC, are used to generate pulses for different switches of the inverter. Performance parameters of the inverter have been determined with various modulation techniques. Parameters, i.e., number of levels, THD, losses, power delivery and efficiency, are considered in the paper. Inverter operation is also verified for change in load and modulation indexes.

Section-wise organization of the paper is summarized as follows. Structure of the considered topology of the AMLI is discussed in Section 2. The methodology of different modulation techniques, i.e., SPWM, NLC and SHEPWM, is given in Section 3. Gate pulses of different switches for SPWM, NLC and SHEPWM methods are discussed in Section 4. Section 5 describes the mathematical model for the loss analysis of the AMLI. Finally, different results of the system simulation and system hardware test bench are obtained and discussed in Section 6.

2. Asymmetrical MLI Topology

A simple unit of the considered novel modular AMLI topology is depicted in Figure 1. The AMLI structure uses twelve MOSFET switches, three sources and ten driver circuits to achieve fifteen levels in the load voltage. This topology can be modified as cascaded connection of basic modules to attain more steps in the load voltage. A higher number of levels may be useful in electric vehicles, pumps, compressors, conveyors and DC transmission applications.

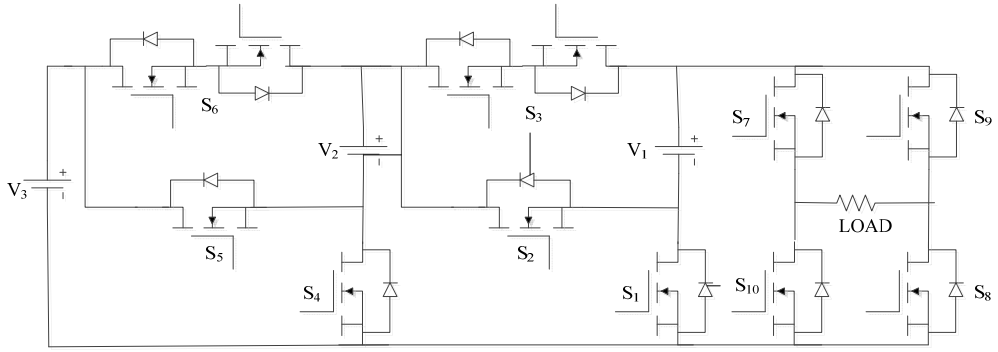

Figure 1. Schematic of 15-level topology of asymmetrical MLI.

Different switching patterns of the 15-level inverter topology are summarized in Table 1. Switches S_7 and S_8 or S_9 and S_{10} are required in the ON state simultaneously to obtain zero load voltage, while switches S_1, S_7 and S_8 simultaneously can be turned on to achieve the first step of load voltage ($+V_1$). Different switching states for obtaining other steps of the load voltage, i.e., $\pm(V_1 + V_2 + V_3)$, $\pm V_3$, $\pm(V_2 + V_3)$, $\pm(V_1 + V_3)$, $\pm(V_1 + V_2)$, $\pm V_1$ and $\pm V_2$, are also given in Table 1. The magnitude of different DC supply is considered based on the load voltage.

Table 1. Current conducting path and switching pattern of asymmetrical MLI.

S. No.	Switching States $S_1S_2 \ldots S_9S_{10}$	Current Conducting Path	Voltage Levels
1	0000001100	S_8–L–S_{10}	0
2	1000001100	V_1–S_7–L–S_8–S_1–V_1	V_1
3	0011001100	V_2–S_3–S_7–L–S_8–S_4–V_2	V_2
4	0101001100	V_3–S_6–S_3–S_7–L–S_8–V_3	V_3
5	0010011100	V_2–S_2–V_1–S_7–L–S_8–S_4–V_2	$V_1 + V_2$

Table 1. *Cont.*

S. No.	Switching States $S_1S_2 \ldots S_9S_{10}$	Current Conducting Path	Voltage Levels
6	0100011100	V_3–S_6–S_2–V_1–S_7–L–S_8–V_3	$V_1 + V_3$
7	0010101100	V_3–S_5–V_2–S_3–S_7–L–S_8–V_3	$V_2 + V_3$
8	0100101100	V_3–S_5–V_2–S_2–V_1–S_7–L–S_8–V_3	$V_1 + V_2 + V_3$
9	0000000011	S_9–L–S_7	0
10	1000000011	V_1–S_9–L–S_{10}–S_1–V_1	$-V_1$
11	0011000011	V_2–S_3–S_9–L–S_{10}–S_4–V_2	$-V_2$
12	0101000011	V_3–S_6–S_3–S_9–L–S_{10}–V_3	$-V_3$
13	0010010011	V_2–S_2–V_1–S_9–L–S_{10}–S_4–V_2	$-V_1-V_2$
14	0100010011	V_3–S_6–S_2–V_1–S_9–L–S_{10}–V_3	$-V_1-V_3$
15	0010100011	V_3–S_5–V_2–S_3–S_9–L–S_{10}–V_3	$-V_2-V_3$
16	0100100011	V_3–S_5–V_2–S_2–V_1–S_9–L–S_{10}–V_3	$-V_1-V_2-V_3$

Flow of current in the load can be estimated on the basis of the switching pattern of power switches. Further, all 15 voltage steps in the load can be achieved by using switching states as per Table 1. It is always checked that flow of electric current follows a closed path and the other parts of the circuit are closed to avoid short circuit. Further, the remaining switches are turned off to obtain a uniform current flow.

Further, it has been noticed that the considered asymmetrical MLI topology is modular, and it is compared with the topologies reported in the literature on the basis of requirement of voltage sources (N_{VS}), number of voltage steps (N_{Step}), number of switches (N_{Swi}), number of driver circuits (N_{Dri}), number of on-state switches ($N_{On\text{-}swi}$), etc., as given in Table 2. It has been observed that the proposed topology of inverter requires a smaller number of switches and driver circuits to obtain 15 voltage steps across the load. The number of switches per voltage level is also lower compared to other configurations reported in the literature. Also, fewer gate driver circuits are required for switches in the proposed topology.

Table 2. Comparison of the proposed AMLI topology with other reported topologies.

References	N_{Step}	N_{VS}	N_{Swi}	N_{Dri}	N_{Diode}	N_{Cap}	$N_{On\text{-}swi}$	N_{swi}/N_{Step}
[8]	15	4	10	9	0	0	4	0.66
[21]	15	3	12	12	2	-	5	0.80
[22]	15	3	12	12	0	0	5	0.80
[23]	15	3	7	7	3	0	5	0.47
[24]	15	3	10	10	0	0	5	0.66
[25]	17	4	10	9	-	-	5	0.59
[26]	17	2	12	11	1	3	6	0.71
[27]	17	4	12	9	0	0	3	0.71
[28]	17	4	12	10	0	0	5	0.71
[29]	11	3	8	7	0	0	3	0.73
[30]	11	3	10	9	0	0	4	0.91
Proposed	15	3	10	8	0	0	4	0.66

3. Modulation Techniques

Under the present paper, three modulation methods, i.e., SPWM, NLC and SHEPWM, have been utilized for producing the pulses for switch operation. A brief description of each of these switching techniques follows:

3.1. SPWM

The sine pulse width modulation (SPWM) method is famous for minimizing the low-frequency harmonics. In this modulation scheme, the amplitude of the sine waveform is emulated by the carrier triangular signal to achieve the gate signal for the inverter. When the amplitude of the sine waveform is greater than triangular signal, then a pulse is produced for the positive cycle. When the amplitude of the triangular signal is greater than the sine waveform, then no pulse is produced [31–33]. Accordingly, switching pulses of fixed magnitude over a definite time interval can be generated for the switching operation of the inverter. A schematic of SPWM is depicted in Figure 2.

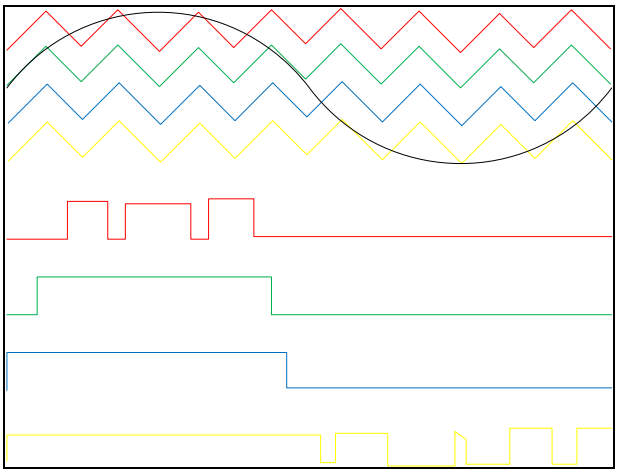

Figure 2. Schematic of SPWM method.

3.2. NLC

The nearest-level-based control scheme uses low switching frequency to produce staircase load voltage. This scheme is inspired by the space vector control method. This modulation method offers low losses and low THD in the load voltage with high efficiency. Different research articles have revealed that switching frequency in the range from 50 Hz to 200 Hz produces more voltage levels with minimum losses. In this control scheme, the required voltage level is compared with a sine waveform to obtain different switching instants. Finally, the nearest voltage level is determined by rounding the reference sinusoidal voltage [34,35]. A schematic of the NLC scheme is shown in Figure 3.

Unidirectional switches of the AMLI function at two times the fundamental frequency, whereas bidirectional switches of the inverter operate at the fundamental frequency. The value of the modulation index (Mi) depends on V_{re}, and it can be modelled as follows:

$$Mi = 2V_{re} \left(N_{Step} - 1\right) V_{1Step} \quad (1)$$

where V_{1Step} is the voltage of a single step, V_{re} is the voltage of the sine wave and N_{Step} represents voltage levels in the load voltage.

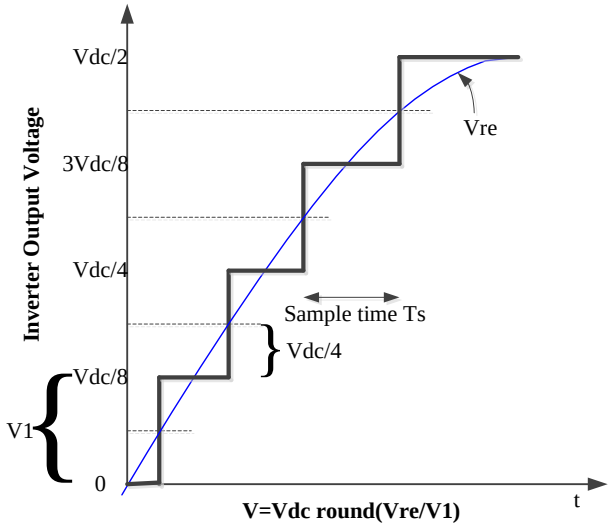

Figure 3. Schematic of NLC scheme.

3.3. SHEPWM

In the present work, the SHEPWM technique has been used to eliminate the harmonic components for specific values of modulation indexes. Therefore, preference is given for obtaining the principle component at the required level. Under the present optimization framework, the fitness function given by Equation (2) is minimized to find the best switching angles for different modulation indexes.

$$f = \min\left[\left|100\frac{V_{Reqd} - V_1}{V_{Reqd}}\right|^4 + \sum_{s=2}^{S}\frac{1}{h_s}\left|50\frac{V_{h_s}}{V_1}\right|^2\right] \quad (2)$$

where V_{Reqd} is the required value of the principle component, and h_s is the harmonic order that needs to be eliminated (i.e., $h_2 = 3$, $h_3 = 5$ and $h_4 = 7$).

The first segment of the objective function ensures that the error between the required load voltage and V_1 is less than 1% to obtain the desired fundamental voltage. If expression fails, then the expression is penalized by the power of 4. The second segment of the fitness function minimizes the lower harmonics under 2% of the fundamental component. If expression violates, then it is penalized by the power of 2. In this paper, firing angles of switches have been determined for the 15-level inverter for modulation indexes varying from 0 to 1.

Further, codes of the particle swarm optimization (PSO) algorithm are written in MATLAB for obtaining the best value of switching angles of the AMLI. Switching angles have been determined for various modulation indexes changing from 0.1 to 1. A Fourier series has been used to examine the different levels of the load voltage. A Fourier series model of the voltage is given as follows [36–39]:

$$V(\omega t) = \sum_{n=1}^{\infty} V_n \sin(nwt) \quad (3)$$

where V_n is the voltage magnitude of the n^{th} harmonic.

Voltage magnitude of harmonic is computed by Equation (4) as:

$$V_n = \begin{cases} \frac{4V_{nom}}{n\pi}\sum_{j=1}^{S} n_j \cos(n\xi_j) & ; \text{ odd value of ns} \\ 0 & ; \text{ even value of ns} \end{cases} \quad (4)$$

where ξ_j signifies the triggering angles estimated in increasing order $(0 < \xi_1 < \xi_2 < \cdots < \xi_S \leq \frac{\pi}{2})$, n_j is the V_{nomj} to V_{nom} and V_{nom} is the nominal value of DC voltage.

In the present paper, lower-order third, fifth and seventh harmonic voltages have been selected, and these voltages are considered for exclusion in the load voltage of the AMLI.

The main aim of the SHEPWM technique is to compute the various firing angles which regulate the principal part of the load voltage. Also, this method reduces the lower-order harmonic voltages. The optimum firing angles of the considered MLI configuration are measured by the following Equation (5) as:

$$\left.\begin{array}{c} \mathrm{Mi} = \left\{\frac{1}{S}(\cos(\xi_1) + \cos(\xi_2) + \cos(\xi_3) + \cos(\xi_4) + \cos(\xi_5) + \cos(\xi_6) + \cos(\xi_7))\right. \\ (\cos(3\xi_1) + \cos(3\xi_2) + \cos(3\xi_3) + \cos(3\xi_4) + \cos(3\xi_5) + \cos(3\xi_6) + \cos(3\xi_7)) = 0 \\ (\cos(5\xi_1) + \cos(5\xi_2) + \cos(5\xi_3) + \cos(5\xi_4) + \cos(5\xi_5) + \cos(5\xi_6) + \cos(5\xi_7)) = 0 \\ (\cos(7\xi_1) + \cos(7\xi_2) + \cos(7\xi_3) + \cos(7\xi_4) + \cos(7\xi_5) + \cos(7\xi_6) + \cos(7\xi_7)) = 0 \end{array}\right\} \quad (5)$$

The modulation index (Mi) of the inverter is computed using Equation (6) as:

$$\mathrm{Mi} = \frac{\pi V_{Req}}{4SV_{nom}};\ 0 < \mathrm{Mi} \leq 1 \quad (6)$$

4. Switching Pulses of Different Modulation Methods

Switching pulses of different switches of the considered topology have been generated for NLC, SPWM and SHEPWM as depicted in Figures 4–6. In all modulation methods, switching of S_7 and S_9 are complementary to each other. Similarly, switching pulses of S_8 and S_{10} are opposite in all methods. Switches S_1–S_6 are used for generating positive step voltage, while switches S_7 to S_{10} are utilized to generate a bipolar voltage across the load. Switching pulses are generated using MATLAB/Simulink to trigger the various switches of the considered AMLI through the real-time Opal-RT 4510 controller.

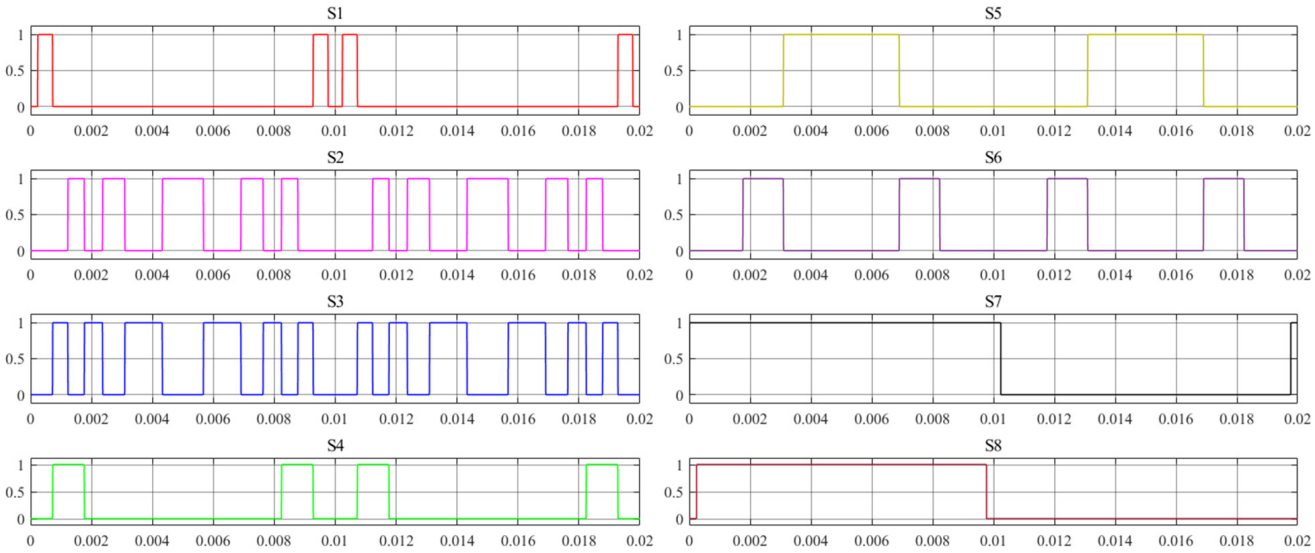

Figure 4. Switching pulses for NLC.

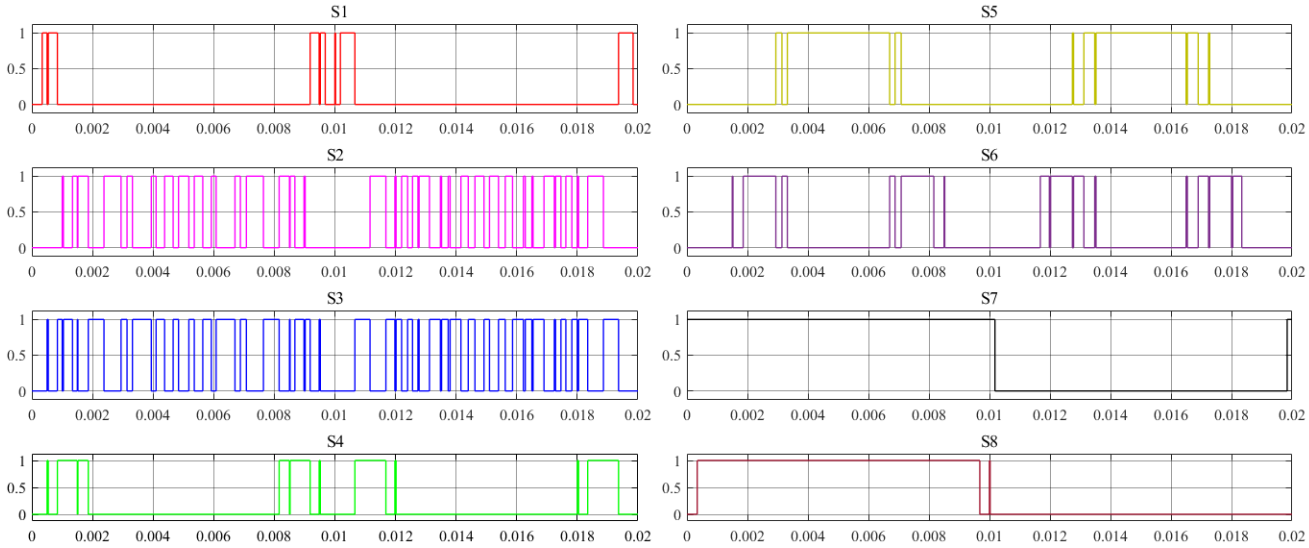

Figure 5. Switching pulses for SPWM.

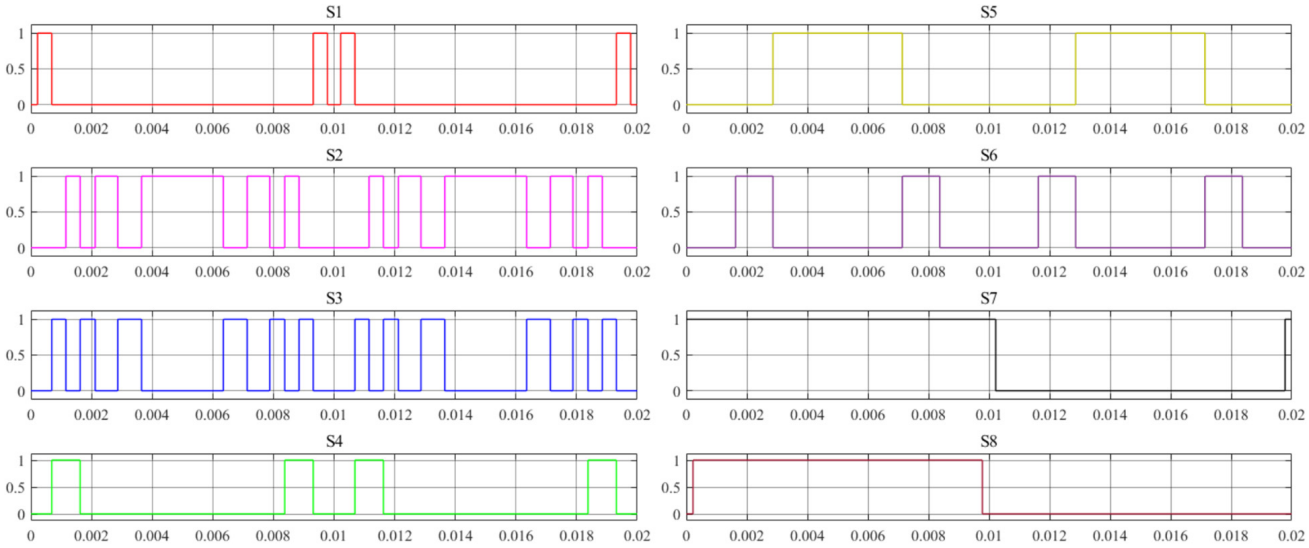

Figure 6. Switching pulses for SHEPWM.

5. Computation of Total Power Loss

In the AMLI configuration, the functioning of power switches is the key contributor in the losses of the inverter. Losses in switches are majorly classified as conduction and switching. Total power loss in the AMLI is the sum of these losses. Conduction loss appears in a switch during the conduction state to OFF state, whereas switching loss persists in a switch for the time period of state change, i.e., OFF to ON and ON to OFF.

The expression of conduction losses (P_{con}) is the function of the voltage across the switch voltage (V_{swi}), device resistance (R_{swi}), rms current (I_{rms}) and average current (I_{avg}) through the switch, while that of switching losses (P_{swi}) depends on switch turn-on time, turn-off time, blocking voltage, switching frequency (f_{swi}) and current. Computation of the conduction loss, switching loss and total power losses (P_{TPL}) of the AMLI are modeled as follows:

$$P_{con} = I_{av}V_{swi} + I_{rms}^2 R_{swi} \tag{7}$$

$$P_{swi} = \frac{V_{Block}I_{ON}T_{swon}f_{swi}}{6} + \frac{V_{Block}I_{OFF}T_{swoff}f_{swi}}{6} \tag{8}$$

$$P_{TPL} = P_{con} + P_{swi} \tag{9}$$

where I_{OFF} and I_{ON} denote the current flowing in the circuit on the basis of switching condition, V_{Block} represents the blocking voltage and T_{swoff} and T_{swon}, respectively, signify the turn-on and turn-off time of a typical switch.

6. Simulation and Experimental Results

Simulation of the considered AMLI has been carried out in MATLAB/Simulink 2019a to obtain 15 voltage steps. Modulation methods, i.e., SPWM, SHEPWM and NLC, are used for the operation of the considered AMLI in the present work. Different AMLI performance parameters are monitored and assessed for several real-time conditions, i.e., voltage steps, frequency change, variation in modulation index, total losses, harmonic spectrum, conduction losses and switching losses are determined.

An experimental test bench of the considered AMLI is developed as presented in Figure 7. Different components have been used in the hardware development of the AMLI, which include MOSFET, driver circuit, current sensor, voltage sensor, DSO, quality analyzer, optocoupler, etc. A summary of the brief specifications of these components is given in Table 3. Simulated results have been further verified in hardware with an OPAL RT 4510 simulator and RL load. Opal RT generates the switching pulses for the inverter setup [40,41]. The same setup is used to verify the results of NLC, SHEPWM and SPWM modulation techniques. Due to the high-frequency limitation of the power quality analyzer (Fluke Power logger 1736), SPWM is tested at 2 kHz switching frequency.

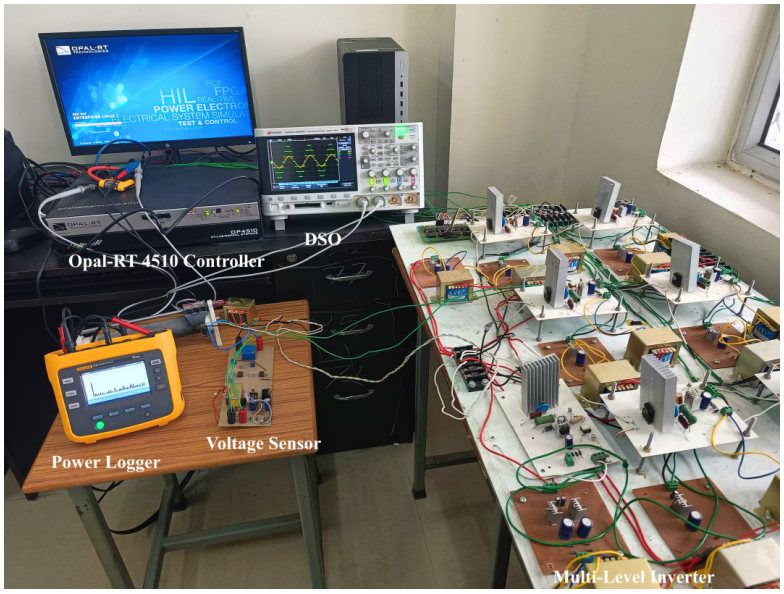

Figure 7. Experimental test bench of the asymmetrical AMLI.

A simulation of the 15-level AMLI is tested for different modulation techniques, and results are compared based on the voltage steps, current, THD, losses and efficiency. The DC voltage sources used in the 15-level modular AMLI are 400 V, 200 V and 100 V, with a peak voltage value of 700 V. The inverter is tested under two test conditions with fixed RL load and sampling time of 10 micro-seconds:

(a) Effect of frequency variation: 50–100 Hz
(b) Effect of variation of modulation index: 0.4, 0.6 and 0.8.

In the first case, the effect of frequency fluctuation, i.e., 50 Hz to 100 Hz, is analyzed. In the simulation results, it is found that there is no change in the steps or level of load voltage for varying frequency with the NLC, SHEPWM and SPWM modulation techniques. Further, simulation results of the 15-level inverter with variable frequency for NLC, SHEPWM and

SPWM are verified by the results on the experimental hardware setup, as clearly visible in Figures 8–10, respectively. Therefore, performance of the inverter is found satisfactory for the change in operating frequency.

Table 3. Summary of brief specifications of different hardware components.

S. No.	Component/Equipment Name	Brief Specifications
1	desktop comupter, HP	8 GB RAM, i7 @ 1.80 GHz, 64-bit operating system
2	Frequency	50 Hz
3	DC voltage sources	400 V, 200 V, 100 V
4	Load component	L = 20 mH and R = 50 Ω
5	Real-time simulator, Opal-RT	4510
6	Voltage sensor	AD202JN
7	Power logger, Fluke	1736
8	Optocoupler	MCT2E
9	Multimeter, Fluke	17B+
10	Digital oscilloscope, Keysight Technologies	DSOX1204G
11	Number of steps in the load voltage	15
12	MOSFET (IRFP460)	20 A, 500 V
13	Current sensor	HTP50

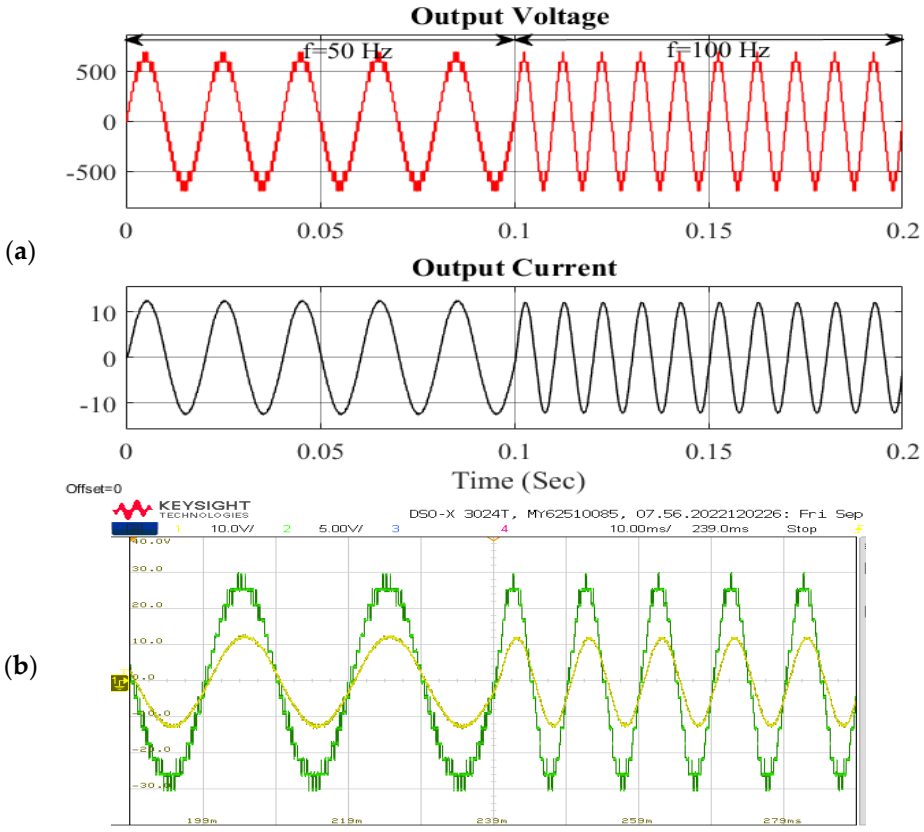

Figure 8. Output voltage and current waveform of AMLI with frequency change using SPWM: (**a**) simulation; (**b**) hardware.

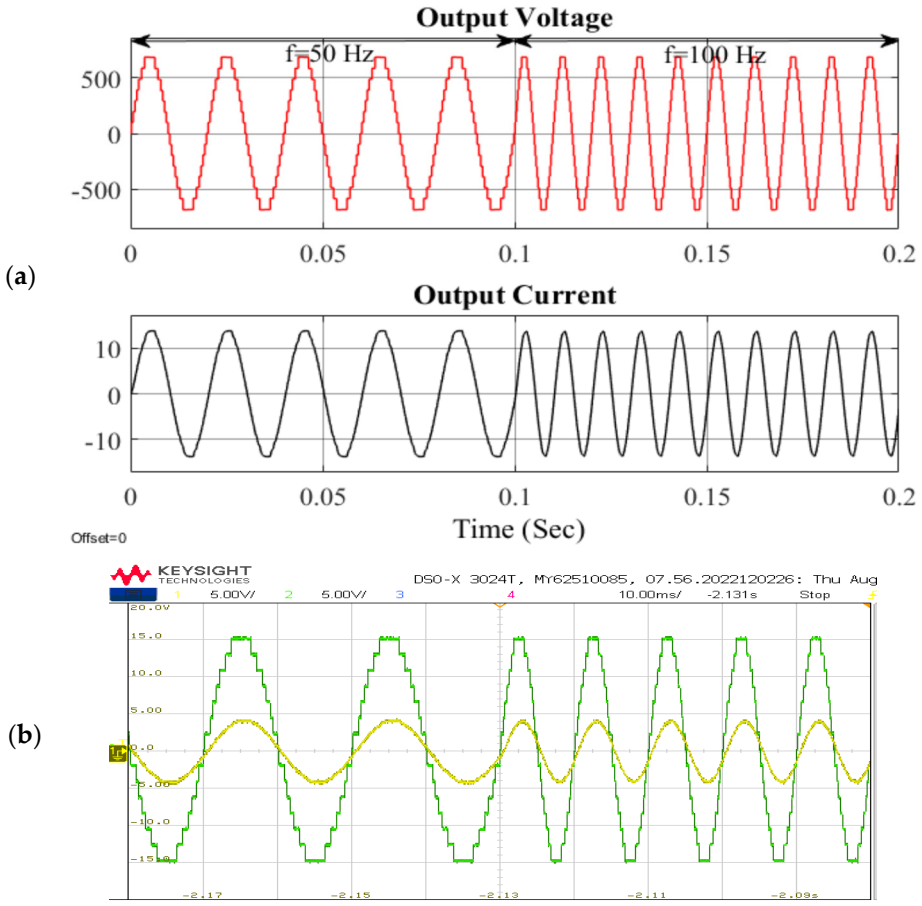

Figure 9. Output voltage and current waveform of AMLI with frequency change using SHEPWM: (**a**) simulation; (**b**) hardware.

In the second case, steps in the output waveforms of the 15-level inverter are tested for distinct values of modulation indexes with NLC, SHEPWM and SPWM modulation techniques. It is found that different levels are achieved with modulation techniques for the same value of modulation index.

For the modulation index of 0.4, the SPWM, SHEPWM and NLC modulation techniques produce seven levels, nine levels and seven levels in the load voltage, respectively. Eleven, fifteen and nine levels are produced with the SPWM, SHEPWM and NLC methods for Mi = 0.6. Further, analysis is performed to obtain 15 steps in the load voltage for different switching methods. It has been observed that 15 levels are achieved in the load voltage with SPWM, SHEPWM and NLC methods for the modulation index of 0.90, 0.80 and 0.95, respectively. Different simulation and hardware results of the inverter with the SPWN, SHEPWM and NLC modulation techniques for various modulation indexes are shown in Figure 11.

Further, the load on the considered MLI has been varied from 25 $\Omega + 40$ mH to 50 $\Omega + 20$ mH to test the performance of the system for Mi = 0.80. The output load voltage waveform and current waveform under dynamic change in load are depicted in Figure 12. It has been found that the considered system shows the stable operation under varying load conditions both in simulation and the experimental hardware test bench. Also, the experimental test results match with the simulation results.

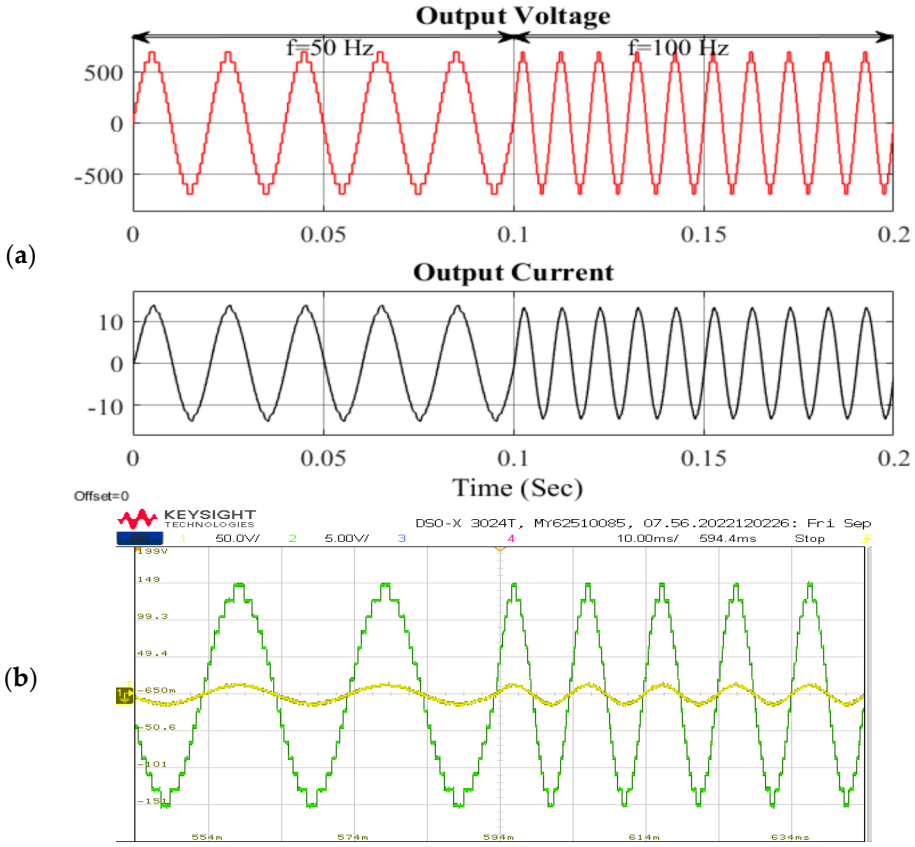

Figure 10. Voltage and current waveform of AMLI with frequency variation using NLC: (**a**) simulation; (**b**) hardware.

Furthermore, power loss analysis of the AMLI has been carried out to compute the conduction losses, switching losses and total losses with the considered switching methods. Accordingly, the efficiency and total load power of the AMLI are estimated for different Mi values from 0.1 to 0.9, as visible in Figure 13. It is perceived that the SHEPWM method offers the highest efficiency of 97.40% while delivering the output load power of 4.77 kW. Total losses are estimated as 125.58 W at Mi = 0.8. In total losses, the share of conduction loss (114.40 W) is greater than that of switching losses (11.18 W).

The efficiency and total losses of the AMLI with the SPWM method are obtained as 97.21% and 106.40 W, respectively, for Mi = 0.9. At this point, the AMLI delivers the load power of 3.71 kW to achieve the considered 15 levels. At Mi = 0.80, efficiency and total losses are estimated as 97.14% and 86.18 W, respectively, with 13 steps in the load voltage. Further, total losses and efficiency with the NLC technique are calculated at Mi = 0.9 as 105.88 W and 97.18%, respectively, to feed the load power of 3.65 kW. At Mi = 0.80, efficiency and total losses of the AMLI are estimated as 97.09% and 88.49 W, respectively. However, only 13 levels are achieved at Mi = 0.8 and Mi = 0.9. At Mi = 0.95, all 15 voltage steps are achieved with lesser efficiency.

The THD spectrum of the 15-level inverter model is measured through the FFT toolbox of MATLAB. Power logger (Fluke 1736) is used to estimate the harmonics of the experimental test bench. Further, the spectrum of harmonic voltages and fundamental voltage are collected for the SPWM, SHEPWM and NLC methods, as shown in Figure 14. It is found that the value of THD in the load voltage is lower in the case of hardware setup in comparison with the simulation.

At Mi = 0.80, it is observed that SHEPWM offers the lowest THD of 5.45% and 5.10% on simulation and hardware setup, respectively, whereas THD in the load voltage with

NLC and SPWM are estimated as 6.66% (Mi = 0.86) and 9.19% (Mi = 0.90), respectively, using the MATLAB simulation. In the AMLI hardware setup, NLC and SPWM offer a lower THD of 5.60% and 6.80%, respectively, as compared to the simulation.

Average power distribution of different voltage sources to meet the load has been estimated for the considered modulation techniques as reported in Table 4. It has been noted that among three sources, voltage source V_3 delivers the highest power to meet the load, followed by voltage source V_2 and V_1. In the case of SHEPWM, the power distribution of voltage sources V_1, V_2 and V_3 as a percentage of load power is calculated as 62.41%, 26.68% and 12.84%, respectively. Power distributions of SPWM and NLC are also estimated as reported in Table 4.

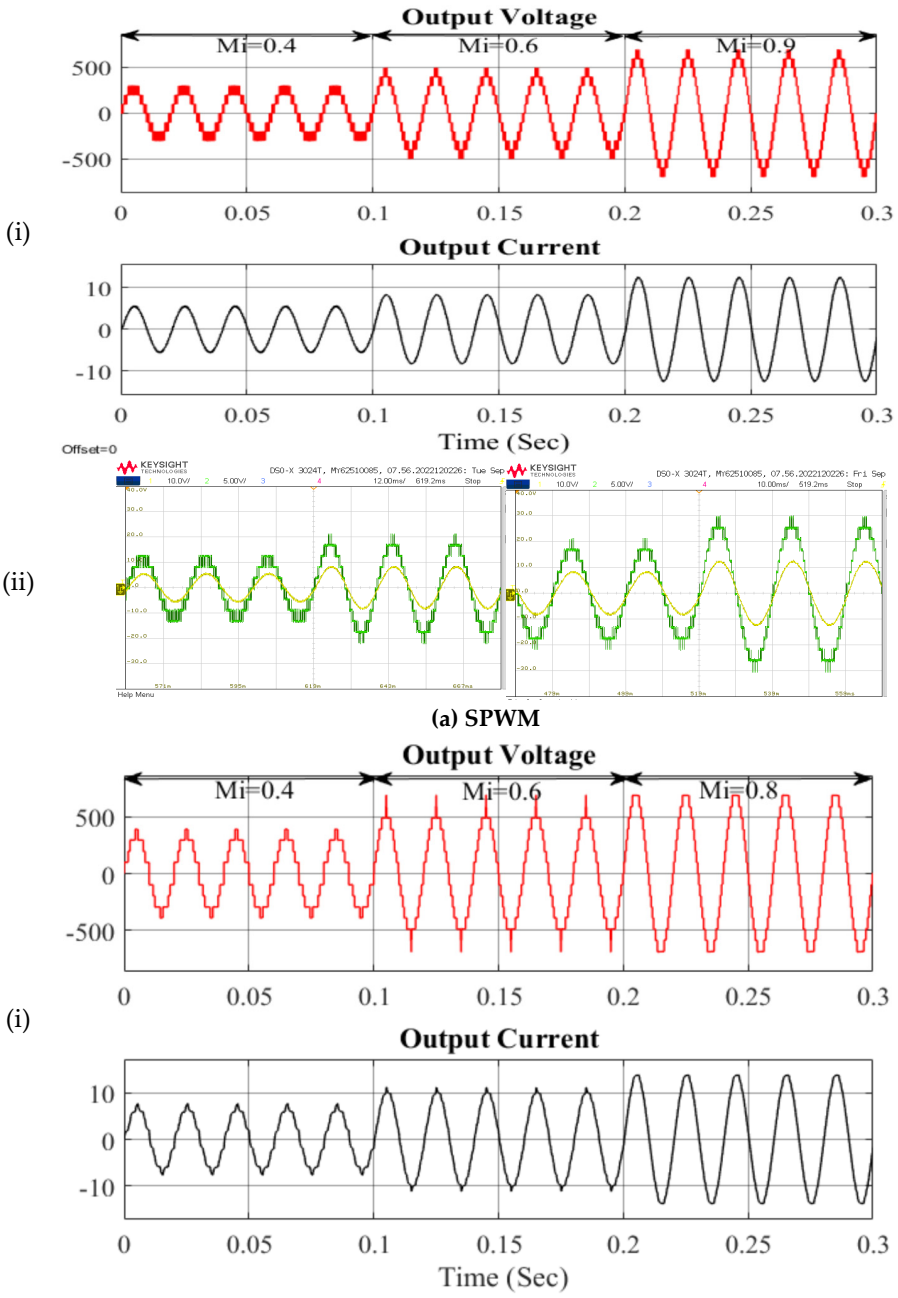

Figure 11. *Cont.*

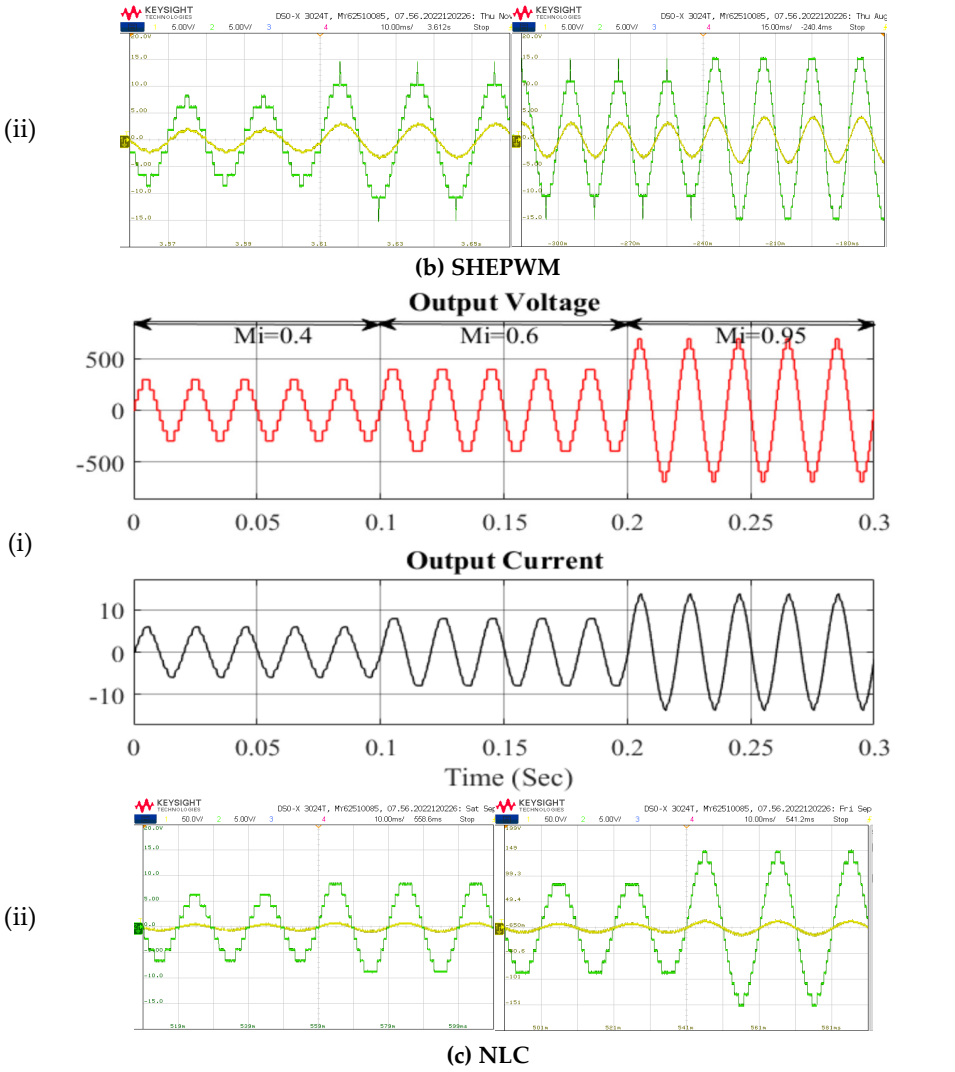

Figure 11. Voltage waveform and current waveform of 15-level AMLI with modulation index: (**i**) simulation; (**ii**) hardware.

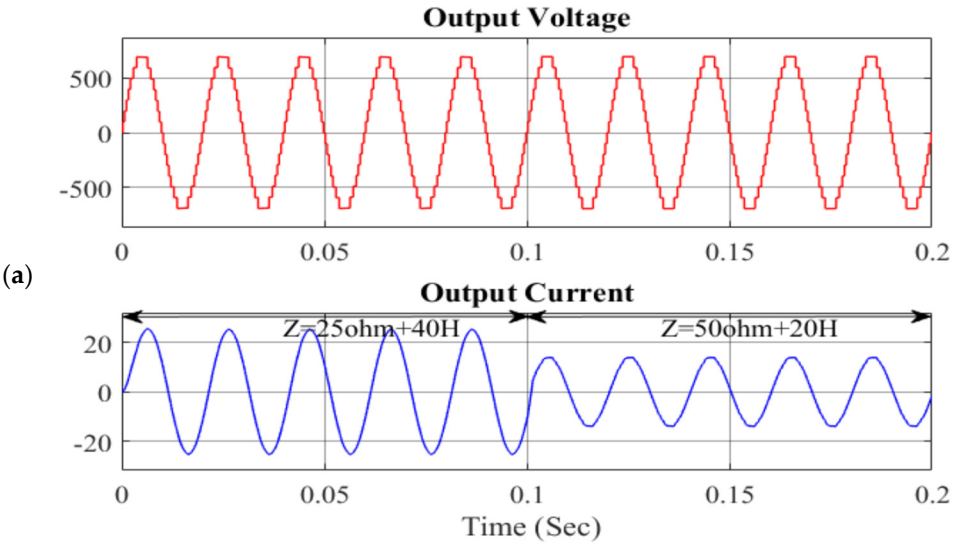

Figure 12. *Cont.*

(**b**)

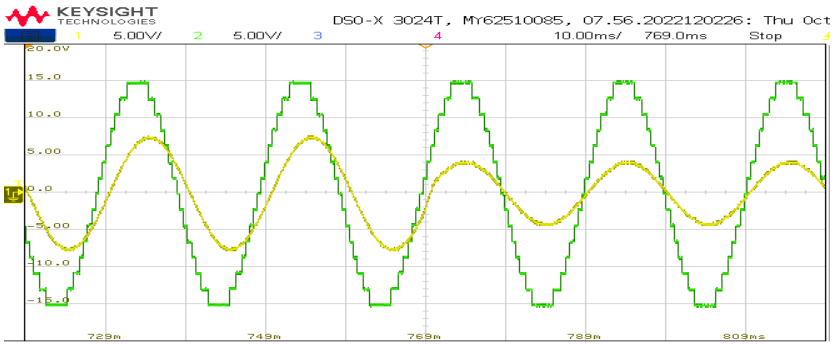

Figure 12. Load voltage and current waveforms under dynamic load change from 25 Ω + 40 mH to 50 Ω + 20 mH: (**a**) simulation; (**b**) hardware.

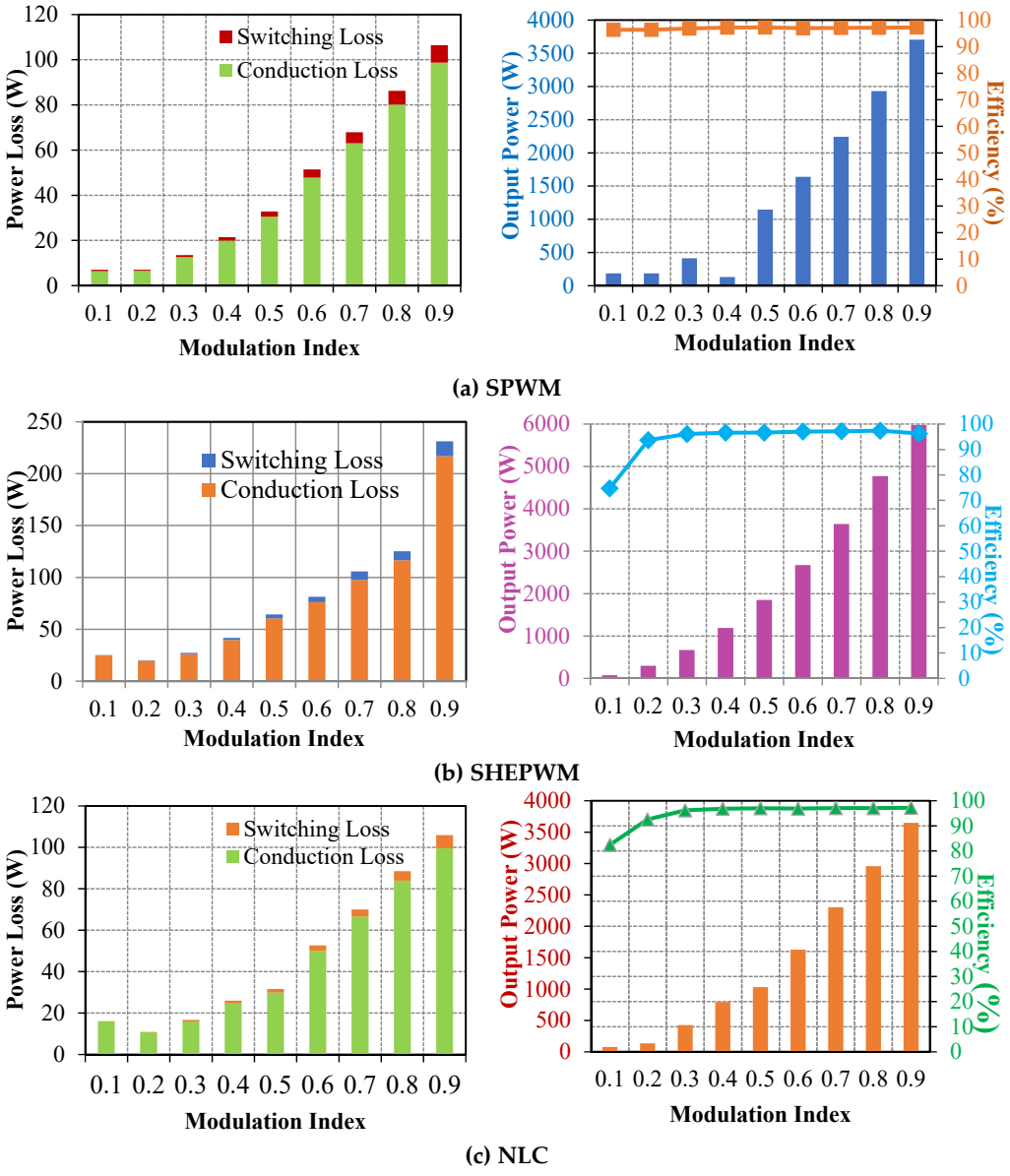

Figure 13. Power loss, efficiency and output power of AMLI with variation in modulation index.

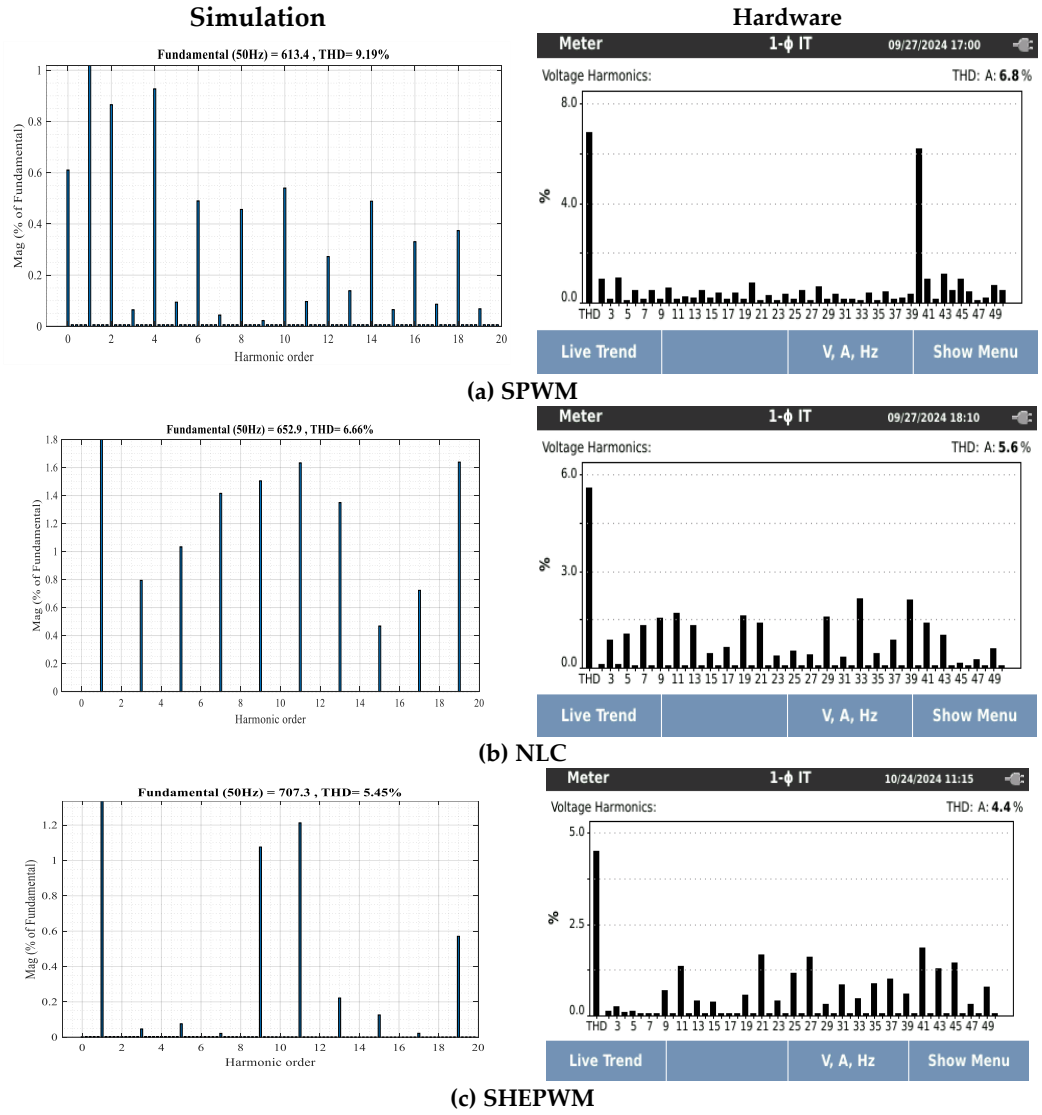

Figure 14. THD spectrum of harmonic voltage of 15-level AMLI.

Table 4. Power distribution of voltage sources as percentage of load.

Modulation Technique	MI	Power Delivered by V_1 (%) with Respect to Load	Power Delivered by V_2 (%) with Respect to Load	Power Delivered by V_3 (%) with Respect to Load
SPWM	0.90	9.18	26.87	66.75
NLC	0.95	9.92	28.27	70.04
SHEPWM	0.80	12.84	26.68	62.41

Finally, a comparison of different performance parameters of the AMLI with the considered modulation techniques is given in Table 5. Performance parameters, i.e., conduction losses, number of voltage steps, total loss, effect of frequency deviation, switching losses and THD, are calculated and compared. It is found that the output waveform remains unchanged with the change in frequency in all methods. Among different methods, the SHEPWM technique gives the AMLI its highest efficiency of 97.40% to meet the load of 4.77 kW. Also, the minimum harmonics in the load voltage with SHEPWM is found to be 5.45% (simulation) and 4.4% (hardware). The value of the load current has been estimated as 9.11 A, 9.93 A and 9.17 A for the SPWM, SHEPWM and NLC methods, respectively.

Table 5. Performance comparison of 15-level AMLI with different switching methods.

S. No.	Performance Parameters	Unit	SPWM	SHEPWM	NLC
1	Mi	-	0.9	0.8	0.95
2	Number of voltage steps achieved	-	15	15	15
3	Impact of frequency deviation on load voltage waveform	-	Unaltered	Unaltered	Unaltered
4	Conduction losses	W	98.69	116.50	109
5	Impact of frequency alternation on current waveform	-	Unaltered	Unaltered	Unaltered
6	Switching losses	W	7.70	8.63	7.85
7	Total losses	W	106.40	125.50	116.80
8	Efficiency	%	97.21	97.40	97.29
9	Power delivery at maximum efficiency	kW	3.71	4.77	4.20
10	THD in simulation	%	9.19	5.45	6.66
11	THD in hardware setup	%	6.80	4.40	5.60
12	Load current	A	9.11	9.93	9.17

7. Conclusions

An asymmetrical 15-level MLI topology with minimal switches is considered in this paper. Further, different modulation techniques are utilized to generate pulses for the power switches, i.e., SPWM, NLC and SHEPWM. All voltage steps of the AMLI with SPWM, SHEPWM and NLC are achieved at operating frequency. Performance of the AMLI with different switching methods has been analyzed and compared. It is noticed that the SHEPWM method offers the best performance of the AMLI on the basis of THD, voltage steps, efficiency, losses and power delivery at Mi = 0.8. The minimum THD of the 15-level AMLI is evaluated using the SHEPWM method as 5.45% (simulation) and 4.40% (experimental setup).

Further, SHEPWM offers the highest power delivery and voltage steps in the considered AMLI at Mi = 0.8. The efficiency of the 15-level inverter is obtained as 97.40% to supply the load power of 4.77 kW. However, the practical efficiency of the 15-level inverter in the laboratory varies from 94.50% to 96%. The obtained experimental results closely resemble the results of the system simulation. Therefore, the proposed design of an asymmetrical MLI can be recommended and incorporated in utility grids and medium-power-based electrical circuits. Hybrid modulation techniques will be explored in future work to enhance efficiency for higher-power applications. Additionally, analysis of the impact of temperature variation on efficiency and switching losses will be investigated in future work.

Author Contributions: Conceptualization, A.S. and A.C.; methodology, A.S. and A.C.; software, A.S. and A.C.; validation, A.S.; formal analysis, A.S., A.C. and A.T.; investigation, A.S.; resources, A.S.; data curation, A.T. and A.C.; writing—original draft preparation, A.S.; writing—review and editing, A.S., A.C. and A.T.; visualization, A.C. and A.T.; supervision, A.C. and A.T.; project administration, A.C. and A.T.; funding acquisition, A.S. All authors have read and agreed to the published version of the manuscript.

Funding: This research received no external funding.

Data Availability Statement: The data presented in this study are available on request from the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Catalbas, N.; Pakfiliz, A.G.; Soysal, G. Multilevel Aircraft-Inverter Design Based on Wavelet PWM for More Electric Aircraft. *Energies* **2024**, *17*, 2054. [CrossRef]
2. Ahmad, M.F.; Bin Arif, M.S.; Mustafa, U.; Abdelrahem, M.; Rodriguez, J.; Ayob, S.M. An Improved Single-Phase Multiple DC Source Inverter Topology for Distributed Energy System Applications. *Energies* **2024**, *17*, 2146. [CrossRef]
3. Nguyen, V.-T.; Kim, J.-W.; Lee, J.-W.; Park, B.-G. Optimal Design of a Submodule Capacitor in a Modular Multilevel Converter for Medium Voltage Motor Drives. *Energies* **2024**, *17*, 471. [CrossRef]
4. Srivastava, A.; Chauhan, A.; Tripathi, A. Design and performance evaluation of a novel modular asymmetrical multilevel inverter with minimal switches. *E-Prime-Adv. Electr. Eng. Electron. Energy* **2024**, *9*, 100733. [CrossRef]
5. Sharma, P.R.; K, N. A review on intelligence algorithms for THD minimization in multi-level inverter. *Int. J. Model. Simul.* **2024**, 1–17. [CrossRef]
6. Saha, S.; Saini, G.; Mishra, S.; Chauhan, A.; Upadhyay, S. A comprehensive review of techno-socio-enviro-economic parameters, storage technologies, sizing methods and control management for integrated renewable energy system. *Sustain. Energy Technol. Assess.* **2022**, *54*, 102849. [CrossRef]
7. Foti, S.; De Caro, S.D.; Scelba, G.; Scimone, T.; Testa; Cacciato, M.; Scarcella, G. An Optimal Current Control Strategy for Asymmetrical Hybrid Multi level Inverters. *IEEE Trans. Ind. Appl.* **2018**, *54*, 4425–4436. [CrossRef]
8. Sarwer, Z.; Siddique, M.D.; Iqbal, A.; Sarwar, A.; Mekhilef, S. An improved asymmetrical multilevel inverter topology with reduced semiconductor device count. *Int. Trans. Electr. Energy Syst.* **2020**, *30*, e12587. [CrossRef]
9. Thakre, K.; Mohanty, K.B.; Chatterjee, A.; Kommukuri, V.S. A modified circuit for symmetric and asymmetric multilevel inverter with reduced components count. *Int. Trans. Electr. Energy Syst.* **2019**, *29*, e12011. [CrossRef]
10. Chattopadhyay, S.K.; Chakraborty, C. Three-Phase Hybrid Cascaded Multilevel Inverter Using Topological Modules With 1:7 Ratio of Asymmetry. *IEEE J. Emerg. Sel. Top. Power Electron.* **2018**, *6*, 2302–2314. [CrossRef]
11. Karri, K.K.; Singh, V.; Pattnaik, S. Symmetrical and asymmetrical source configured multilevel inverter with reduced device count. *Electr. Eng.* **2024**, *106*, 263–277. [CrossRef]
12. Singh, A.; Bhandari, S.; Kumar, J. Suppression of Harmonics in a Novel Multilevel Inverter Using Multi-Carrier Based PWM Technique. *J. Electr. Eng. Technol.* **2024**, *19*, 5027–5043. [CrossRef]
13. Vosoughi Kurdkandi, N.; Varesi, K.; Fallah Ardashir, J.; Gao, W.; Cao, Z.; Mi, C. Transformer-Less Seven-Level Inverter with Triple Boosting Capability and Common Ground. *Energies* **2024**, *17*, 3115. [CrossRef]
14. Choudhary, A.; Singh, A.K.; Mandal, R.K.; Saha, A.K. Switched Capacitor Inverter with Reduced Inrush Current and High Boosting Gain. *Energies* **2024**, *17*, 3064. [CrossRef]
15. Bana, P.R.; Panda, K.P.; Panda, G. Power Quality Performance Evaluation of Multilevel Inverter with Reduced Switching Devices and Minimum Standing Voltage. *IEEE Trans. Ind. Inform.* **2020**, *16*, 5009–5022. [CrossRef]
16. Hussan, M.R.; Sarwar, A.; Siddique, M.D.; Iqbal, A.; Alamri, B. A Cross Connected Asymmetrical Switched-Capacitor Multilevel Inverter. *IEEE Access* **2021**, *9*, 96416–96429. [CrossRef]
17. Fahad, M.; Siddique, M.D.; Iqbal, A.; Sarwar, A.; Mekhilef, S. Implementation and Analysis of a 15-Level Inverter Topology with Reduced Switch Count. *IEEE Access* **2021**, *9*, 40623–40634. [CrossRef]
18. Srivastava, A.; Chauhan, A.; Tripathi, A. Comparative Analysis of Two-Level &; Three-Level Svpwm Based DTC IM Drives. In Proceedings of the 2021 International Conference on Artificial Intelligence and Smart Systems (ICAIS), Coimbatore, India, 25–27 March 2021; pp. 1612–1618. [CrossRef]
19. Saha, S.; Saini, G.; Chauhan, A.; Upadhyay, S.; Elavarasan, R.M.; Hossain Lipu, M.S. Optimum design and techno-socio-economic analysis of a PV/biomass based hybrid energy system for a remote hilly area using discrete grey wolf optimization algorithm. *Sustain. Energy Technol. Assess.* **2023**, *57*, 103213. [CrossRef]
20. Chouhan, J.; Gawhade, P.; Ojha, A.; Swarnkar, P. A comprehensive review of hybrid energy systems utilizing multilevel inverters with minimal switch count. *Electr. Eng.* **2024**. [CrossRef]
21. Joshi, Y.; Letha, S.S.; Bakhsh, F.I.; Jaat, G.L.; Tilak, S. Harmonic elimination of a fifteen-level inverter with reduced number of switches using genetic algorithm. *IET Power Electron.* **2023**, 1–15. [CrossRef]
22. Rathore, K.; Bansal, P. A New 15-Level Asymmetrical Multilevel Inverter Topology with Reduced Number of Devices for Different PWM Techniques. In Proceedings of the 2018 2nd IEEE International Conference on Power Electronics, Intelligent Control and Energy Systems (ICPEICES), Delhi, India, 22–24 October 2018; pp. 355–360.
23. Shankar, J.G.; Edward, J.B. A 15-level asymmetric cascaded H bridge multilevel inverter with less number of switches for photo voltaic system. In Proceedings of the 2016 International Conference on Circuit, Power and Computing Technologies (ICCPCT), Nagercoil, India, 18–19 March 2016; pp. 1–10.
24. Sarwer, Z.; Siddique, M.D.; Sarwar, A.; Mekhilef, S. An Improved 15-Level Asymmetrical Multilevel Inverter with Reduced Switch Count. In *Renewable Power for Sustainable Growth*; Iqbal, A., Malik, H., Riyaz, A., Abdellah, K., Bayhan, S., Eds.; Lecture Notes in Electrical Engineering; Springer: Singapore, 2021; p. 723.

25. Kakar, S.; Ayob, S.B.M.; Iqbal, A.; Nordin, N.M.; Arif, M.S.B.; Gore, S. New asymmetrical modular multilevel inverter topology with reduced number of switches. *IEEE Access* **2021**, *9*, 27627. [CrossRef]
26. Arif, M.S.B.; Mustafa, U.; Siddique, M.D.; Ahmad, S.; Iqbal, A.; Ashique, R.H.; Ayob, S.B. An improved asymmetrical multi-level inverter topology with boosted output voltage and reduced components count. *IET Power Electron.* **2021**, *14*, 2052–2066. [CrossRef]
27. Samadaei, E.; Sheikholeslami, A.; Gholamian, S.A.; Adabi, J. A Square T-Type (ST-Type) Module for Asymmetrical Multilevel Inverters. *IEEE Trans. Power Electron.* **2018**, *33*, 987–996. [CrossRef]
28. Alishah, R.S.; Hosseini, S.H.; Babaei, E.; Sabahi, M. A New General Multilevel Converter Topology Based on Cascaded Connection of Submultilevel Units with Reduced Switching Components, DC Sources, and Blocked Voltage by Switches. *IEEE Trans. Ind. Electron.* **2016**, *63*, 7157–7164. [CrossRef]
29. Siddique, M.D.; Mekhilef, S.; Shah, N.M.; Memon, M.A. Optimal Design of a new Cascaded Multilevel Inverter Topology with reduced switch count. *IEEE Access* **2019**, *7*, 24498–24510. [CrossRef]
30. Shalchi Alishah, R.; Sabahi, M.; Nazarpour, D.; Hosseini, S.H. Novel multilevel inverter topologies for medium and high-voltage applications with lower values of blocked voltage by switches. *IET Power Electron.* **2014**, *7*, 3062–3071. [CrossRef]
31. Odeh, C.I.; Lewicki, A.; Morawiec, M.A. Simplified SPWM Scheme for a Compact 3-Level Dual-Output Inverter. *IEEE Trans. Circuits Syst. II Express Briefs* **2024**, *71*, 4351–4355. [CrossRef]
32. Xu, L.; Zhu, Z.Q.; Yan, L. Low Switching Frequency SPWM Strategies for Open-Winding Machine with Low Current Harmonics. *IEEE Trans. Ind. Appl.* **2022**, *58*, 2042–2054. [CrossRef]
33. Sarker, R.; Datta, A.; Debnath, S. FPGA-Based High-Definition SPWM Generation with Harmonic Mitigation Property for Voltage Source Inverter Applications. *IEEE Trans. Ind. Inform.* **2021**, *17*, 1352–1362. [CrossRef]
34. Memon, M.A.; Mekhilef, S.; Mubin, M. Selective harmonic elimination in multilevel inverter using hybrid APSO algorithm. *IET Power Electron.* **2018**, *11*, 1673–1680. [CrossRef]
35. Konstantinou, G.; Pou, J.; Ceballos, S.; Darus, R.; Agelidis, V.G. Switching Frequency Analysis of Staircase-Modulated Modular Multilevel Converters and Equivalent PWM Techniques. *IEEE Trans. Power Deliv.* **2016**, *31*, 28–36. [CrossRef]
36. Kundu, S.; Burman, A.D.; Giri, S.K.; Mukherjee, S.; Banerjee, S. Comparative study between different optimisation techniques for finding precise switching angle for SHE-PWM of three-phase seven-level cascaded H-bridge inverter. *IET Power Electron.* **2018**, *11*, 600–609. [CrossRef]
37. Sadoughi, M.; Pourdadashnia, A.; Farhadi-Kangarlu, M.; Galvani, S. PSO-Optimized SHE-PWM Technique in a Cascaded H-Bridge Multilevel Inverter for Variable Output Voltage Applications. *IEEE Trans. Power Electron.* **2022**, *37*, 8065–8075. [CrossRef]
38. Wu, M.; Xue, C.; Li, Y.W.; Yang, K. A Generalized Selective Harmonic Elimination PWM Formulation with Common-Mode Voltage Reduction Ability for Multilevel Converters. *IEEE Trans. Power Electron.* **2021**, *36*, 10753–10765. [CrossRef]
39. Shanono, I.H.; Abdullah, N.R.H.; Daniyal, H.; Muhammad, A. Optimizing performance of reduced switch multi-level inverter with moth-flame algorithm and SHE-PWM. *J. Eng.* **2023**, *2023*, e12281. [CrossRef]
40. *Data Collected Electronics Components and Utilities*; Sharvi Electronics Catalogue: Bengaluru, India, 2023.
41. *Data Collected Opal-RT Real Time Digital Simulator*; Opal-RT Technologies Catalogue: Bengaluru, India, 2023.