

Article

Sub-Module Capacitor Voltage Ripple Suppression in MMDTC-Based PET Using Three-Port Active Bridge

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Abstract

For power electronic transformer (PET) based Modular Multilevel DC-Link Based T-type Converters (MMDTC) with Double Active Bridges (DABs) (namely DABs-based MMDTC-PET), the sub-module capacitor voltages exhibit relatively large ripples. To reduce the voltage ripple of sub-module capacitors, this paper proposes a novel MMDTC-PET structure that utilizes the Three-Port Active Bridges (TABs) to replace the DABs as the isolation stage (TABs-based MMDTC-PET). When the two full bridges of the TAB on the primary side adopt identical phase-shift modulation, the two sub-module capacitors within the upper and lower arms form a parallel connection. This configuration endows the sub-module capacitors with switched-capacitor characteristics, suppressing voltage ripple in the sub-module capacitors and enabling power ripple flow to the secondary side. Meanwhile, by leveraging the characteristic that the AC power components of the upper and lower arm sub-modules have equal amplitudes but opposite phases, these AC power components are mutually canceled on the secondary side of the TAB. Simulation and experimental results verify the effectiveness of the proposed scheme.

Keywords: modular multilevel DC-Link; T-type converter; power electronics transformer; three-port active bridge; switched-capacitor; capacitor voltage ripple



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1. Introduction

Power Electronic Transformers (PETs) are popular power electronic devices integrating power electronics with high-frequency transformers. Unlike traditional transformers [1–3], PETs provide not only voltage conversion and electrical isolation but also advanced regulation functions including fault isolation, power quality regulation, and voltage/current control [4,5].

PETs are categorized into single-stage, two-stage, and three-stage configurations based on conversion series. Three-stage PETs offer the most comprehensive functionality, widest adjustment range, and highest practicality [6,7]. As shown in Figure 1, the three-stage structure comprises input, isolation, and output stages. The isolation stages usually adopt double active bridge (DAB). PETs typically interface with medium- and high-voltage grids. Due to voltage withstand limitations of power devices, multilevel topologies like CHB and MMC have become standard for PET input stages [8–11]. However, CHB- and MMC-based PETs suffer from high device count and complex control requirements. This paper proposes the Modular Multilevel DC-Link Based T-type Converter (MMDTC) as

the PET input stage [12]. Like CHB-PET and MMC-PET, MMDTC sub-module capacitors generate low-frequency voltage ripples, requiring large capacitance values for suppression. Reducing sub-module capacitor voltage ripple enables lower capacitance values and lower hardware costs.

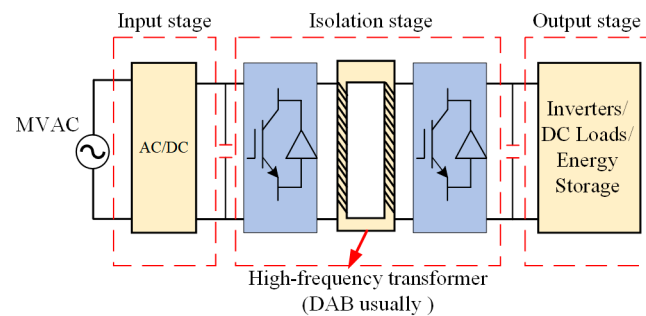


Figure 1. Schematic diagram of PET system with three stages.

Reference [13] exploits the phase relationship between arm output voltages and capacitor voltages, allowing substantial sub-module capacitor ripple to reduce capacitance requirements. However, this method is limited to reactive power compensation applications. Current capacitor voltage ripple reduction methods primarily target CHB-PET and MMC-PET systems, employing four main approaches: Additional hardware circuits, harmonic injection, control strategy optimization, and power path construction. The hardware circuit approach involves large-capacity capacitors and additional filters [14–16]. While simple and effective, it significantly increases PET volume and cost. The harmonic injection approach, widely used in CHB- and MMC-PETs [17,18], is unsuitable for MMDTC since it lacks circulating current loops and synthesizes line voltage through upper and lower arm outputs, making both circulating current and zero-sequence voltage injection inapplicable. Control strategy optimization mitigates capacitor voltage ripple through enhanced algorithms. Reference [19] introduced a three-phase AC/DC/DC converter controller that reduces capacitance by eliminating ripple. Reference [20] developed active ripple suppression techniques. Reference [21] presented phase-shift control with feedback linearization and second-order ripple feedforward based on large-signal DC/DC converter models. Reference [22] proposed output impedance-based methods using current feedforward to reduce capacitor values. However, the above control optimization methods demonstrate limited ripple suppression capability.

The power path construction method creates paths to decouple ripple power from sub-module capacitors and transfer it to the low-voltage side for cancellation, thereby reducing or eliminating voltage ripple. References [23–25] integrate CHB with single-inductor four-active-bridge configurations to establish low-frequency ripple power paths, minimizing sub-module capacitor ripple without complex control. Reference [26] employs primary synchronous switch modulation of four-port active bridges to enable switched-capacitor characteristics in three-phase MMC arms, achieving ripple power cancellation through three-phase symmetry. Reference [27] presents a three-phase integrated PET topology that reduces DC-link capacitor values by 85%. Reference [28] integrates an isolated three-port DC-DC converter with MMC, providing fundamental-frequency power paths to reduce capacitor voltage ripple. Reference [29] introduces cascaded modular isolated back-to-back PET with six-terminal active bridges, proposing switching synchronization hybrid phase-shift modulation to decouple low-frequency ripple components. Reference [30] links all sub-module capacitors to a common bus for switched-capacitor operation, substantially reducing capacitor values without additional voltage balance control. Reference [31] integrates MMC with resonant push-pull converters to create power decoupling paths among sub-modules, naturally eliminating second-harmonic circulating current and reducing

ripple voltage. While these methods theoretically enable complete ripple suppression by exploiting power ripple symmetry, most rely on mutual coupling control among three-phase sub-modules of MMC or CHB. This increases switching device driving complexity, reduces control flexibility, and is unsuitable for MMDTC with only a single DC link.

To address the inherent limitations of existing capacitor voltage ripple suppression methods for MMDTC-based PET, this paper proposes a novel approach utilizing TABs in the isolation stage. The main contributions of this work are summarized as follows:

- (1) Novel TAB-based topology for MMDTC-PET: A TAB-based MMDTC-PET structure is proposed where the two input terminals of each TAB are connected to corresponding sub-modules in the upper and lower arms, respectively. This configuration enables direct power coupling between paired sub-modules while maintaining isolation from the LVDC bus.
- (2) Switched-capacitor principle implementation: By employing identical phase-shift modulation for the two input-side full bridges of TAB, the sub-module capacitors in upper and lower arms naturally form a switched-capacitor configuration under high-frequency switching states to suppress the capacitor voltage ripple.
- (3) Inherent ripple power cancelation mechanism: The proposed scheme leverages the characteristic that AC power components in upper and lower arms have equal amplitudes but opposite phases. These components are automatically transferred through the low-impedance switched-capacitor path to the secondary side where they cancel out, achieving ripple suppression without active control intervention.

2. DAB-Based MMDTC-PET

2.1. Topology Structure

Similarly to CHB- and MMC-PETs, the input port of each DAB is individually connected to its corresponding submodule. The output port of all DABs are connected in parallel to form a low-voltage DC (LVDC) bus, as illustrated in Figure 2. The MMDTC adopts a T-type configuration comprising three phases (A, B, and C). Each phase consists of three high-voltage switching devices, which can be implemented using thyristors, IGCTs, or series-connected IGBTs [12,13]. The DC-link is formed by the series connection of the upper and lower arms. Each arm comprises N cascaded half-bridge submodules (HBSMs), with all HBSMs utilizing IGBT-based power modules.

2.2. Working Principle

The working principle of the DAB-based MMDTC-PET can be described as follows: The upper and lower arm generate non-negative multilevel voltage waveforms according to a predetermined pattern. Subsequently, the T-type structure synthesizes the desired three-phase multilevel line voltages based on this pattern. Specifically, the switching functions of each phase in the T-type structure are defined as S_x ($x = a, b, c$), where $S_x = 1, 0$, and -1 correspond to the conduction states of the upper, middle, and lower switches in phase x , respectively. Each fundamental frequency cycle is divided into six sectors (I–VI), with the operational modes of the T-type structure defined accordingly within these sectors. Based on these operational modes, the relationship between the arm output voltage and the line voltage can be derived, as illustrated in Figure 3.

Power from the high-voltage grid is delivered to the input port of each DAB through the HBSM. After conversion by the DABs, the power is subsequently transferred to the LVDC bus. It should be noted that capacitor C (Figure 2b) serves as an interface for power transfer between the HBSM and the DAB. However, due to inherent power fluctuations at the HBSM input, voltage ripple across the capacitor is unavoidable. The generation mechanism of this voltage ripple will be elaborated in the following section.

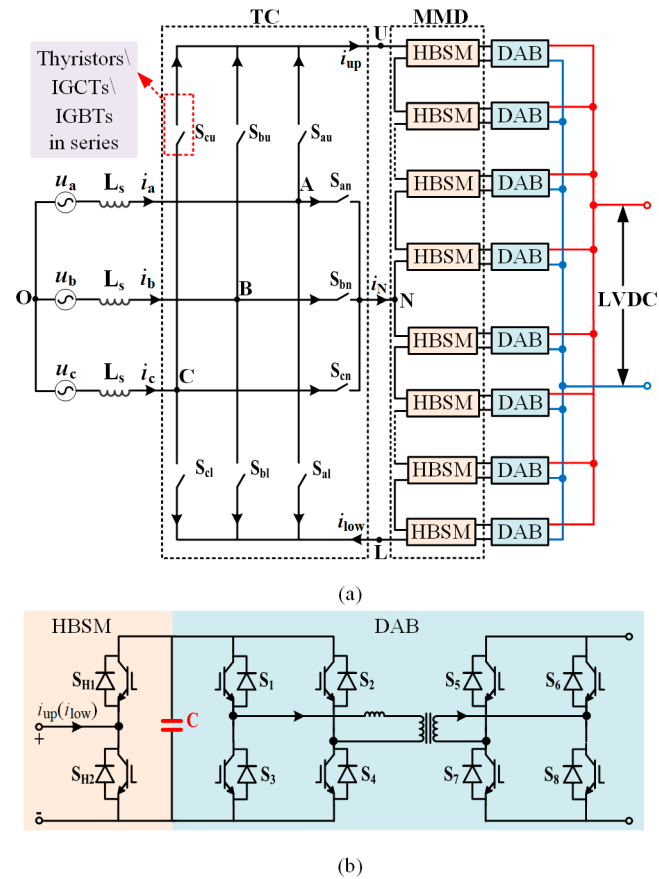


Figure 2. Schematic diagram of (a) the DAB-based MMDTC-PET and (b) the detailed configuration of the connection between the HBSM and the DAB.

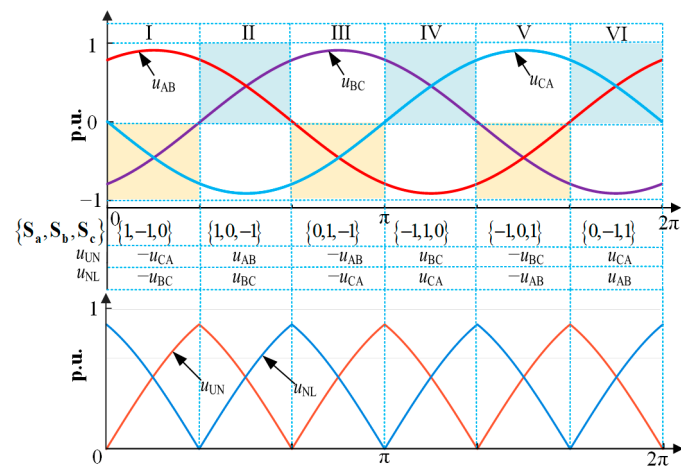


Figure 3. The relationship diagram illustrating the connections among arm voltages, three-phase line voltages, and switching states in the T-type structure.

2.3. The Generation Mechanism of Voltage Ripple Across Capacitor

The output phase-voltages of MMDTC are defined as follows:

$$\begin{cases} u_{AO} = V \sin(\omega t + \frac{\pi}{6}) \\ u_{BO} = V \sin(\omega t - \frac{\pi}{2}) \\ u_{CO} = V \sin(\omega t + \frac{5\pi}{6}) \end{cases} \quad (1)$$

where V denotes the amplitude of the output phase voltage, and $\omega = 2\pi f$. Based on Equation (1), the expression for the three-phase line voltage can be derived as follows:

$$\begin{cases} u_{AB} = \sqrt{3}V \sin(\omega t + \frac{\pi}{3}) \\ u_{BC} = \sqrt{3}V \sin(\omega t - \frac{\pi}{3}) \\ u_{CA} = -\sqrt{3}V \sin(\omega t) \end{cases} \quad (2)$$

As shown in Figure 3, the upper and lower arm voltages, u_{UN} and u_{NL} , can be derived as follows:

$$u_{UN} = \begin{cases} \sqrt{3}V \sin \theta, & \theta \in [0, \frac{\pi}{3}) \\ \sqrt{3}V \sin(\theta + \frac{\pi}{3}), & \theta \in [\frac{\pi}{3}, \frac{2\pi}{3}] \end{cases} \quad (3)$$

$$u_{NL} = \begin{cases} -\sqrt{3}V \sin(\theta - \frac{\pi}{3}), & \theta \in [0, \frac{\pi}{3}) \\ \sqrt{3}V \sin(\theta - \frac{\pi}{3}), & \theta \in [\frac{\pi}{3}, \frac{2\pi}{3}] \end{cases} \quad (4)$$

where $\theta = \omega t - \text{floor}(\omega t / (\frac{2\pi}{3}))$, and the *floor* function is represented by *floor*(x).

The three-phase output current of MMDTC is defined as follows:

$$\begin{cases} i_a = I \sin(\omega t + \frac{\pi}{6} + \varphi) \\ i_b = I \sin(\omega t - \frac{\pi}{2} + \varphi) \\ i_c = I \sin(\omega t + \frac{5\pi}{6} + \varphi) \end{cases} \quad (5)$$

where I denotes the amplitude of the output current, whereas φ signifies the power factor angle. According to the working principle of the T-type structure depicted in Figure 3, the arm current can be deduced as follows:

$$i_{up} = -I \sin(\theta + \frac{\pi}{6} + \varphi) \quad \theta \in [0, \frac{2\pi}{3}] \quad (6)$$

$$i_{low} = \begin{cases} I \sin(\theta - \frac{\pi}{2} + \varphi) & \theta \in [0, \frac{\pi}{3}) \\ I \sin(\theta + \frac{5\pi}{6} + \varphi) & \theta \in [\frac{\pi}{3}, \frac{2\pi}{3}] \end{cases} \quad (7)$$

Neglecting the power losses within the MMDTC and assuming equal power transmission through each HBSM, the power delivered to each HBSM in both the upper and lower arms can be derived from Equations (3), (4), (6) and (7).

$$p_{up} = \begin{cases} \frac{\sqrt{3}VI}{2N} [\cos(2\theta + \frac{\pi}{6} + \varphi) - \cos(\frac{\pi}{6} + \varphi)], & \theta \in [0, \frac{\pi}{3}) \\ \frac{\sqrt{3}VI}{2N} [-\sin(2\theta + \varphi) - \cos(\frac{\pi}{6} - \varphi)], & \theta \in [\frac{\pi}{3}, \frac{2\pi}{3}] \end{cases} \quad (8)$$

$$p_{low} = \begin{cases} \frac{\sqrt{3}VI}{2N} [\cos(2\theta - \frac{5\pi}{6} + \varphi) - \cos(\frac{\pi}{6} - \varphi)], & \theta \in [0, \frac{\pi}{3}) \\ -\frac{\sqrt{3}VI}{2N} [-\sin(2\theta + \varphi) + \cos(\frac{\pi}{6} + \varphi)], & \theta \in [\frac{\pi}{3}, \frac{2\pi}{3}] \end{cases} \quad (9)$$

By expanding the above equations using Fourier series analysis and neglecting higher-order harmonic terms, the power expressions for the HBSMs can be written as:

$$p_{up}(t) \approx a_0 + a_1 \cos(3\omega t) - b_1 \sin(3\omega t) \quad (10)$$

$$p_{low}(t) \approx a_0 - a_1 \cos(3\omega t) + b_1 \sin(3\omega t) \quad (11)$$

where $a_0 = -\frac{3VI}{4N} \cos(\varphi)$, $a_1 = \frac{6\sqrt{3}VI}{5\pi N} \cos(\varphi)$, $b_1 = -\frac{4\sqrt{3}VI}{5\pi N} \cos(\varphi)$.

As clearly observed from Equations (10) and (11), the power transmitted by the HBSMs consists of a DC component and a triple-frequency component. Furthermore, the

amplitudes of the triple-frequency power transmitted by the HBSMs in the upper and lower arms are identical, while their phases are opposite.

To facilitate the analysis of power flow characteristics between the HBSM and DAB, power transmission schematic diagrams of the upper and lower arm submodules are presented. As shown in Figure 4, p_{upD} and p_{lowD} denote the power flowing into the DAB from HBSM of the upper and lower arms, respectively; p_{upC} and p_{lowC} represent the power flowing into the capacitors C ; and p_L denotes the power delivered to the LVDC bus. For the DC components in p_{up} and p_{low} , the capacitive impedance approaches infinity at DC. Consequently, these DC components are entirely transferred to the DAB. In contrast, the capacitive impedance is relatively low for the AC components, allowing only a portion of the AC components to reach the DAB, while the remainder is absorbed by the capacitor. This diversion of AC components to the capacitor C_{up} (C_{low}) inevitably generates voltage ripple across it, which will be analyzed in detail in the following section.

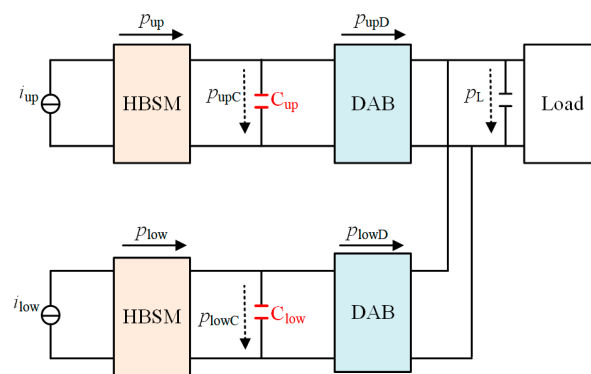


Figure 4. Schematic diagram of the power transmission mechanism of DABs in the upper and lower arm.

Assuming that the proportion of the AC component transmitted to the DAB is denoted by ξ , then p_{upD} and p_{lowD} can be mathematically expressed as follows:

$$\begin{cases} p_{upD} = \bar{p}_{up} + \xi \tilde{p}_{up} \\ p_{lowD} = \bar{p}_{low} + \xi \tilde{p}_{low} \end{cases} \quad 0 \leq \xi \leq 1 \quad (12)$$

where $\bar{p}_{up}$, $\tilde{p}_{up}$, $\bar{p}_{low}$ and $\tilde{p}_{low}$ denote the DC and AC components of p_{up} and p_{low} , respectively.

Furthermore, the AC power across capacitors C_{up} and C_{low} is obtained:

$$\begin{cases} \tilde{p}_{upC} = (1-\xi) \tilde{p}_{up} \\ \tilde{p}_{lowC} = (1-\xi) \tilde{p}_{low} \end{cases} \quad 0 \leq \xi \leq 1 \quad (13)$$

Based on the principle of instantaneous power conservation, the following relationship can be derived:

$$\tilde{p}_{upC} \approx C \bar{u}_{C-up} \frac{d\tilde{u}_{C-up}}{dt} \quad (14)$$

where $\bar{u}_{C-up}$ represents the DC component of the capacitor voltage, while $\tilde{u}_{C-up}$ corresponds to its AC component.

Furthermore, the instantaneous voltage across the capacitor in the upper arm can be expressed as derived in Equation (15). Similarly, the instantaneous voltage across the capacitor in the lower arm is given by Equation (16).

$$\tilde{u}_{C-up}(t) = U_{peak} - \frac{VI(1-\xi)(\pi-3\theta)[\cos(3\theta-\varphi) + 5\cos(3\theta+\varphi)]}{5\sqrt{3}CN\pi\bar{u}_{C-up}\omega}, \quad \theta \in [0, \frac{2\pi}{3}] \quad (15)$$

$$\tilde{u}_{C_low}(t) = U_{peak} + \frac{VI(1-\xi)(\pi-3\theta)[\cos(3\theta-\varphi) + 5\cos(3\theta+\varphi)]}{5\sqrt{3}CN\pi\tilde{u}_{C_low}\omega}, \quad \theta \in [0, \frac{2\pi}{3}] \quad (16)$$

By applying Fourier expansion to Equations (15) and (16), the corresponding frequency-domain representations can be obtained:

$$\tilde{u}_{C_up}(t) \approx c_0 - c_1 \cos(3\omega t) - d_1 \sin(3\omega t) \quad (17)$$

$$\tilde{u}_{C_low}(t) \approx c_0 + c_1 \cos(3\omega t) + d_1 \sin(3\omega t) \quad (18)$$

where

$$\begin{aligned} c_0 &= U_{peak} + \frac{24VI(1-\xi)\sin(\varphi)}{30\sqrt{3}CN\tilde{u}_{C_up}\omega} \\ c_1 &= \frac{2VI(1-\xi)\sin(\varphi)}{5\sqrt{3}CN\tilde{u}_{C_up}\omega} \\ d_1 &= -\frac{\sqrt{3}VI(1-\xi)\cos(\varphi)}{5\pi CN\tilde{u}_{C_up}\omega} \end{aligned} \quad (19)$$

As can be observed from Equations (17) and (18), a triple-frequency ripple voltage is generated across the capacitor. The magnitude of this ripple voltage is inversely proportional to the transmission ratio ξ . In other words, an increase in ξ results in a decrease in the triple-frequency ripple. Ideally, when $\xi = 1$, the triple-frequency ripple in the capacitor voltage disappears entirely.

However, the DAB operates in a high-frequency state and exhibits relatively high input inductive impedance [32], which significantly hinders the transmission of the AC component. Consequently, ξ tends to be small, indicating that the majority of the AC component from the HBSM will flow into the capacitor. To mitigate capacitor voltage fluctuations, a capacitor with a relatively large capacitance value is typically required.

Interestingly, increasing the transmission ratio ξ can reduce the capacitor voltage ripple, thereby allowing for a lower required capacitance value. To achieve this, this paper proposes using the TAB in place of the DAB. By applying the switched-capacitor principle to decrease the input inductive reactance and consequently increase the transmission ratio ξ , the capacitor voltage ripple can be effectively suppressed. The detailed analysis is presented as follows.

3. The Proposed TAB-Based MMDTC-PET

3.1. Topology Structure

The topology of the TAB-based MMDTC-PET is illustrated in Figure 5. The TAB comprises two input ports and one output port. These input ports are, respectively, connected to a sub-module in the upper and lower arms, while the output port is linked to the LVDC.

The equivalent model of the TAB is illustrated in Figure 6a. The two full-bridges at the input port of the TAB employ an identical phase-shift modulation strategy, as detailed in Figure 6b. Here, u_1 and u_2 represent the output voltages of these two full-bridge converters at the input port, respectively, while u_3 denotes the output voltage at the output port. The phase angles of the modulation signals for the two input-side full bridges are denoted by β_1 and β_2 , with $\beta_1 = \beta_2$. The phase angle of the modulation signal for the output-side full bridge is β_3 , and the phase-shift angle is defined as $\beta = \beta_3 - \beta_1$. By adjusting the magnitude of this phase-shift angle β , the power flow through the TAB can be effectively controlled.

All three full-bridge employ PWM modulation with a switching period of T_s and a duty cycle of 50%. During the first half of the switching period T_{s1} , the switching devices S_1/S_4 and S_5/S_8 are turned on. As a result, both input-side full-bridges output a positive voltage level, allowing the capacitors C_{up} and C_{low} to be directly connected in parallel. Similarly, during the second half of the switching period T_{s2} , the switching devices S_2/S_3 and S_6/S_7 are activated. Again, both input-side full bridges generate a negative

voltage level, enabling C_{up} and C_{low} to be connected in parallel as illustrated in Figure 6c,d. Under high-frequency PWM modulation, C_{up} and C_{low} together form a switched-capacitor structure, enabling continuous charging and discharging between the two capacitors.

3.2. Analysis of the Voltage Ripple Suppression Principle

Figure 7a presents a schematic diagram of the current flow path in the switched-capacitor circuit, while Figure 7b illustrates the corresponding equivalent impedance model. In these diagrams, i_{sm_up} and i_{sm_low} denote the equivalent AC current sources representing the sub-modules. Due to the very low line impedance of the two capacitors connected in parallel, their voltages constrain each other and tend to equalize.

In the TAB, no external inductor is connected to the primary side of the transformer winding. However, the transformer winding inherently exhibits leakage inductance. Taking into account the influence of the transformer's leakage impedance, L_{up} and L_{low} represent the leakage inductances of the transformers associated with the upper and lower arm sub-module.

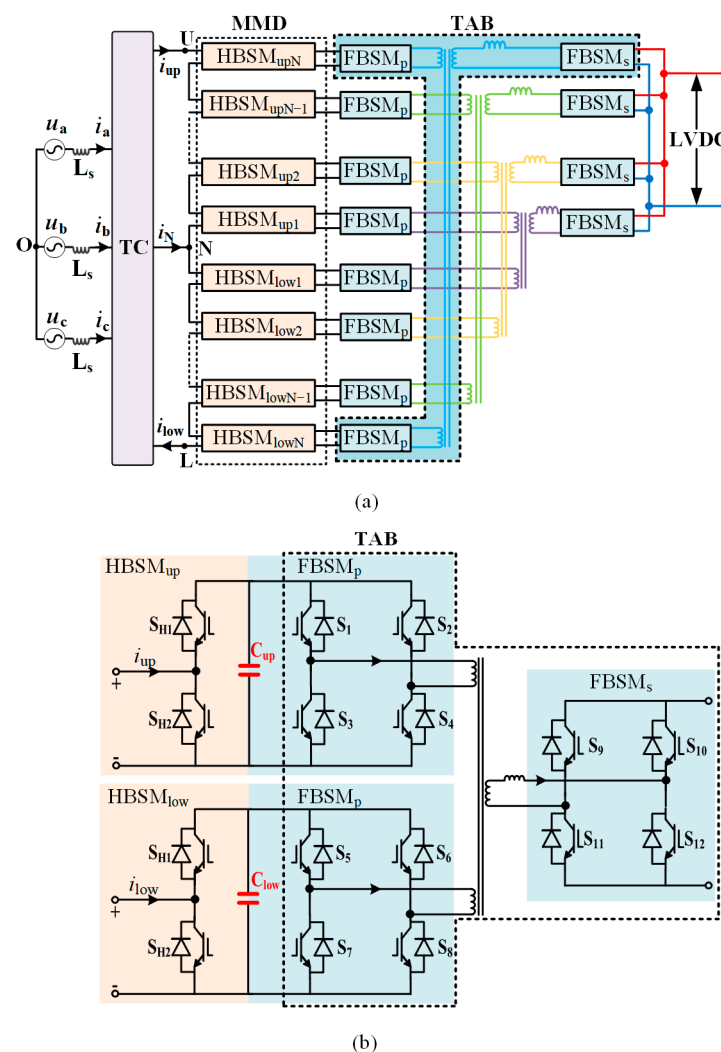


Figure 5. Schematic diagram of (a) the proposed TAB-based MMDTC-PET and (b) the detailed configuration of the connection between the HBSMs and the TAB.

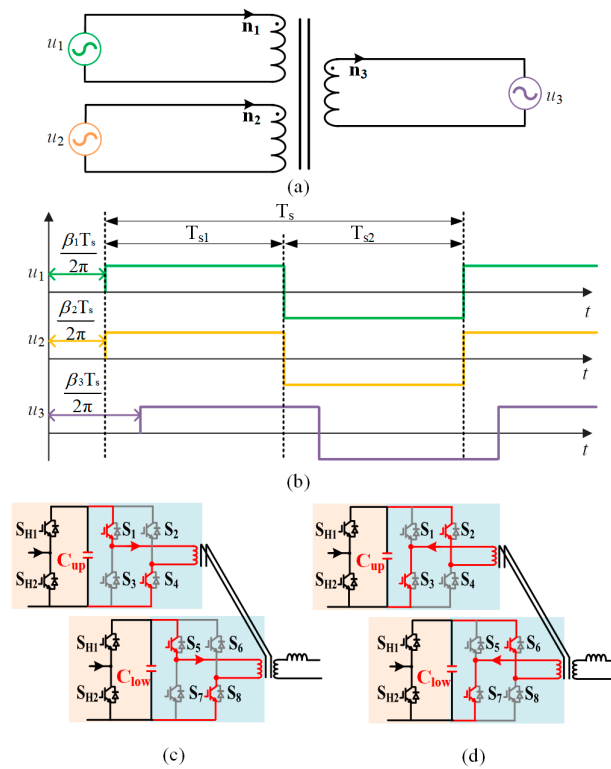


Figure 6. Schematic diagram of (a) equivalent model, (b) phase-shift modulation, (c) two capacitors connected in parallel during the first half cycle T_{s1} , and (d) two capacitors connected in parallel during the second half cycle T_{s2} using the proposed TAB scheme.

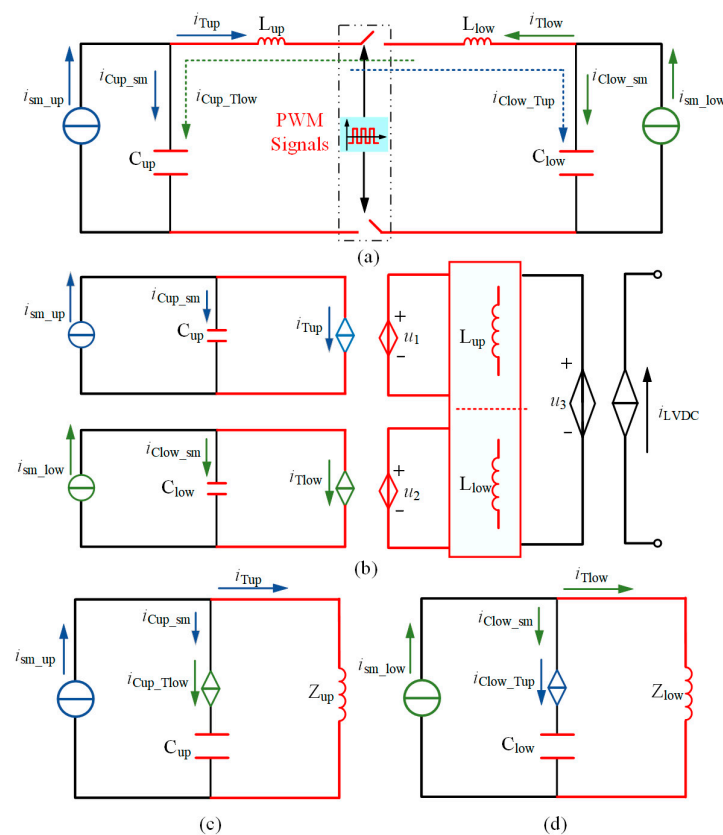


Figure 7. Schematic diagram of (a) the simplified conduction path based on the switched-capacitor circuit, (b) the equivalent impedance model based on the switched-capacitor circuit, (c) the equivalent circuit from the perspective of the first input port, and (d) the equivalent circuit from the perspective of the second input port using the proposed TAB scheme.

Define the equivalent impedances of the upper and lower arm sub-modules as Z_{up} and Z_{low} , respectively, as illustrated in Figure 7c,d. Taking the upper arm as an example, its equivalent input impedance with respect to the lower arm is:

$$Z_{up} = Z_{Clow} + Z_{Llow} + Z_{Lup} \quad (20)$$

where Z_{Clow} represents the capacitive impedance of the sub-module within the lower arm, and is expressed as $Z_{Clow} = 1/j\omega C_{low}$. Z_{Lup} , Z_{Llow} denote the inductive impedances associated with the leakage inductance, and are given by $Z_{Lup/low} = j\omega L_{up/low}$.

The ripple currents of the sub-module capacitors in the upper and lower arms, originating from the equivalent AC current source input and the primary side of the TAB, are denoted as i_{Cup/low_sm} and $i_{Tup/low}$, respectively. Taking the upper arm as an example, based on the circuit's equivalent model, the relationships among i_{sm_up} , i_{Cup_sm} , and i_{Tup} can be derived:

$$\begin{cases} i_{sm_up} = i_{Cup_sm} + i_{Tup} \\ i_{Tup} = i_{sm_up} \cdot \frac{Z_{Cup}}{Z_{Cup} + Z_{up}} \\ i_{Cup_sm} = i_{sm_up} \cdot \frac{Z_{up}}{Z_{Cup} + Z_{up}} \end{cases} \quad (21)$$

In Figure 7a, the current flowing into the upper arm from the equivalent AC current source i_{Tlow} is denoted as i_{Cup_Tlow} . According to Kirchhoff's Current Law (KCL), it can be obtained that $i_{Cup_Tlow} = i_{Tlow}$. Based on the superposition theorem and assuming that all sub-module capacitances and transformer parameters are identical, it follows that $Z_{Cup} = Z_{Clow} = 1/j\omega C$ and $Z_{Lup} = Z_{Llow} = j\omega L$, where C represents the capacitance and L denotes the leakage inductance. Under these conditions, the current i_{Cup} flowing through the capacitor can be expressed as:

$$\begin{aligned} i_{Cup} &= i_{Cup_sm} + i_{Cup_Tlow} \\ &= i_{sm_up} \cdot \frac{Z_{up}}{Z_{Cup} + Z_{up}} + i_{sm_low} \cdot \frac{Z_{Clow}}{Z_{Clow} + Z_{low}} \\ &= i_{sm_up} \cdot \frac{1}{1 - \frac{1}{\omega^2 CL}} \end{aligned} \quad (22)$$

Based on the fundamental relationship between voltage and current in a capacitor, the following expression can be derived:

$$\frac{d\tilde{u}_{C_up}}{dt} = \frac{1}{(1 - \frac{1}{\omega^2 CL})CN\bar{u}_{c_up}\omega} \left[\frac{6\sqrt{3}VI \cos(\varphi)}{5\pi} \cos(2\theta) - \frac{4\sqrt{3}VI \cos(\varphi)}{5\pi} \sin(2\theta) \right], \theta \in [0, \frac{2\pi}{3}] \quad (23)$$

Integrating the expression yields the voltage across the capacitor:

$$\tilde{u}_{C_up} = U_{peak} + \frac{LVI\omega(\pi - 3\theta)[\cos(3\theta - \varphi) + 5\cos(3\theta + \varphi)]}{5\sqrt{3}N\pi\bar{u}_{c_up}(1 - CL\omega^2)}, \theta \in [0, \frac{2\pi}{3}] \quad (24)$$

when $\theta = 0$, the valley value U_{valley} is achieved. Let $\Delta\tilde{u}_{C_up} = U_{peak} - U_{valley}$, that is:

$$\begin{aligned} \Delta\tilde{u}_{C_up} &= U_{peak} - U_{valley} \\ &= \frac{2\sqrt{3}VI\omega \cos(\varphi)}{5N\bar{u}_{c_up}(\frac{1}{L} - C\omega^2)} \end{aligned} \quad (25)$$

As can be seen from Equations (22) and (25), the presence of leakage inductance L prevents the ripple current from being completely decoupled from the sub-module capacitor. However, by minimizing the leakage inductance during the design phase, its impact can be significantly reduced. Therefore, the leakage inductance L of the high-frequency transformer in the TAB is designed to be as small as possible, enabling i_{cup} to approach zero. This indicates that by utilizing the low-impedance characteristic of

the switched-capacitor circuit's equivalent connection, the fluctuating current i_{sm_up} is effectively decoupled from the sub-module capacitor and redirected to the secondary side of the high-frequency transformer at the TAB level, without requiring additional control for ripple power transfer.

Therefore, the ripple power transmission process can be equivalently described as follows: The AC components $i_{sm_up/low}$ are transferred to the secondary side of the high-frequency transformer through the low-impedance path formed in the switched-capacitor circuit. Due to the characteristic that the amplitudes of the low-frequency ripple power in the upper and lower arms are equal while their phases are opposite, the ripple current that would otherwise flow into the sub-module capacitor cancels out on the common low-voltage DC bus, thereby eliminating its impact on the sub-module capacitor. As a result, only DC power flows into the LVDC bus, and the capacitor voltages of the sub-modules in both the upper and lower arms are mutually clamped, exhibiting only minor voltage ripples.

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4. Simulation and Experimental Validation

4.1. Simulation Results

To verify the effectiveness of the proposed TAB in mitigating low-frequency voltage ripple across the capacitor, simulation models for both the DAB-MMDTC-PET and TAB-MMDTC-PET systems were developed using Simulink. The detailed simulation parameters are provided in Table 1.

Table 1. The main parameters of simulation.

Variable	Symbol	Value
Rated grid phase voltage	V_g	10 kV
AC filtering inductor	L_s	2 mH
Rated active power	P_{rated}	1 MW
Fundamental frequency	f	50 Hz
Number of SMs per arm	N	20
Voltage of submodule capacitor	u_c	750 V
Submodule capacitor	C	0.5 mF
Carrier frequency	f_c	10 kHz
LVDC bus voltage	u_{LVDC}	750 V
DAB Transformer Turn Ratio	$n_1:n_2$	1:1
TAB Transformer Turn Ratio	$n_1:n_2:n_3$	1:1:1
DAB additional inductor	L	25 μ H
TAB additional inductor	L	25 μ H
Switching frequency	f_s	40 kHz

Figure 8a–d present comparative simulation results for both the conventional DAB scheme and the proposed TAB scheme, illustrating output line voltages, output currents, arm voltages, and arm currents. The results demonstrate that the fundamental opera-

tional characteristics of the MMDTC remain consistent regardless of the isolation stage configuration employed.

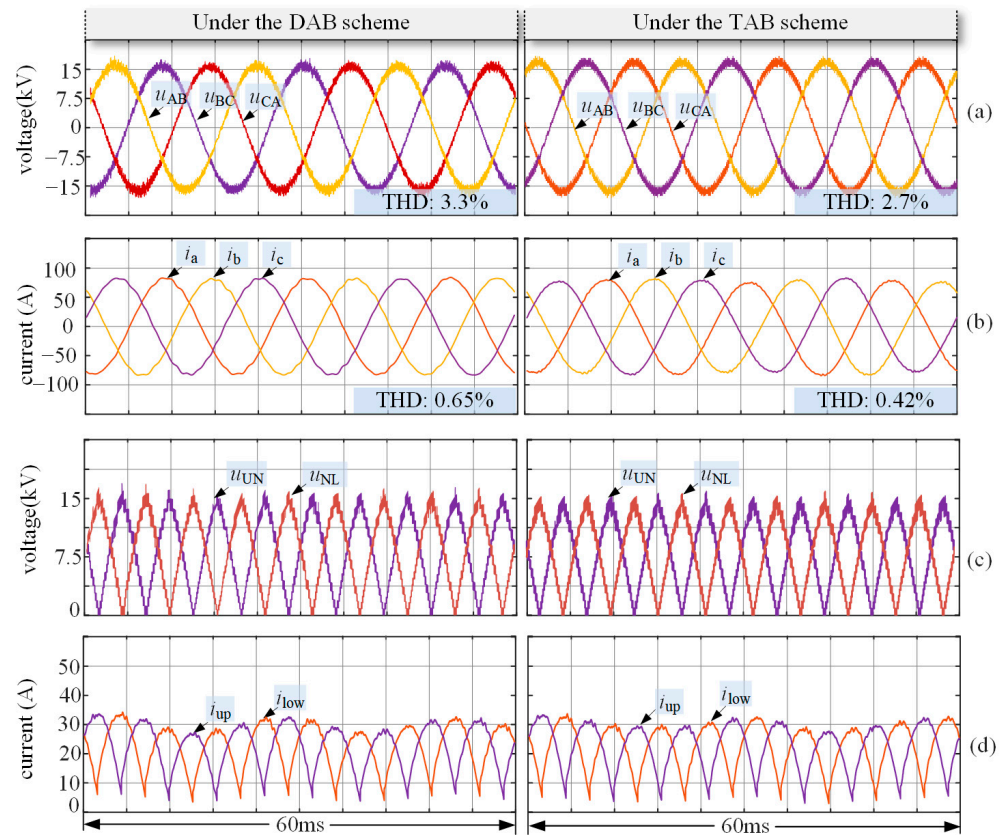


Figure 8. Simulation results of (a) output line voltages, (b) output currents, (c) arm voltages, and (d) arm currents under the DAB scheme and proposed TAB scheme, respectively.

For the conventional DAB scheme, Figure 9 displays current waveforms and corresponding FFT analyses at three critical measurement points: The HBSM output, the sub-module capacitor input, and the DAB input. As shown in Figure 9a, the HBSM output current comprises a DC component of 34 A and a triple-frequency component of 36 A. Figure 9b,c reveals that the triple-frequency AC component predominantly flows into the sub-module capacitor, while the DC component is primarily transferred to the DAB input. These observations validate the theoretical analysis presented in Section 2.3.

For the proposed TAB scheme, Figure 10 presents current waveforms and FFT analyses at the corresponding measurement points. Comparing Figures 9a and 10a, the DC and triple-frequency AC components at the HBSM output remain virtually identical. However, a dramatic reduction in the triple-frequency AC component is observed in the sub-module capacitor current when comparing Figures 9b and 10b. This significant improvement results from the effective redirection of the triple-frequency AC component to the TAB, as evidenced in Figure 10c, demonstrating the successful implementation of the ripple power decoupling mechanism.

Figure 11 compares the capacitor voltages of all sub-modules in both upper and lower arms under the conventional DAB scheme and the proposed TAB scheme. The comparison clearly demonstrates that the sub-module capacitor voltage ripple ratio is dramatically reduced from 24% to 2.5% under identical operating conditions, validating the superior ripple suppression capability of the proposed TAB scheme.

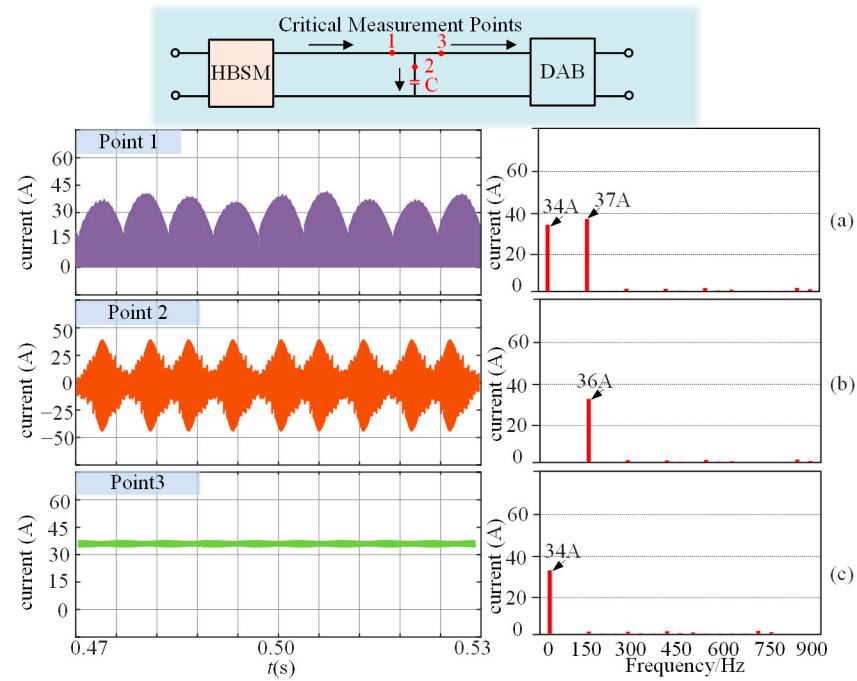


Figure 9. Current and its FFT analysis at (a) the output port of HBSM, (b) the input port of submodule capacitor, and (c) the input port of DAB. The arrow indicate the direction of current flow, and the numbers represent the sequence numbers of the measurement points.

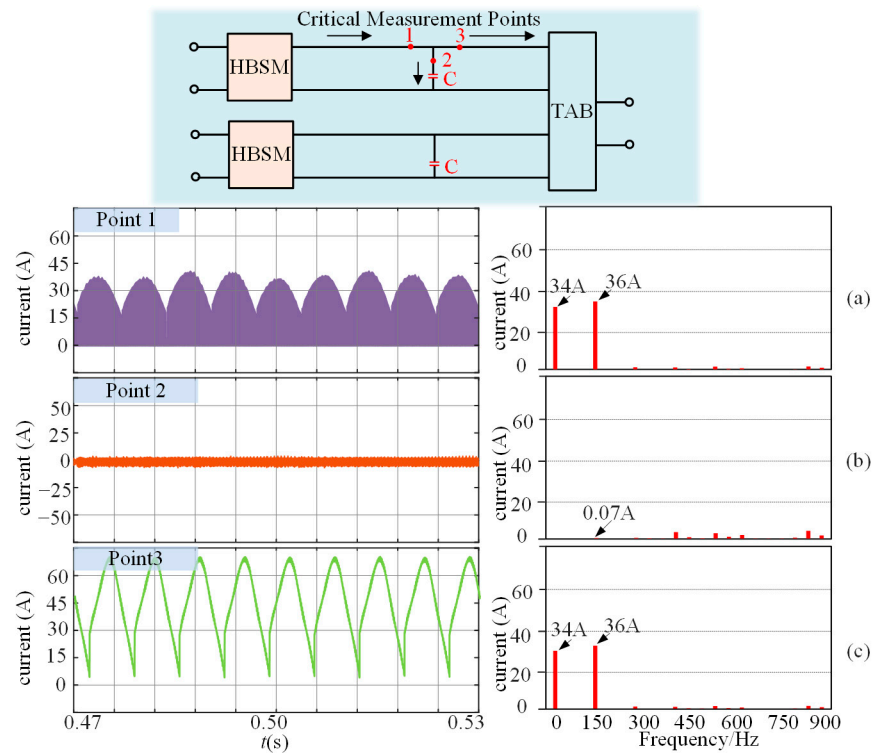


Figure 10. Current and its FFT analysis at (a) the output port of HBSM, (b) the input port of submodule capacitor, and (c) the corresponding input port of TAB.

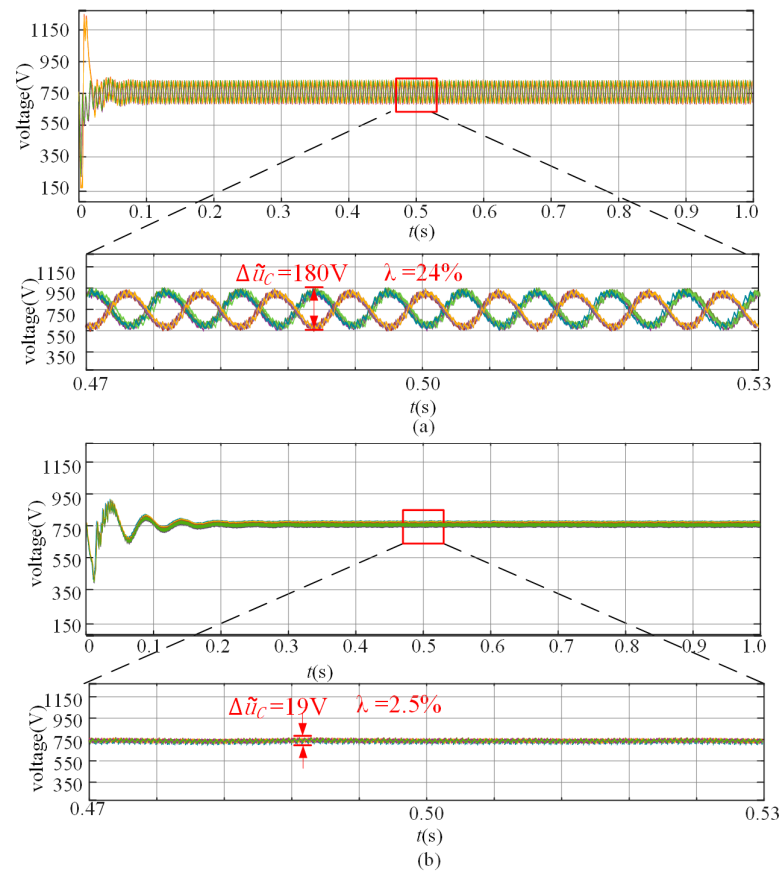


Figure 11. Comparison of all submodule capacitor voltages using (a) the DAB scheme and (b) the proposed TAB scheme, respectively.

Figure 12a–c illustrates the input and output port currents of the TAB along with their corresponding FFT analyses. The results reveal prominent triple-frequency components in both input ports with opposite phase relationships. Notably, the output port exhibits negligible triple-frequency content, confirming that the equal-amplitude, opposite-phase triple-frequency components from the two input ports effectively cancel at the output. This phenomenon validates the natural ripple cancellation mechanism inherent in the proposed topology.

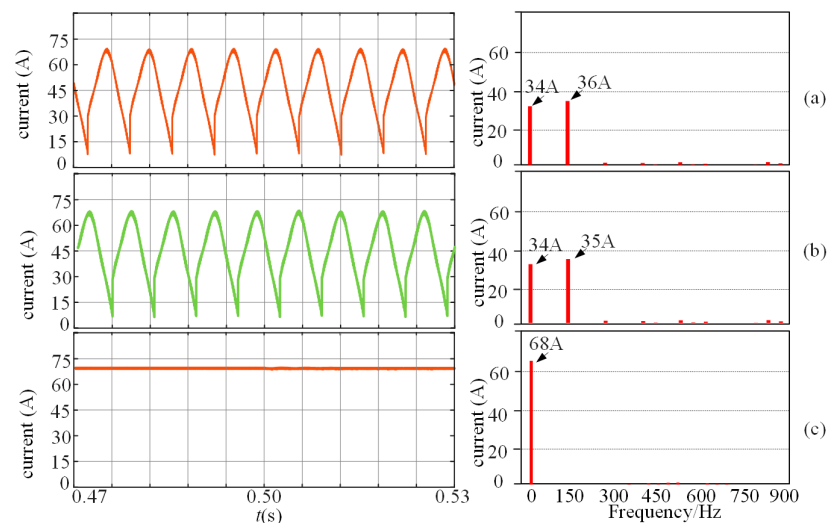


Figure 12. Current and its FFT analysis at (a) the input port of the TAB in the upper arm, (b) the input port of the TAB in the lower arm, and (c) the output port of the TAB.

Figure 13 presents the system's dynamic response under sudden load variations on the LVDC side. The results include three-phase grid-connected currents (Figure 13a), LVDC bus voltage and current (Figure 13b,c), and sub-module capacitor voltages (Figure 13d). The waveforms demonstrate rapid convergence to steady-state following the load disturbance, confirming the system's robust dynamic performance and stability under transient conditions.

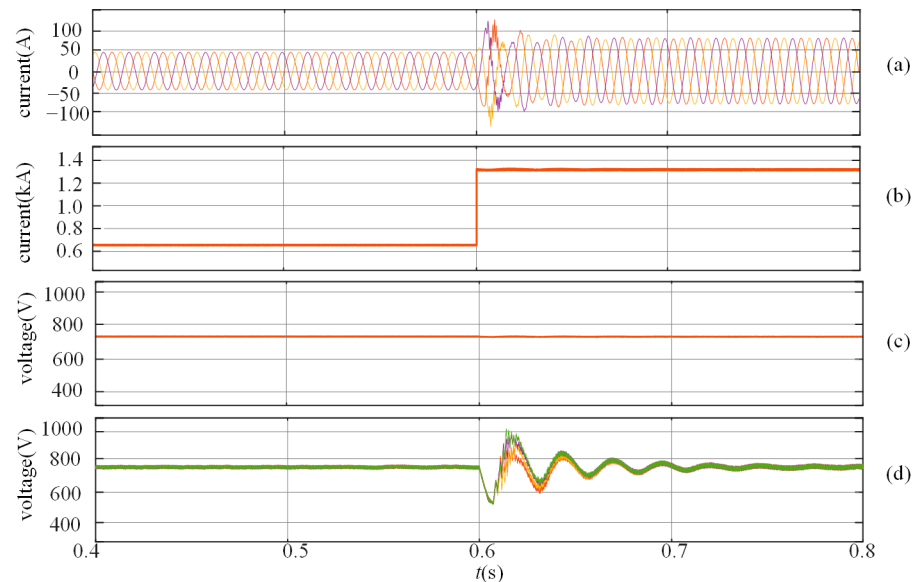


Figure 13. Simulation results showing (a) three-phase output current, (b) LVDC bus current, (c) LVDC bus voltage, and (d) all SM capacitor voltage waveforms under a sudden load change on the LVDC side.

For a more intuitive comparison, this paper compares the hardware costs of using two DABs versus one TAB structure. Both topologies primarily consist of capacitors, IGBT devices, and high-frequency transformers.

In terms of capacitor cost, the submodule capacitor selection refers to Table 2(a), with the specific model being ALF80(1)122FP500 manufactured by KEMET. Assuming a capacitor voltage fluctuation ratio λ of 2.5%, the required capacitance values for the DAB and TAB schemes were calculated, with the results presented in Table 2(b). The selected capacitors have a rated voltage of 500 V and a nominal capacitance of 1.2 mF. In practical applications, series-parallel combinations are required to achieve the desired capacitance value. Compared to the DAB-based solution, the TAB structure reduces capacitor costs by approximately 87.5%, from \$317.44 to \$39.68.

Regarding switching device costs, the selected IGBT models are Infineon's APTGL90H-120T3G and FF50R12RT4HOSA1, with detailed parameters provided in Table 2(c). As shown in Table 2(d), since the current flowing through the secondary-side switching devices in the TAB topology is twice that of the primary side, secondary-side devices with double the rated current must be used. Ultimately, the total cost of switching devices is reduced by approximately 3%, from \$971.2 to \$936.8.

In terms of high-frequency transformers, the conventional DAB approach requires two independent transformers along with their associated magnetic components and control circuits. In contrast, the proposed TAB method uses only one three-winding transformer, effectively reducing the number of magnetic components while maintaining equivalent functionality.

Table 2. (a). Technical parameters list of capacitor. (b). Comparison results in terms of capacitor costs. (c). Technical parameters list of IGBTs. (d). Comparison results in terms of IGBT costs.

(a)				
Model	Capacitance	Cost Per	Normal Voltage	
ALF80(1)122FP500	1.2 mF	\$19.84	500 V	
(b)				
Type	Double DABs		Single TAB	
Capacitance required	4.8 mF		0.5 mF	
Total Number of capacitors	18 (Two in series and nine in parallel)		2 (Two in series)	
Total cost	\$317.44		\$39.68	
(c)				
Model	Normal Voltage	Cost Per	Rated Current	Switching Frequency
APTGL90H120T3G (IGBT)	1200 V	\$112.8	110 A	20–50 kHz
FF50R12RT4HOSA1(IGBT)	1200 V	\$60.7	50 A	20–50 kHz
(d)				
Type	Double DABs		Single TAB	
Total Number of IGBTs	16(FF50R12RT4HOSA1)		8(FF50R12RT4HOSA1) + 4(APTGL90H120T3G)	
Total cost	\$971.2		\$936.8	

4.2. Experimental Results

Due to the limitations of the power electronics experimental setup in our laboratory, constructing a complete TAB-based MMDTC-PET circuit is highly challenging. Consequently, a simplified experimental approach was adopted, as illustrated in Figure 14. Two DC-DC converters are utilized to emulate the triple-frequency power output of the upper and lower arm submodules in the MMDTC. Specifically, the PWM signals for the DC-DC converters are generated by comparing a modulation wave containing triple-frequency components with a triangular carrier wave. Furthermore, the amplitudes of these triple-frequency components are identical in both modulated waves, but their phases are opposite. The prototype of the experimental platform is illustrated in Figure 15, where RT-LAB serves as the controller and the detailed experimental parameters are summarized in Table 3.

Table 3. The main experimental parameters.

Variable	Symbol	Value
Rated active power	P_{rated}	500 W
Input voltage of DC-source	U_1	105 V
Output voltage of TAB	U_2	100 V
Load	R	20 Ω
PWM carrier frequency	f_c	10 kHz
Switching frequency	f_s	10 kHz
Submodule capacitor	C	470 μ F
TAB additional inductor	L	167 μ H

Figure 16 presents the current waveforms at the three critical measurement points—1', 2', and 3'—as shown in Figure 14, along with their corresponding FFT analyses. The current at each measurement point represents the DC-DC converter output current, the capacitor input current, and the TAB input current, respectively. The FFT results demonstrate that

the majority of triple-frequency components present in the DC-DC output current are directed toward the TAB, whereas the capacitor input current consists only of higher-order harmonics. Figure 17 illustrates the current waveforms at measurement points 2', 4', and 5'. The currents at points 2' and 4' correspond to the TAB input current, while the current at point 5' represents the TAB output current. As shown in Figure 17, the input current to the TAB contains triple-frequency components with opposite phase relationships, whereas the output current is free from such triple-frequency fluctuations.

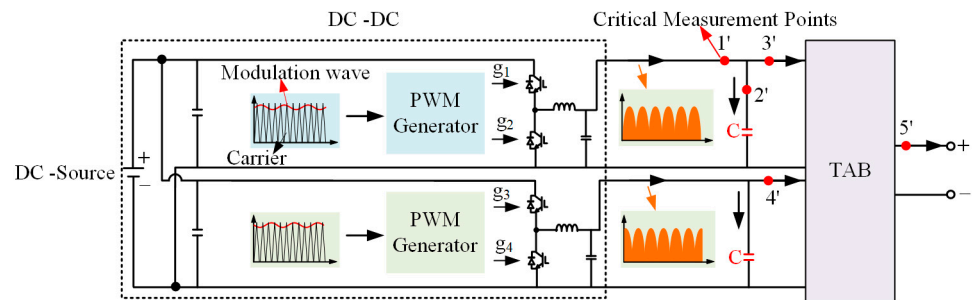


Figure 14. Structural Composition of the Experimental Platform.

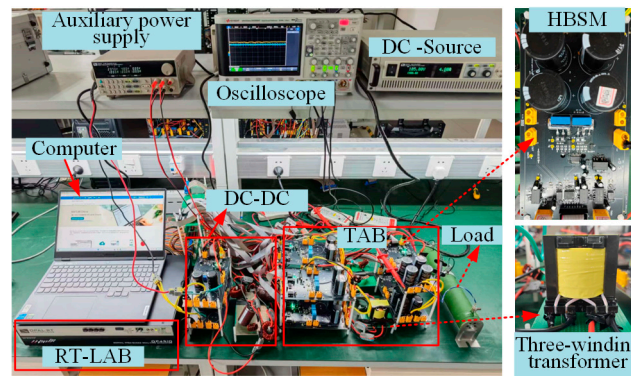


Figure 15. Photographs of the experimental prototype.

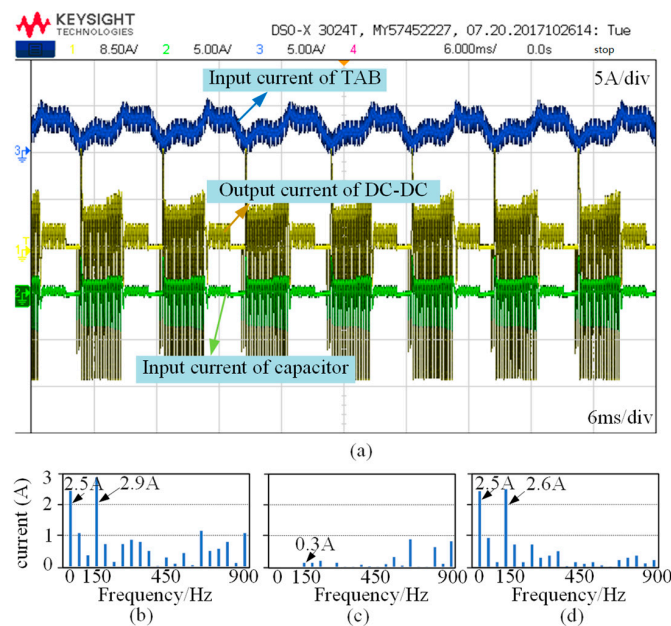


Figure 16. Experimental results of (a) the current waveforms observed at the measurement points 1', 2', and 3', (b) FFT analysis of output current of DC-DC, (c) FFT analysis of input current of capacitor, and (d) FFT analysis of input current of TAB.

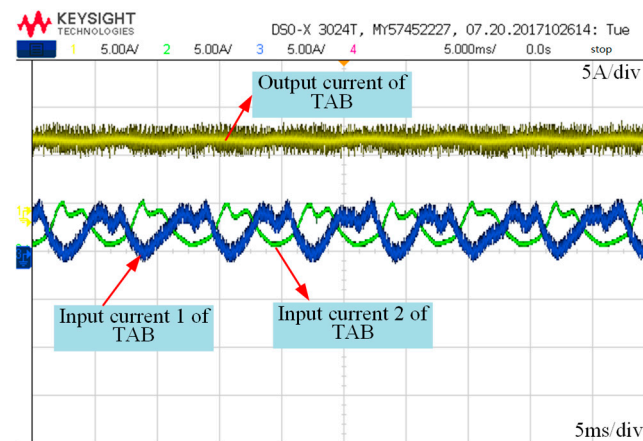


Figure 17. Experimental results of input current and output current of TAB.

Figure 18 presents the output voltage waveforms of the DC-DC converter and the TAB output voltage. As shown, the output voltages of the two DC-DC converters exhibit triple-frequency ripple that are phase-opposed. The amplitude of the ripple voltage is 10 V, whereas the TAB output voltage remains consistently stable at 100 V. This indicates that, under the same phase modulation of the two full bridges on the primary side, the triple-frequency ripple component in the input current automatically cancels out on the output side due to the opposite phase characteristics of the triple-frequency components. Only the DC component is transferred to the output side of the TAB, which verifies the effectiveness of the TAB's cancelation scheme for triple-frequency ripple.

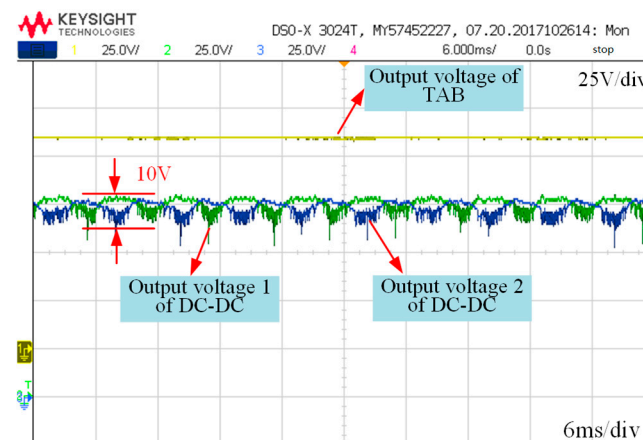


Figure 18. Experimental results of the output voltage of DC-DC converter and the output voltage of TAB.

5. Conclusions

This paper proposes a novel TAB-based MMDTC-PET topology to effectively suppress sub-module capacitor voltage ripple. By replacing conventional DABs with TABs and employing identical phase-shift modulation for the two primary-side full bridges, the proposed scheme creates a switched-capacitor configuration that provides a low-impedance path for ripple power. The theoretical analysis reveals that this configuration enables the redirection of triple-frequency AC components away from sub-module capacitors to the TAB secondary side, where they naturally cancel due to their equal-amplitude, opposite-phase characteristics in upper and lower arms. Simulation results demonstrate that the proposed method reduces capacitor voltage ripple from 24% to 2.5%.

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