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Design and Implementation of a Full SiC-Based Phase-Shifted Full-Bridge DC-DC Converter with Nanocrystalline-Cored Magnetics for Railway Battery Charging Applications

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Abstract

This paper presents the design and implementation of a high-efficiency, full silicon carbide (SiC)-based center-tapped phase-shifted full-bridge (PSFB) converter for NiCd battery charging applications in railway systems. The converter utilizes SiC MOSFET modules on the primary side and SiC diodes on the secondary side, resulting in significant efficiency improvements due to the superior switching characteristics and high-temperature tolerance inherent in SiC devices. A nanocrystalline-cored center-tapped transformer is optimized to minimize voltage stress on the rectifier diodes. Additionally, the use of a nanocrystalline core provides high saturation flux density, low core loss, and excellent permeability, particularly at high frequencies, which significantly enhances system efficiency. The converter also compensates for temperature fluctuations during operation, enabling a wide and adjustable output voltage range according to the temperature differences. A prototype of the 10-kW, 50-kHz PSFB converter, operating with an input voltage range of 700–750 V and output voltage of 77–138 V, was developed and tested both through simulations and experimentally. The converter achieved a maximum efficiency of 97% and demonstrated a high power density of 2.23 kW/L, thereby validating the effectiveness of the proposed design for railway battery charging applications.

Keywords: phase-shifted full-bridge; DC-DC converter; full SiC-based; integrated magnetics; nanocrystalline core; battery charging

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1. Introduction

The increasing electrification of railway systems has significantly elevated the demand for advanced and efficient power electronics, particularly in battery charging systems. Nickel–cadmium (NiCd) batteries are widely utilized in railway applications due to their long cycle life, resilience to extreme temperatures, and ability to handle high charging and discharging currents. Despite the growing adoption of lithium-ion chemistry, NiCd batteries remain prevalent in railway systems due to their proven reliability, robustness against temperature extremes, and regulatory compliance in certain regions [1]. However, ensuring their safe and efficient operation requires advanced charging solutions that provide precise temperature-compensated voltage adjustments to maintain safety and performance [2]. To achieve this, an efficient isolated DC-DC converter is essential, providing galvanic isolation between the high-voltage input and low-voltage battery circuits. This isolation

not only ensures compliance with stringent railway safety standards but also mitigates risks such as electrical faults, ground loops, and electromagnetic interference (EMI) [3]. Furthermore, the converter must deliver high efficiency and reliability over wide input and output voltage variations, addressing the unique electromagnetic and thermal challenges specific to railway environments [4].

A variety of isolated DC-DC converter topologies have been developed to meet these requirements [5,6]. Isolated boost converters are commonly used for their ability to handle input voltage variations; however, they suffer from reduced efficiency and increased control complexity when faced with the wide voltage fluctuations characteristic of railway systems [7–9]. Similarly, LLC resonant converters, while highly efficient in specific operational ranges, experience reduced performance and control challenges when subjected to broad input and output voltage ranges [10]. Dual active bridge (DAB) converters, another alternative, are effective in bidirectional applications. However, in unidirectional configurations such as battery charging, DAB topologies often involve unnecessarily complex control schemes and increased switching losses, which reduce overall efficiency [11,12].

Among the various soft-switching topologies, the phase-shifted full-bridge (PSFB) converter stands out for its ability to achieve high efficiency and robust performance across wide input and output voltage ranges [13]. A critical aspect of the PSFB converter is its inherent zero-voltage switching (ZVS) capability, which minimizes switching losses and electromagnetic interference (EMI), thereby enhancing both efficiency and thermal performance [14,15]. PSFB converters are particularly advantageous for railway systems due to their relatively simple control mechanism and robust behavior under fluctuating input voltages and temperature-dependent charging profiles for NiCd batteries [16]. In this context, the adoption of silicon carbide (SiC) MOSFETs and diodes further enhances switching performance and thermal robustness, making PSFB converters even more suitable for the harsh operating conditions encountered in railway environments [17]. A key design challenge, however, is ensuring ZVS across a wide load range, which typically requires the addition of external inductance to store the energy necessary for soft switching. In many studies, ZVS is achieved by placing an external inductor in series with the transformer's primary winding [18]. While effective, this method introduces drawbacks such as increased system size and weight, higher conduction losses, and the need for separate thermal management—all of which negatively affect power density, a critical factor in space-constrained applications.

To overcome these limitations, researchers have explored integrating the required inductance directly into the transformer structure [19–22], most commonly using ferrite cores [23]. Ferrite core-based integrated transformers offer a cost-effective solution with acceptable magnetic performance; however, their high core losses at elevated frequencies (e.g., 50 kHz) and limited saturation flux density restrict their efficiency and power-handling capability in high-power applications. To address these limitations, hybrid transformer designs combining nanocrystalline and ferrite cores have been proposed [24]. These aim to leverage the high saturation flux density, low core losses, and excellent thermal stability of nanocrystalline materials, while preserving the structural simplicity and economic advantages of ferrite cores. Nevertheless, the inclusion of ferrite still constrains performance due to its inherent core losses and reduced thermal capability.

Recently, integrated transformers utilizing shell-type nanocrystalline cores have been investigated in high-frequency converter applications [25]. These designs offer improved compactness and frequency performance thanks to the superior magnetic properties of nanocrystalline materials. However, compared to core-type configurations, shell-type cores often suffer from increased leakage flux due to their structural layout, leading to higher stray losses and reduced efficiency. Additionally, their geometry limits effective heat dissipation,

compromising thermal performance in high-power systems. Limited flexibility in winding arrangements and increased manufacturing complexity further hinder their applicability. These drawbacks highlight the need for improved integrated transformer designs that can meet the demanding requirements of modern PSFB converters in railway applications.

As a result of these considerations, a center-tapped configuration with a core-type nanocrystalline integrated transformer was designed and optimized through finite element analysis (FEA) to address the limitations of conventional transformer approaches. This transformer was implemented into an isolated PSFB DC-DC converter, resulting in a compact, high-efficiency, and high-power-density solution for charging NiCd batteries in railway vehicles. Leveraging the superior magnetic characteristics of nanocrystalline cores, the proposed design enhanced power density and thermal stability while minimizing system volume and losses. To suppress oscillations caused by the interaction between transformer leakage inductance and output rectifier parasitic capacitances, an RCD snubber network was employed. The converter utilizes SiC MOSFETs on the primary side and SiC diodes on the secondary side to exploit the high-speed switching capability and thermal robustness of wide-bandgap semiconductors. Additionally, a temperature-compensated charging voltage curve was implemented to ensure safe and efficient battery operation under varying ambient conditions. Operating at a switching frequency of 50 kHz, the converter achieved a peak efficiency of 97% and demonstrated high power density. A 10 kW hardware prototype was developed and experimentally validated through long-term testing. This work demonstrates a significant improvement in power density, efficiency, and reliability, offering an optimized solution for isolated PSFB converters in railway battery charging applications.

2. Operation Principles of Center-Tapped Phase-Shifted Full-Bridge Converter

Figure 1 illustrates the center-tapped phase-shifted full-bridge (PSFB) DC-DC converter. The designed converter operates at a power level of 10 kW and a switching frequency of 50 kHz. To minimize switching losses on the primary side, 1200 V SiC MOSFETs are used as the main switching devices. In this topology, the full-bridge MOSFETs are driven with a fixed 50% duty cycle, while the output voltage is regulated by adjusting the phase shift between the diagonal switches on the left and right sides. A blocking capacitor is connected in series with the primary windings to prevent transformer saturation under flux imbalance conditions. To achieve ZVS across a wide load range, leakage inductance is necessary to reduce activation losses in MOSFETs to nearly zero. This leakage inductance has been integrated into the center-tapped nanocrystalline-cored transformer. The nanocrystalline material provides the advantage of reduced core losses, enhancing the overall efficiency and thermal performance of the converter. On the secondary side, 1200 V SiC diodes are employed in the rectifier stage. The SiC diodes provide zero reverse recovery and low reverse recovery charge characteristics, which are crucial for minimizing oscillations and overshoot. Despite these measures, parasitic oscillations still occur due to the resonance between the leakage inductance of the transformer and the output capacitance of the diodes. To mitigate this effect, an RCD snubber circuit is employed. The RCD snubber effectively dampens the resonance, minimizing oscillations and reducing the voltage stress on the diodes, which contributes to improved stability and reliability of the converter. The selection of the RCD snubber components is based on both energy absorption and damping requirements. The snubber capacitor was sized to absorb the energy stored in the transformer leakage inductance during each switching transition, calculated as one-half of the product of the leakage inductance and the square of the peak current at turn-off. This limits the voltage overshoot across the output rectifier diodes to within a safe margin.

The snubber resistor was selected to provide adequate damping for the resonant circuit formed by the leakage inductance and the snubber capacitance, with its value estimated using the square root of the inductance-capacitance ratio. In addition, the diode used in the snubber path was carefully chosen to withstand the reverse voltage stress and fast switching transients without introducing significant recovery losses. A fast-recovery or Schottky-type diode with sufficient reverse voltage rating and low junction capacitance was selected to ensure reliable operation of the snubber circuit under repetitive high-frequency switching conditions. Together, these components form an effective damping network that suppresses parasitic oscillations and protects the output stage from excessive voltage stress. A fast reverse-recovery silicon Schottky ORing diode is implemented to decouple the battery from the DC bus. This ORing diode prevents uncontrolled cross-charging or discharging between batteries. By eliminating reverse current paths, this component enhances system reliability and reduces energy losses, ensuring efficient power management in the converter.

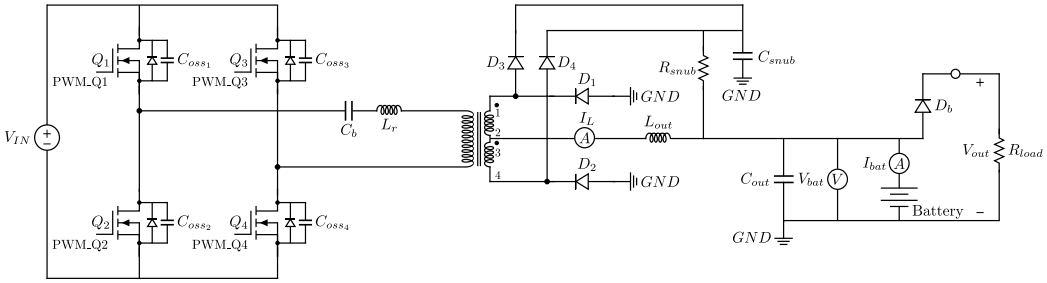


Figure 1. Center-tapped phase-shifted full-bridge converter.

At the converter's output, two current probes are used to measure the inductor current and battery current, while a voltage probe is employed to monitor the battery voltage. The system consists of voltage and current controllers. The outer voltage controller compares the measured battery voltage with the temperature-compensated reference voltage and sends the resulting error to a proportional-integral (PI) controller, which generates the reference current value at its output. The control system, including the voltage and current controllers, is illustrated in Figure 2.

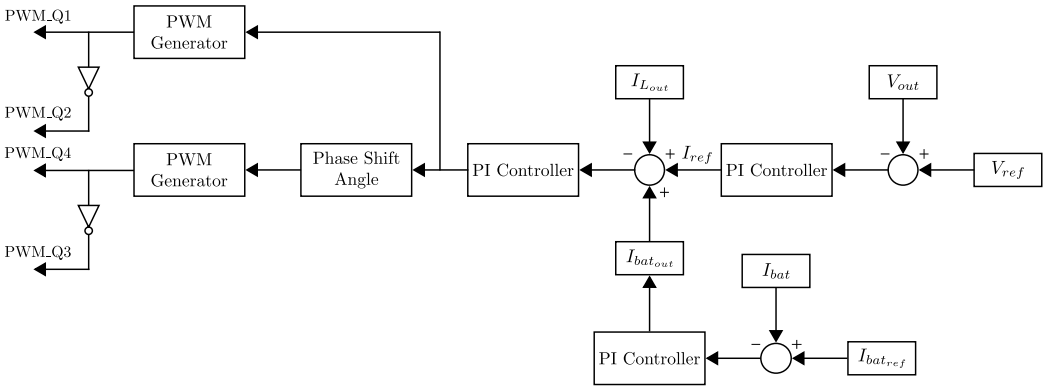


Figure 2. Center-tapped phase-shifted full-bridge converter controller block diagram.

As illustrated in Figures 1 and 2, the output of the battery charging unit is connected to both the DC loads and the battery. In conventional charger topologies utilizing basic output control strategies, the system primarily supplies power to the DC loads, with the remaining current directed to the battery. However, to preserve battery longevity, a maximum charging current threshold is specified for each battery type, necessitating closed-loop control. To address this, a battery-associated PI controller is employed, which

compares the measured battery current with the reference current generated by the main processor. This enables precise regulation of the charging current and ensures compliance with battery-specific charging constraints.

The control algorithm is designed with two operational objectives: (1) under heavy load conditions, it dynamically reduces the battery charging current to maintain uninterrupted power delivery to the DC loads; and (2) under light load conditions, it maintains the battery charging current at the predefined upper limit. Depending on system requirements, this scheme allows the implementation of either a slow charging profile (typically 0.2 C–0.3 C) or a fast charging mode of up to 1 C, providing flexibility in the charging strategy while ensuring system stability and battery health. The battery current reference, the output current reference, and the inductor current are fed into a PI controller, which generates the phase-shift angle as its output. This phase-shift angle is then used to produce PWM signals for the MOSFETs via the PWM generator, ensuring accurate and efficient operation of the converter.

Figure 3 illustrates the gate drive signals applied to the primary-side MOSFETs of the converter, as generated by the digital controller. The figure specifically shows the signals delivered from the controller to the gate driver circuits, which in turn drive the MOSFETs Q_1 through Q_4. The waveforms for Q_1 and Q_4 correspond to the leading leg of the full-bridge configuration. A phase-shift angle, denoted as θ, is present between these signals. The gate signals for Q_2 and Q_3 represent complementary signals to Q_1 and Q_4, respectively, with an appropriate dead time inserted to prevent shoot-through conditions. Figure 4 shows the primary current and voltage waveforms. The waveform shown in blue represents the primary voltage of the transformer, which alternates approximately between $+V_{IN}$ and V_{IN}, depending on the switching state of the full-bridge legs. The red waveform indicates the primary current. The peak value of the current waveform is denoted as I_{max}. The parameter I_{cr} refers to the critical current threshold; its definition is discussed later. The symbol I_{p2} denotes the value of the primary current at the instant of time t_2.

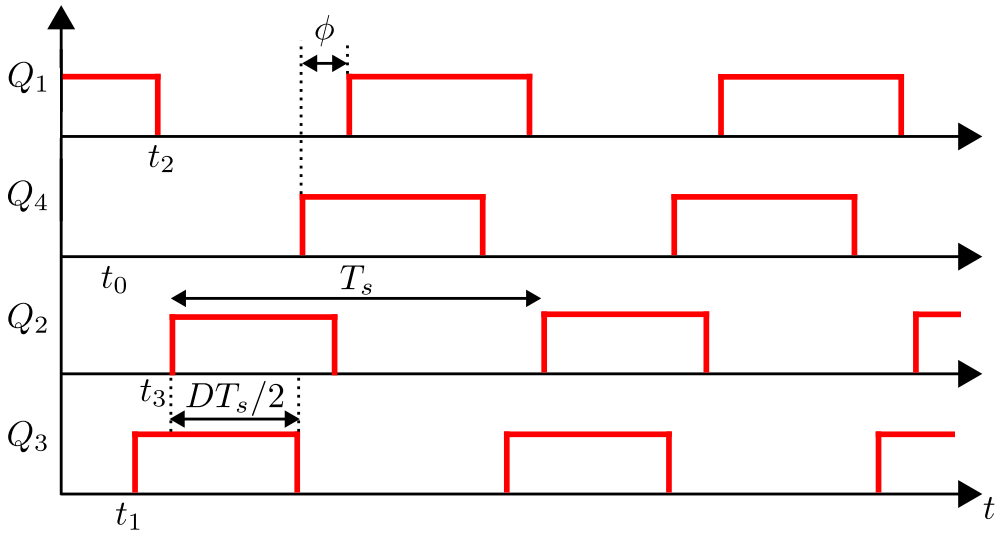


Figure 3. Primary side MOSFETs gate signals.

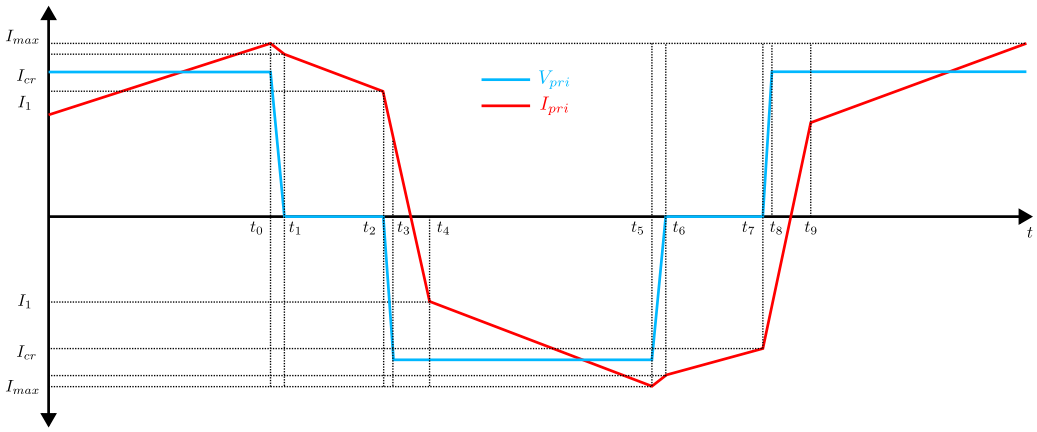


Figure 4. Transformer primary current and voltage waveforms.

Figure 5 presents the current paths and the components in conduction for each of the six distinct operation modes over a full switching period. The following section provides a detailed explanation of these mode transitions based on the converter's operating principles.

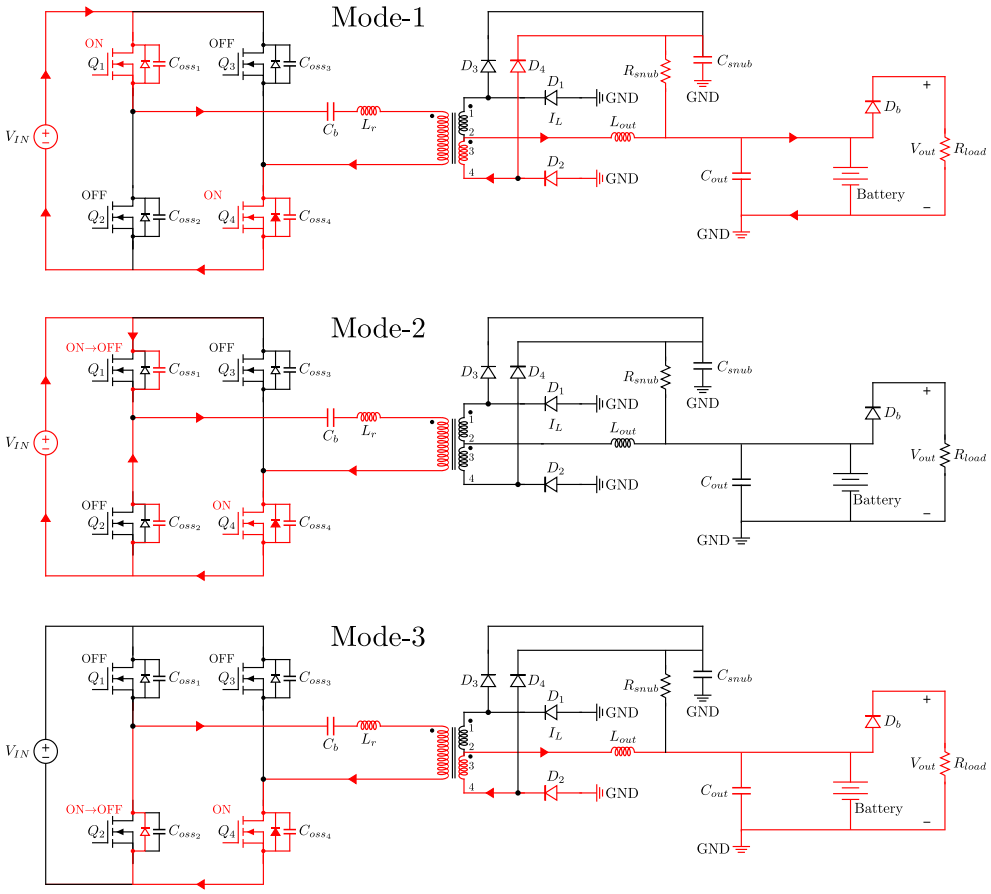


Figure 5. *Cont.*

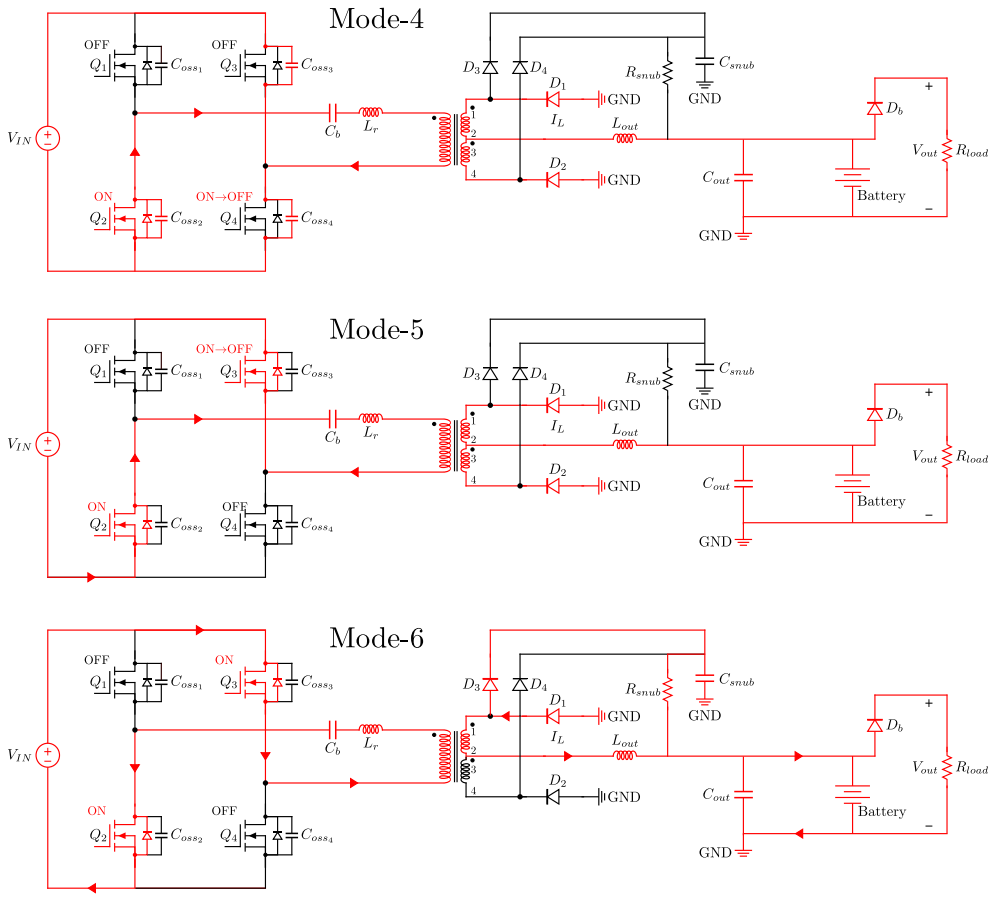


Figure 5. Circuit current paths and active components during the six operation modes in the PSFB converter.

Mode 1: ($t < t_0$) The transformer transfers power from the input to the output, which represents the power transfer mode. The Q_1 and Q_4 MOSFETs transition to conduction mode with ZVS as a result of discharging the energy stored in the transformer leakage inductance through their output capacitances. This discharge causes the drain-source voltages to decrease to zero before the activation event, allowing the MOSFETs to activation via ZVS. During this activation interval, the current begins to flow through the snubber diode D_4. Voltage spikes and oscillations occur due to resonance between the leakage inductance and the output capacitances of rectifier diodes, which are damped by the RCD snubber circuit. The rectifier diode D_2 also conducts the output current through the output filter inductor. The primary current increases with a slope and reaches its maximum at the end of this mode.

Mode 2: ($t_0 < t_1$) This mode transition occurs by turning off the MOSFET Q_1, subsequently facilitating the primary current to traverse through the capacitors C_{oss_1} and C_{oss_2}, as explicitly illustrated in the corresponding figure. The primary current simultaneously performs two critical operations: the charging of C_{oss_1} and the discharging of C_{oss_2}. During the charging process, the energy required to charge C_{oss_1} and discharge C_{oss_2} is supplied by the combined energy stored in the leakage inductance of the transformer and the reflected output inductance on the primary side. The significant magnitude of energy preserved in the output inductor significantly amplifies this bidirectional charge transfer process, thereby enabling the left-leg switches (Q_1 and Q_2) to achieve optimal ZVS conditions, even under minimal load scenarios. At the end of this mode, the voltage across C_{oss_1} asymptotically approaches V_{in}, while the voltage across C_{oss_2} drops to nearly zero. In addition, the transformer's primary voltage drops to zero. When expressing the interval required for C_{oss_1} to reach V_{in} and C_{oss_2} to reach zero voltage as the duration d, the minimum dead-time

interval between switching operations must exceed d to ensure proper ZVS conditions. In scenarios where the dead-time interval is shorter than the calculated minimum duration d, the voltage across C_{oss_2} fails to reach zero before the Q_2 MOSFET begins conduction, leading to a quasi-ZVS operation. This suboptimal switching condition leads to a substantial increase in the number of switching losses on the switch, significantly affecting the overall efficiency of the converter.

Mode 3: ($t_1 < t_2$) Mode 3 begins when the voltage across the capacitor C_{oss_2} is fully discharged to zero. During this mode, MOSFET Q_4 and diode D_2 enter the conduction modes. In particular, power transfer through the transformer is interrupted as the primary transitions to a freewheeling state. This freewheeling action causes the primary current to gradually decrease, influenced by the circuit's parasitic elements and conduction losses.

Mode 4: ($t_2 < t_3$) This mode of operation, similar to Mode 2, is a short interval characterized by the charging and discharging voltages of MOSFET output capacitors. It is triggered by the turn-off of the MOSFET Q_4. This turn-off initiates with a primary current flow that charges the capacitor C_{oss_4} while simultaneously discharging the capacitor C_{oss_2}. This charging and discharging process results in the capacitor C_{oss_4} reaching a voltage level of V_{in}, while the capacitor C_{oss_3} is completely discharged to 0 V. Unlike Mode 2, in this mode, the total energy required for the charging and discharging of the capacitors is supplied by the energy stored in the transformer's leakage inductance. Because the energy stored in the leakage inductance is much lower compared to the energy stored in the output inductance, at light loads, the charging and discharging of the output capacitors are incomplete, and the interval ends when the stored energy is depleted. Due to the voltage across the Q_3 MOSFET, a quasi-ZVS transition occurs, but a completely lossless activation is not achieved. Therefore, to achieve ZVS under the desired load conditions, the leakage inductance must be designed to accommodate the energy requirements at light loads.

Mode 5: ($t_3 < t_4$) At the end of Mode 4, and with the full discharge of C_{oss_3} to 0 V, diode D_3 becomes forward-biased and enters its conduction state. This initiates a freewheeling current that circulates between MOSFET Q_2 and the diode D_3. Consequently, the primary current begins to decrease, and since the voltage across the transformer remains at 0 V, no power transfer occurs in this interval.

Mode 6: ($t_4 < t_5$) Mode 6 begins with the activation of the switch Q_3. With the voltage across the transformer reaching V_{in}, power transfer from input to output is re-established, and energy begins to accumulate in the output inductor. At the end of this mode, the current exhibits a tendency to increase in the negative direction, reaching its peak value.

3. Design Considerations of PSFB with Nanocrystalline-Cored Magnetics

The design of a PSFB DC-DC converter for railway battery charging systems involves the careful optimization of numerous interconnected circuit parameters to ensure efficiency, reliability and compliance with stringent railway standards. The performance of the converter, particularly in achieving ZVS, is heavily influenced by the interaction between the leakage inductance of the transformer, the parasitic capacitance of the semiconductor switches, and the transformer turn ratio.

Advanced magnetic designs, such as those using nanocrystalline-cored transformers, provide significant advantages to meet these requirements. Nanocrystalline cores offer superior magnetic properties, including high saturation flux density, low core loss, and excellent permeability at high frequencies. These features enable the integration of the transformer and leakage inductor into a single magnetic structure, enhancing system efficiency, reducing size, and increasing power density. However, this integration introduces challenges in balancing leakage inductance with ZVS requirements and ensuring thermal stability under varying conditions. Another key aspect of PSFB design is the precise calcu-

lation and optimization of critical circuit parameters, such as dead time, transformer turns ratio, and component values for snubber circuits. These parameters must be fine-tuned to achieve efficient operation across a wide range of input and output voltages, as required in railway systems.

3.1. Leakage Inductance and Dead Time Requirements for Achieving ZVS Operation

When the stored inductive energy exceeds the capacitive energy, full ZVS operation occurs. Under this condition, the MOSFET transitions during activation without any voltage stress, resulting in a lossless activation event. Conversely, under the inductive energy, which is insufficient compared to the capacitive energy, quasi-ZVS or hard-switching operations can be observed. In this case, the MOSFET turns on with a voltage across it, leading to quite high MOSFET losses during the activation transition. This highlights the importance of achieving adequate inductive energy for efficient ZVS operation, particularly at lower load levels.

The energy equation required to achieve ZVS operation for the left leg switches: The energy equation required for the switches on the left leg to achieve ZVS operation is influenced by the contributions of the magnetizing inductance, the leakage inductance, and the reflected output inductance on the primary side. The resulting inductive energy equation can be expressed as follows:

$$E_I = (1/2L_M I_M^2) + 1/2L_r(I_M + I_{max})^2 + (1/2L_{out} I_{out}^2) > E_c \quad (1)$$

$$E_c = 1/2 \times \ (2C_{oss} + C_p)V_{in}^2 \quad (2)$$

where L_m is the magnetizing inductance, I_M is the magnetizing peak current, L_r is the transformer leakage inductance, I_o is the peak output inductor current, L_{out} is the output inductor, C_{oss} are the MOSFET output capacitances, C_p is the parasitic capacitance of the transformer, and V_{in} is the input voltage. The energy equation required to achieve ZVS operation for the right leg switches:

$$E_I = (1/2 \times L_r I_{cr}^2) > E_c = 1/2 \times (2C_{oss} + C_p)V_{in}^2 \quad (3)$$

where I_{cr} is the critical current that can be expressed as follows:

$$I_{cr} = I_M + I_o \times \frac{N_{sec}}{N_{pri}} = \sqrt{\frac{(2C_{oss} + C_p)V_{in}^2}{L_r}} \quad (4)$$

ZVS can be achieved under load conditions where the transformer primary current (I_{pri}) exceeds the critical current at the beginning of "Mode 3". However, in addition to this, the dead time must be long enough to allow for the voltage transition, which is influenced by the parameters of the resonant circuit. During the interval in which ZVS operation occurs, the dead time must be sufficiently long to allow the complete charging and discharging of the switch parasitic capacitances. During the voltage transition in the ZVS operation, the transition is completed within one-fourth of the resonant period ($T_r/4$). If the dead time is shorter than $T_r/4$, the voltage transition remains incomplete, resulting in quasi-ZVS. In contrast, if the dead time exceeds $T_r/4$, the resonance may persist, disrupting the ZVS. The resonant frequency can be calculated as follows:

$$f_r = \frac{1}{2\pi\sqrt{(L_r(2C_{oss} + C_p)}} \quad (5)$$

3.2. Calculation of Critical Circuit Parameters

The determination of the transformer's turns ratio is essential to achieve a precise regulation of the output voltage, particularly under varying input voltage and load conditions. The turns ratio must be carefully calculated to account for the duty cycle loss, which is the portion of each switching cycle used for reversing current polarity in the primary winding and transitioning current on the secondary side. This loss reduces the effective duty cycle available for power transfer, impacting the voltage regulation capability of the system. To ensure accurate regulation, the turns ratio can be calculated using the following equation.

$$\frac{V_{out}}{V_{in}} = \frac{D}{n} - \frac{I_o L_r f}{n^2 V_{in}} \tag{6}$$

If the maximum duty cycle is set to 0.85 and the switching frequency is set to 50 kHz, the turns ratio can be calculated as 4.

$$\frac{138}{650} = \frac{0.85}{n} - \frac{I_o L_r f}{n^2 V_{in}} \tag{7}$$

To refine the energy equation described for the right-leg MOSFETs, the minimum leakage inductance (L_r) can be calculated using the following expression derived from the energy balance.

$$L_r = \frac{2E_c}{I_{cr}^2} = 11\ \mu\text{H} \tag{8}$$

In flux-unbalanced situations, the blocking capacitor is introduced to prevent the transformer from saturating. The value of the blocking capacitor (C_b) is calculated using the following equation.

$$C_b = \frac{I_o/n}{\Delta V_{C_b}} = 7.5\ \mu\text{F} \tag{9}$$

To limit the output current ripple (ΔI_o) to 15% of the output current (I_o), the value of the output inductor can be calculated using the following equation.

$$L_o >= \frac{V_{o,nom}(1-D)T}{\Delta I_o} = 25\ \mu\text{H} \tag{10}$$

3.3. Leakage Integrated Center-Tapped Transformer Design Criteria

3.3.1. Core Materials Comparison

The choice of core material significantly influences the performance, efficiency, and reliability of high-frequency transformers. A variety of core materials—including Mn-Zn ferrite, Fe-based amorphous, oriented Si-Fe, and nanocrystalline cores—can be utilized for high-frequency transformer designs, each offering unique advantages and limitations depending on the application requirements and operating conditions. Oriented Si-Fe steel provides very high saturation flux density (up to 2 T) but suffers from prohibitive eddy-current losses above 10 kHz (7.1 W/kg at 10 kHz, 250 W/kg at 100 kHz), limiting its use to very low-frequency transformers. Ferrite cores are widely used in cost-sensitive, low-frequency applications due to their low cost, high electrical resistivity, and ease of manufacturing; they exhibit core-loss densities of approximately 0.2 W/kg at 1 kHz, rising to 20 W/kg at 100 kHz (Table 1), however, their modest saturation flux density (0.49 T at 25 °C, dropping to 0.39 T at 100 °C), moderate Curie temperature (>210 °C), and inherently brittle ceramic structure—which is prone to cracking under mechanical stress and experiences a 20% flux reduction at elevated temperatures—impose serious limitations in high-power applications. Fe-based amorphous cores are formed by rapid quenching of metallic alloys into a non-crystalline structure, resulting in lower magnetic losses (0.15 W/kg at 1 kHz

and 60 W/kg at 100 kHz) and are therefore suited to mid-frequency, moderate-power applications. Nanocrystalline FINEMET®(Proterial Ltd., Tokyo, Japan) F3CC cut cores combine low losses (0.08 W/kg at 1 kHz, 7 W/kg at 50 kHz, and 25 W/kg at 100 kHz) with high saturation flux density (1.2 T), making them the preferred choice for high-frequency, high-power designs such as 50 kHz PSFB converters. These attributes make nanocrystalline cores the optimal choice for modern high-frequency, high-power-density converters (e.g., 50 kHz PSFB), whereas Si-Fe remains suited to line-frequency applications, ferrite to cost-sensitive >50 kHz designs, and amorphous alloys to niche mid-frequency roles. Moreover, the exceptionally high initial permeability of nanocrystalline alloys (>100,000 at 10 kHz) ensures a compact winding design by maximizing magnetizing inductance and minimizing leakage inductance, which in turn improves voltage regulation and reduces circulating currents in PSFB topologies. The nanocrystalline core exhibits outstanding thermal resilience, preserving over 90% of its initial permeability at temperatures up to 150 °C and thus ensuring stable inductive performance even under severe thermal stress. Collectively, these power-electronics-centric benefits enable a nearly 30% reduction in transformer volume and enhance overall system efficiency, making nanocrystalline cores indispensable for compact, high-power railway battery-charger converters.

Table 1. Core-loss densities of various high-frequency transformer core materials at $B_m = 0.1$ T (W/kg).

Core Material	1 kHz	10 kHz	50 kHz	100 kHz
Oriented Si-Fe (grain-oriented, 3% Si, $t = 0.23$ mm)	0.7	7.1	80.0	≈250
Mn-Zn Ferrite	0.2	2.0	10.0	20
Fe-based Amorphous	0.15	4.0	30.0	60.0
Nanocrystalline Core (FINEMET® F3CC)	0.08	0.4	7.0	25

3.3.2. Winding Material Selection

In high-frequency transformer designs, the choice of winding material is critical for optimizing efficiency and minimizing losses. Commonly used materials include solid wire, copper foil, and Litz wire, each with unique advantages and challenges. Solid wire is simple and cost-effective, but suffers from significant skin effects at high frequencies, where current concentrates near the conductor's surface, effectively increasing resistance and reducing efficiency. Copper foil, on the other hand, provides a larger surface area, which helps reduce resistance and mitigate the skin effect, making it more efficient at higher frequencies. However, its use introduces challenges such as an increased parasitic capacitance between the foil layers, potentially leading to unwanted resonances and additional losses. Careful design and spacing are required to minimize these effects, which can complicate the manufacturing process. In contrast, Litz wire, composed of multiple thin, individually insulated strands twisted or braided together, is designed specifically to address the challenges of high-frequency operation. By distributing current uniformly across the conductor's cross-section, Litz wire minimizes both skin and proximity effects, significantly reducing AC resistance and improving overall transformer efficiency. This makes the Litz wire the optimal choice for high-frequency applications, such as the 50 kHz PSFB converter in this design.

3.3.3. Critical Parameters of Leakage Integrated Transformer

Area product method: The area product method allows for the sizing and dimensional limitation of the transformer. The formula for the area product can be expressed as

$$A_p = A_c A_w = \frac{P10^4}{K_f K_u B_m f_s w J} \tag{11}$$

A_c is the cross-sectional area of the core, W_a is the window area of the core, P is the maximum operating power of the transformer, K_f is the waveform coefficient, K_u is the window utilization factor, B_m is the maximum flux density, f_{sw} is the switching frequency of the transformer, and J is the current density of the conductor. If the transformer area product (AP) is calculated using the above formula, it is determined that the AP must exceed 96 cm^2 to meet the design requirements. Considering that the ANCC63 nanocrystalline C-core, manufactured by Gaotune, has an individual AP of 53 cm^2, the required area product can be achieved by stacking two ANCC63 cores. This stacked configuration ensures that the combined AP meets the necessary specifications while maintaining the efficiency, compactness, and reliability of the transformer under the given operating conditions.

Determining Flux Density and Number of Turns: According to Faraday's law, the flux induced in each turn of the core can be expressed as follows:

$$V_{turn}(t) = \frac{\Phi(t)}{dt} \tag{12}$$

but flux (Φ) passes through each winding, allowing the net voltage across the windings to be calculated by the following:

$$V(t) = nV_{turn}(t) = n\frac{\Phi(t)}{dt} = n\frac{A_c dB(t)}{dt} \tag{13}$$

Consequently, the general formulation can be expressed as follows:

$$V_p = \frac{N_p K_f B_s f_s w A_c}{10^4} = n\frac{A_c dB(t)}{dt} \tag{14}$$

If the equation is rearranged, the primary turns can be calculated as follows:

$$N_p = \frac{V_{pri}(10^4)}{K_f B_s f_{sw} A_c} \tag{15}$$

The primary turns N_{pri} are calculated as 22.4, but to simplify manufacturing and consider the primary to the secondary turns ratio of 4, the primary turns can be rounded to 24. This adjustment simplifies the winding and production process while maintaining efficient transformer operation. With the primary turns set to 24, the secondary turns are equal to 6×2. Using these values, the flux density B_{max} is calculated to be 0.186 T. This value is within the acceptable limits for the nanocrystalline core material, ensuring efficient magnetic performance and minimizing core losses.

3.3.4. Magnetizing Inductance Calculation

The magnetizing inductance of the transformer can be determined by adjusting the number of primary turns and the air gap. A higher air gap reduces the magnetizing inductance, which increases the magnetizing peak current and extends the ZVS range of the converter. However, this leads to higher conduction losses and increased core losses

because of fringing flux around the air gap. The calculation of magnetizing inductance can be expressed as follows.

$$L_m = \frac{\mu_0 A_c N_p^2}{l_g + \frac{l_c}{\mu_r}} \tag{16}$$

Using the formula provided, the magnetizing inductance can be calculated by introducing an air gap between the cores. However, because of the laminated structure of the nanocrystalline cores, introducing an air gap results in significant fringing flux, which concentrates near the gap and causes high core losses. This phenomenon occurs because the magnetic flux density in the gap region becomes highly non-uniform, increasing eddy currents and hysteresis losses in the surrounding laminations. These losses can significantly reduce the overall efficiency of the transformer and lead to thermal management challenges. To minimize these losses, no air gap was introduced between the cores. By avoiding an air gap, the magnetizing inductance is maximized, reducing the magnetizing current. A lower magnetizing current translates to reduced conduction losses in the converter's primary-side switches, enhancing overall efficiency. However, this approach has a trade-off: The ZVS range decreases as a result of the higher magnetizing inductance, as the energy required for achieving ZVS is reduced. Despite this trade-off, the converter leakage inductance has been carefully designed to provide the necessary energy for ZVS operation under the targeted load conditions. In this design, leakage inductance was optimized to 10 µH, ensuring that ZVS is achieved throughout the desired operating range without relying on additional magnetizing current. This approach balances efficiency, component losses, and ZVS performance, avoiding the drawbacks of excessive magnetizing current. L_m is the magnetizing inductance, μ_o is the magnetic permeability of air, N_p is the primary turns, l_g is the length of the air gap, l_c is the length of the core magnetic path and μ_r is the relative magnetic permeability of the core material.

3.3.5. FEA Simulations

The leakage-integrated transformer, summarized in Table 2, was implemented in a 3D finite-element model to validate its electromagnetic performance under a 50 kHz switching waveform. A center-tapped core (124 × 110 × 94 mm^3) with sandwich winding of litz wire (1750 × 0.08 mm) was used to realize a 4:1 turn ratio (24-turn primary, two 6-turn secondary windings). The simulation targets—9.5 µH leakage inductance and 12 mH magnetizing inductance—were met.

Table 2. Parameters of the leakage integrated transformer.

Parameters Name	Value
Structure	Center-tapped
Winding Type	Sandwich Winding
Wire Type	Litz Wire (1750 × 0.08 mm)
Primary to Secondary Turns Ratio	4
Mechanical Dimensions	124 × 110 × 94 mm^3
Nominal Power	10 kW
Leakage Inductance	9.5 µH
Magnetizing Inductance	12 mH
Core Loss	17 W
Primary Winding Loss	7 W
Secondary Winding Loss	12 W × 2

The 3D Maxwell transformer model, converted from PEmag, is illustrated in Figure 6. The yellow wires in the inner layer represent the 24-turn primary winding, while the red

wires on the left leg represent the 6-turn secondary-1 winding, and the blue wires on the right leg represent the 6-turn secondary-2 winding.

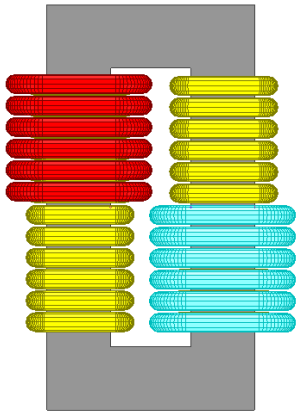


Figure 6. 3D ANSYS model of the transformer; primary winding (yellow), secondary-1 winding (red), secondary-2 winding (blue), core (gray).

***Leakage Inductance Evaluation with Different Winding Configurations*:** The transformer leakage inductance was analyzed for different winding configurations using the ANSYS Maxwell (2025/R1) tool, with the goal of achieving an optimal balance between switching and conduction losses. Configuration 1, as shown in Figure 7, utilizes a sandwich winding structure that resulted in a leakage inductance of 5 μH, significantly lower than the desired value. This configuration limits the energy available for ZVS, particularly at light loads, leading to increased switching losses and reduced efficiency. Configuration 2, depicted in Figure 7, aimed to increase leakage inductance by maximizing physical separation between the primary and secondary windings. However, this resulted in an excessively high leakage inductance of 81 μH, causing a rise in the primary RMS current and increased conduction losses, which negatively affected the overall efficiency and thermal performance of the converter. Configuration 3, illustrated in Figure 7, achieved a leakage inductance of 11 μH, which corresponds to the design target. This configuration enabled effective ZVS operation up to 30% of the load, reducing switching losses and improving efficiency while maintaining lower primary RMS currents. This balance established Configuration 3 as the optimal design for achieving the desired performance.

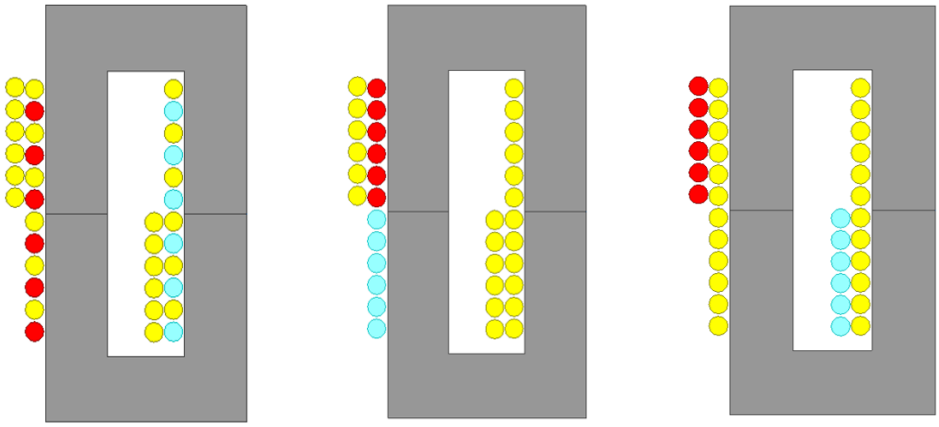


Figure 7. Different winding configurations in the 2D ANSYS transformer model; Winding configuration 1 (**left**), winding configuration 2 (**middle**), winding configuration 3 (**right**); primary winding (yellow), secondary-1 winding (red), secondary-2 winding (blue).

***Maxwell 2D Simulations*:** Using the ANSYS Maxwell tool, transient analysis enables the detailed evaluation of various transformer characteristics, including fringing flux, leakage inductance, core losses, and flux density distribution. These analyses provide critical insights into the electromagnetic behavior and the performance of the transformer. However, performing these analyses on a 3D model can be extremely time-consuming due to the high computational demands involved in processing complex geometries and detailed simulations. To overcome this challenge, the 2D model shown in Figure 8 is utilized for the analysis, with the actual core depth of 60 mm incorporated into the simulation to account for the third dimension. This approach significantly reduces the simulation time without compromising the accuracy of the results. By maintaining the physical depth in the 2D simulation, the analysis captures all essential characteristics, including fringing effects and magnetic field distributions, as effectively as a 3D simulation.

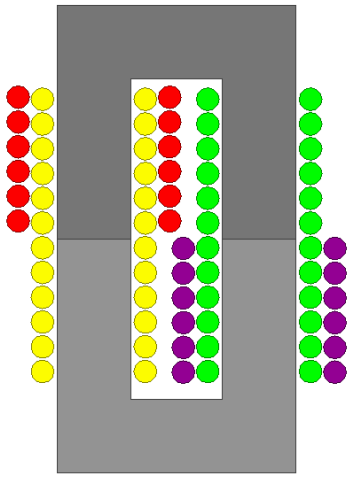


Figure 8. Maxwell 2D transformer model; primary winding (yellow and green), secondary-1 winding (red), secondary-2 winding (purple).

The transformer flux lines are visualized on the transformer's surface in Figure 9, illustrating the magnetic field distribution. Due to the absence of an air gap in the design, the flux lines are uniformly distributed throughout the core, ensuring efficient magnetic coupling and minimizing localized saturation.

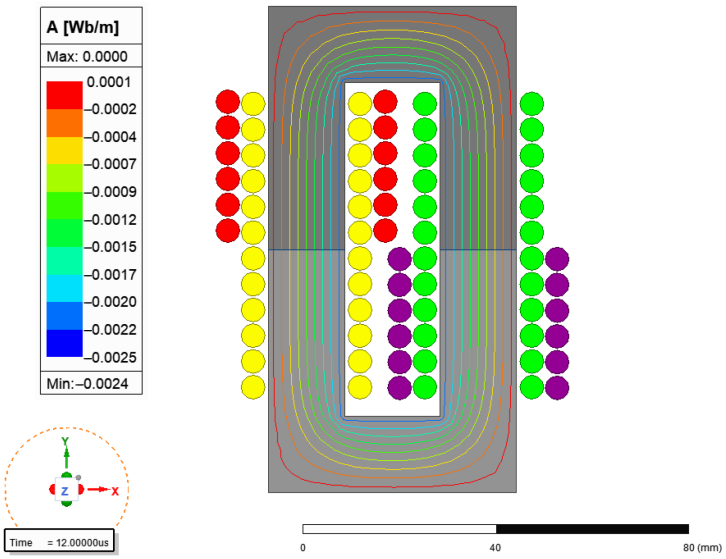


Figure 9. Transformer flux lines distributions.

In Figure 10, the flux density distribution on the core surface can be observed, providing a detailed view of the magnetic field's intensity across the core. It is observed that the flux density can rise as high as 325.6 mT near the edges of the core. This localized increase is primarily due to fringing flux effects and the geometric constraints at the core edges, where the magnetic path is less confined. However, because of the use of a nanocrystalline core, which has a high saturation flux density of 1.2 T, the core remains unsaturated even in these regions of increased flux density. This material property ensures that the core operates efficiently under all conditions, maintaining magnetic stability and preventing energy losses associated with saturation. The absence of saturation highlights the core's ability to handle high flux levels uniformly, making it ideal for demanding applications like railway battery chargers.

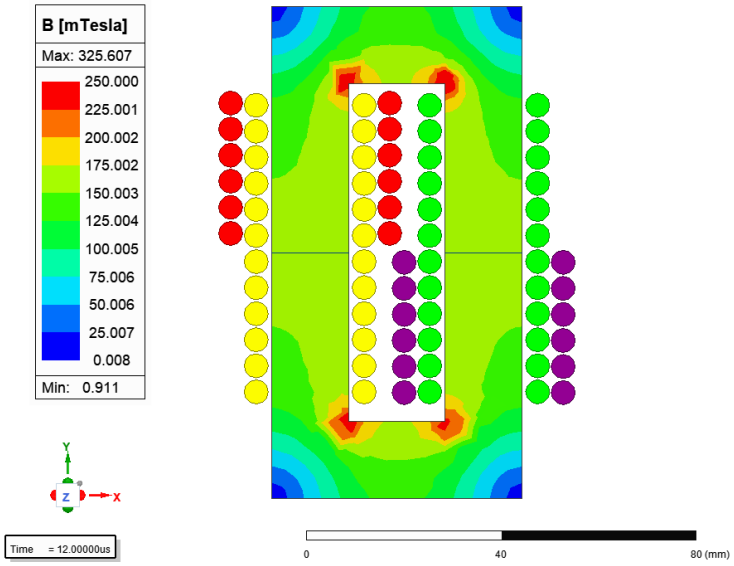


Figure 10. Transformer flux density distributions.

In Figure 11, the average flux density on the core is calculated, showing a maximum value of 190 mT, which is very close to the theoretically calculated value of 186 mT. This close agreement indicates that the theoretical calculations and the simulation results align well, validating the accuracy of the design approach and the reliability of the simulation process.

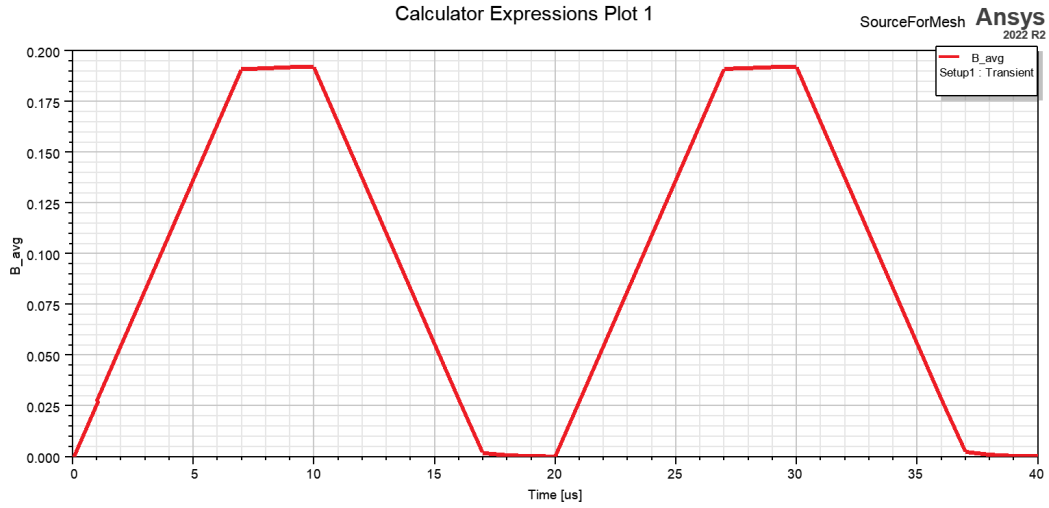


Figure 11. Transformer average flux density waveform.

4. Experimental Results

This section will discuss the realization and testing of the nanocrystalline-cored transformer with integrated leakage inductance. The focus will be on the implementation process, the methods used to achieve the desired leakage inductance, and the experimental validation of the transformer performance under operating conditions. Figure 12 illustrates the implemented version of the designed transformer, where the core structure, winding configuration, terminal outputs, and mounting case can be clearly observed. This figure represents the appearance of the transformer before the molding process. The molded version of the same transformer is presented in Figure 13, where the final encapsulated structure can be seen. The transformer was molded using a thermally conductive material with a thermal conductivity of 3 W/mK, which significantly improves heat dissipation from the winding and core regions to the baseplate. This molding process effectively eliminates potential thermal hotspots and enhances the overall thermal performance of the transformer under high-power operation.

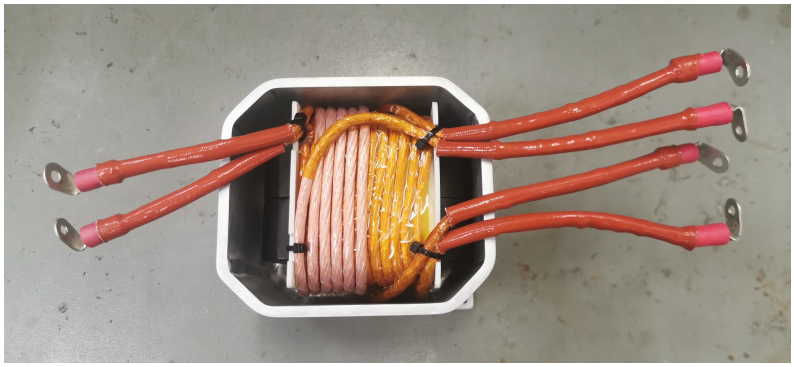


Figure 12. Implementation of integrated transformer.

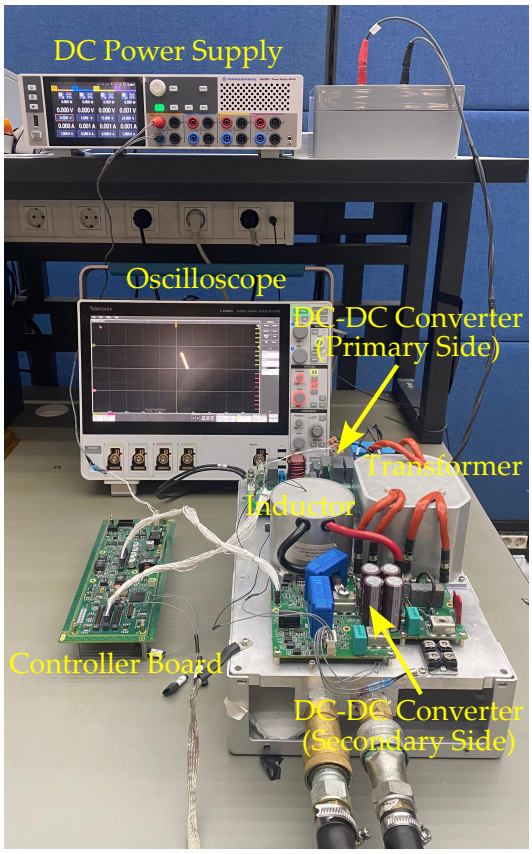


Figure 13. Experimental setup of the prototyped center-tapped PSFB DC-DC converter.

After the experimental system is set up, the compliance of the converter with the design specifications is tested through various measurements. These measurements validate the performance of the converter, including its efficiency, voltage regulation, current handling capabilities, and the achievement of ZVS. By comparing the experimental results with simulation data, the functionality and reliability of the converter design are confirmed under real-world operating conditions.

Center-Tapped PSFB DC-DC Converter Experimental Setup

For experimental studies, the setup shown in Figure 13 was prepared. The control loops and sensor readings implemented in the simulation environment were realized on a control board equipped with a C2000 series processor. The 32-bit TI C2000 microcontrollers are optimized for real-time control applications, enhancing closed-loop performance in areas such as industrial motor drives, solar inverters, digital power, electric vehicles and transportation, motor control, and sensing applications.

The development environment used in this study is Code Composer Studio™, an integrated development environment (IDE) designed for TI microcontrollers and processors. It includes a comprehensive set of tools for developing and debugging embedded applications. As shown in Figure 13, the system consists of a control board, a transformer, an inductor, and the primary and secondary sections of a phase-shifted full-bridge rectifier. The converter output provides two separate outputs for the battery and DC loads. To realize DC loads, a 110 V, 10 kW passive load bank was used. Load banks are commonly utilized to test power electronics equipment, such as generators, uninterruptible power supplies, voltage regulators, and power transformers. In addition, a programmable power supply was used to model the battery.

Figures 14 and 15 show the oscilloscope waveforms of the converter's output current, the drain-source voltage, and the gate signal applied to Q_1 and Q_3 MOSFETs under full-load conditions. As highlighted in the boxed region of the figures, the ZVS phenomenon can be clearly observed: the drain-source voltage of the Q_1 and Q_3 MOSFETs drops to zero before the gate activation signal is applied. This indicates that complete ZVS is achieved at full load, thereby confirming the effectiveness of the soft-switching design.

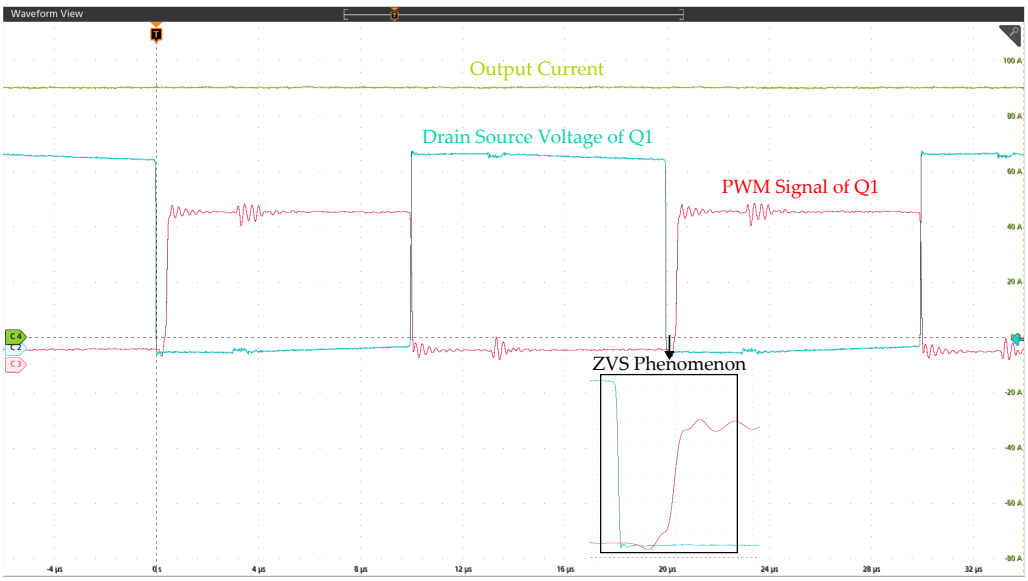


Figure 14. Output current, drain source voltage of Q1, and PWM signal of Q1 waveforms of the PSFB converter at full load.

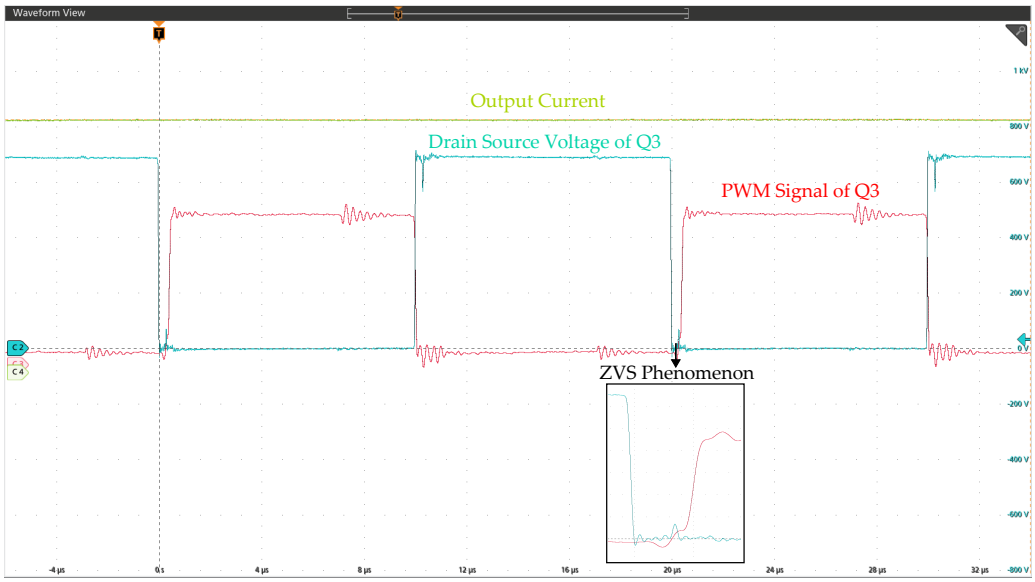


Figure 15. Output current, drain source voltage of Q3, and PWM signal of Q3 waveforms of the PSFB converter at full load.

In Figure 16, the voltage across the rectifier diode is observed under full load conditions. The peak value of the voltage across the diodes reaches approximately 700 V. This voltage can be reduced by decreasing the value of the snubber resistor; however, doing so would result in increased losses in the snubber resistor, negatively impacting both efficiency and thermal performance.

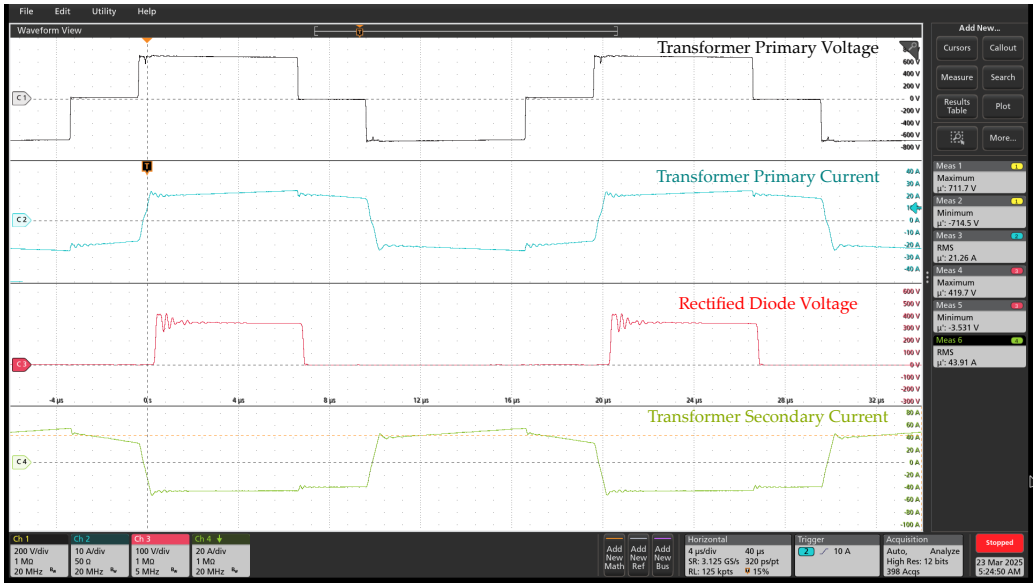


Figure 16. Transformer primary voltage, transformer primary current, rectified secondary diode voltage, and transformer secondary current waveforms of the PSFB converter at full load.

In Figure 17, it is observed that the converter can operate at 10 kW power, achieving an input voltage of 700 V, an output current of 90 A, and an output voltage of 110 V. In Figure 17, the primary current and the primary voltage of the transformer are observed under full load conditions.

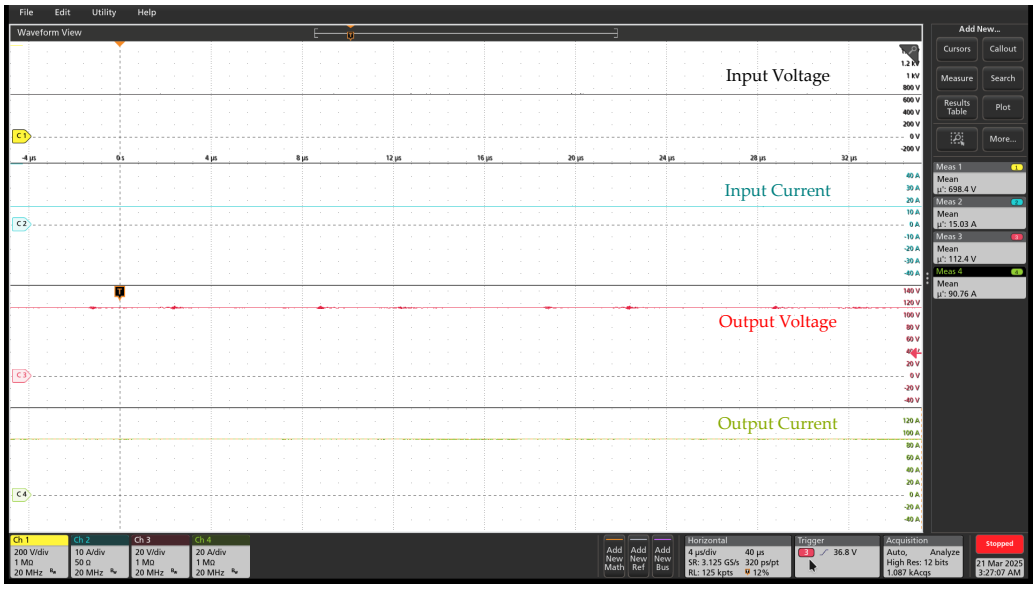


Figure 17. Input voltage, input current, output voltage, and output current of waveforms of the PSFB converter at full load.

Figure 18 shows the temperature profiles of the output inductor, the primary MOSFET, the rectifier diode, and the nanocrystalline core transformer during a continuous full-load operation of two hours at 10 kW, with the liquid cooling loop temperature held constant at 40 °C. Thermocouples were installed at the hotspot locations of these critical components to monitor their real-time thermal behavior. Specifically, the thermocouple for the inductor was placed between the core and winding. The MOSFET thermocouple was mounted at the closest possible point between the device body and the heatsink, capturing junction-proximate thermal conditions. For the transformer, the thermocouple was positioned at the expected hotspot near the core joint—an area affected by fringing flux and poor internal heat dissipation. Throughout the test, the converter maintained stable input/output voltages and currents, confirming robust full-load operation. After two hours, the inductor reached 80.5 °C, the MOSFET junction 62.7 °C, the rectifier diode 73.2 °C, and the transformer core 103.4 °C. These results demonstrate that all monitored components remained within their rated temperature limits, validating the effectiveness of the thermal design and confirming the converter's ability to deliver continuous 10 kW output.

Figure 19 illustrates the converter's efficiency curve across varying load conditions. At light loads, the efficiency remains relatively low due to the dominance of core losses in the output inductor and transformer. As the output power increases, soft-switching begins to emerge, and full ZVS is achieved beyond approximately 30% of the load. This transition reduces switching losses significantly. Furthermore, as conduction losses become more dominant at higher loads, the relative impact of core losses diminishes. As a result, the overall efficiency improves steadily, reaching nearly 97% at full load power.

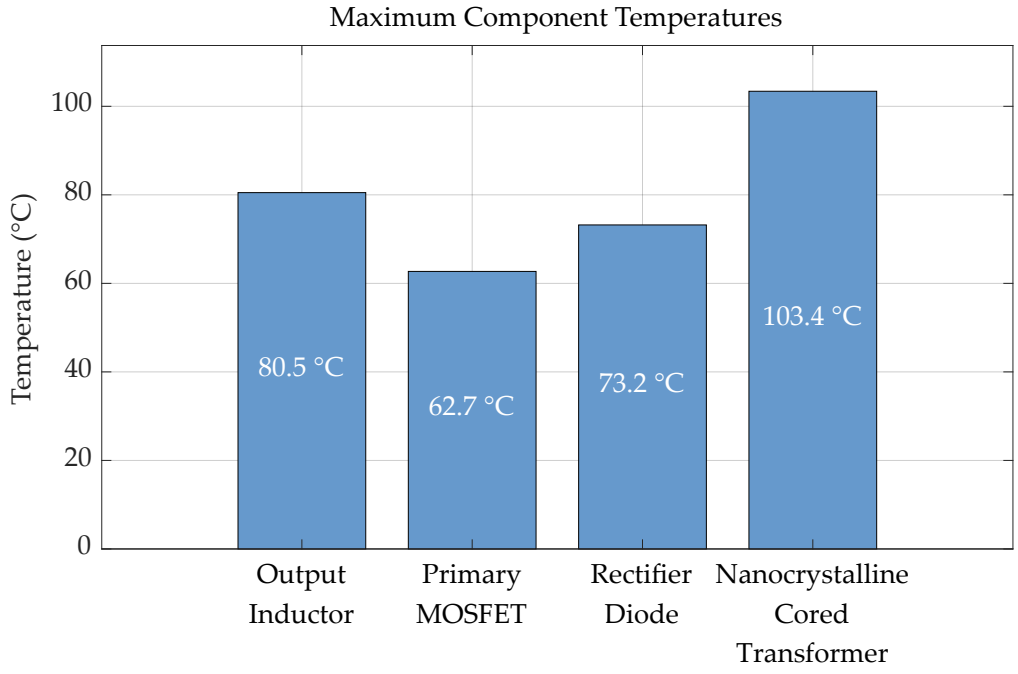


Figure 18. Output inductor, primary MOSFET, rectifier diode, and nanocrystalline-cored transformer temperature measurements at full load.

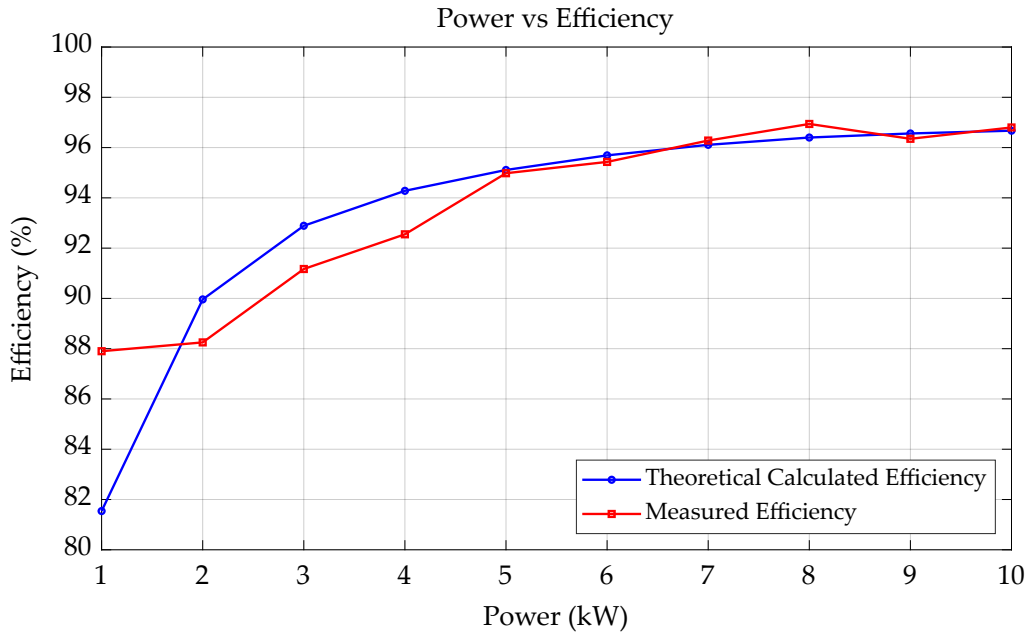


Figure 19. Prototyped PSFB converter overall efficiency with different output loads.

5. Conclusions

This study successfully presented the design and implementation of a high-efficiency, full SiC-based center-tapped phase-shifted full-bridge (PSFB) DC-DC converter for NiCd battery charging applications in railway systems. Significant focus was placed on the design of the nanocrystalline-cored integrated transformer and its experimental validation under various load conditions. The converter was rigorously tested across a wide range of load scenarios, from light loads to full-load operation, to evaluate its performance, efficiency, and stability. A detailed experimental setup was developed where the thermistors were strategically placed at multiple locations on the transformer to monitor its thermal behavior.

These measurements demonstrated that the nanocrystalline core exhibited excellent thermal management, maintaining optimal performance even under full-load conditions. The system's ability to handle high thermal and electrical stresses was further validated through full-load testing, confirming the reliability of the proposed design. The experimental results showed that the converter achieved a maximum efficiency of 97% and maintained stable operation throughout its operating range, validating the effectiveness of the integrated magnetic design. The use of a nanocrystalline core significantly contributed to compactness and efficiency by combining the transformer and the leakage inductor into a single core. Future work will explore the integration of nanocrystalline magnetic materials into planar transformer structures to reduce profile height further and enhance power density. Such an approach would also improve thermal management and support the development of compact, modular power architectures for railway applications.

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