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A Novel Multilevel Inverter Topology Generating a 19-Level Output Regulated by the PD-PWM Method

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Abstract

Traditional multilevel inverter topologies, such FC, NPC, and CHB, have a few significant disadvantages. They need a great number of parts, which raises the complexity, expense, and switching losses. Furthermore, their intricate control schemes make voltage balancing and synchronization challenging. Lastly, under some circumstances, they experience severe harmonic distortion, necessitating the inclusion of expensive filters to enhance signal quality. This paper proposes a novel multilevel converter topology that uses the phase-disposition PWM (PD-PWM) technique to control a 19-level output. This new configuration maintains performance comparable to the CHB-MLI reference while using fewer switches, simplifying control, and reducing costs. Our approach is based on extensive simulations conducted in the MATLAB Simulink environment, with results compared to the CHB-MLI. A low-pass filter is added to improve the output voltage quality, reducing the THD% to 1.33%. This strategy offers several advantages, including simpler control, lower costs, increased reliability, and higher-quality output. The system was replicated using MATLAB Simulink and validated through hardware-in-the-loop (HIL) testing. The HIL method ensures real-world testing without causing damage to the hardware. The integrated system includes sensors and necessary hardware for a comprehensive energy management solution.

Keywords: PD-PWM: phase-disposition pulse width modulation; CHB-MLI: cascaded H-bridge multilevel inverter; THD: total harmonic distortion; hardware in the loop

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1. Introduction

One of the main pillars in the movement toward climate neutrality is electric cars, or EVs [1]. Since every EV charger needs an inverter to power the car, the system is essential. Numerous topologies of inverters are available, and multilayer inverters (MLIs) are the subject of more and more research due to developments in academia and industry [2,3]. Due to their capacity to generate high-quality voltage waveforms with lower total harmonic distortion (THD), multilevel converter topologies have become more and more common in recent years [4–9]. Numerous advantages result from this trait, such as increased energy efficiency, less strain on electrical components, and fewer running expenses [10–14]. Additionally, by aiding in the decarbonization process, most notably by integrating hydrogen into transportation, multilevel converters might indirectly help alternative energy transport systems. These converters, for instance, can be employed in

hydrogen rail systems to increase energy conversion, optimize power supply, and boost on-board electrical system efficiency [12]. However, to manage increasing voltage levels, traditional multilevel converter topologies like NPC, FC, and CHB are becoming more complicated and need many components. This study suggests a novel multilevel converter architecture to overcome these issues. It can provide harmonic performance on par with the CHB design while utilizing a notably smaller number of switches. Even with fewer switches, the new design uses the same control method (PD-PWM) to produce a voltage harmonics rate comparable to the CHB topology.

The structure of this article is as follows: A general survey of fundamental multilevel converter topologies is presented in Section 2, and the generalized configuration of the suggested topology is presented in Section 3. This section also covers the control of the modulation method (PWM), as well as the states and operating mode of a 19-level single-phase sinusoidal inverter. Section 4 presents hardware-in-the-loop (HIL) testing, a method used in the development and testing of complex process systems. A low-pass filter is proposed in Section 5 to improve the circuit and minimize harmonic content and compare the number of switches and THD of the proposed topology with traditional topologies, and also with the results found experimentally. The final section presents future prospects and conclusions.

2. State of the Art: Multilevel Converter Topologies

To fully understand multilevel converters, we must first understand their topologies. These topologies come in a variety of forms, all of which are intended to provide an excellent voltage waveform at the output. The authors of papers [15–17] have thoroughly examined the various MLI topologies, including active neutral-point-clamped (ANPC), cascaded multilevel inverter (H-bridge), flying capacitor topology (FC), and diode-clamped multilevel inverter (NPC), without overlooking the new topologies with component reduction. The development of converter topologies since 1970 is depicted in Figure 1. The novel multilevel converter topology introduced by [16] demonstrates significant improvements in energy efficiency and reduced impact on the supply network, which aligns with the goals of our PD-PWM approach. By optimizing the switching strategy and minimizing component count, their work supports the advancements in control techniques that we explore in our study [18] provide an in-depth analysis of the Packed E-Cell (PEC) converter topology, including its operational principles and experimental validation. Their work underscores the potential of advanced topologies like PEC to enhance performance and efficiency, complementing our exploration of the PD-PWM technique for multilevel converters. By incorporating such recent advancements, our study aims to build on these innovations to further optimize control strategies and improve converter performance. Ref. [19] discusses advanced methods for power flow control and energy utilization in AC electrified railways, which highlights the ongoing efforts to optimize energy efficiency in complex systems. Similarly, our paper on the PD-PWM technique for multilevel converters explores innovative strategies to enhance performance and efficiency, demonstrating how advanced control techniques can significantly improve system operation in various applications for railway traction systems. Ref. [20] suggests a multi-port power conditioning (MP-PC) device that uses an architecture based on a full-bridge modular converter (full-bridge MMC). In this application, multilevel converters—like MMC—are essential for ensuring accurate voltage regulation and power balancing while facilitating the smooth integration of renewable energies into the rail network. To enhance power quality in multi-zone railway systems, Ref. [21] focuses on multilevel converters, such as the modular five-branch full-bridge converter (FB5B-MMC).

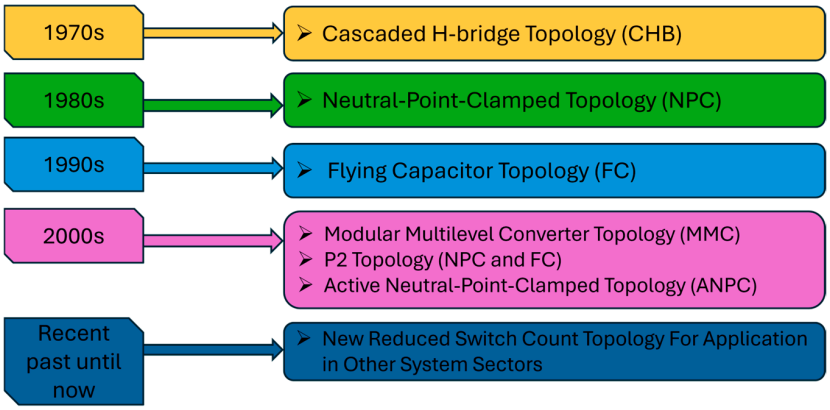


Figure 1. The development of different MLI topologies.

2.1. Diode-Clamped Multilevel Inverter (NPC)

Power conversion systems frequently employ active neutral point (ANP) multilevel converters as their converter topology [18]. The same goal of this kind of converter was initially applied in 1980 to lower the rate at which the converter introduces TDH harmonics into electrical applications. The two topologies—three and five levels—that will be covered in more detail below are depicted in Figure 2.

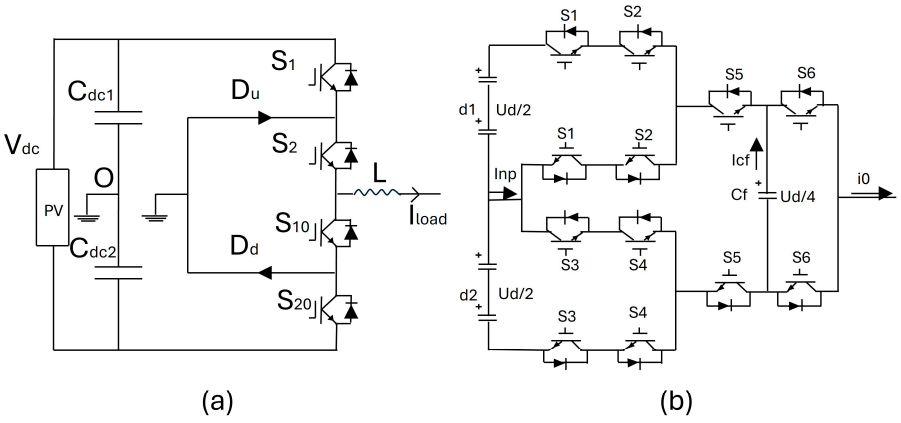


Figure 2. NPC converter: three levels [18] (**a**); five levels [22] (**b**).

For a three-level NPC converter (see Figure 3), we have three possible operating stages giving three different levels, as shown in Table 1.

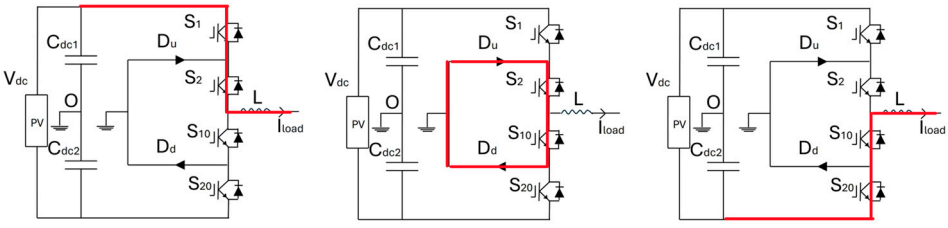


Figure 3. Three different levels of inverter.

Table 1. Possible status of the three-level NPC inverter.

T_1	T_2	T_3	T_4	V_{out}
1	1	0	0	$V_{DC/2}$
0	0	1	1	$V_{-DC/2}$
0	1	1	0	0

We have five possible operational phases, or five separate levels, for the five-level NPC converter. Switch operation details are displayed in Table 2. By eliminating the need for passive filters in this context, thanks to a simple control mechanism, the NPC architecture offers several advantages. These include producing a high-quality waveform from three levels onwards, providing better spectral performance compared to a conventional three-phase inverter [22]. A DC/AC inverter with an LC filter is cascaded with a boost converter to synchronize the grid frequency with the inverter [23]. However, when the number of levels exceeds three, voltage balancing across capacitors becomes increasingly complex, as it is influenced by the load's power factor and modulation index. Consequently, the number of diodes increases unnecessarily with additional levels, making power flow control for each converter more challenging [24].

Table 2. Possible status of the five-level NPC inverter.

S1	S2	S3	S4	S5	S6	S7	S8	V_{out}
1	1	1	1	0	0	0	0	$V_{DC/2}$
0	1	1	1	1	0	0	0	$V_{DC/4}$
0	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	$-V_{DC/4}$
0	0	0	0	1	1	1	1	$-V_{DC/2}$

2.2. Capacitor-Clamped Multilevel Inverter (FC)

As a direct replacement for the NPC architecture, the FC (flying-capacitor multilevel inverter) topology was introduced in 1992 [25]. One benefit of this design is that it can address the issue of loopback diodes in multilevel NPC inverters [26]. The term "flying-capacitor inverter" refers to this topology's usage of capacitors rather than diodes. The drawbacks of diodes, including conduction losses and reliability issues, are removed by using capacitors. The various voltage levels needed for inverter functioning are created in large part by flying capacitors [26]. The architecture of the three-level FC inverters is shown in Figure 4.

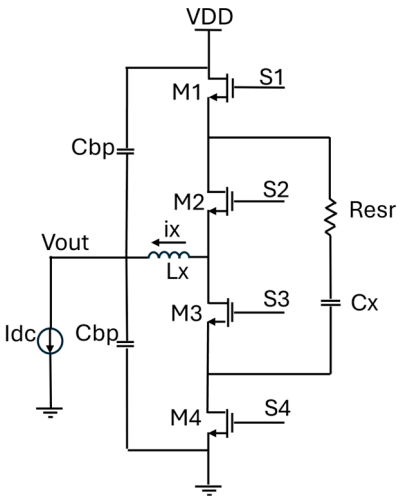


Figure 4. Three-level FC converters [26].

A method for active voltage balancing that makes use of valley current detection and constant effective duty cycle management is presented in the research work conducted by [26]. By balancing the voltage between the capacitors, this technique maximizes the dependability and efficiency of the inverter. A thorough analysis of switched-capacitor inverters, including flying-capacitor inverters, is given in the contribution in [23]. Compared

to conventional NPC inverters, flying-capacitor multilevel inverters have a few advantages. Voltage balancing techniques and a thorough description of these inverters are included in [27–29], which facilitates a better understanding of their functioning and directs future research in this area.

2.3. Cascaded Multilevel Inverter (H-Bridge)

Multilevel inverters frequently employ H-bridge converter topologies. Unidirectional multilevel chargers find applications in electric vehicles [30]. They provide excellent voltage wave quality and great performance. To increase their effectiveness and efficiency, researchers have conducted a few experiments in this regard. For instance, the authors conducted an intriguing study on power balancing in modular multilevel converters and H-bridge cascade converters with an emphasis on imbalanced operations. With a focus on solar system applications, Ref. [31] suggests a novel multilevel inverter topology based on H-bridge cascade converters and the extended quasi-Z-boost current source. There are benefits to this topology in terms of cost, dependability, and efficiency. Paper [6] presents a comparative analysis of multilevel converters, including those based on H-bridge converters. This paper investigates multilevel converter applications, control systems, and both traditional and sophisticated topologies. Ref. [32] provides yet another in-depth analysis of multilevel converters with parallel connectivity. The many topologies of parallel multilevel converters are examined in this review, with an emphasis on the benefits and drawbacks of each. It also looks at these converters' applications and control strategies. A thorough understanding of H-bridge and multilevel converters is provided by Refs. [33–36], which include comprehensive details on topologies, control systems, and related applications.

2.4. Active Neutral-Point-Clamped (ANPC)

The application of active neutral-point-clamped converters, or ANPCs, has increased interest in power conversion. Reduced switching losses and enhanced output wave quality are two benefits of ANPC converters [37,38]. Five-level ANPC converter design and simulation have received a lot of attention in the literature, which shows how promising they are for practical use [39]. Extensive study has also been conducted on the control of active multilevel converters. For instance, a five-level, six-switch ANPC converter has been effectively controlled using sliding mode control. This control strategy produces robustness to disturbances and accurate reference tracking performance, as shown in Figure 5.

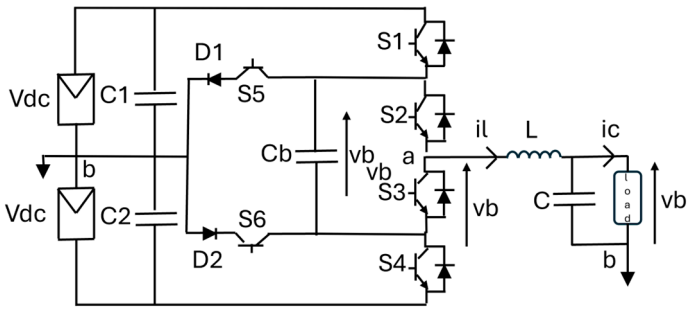


Figure 5. The 6S-5L-ANPC inverter proposed in [39].

Furthermore, Ref. [40] provides an overview of the most recent developments in the multilevel converter sector. The development of active multilevel converter technology was aided by the knowledge and experience those experts and researchers shared. ANPC converters hold great potential as energy conversion solutions. Power electronics researchers are becoming more and more interested in these technologies, as seen by studies into their design, simulation, control, and performance.

2.5. New Topologies with Reduced Commutations

Ref. [41] presents a comparative analysis of reduced-switching multilevel inverter topologies. The authors of this study looked at several inverter topologies and assessed how well they performed in terms of the quantity of switches needed.

Comparably, Figure 6 is a study of multilevel inverter topologies with fewer switches and is provided in Ref. [35]. This paper provides an outline of these novel topologies' benefits as well as the advancements made in the field. The authors of a different publication [42] suggested a new cascaded hybrid inverter with fewer switches by utilizing switched capacitors for home loads and renewable energy sources. This study offers a creative way to cut down on the number of switches required in multilevel inverters. Furthermore, a case study was conducted to build and analyze a new multilevel inverter topology that utilized the PDPWM approach and had fewer switches [43,44]. By lowering the number of switches needed while keeping output quality good, this research helps multilevel inverters operate better. A novel converter topology with nine levels and nine switches and optimal modulation control was introduced by the authors of a different study [45]. The significance of creating novel topologies and cutting-edge modulation approaches to raise inverter quality and efficiency was underlined.

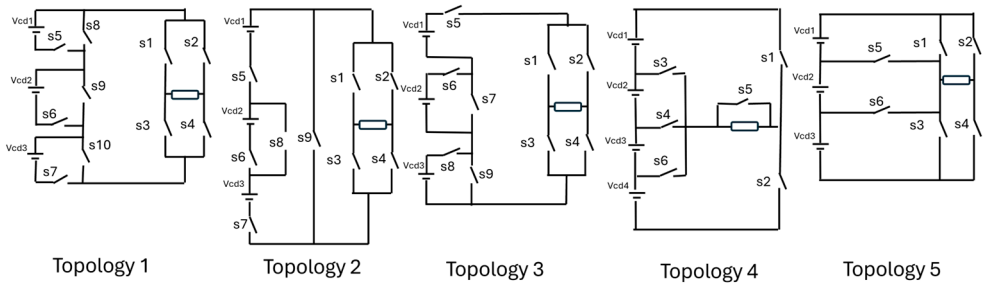


Figure 6. The five topologies proposed by [35].

3. Proposed Topology

3.1. Circuit Description

Multilevel converters with fewer components provide several benefits, such as faster system integration, reduced costs, increased dependency, and simpler control. The suggested example shows that it is possible to achieve high output levels while using the fewest possible components. While having fewer switches often simplifies the design and execution of the control algorithm, reducing the number of switches in a multilevel converter while enhancing performance will give various advantages [46]. One of these advantages is control simplicity. This will help to simplify and maybe strengthen control by facilitating modulation, voltage level management, and switch coordination [47]. Additionally, cutting back on the number of switches helps save the cost of buying, installing, and maintaining individual components [48]. This can be especially helpful in applications where costs are a concern, not to mention the reliability guaranteed, as having fewer components lowers the chance that any one of them would fail, which can raise the system's total reliability [49].

In critical applications where system availability is crucial, this can be especially significant. It may be simpler to integrate a multilevel converter into a larger system by using an architecture with fewer switches for electronic design and component layout [50,51]. The suggested structure, which generates a 19-level output voltage waveform using 9 switches, 5 diodes, and 3 DC power sources, is depicted in Figure 7. Several topologies in the literature, including the CHB-MLI topology, which calls for 36 switches and 9 DC power sources, are not like this method. Unequal DC voltage sources are included in our suggested topology. The "level generation part" is the process of switching S1, S2, S3, S4, and S5 to create

the various levels in the output waveform. The "polarity generation part" is the process of flipping S6, S6′, S7, and S7′ to reverse the polarity of the output waveform. Five diodes (D1, D2, D3, D4, and D5) are also incorporated into the circuit to guarantee appropriate current flow and prevent short circuits.

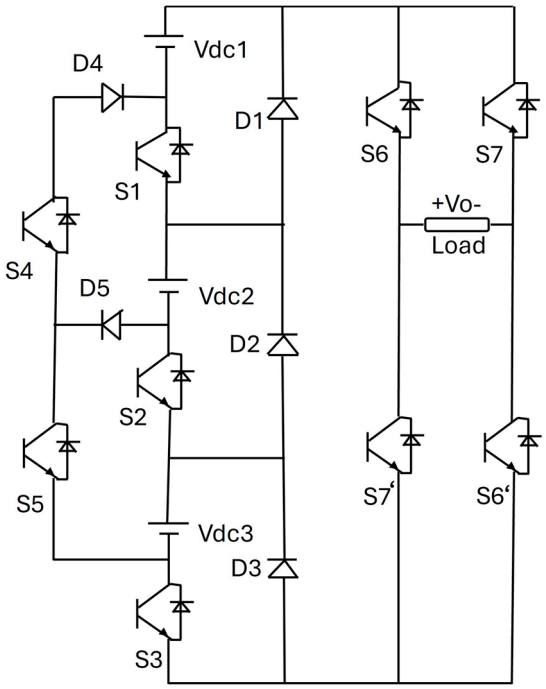


Figure 7. Proposed new topology.

3.2. Operating Modes and States

The various operating modes of the proposed topology are illustrated in Figure 7, which provides an overview of how the circuit operates under different conditions. Each half-cycle—positive and negative—is divided into multiple distinct modes, as detailed in Figure 8(A1–I1) for the positive half-cycle and (A2–I2) for the negative half-cycle. For each mode, the red line in the diagrams indicates the current flow direction, always providing a clear representation of system operation. A complete cycle comprises nineteen distinct operating modes: nine modes during the positive half-cycle, nine modes during the negative half-cycle, and a single mode corresponding to the zero period where no output voltage is generated. Each of these modes is responsible for generating a specific level of the output voltage, thereby enabling the precise control of the multilevel inverter's output waveform. The switching states for all modes are detailed in Table 3, where the binary values "1" and "0" indicate the ON and OFF states of the switches, respectively. Modes 1 to 9 correspond to the positive half-cycle, Mode 10 represents the zero period, and Modes 11 to 19 define the negative half-cycle. A notable feature of the proposed topology is the symmetry in the switching sequence for switches S1, S2, S3, S4, and S5 across both half-cycles, which simplifies the control strategy and ensures consistent performance. Moreover, the complementary operation of switches S6 and S7 is a key aspect of the topology. During the positive half-cycle, switch S6 is active, while S7 remains off. Conversely, during the negative half-cycle, S7 is active, and S6 remains off. This alternating operation not only enhances the efficiency of the circuit but also ensures proper current direction and accurate level generation. The suggested topology's output voltage of nineteen levels will have many benefits, especially for applications that demand harmonic suppression and good output quality. An ideal sinusoid-like output voltage waveform is more closely approximated by a high number of levels. In applications where power quality is crucial, like power

supply systems, this lowers harmonics and enhances voltage quality. It is important to keep in mind that output harmonics can be reduced by using multilevel converters. Lower harmonic distortion levels can be attained by increasing the number of levels, which is crucial for fulfilling power quality requirements. Because multilevel converters can provide output waveforms with cleaner characteristics, they might be more appropriate for use with renewable energy sources like wind turbines and solar panels. The various switching states of the suggested topology are displayed in Table 3, which integrates redundant vectors and should enhance system performance in a few ways, including a decrease in harmonic distortions through improved output waveform optimization, which helps to reduce harmonics and enhance output voltage quality. Through loss distribution and thermal management, switching losses can be distributed more effectively, localized heating can be decreased, and component life can be extended, not to mention that enhanced control flexibility allows the system to apply sophisticated modulation strategies that can be modified to fit specific operating conditions.

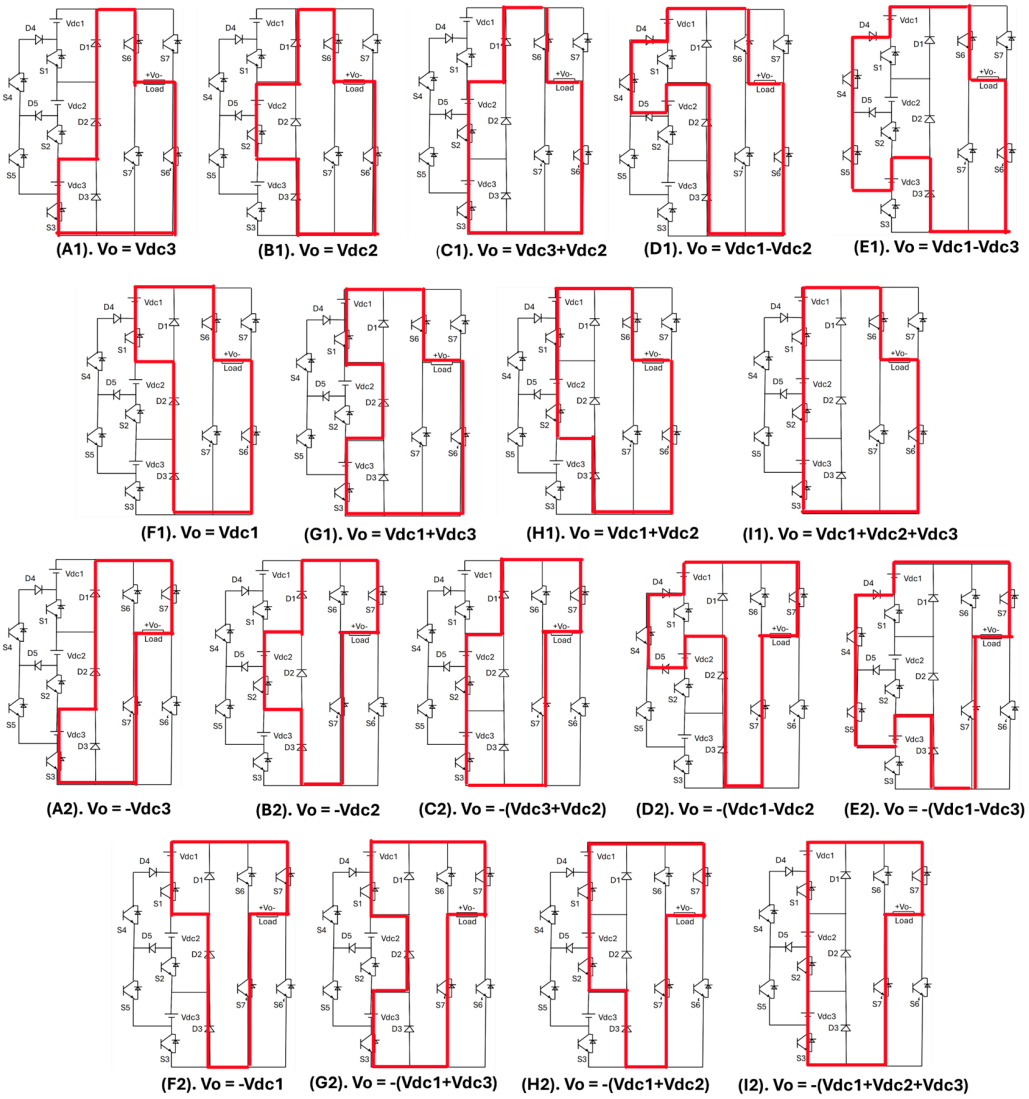


Figure 8. Device conduction states for generating levels during the positive half-period (A1 to I1) and the negative half-period (A2 to I2).

Table 3. The states of the commutations of the proposed topology.

Mode	V_{out}	S1	S2	S3	S4	S5	S6	S7
1	$9E = V_{dc1} + V_{dc2} + V_{dc3}$	1	1	1	0	0	1	0
2	$8E = V_{dc1} + V_{dc2}$	1	1	0	0	0	1	0
3	$7E = V_{dc1} + V_{dc3}$	1	0	1	0	0	1	0
4	$6E = V_{dc1}$	0	0	0	1	1	1	0
5	$5E = V_{dc1} - V_{dc3}$	0	0	0	1	1	1	0
6	$4E = V_{dc1} - V_{dc2}$	0	0	0	1	0	1	0
7	$3E = V_{dc2} + V_{dc3}$	0	1	1	0	0	1	0
8	$2E = V_{dc2}$	0	1	0	0	0	0	1
9	$1E = V_{dc3}$	0	0	1	0	0	1	0
10	0	0	0	0	0	0	0	0
11	$-1E = -V_{dc3}$	0	0	1	0	0	0	1
12	$-2E = -V_{dc2}$	0	1	0	0	0	0	1
13	$-3E = -(V_{dc2} + V_{dc3})$	0	1	1	0	0	0	1
14	$-4E = -(V_{dc1} - V_{dc2})$	0	0	0	1	0	0	1
15	$-5E = -(V_{dc1} - V_{dc3})$	0	0	0	1	1	0	1
16	$-6E = -V_{dc1}$	0	0	0	0	0	0	1
17	$-7E = -(V_{dc1} + V_{dc3})$	1	0	1	0	0	0	1
18	$-8E = -(V_{dc1} + V_{dc2})$	1	1	0	0	0	0	1
19	$-9E = -(V_{dc1} + V_{dc2} + V_{dc3})$	1	1	1	0	0	0	1

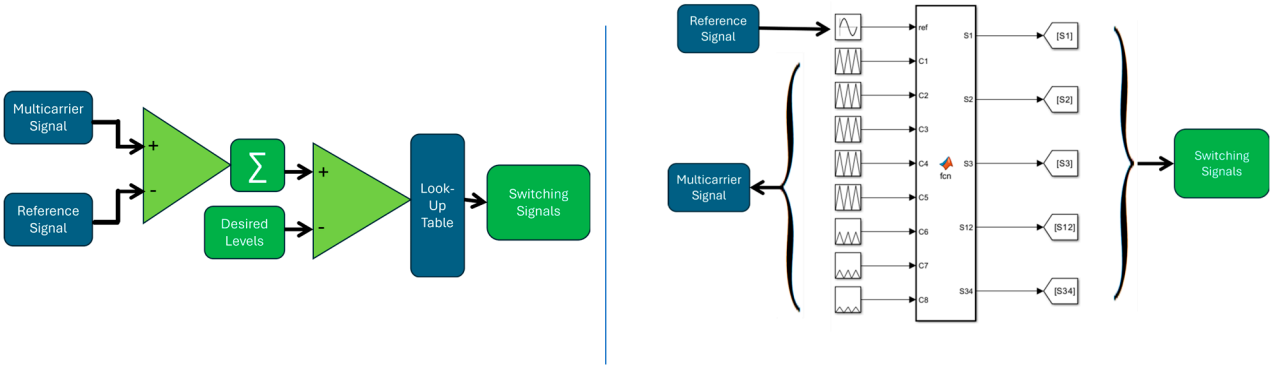
3.3. The PD-PWM Control Strategy

Derivative converter modulation technique selection is based on application requirements, including control complexity, output quality, reaction time, and efficiency. Simpler techniques like PWM or SPWM [52] are appropriate for general-purpose applications whereas more sophisticated techniques like SVPWM or PSM are better for high-efficiency systems. Designing an ideal system requires an understanding of the trade-offs.

The modulation approach selected has a direct impact on how effective the suggested remedy is. The phase-disposition modulation (PD-PWM) technique was chosen following a careful analysis [53]. Power switches in multilevel inverters are frequently inspected using this method. The phase and frequency of the triangle carriers are maintained constant in the PD-PWM that is used [42]. Phase-disposition pulse width modulation (PD-PWM) is a widely used modulation technique in multilevel inverters due to its simplicity and effectiveness in generating high-quality output voltages. In PD-PWM, all carrier signals are aligned in phase and distributed uniformly across the amplitude range of the reference signal. For a 19-level inverter, 18 carrier signals are used, each corresponding to a voltage step in the inverter. These carriers are compared with the reference sinusoidal waveform to produce switching signals that control the power switches in the inverter. The primary role of PD-PWM in a 19-level multilevel inverter is to achieve a high-resolution output voltage with minimal distortion. By aligning the carriers in the same phase, PD-PWM effectively reduces low order harmonics, resulting in a significant improvement in the power quality of the output.

This is particularly important in high-power applications, where total harmonic distortion (THD) must be minimized to meet stringent standards. The high number of levels naturally lowers THD, and PD-PWM further enhances this by ensuring smooth transitions between voltage levels. Additionally, PD-PWM simplifies the implementation process, especially in digital control platforms like DSPs or FPGAs, reducing computational complexity and making it ideal for efficient and reliable operation. The PD-PWM technique was first implemented and tested in MATLAB/Simulink R2024b to validate its performance in controlling a 19-level multilevel inverter like in Figure 9. The model comprised a sinusoidal reference signal and 18 uniformly distributed carrier signals aligned in phase.

These carriers were compared to the reference waveform using logical comparison blocks to generate switching signals for the power electronic switches in the inverter. The inverter topology employed in the simulation was a cascaded H-bridge configuration, with each H-bridge connected to a DC source. The stepped output voltage waveform produced by the inverter closely approximated a sinusoidal waveform, significantly reducing harmonic content. Performance analysis was conducted using Fast Fourier Transform (FFT) tools to evaluate the total harmonic distortion (THD).



(**a**) (**b**)

Figure 9. PD-PWM control: block diagram [54] (**a**); PWM in MATLAB with function (**b**).

The PD-PWM technique was selected for this work due to its simplicity of implementation in controllers and its excellent compatibility with multilevel inverter topologies. Compared to more advanced methods such as Space Vector PWM (SVPWM), PD-PWM offers reduced computational complexity, fast real-time performance, and effective harmonic suppression, making it particularly suitable for hardware-constrained applications.

Figure 10 shows our reference signal compared with the 18 carriers we used. The PD-PWM method demonstrated excellent harmonic mitigation, with results showing a low THD and improved output voltage quality. Various scenarios, including changes in load, modulation index, and carrier frequency, were simulated to assess system stability and efficiency. The results confirmed the robustness of the PD-PWM technique in ensuring smooth transitions between voltage levels and maintaining stable operation across different operating conditions. This section provides a comprehensive overview of the proposed circuit, its various operating modes, and the control strategy based on PD-PWM.

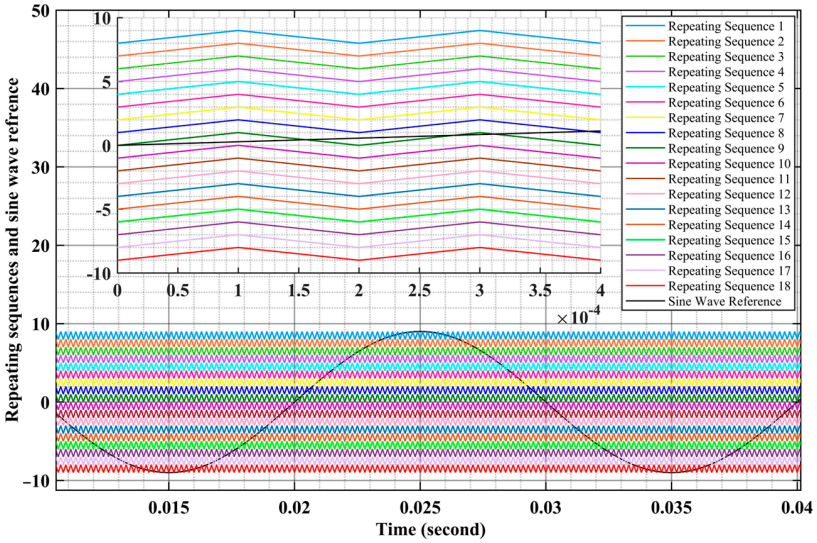


Figure 10. PD-PWM.

3.4. Total Harmonic Distortion (THD) and MTTF Calculation

Total harmonic distortion (THD) is an important metric for assessing the caliber of the inverter output voltage. It is described by the following expression and quantifies the existence of harmonic components in relation to the fundamental component. In [55], the following equation defines it:

$$\text{THD} = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{\text{V1}} * 100\% \quad (1)$$

where V_n is the RMS value of the output voltage's nth harmonic component and V_1 is the RMS value of the fundamental component, which is usually 50 Hz.

Increasing the number of voltage levels in multilevel inverters, especially those that use phase-disposition PWM (PD-PWM), greatly enhances the approximation of a sinusoidal waveform, which lowers harmonic content. A condensed estimate of THD under optimal circumstances is as follows:

$$\text{THD} = \frac{1}{\sqrt{(2m-1)}} \quad (2)$$

where *m* is the output waveform's number of voltage levels. This demonstrates that THD falls as *m* rises, which is consistent with our design objective.

This work's goal is to provide a novel multilevel inverter topology that achieves a very low THD while reducing the number of components. Reduced motor and transformer losses, less electromagnetic interference, and increased system dependability and efficiency are just a few advantages of lower THD. These features are especially beneficial for applications involving renewable energy and industry.

THD reduction offers several benefits, including less electromagnetic interference, which improves inverter stability; less strain on electronic components, which extends their lifespan; and reduced motor and transformer losses, which boost efficiency. Because of these improvements, our architecture is particularly suitable for industrial and renewable energy applications where minimizing harmonic distortion is necessary to maximize system efficiency. This study shows that, in comparison to traditional options, our design significantly reduces THD due to improved switching control and an optimized component count.

This analytical expectation is supported by the experimental and simulated data shown in Section 5. When compared to traditional structures, our suggested topology shows a significant decrease in THD, confirming the efficiency of the control technique and the optimized architecture.

Our topology has a lower failure rate since it requires fewer components. And longer life and improved robustness result from having fewer MOSFETs and capacitors. In [56], a converter's failure rate is often calculated by adding the failure rate of its essential parts:

$$\lambda_{total} = \sum_{i=1}^{n} \lambda_i \quad (3)$$

where the failure rate of the i-th component (MOSFET, diode, capacitor, inductor, etc.) is represented by λ_i. The topology's total number of components is denoted by n.

The following formula can be used to determine the Mean Time to Failure (MTTF) after the overall failure rate (λ_{total}) has been determined:

$$MTTF = \frac{1}{\lambda_{total}} \quad (4)$$

where *MTTF* is expressed in hours.

These component failure rates are typically represented as "Failures In Time," or FIT, which is the number of failures per 10^9 h of operation. These figures are derived from standard approximations for electronic power parts:

- MOSFETs: λ(MOSFET) = 50 FIT;
- Diodes: λ(diode) = 20 FIT;
- Capacitors: λ(Capacitors) = 5 FIT;
- Inductors: λ(inductor) = 2 FIT.

To compare the failure rate of our topology with that of traditional topologies, we find the following:

- MTTF for CHB topology (36 MOSFETs, 0 diodes): 555,556 h;
- MTTF for NPC topology (36 MOSFETs, 306 diodes): 126,263 h;
- MTTF for FC topology (36 MOSFETs, 153 capacitors): 389,864 h;
- MTTF for our proposed topology (9 MOSFETs, 3 diodes): 1,960,784 h.

Our suggested topology provides a lifetime that is 3.5 times longer than that of the CHB topology, almost 15 times longer than that of the NPC topology, and 5 times longer than that of the FC topology.

This demonstrates how our topology decreases the number of crucial parts (capacitors, diodes, and MOSFETs), significantly lowering the failure rate and boosting system dependability.

4. Hardware-in-the-Loop

Hardware-in-the-loop (HIL) simulation or testing is a method utilized in the development and testing of intricate process systems [57]. HIL simulation offers an efficient platform by integrating the complexity of the controlled plant into the testing environment. This complexity is introduced into the test and development phases by incorporating a mathematical representation of all relevant dynamic systems, known as the "plant simulation". The HIL process has been in existence for less than 15 years. The increasing adoption of the HIL process across industries is primarily propelled by two key factors: time to market and system complexity. HIL simulation constitutes a form of real-time simulation where input and output signals exhibit time-dependent values identical to those of the actual process. HIL necessitates collaboration between the host and target systems. Typically conducted in laboratory settings, HIL is employed on the ground to conveniently and safely evaluate prototype controllers under various operational loads and conditions. The system is controlled by the DSP F28379D board [58].

The real-time implementation of the PD-PWM control strategy was carried out using the TMS320F28379D digital signal processor (DSP) and validated via a hardware-in-the-loop (HIL) platform. The PD-PWM logic developed in Simulink was converted to C code using Embedded Coder and loaded onto the DSP. The HIL system emulated the physical inverter and load, providing a safe and controlled environment to test the PD-PWM algorithm under realistic conditions.

The DSP and the PWM modules were utilized to generate high-resolution switching signals, which were fed into the HIL platform. The real-time feedback from the HIL system, including voltage levels, harmonic distortion, and dynamic responses, enabled fine-tuning of the PD-PWM algorithm. The results showed that the technique effectively minimized THD, maintained voltage balance across the inverter stages, and ensured stable performance under varying operating conditions. Figure 11 demonstrates the schematic of the system proposed using HIL.

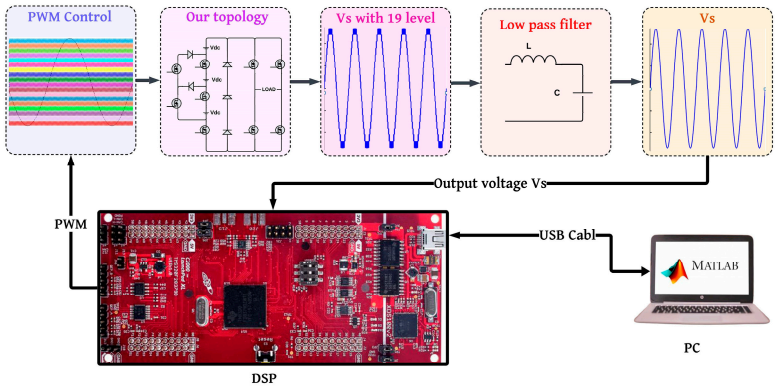


Figure 11. The proposed system using HIL.

The hardware-in-the-loop (HIL) approach, utilizing the DSP F28379D, is instrumental in controlling a multilevel converter using the PD-PWM technique. The DSP F28379D, with its dual-core architecture and high-resolution PWM capabilities, acts as the real-time controller, enabling the precise modulation of pulse width signals. To implement HIL with MATLAB-Simulink R2024b, follow these steps:

1. Model Development in Simulink: Begin by creating a detailed Simulink model of the multilevel converter and the PD-PWM control algorithm. Ensure that the model includes all relevant components, such as the converter topology, switching signals, and control logic.
2. Code Generation: Use MATLAB's Embedded Coder to generate C code from your Simulink model. This code will be deployed onto the DSP F28379D. Configure the code generation settings to match the target hardware specifications, including the processor 306 type and peripheral interfaces.
3. Configure DSP with Code Composer Studio (CCS): Open the generated code in Code Composer Studio (CCS), the integrated development environment for the DSP F28379D. Set up the project in CCS, configuring the DSP's CPU cores, clock settings, and peripherals (such as the ADC for sensor inputs and the PWM module for controlling the converter).
4. Simulink Real-Time Interface: Establish communication between MATLAB-Simulink and the DSP F28379D by setting up the Simulink Real-Time (SLRT) or external mode. This allows you to run the Simulink model in real-time while monitoring and tuning parameters on the fly.
5. HIL Simulation: Connect the DSP F28379D to the PC running MATLAB-Simulink via a JTAG debugger (Texas Instruments, Dallas, TX, USA) or USB interface. Start the HIL simulation, where the DSP controls the multilevel converter model running in Simulink. The DSP processes real-time data from the model, and the PWM signals are generated and fed back into the simulation, allowing for closed-loop testing.
6. Testing and Validation: Monitor the system's performance in real-time through Simulink. Adjust control parameters as needed to optimize performance. Validate the control strategy by comparing the HIL results with the expected outcomes from the purely simulated model.
7. Iterative Refinement: Make sure the control algorithm satisfies performance objectives, such as lowering total harmonic distortion (THD) and speeding up response time, by using input from HIL testing. The system will be prepared for deployment in a real-world setting after validation.

This process ensures that the control strategy for the multilevel converter is rigorously tested and optimized in a safe and controlled environment before being applied to actual hardware, minimizing risks and improving system reliability.

5. Results and Discussion

5.1. Simulation Results

The simulation of the proposed topology was carried out in the MATLAB/Simulink environment on an Intel CORE i7 10TH GEN to study and compare its performance. Table 4 shows the parameters chosen for the simulations, as well as the modulation carried out using the PD-PWM strategy, with a fundamental frequency of 50 Hz used for the reference, to use 18 carriers of 5 kHz. Figure 12 shows the reference and control signal using the PD-PWM strategy for switches S1, S2, S3, S4, and S5. Hybrid bridges S6 and S7 control four switches at the same time, two switches for each bridge.

Table 4. Simulation parameters.

Fundamental Frequency	Load	DC	Carrier Frequency
50 Hz	10 Ω	V_{dc1} = 180 V V_{dc2} = 60 V V_{dc3} = 30 V	5 kHz

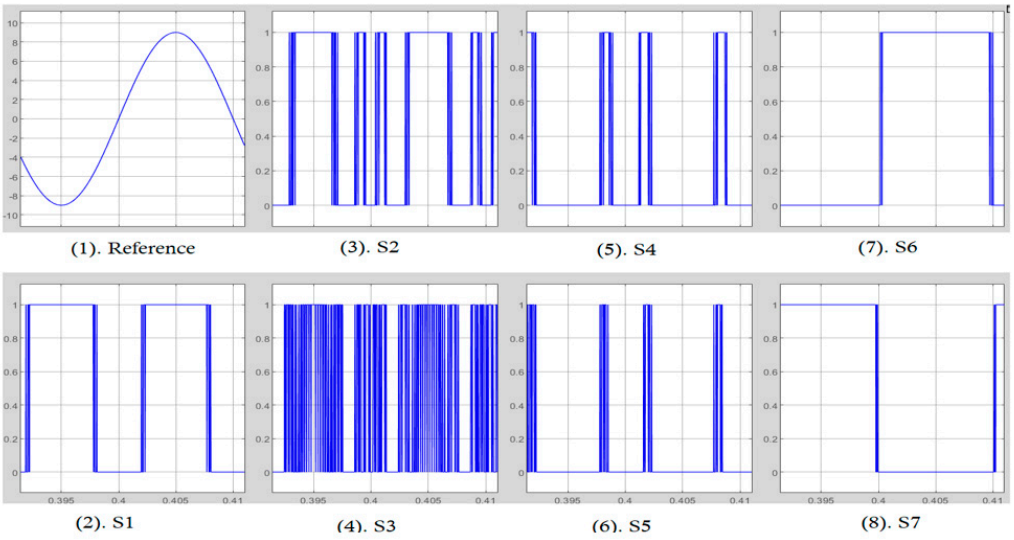


Figure 12. Gate sequence across the switches for 19-level inverter (2, 3, 4, 5, 6, 7, and 8). Switching control of S1, S2, S3, S4, S5, S6, and S7.

In conducting a comprehensive examination of the proposed new topology, our initial step involved a thorough comparison with 19-level CHB-MLIs under identical conditions to those of our topology. To energize the CHB-MLIs, we employed nine DC sources, each boasting a voltage rating of 30 V. Accompanying this setup were 36 switches, as depicted in Figure 13, portraying the schematic layout of the CHB converter necessary to achieve 19 levels. The depiction of this converter schematic not only reveals the intricacies of the circuit but also underscores the considerable number of components involved, including the 36 switches and 9 DC voltage sources.

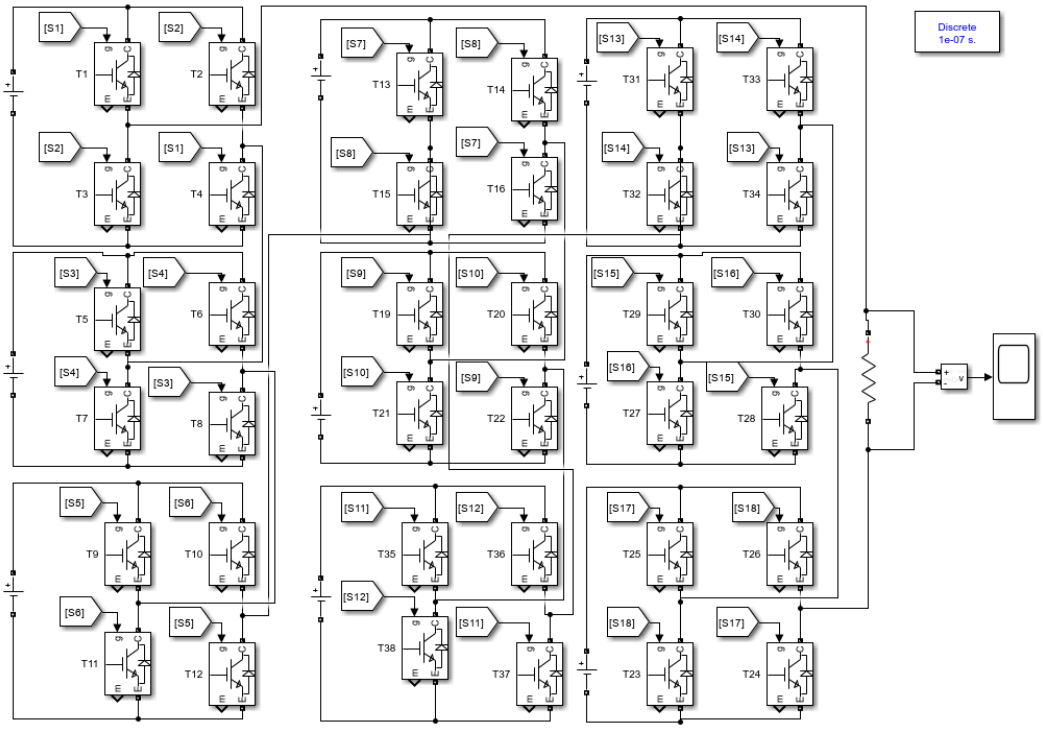


Figure 13. The simulation of CHB converter-19L on MATLAB Simulink.

The complexity of the circuitry, coupled with the substantial count of components, poses significant challenges in both operation and implementation, particularly concerning cost and maintenance considerations. Managing such a circuit demands meticulous attention to detail and incurs notable expenses, not only in terms of initial setup but also in ongoing maintenance requirements. Thus, while the 19-level CHB-MLI configuration may offer certain advantages, its practical realization remains daunting due to its inherent complexity and the associated logistical challenges.

Figure 14 shows the simulation of the new topology, in which only nine switches and three DC power sources (30 V, 60 V, and 180 V) were used to implement a 19-level converter.

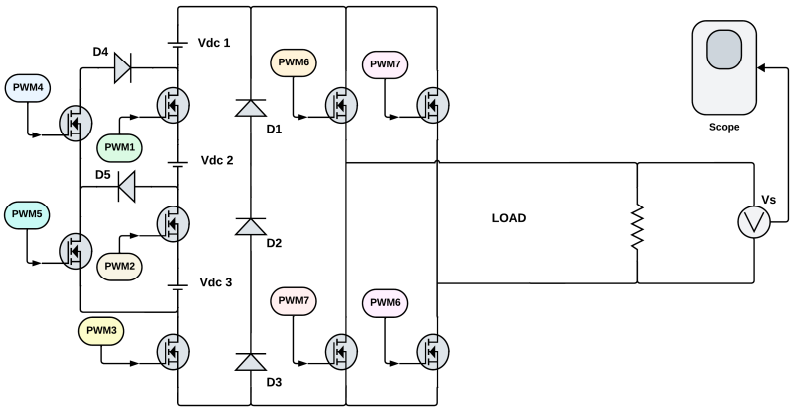


Figure 14. The simulation of our new topology on MATLAB Simulink 19L.

Figure 15 provides a visual representation of the simulated models for both the conventional CHB-MLI and the newly proposed topology. These models depict the output voltage waveforms, offering insights into their respective performance characteristics. Additionally, accompanying the visual representations, FFT (Fast Fourier Transform) analysis was conducted, revealing the frequency spectrum of the output signals. This comprehensive analysis aids in assessing the efficacy and suitability of the proposed topology compared

to the established CHB-MLI configuration. This significant reduction in the number of components makes the solution feasible and testable, and we note that the output voltage reaches its maximum 269.2 V and a THD% of 6.23%.

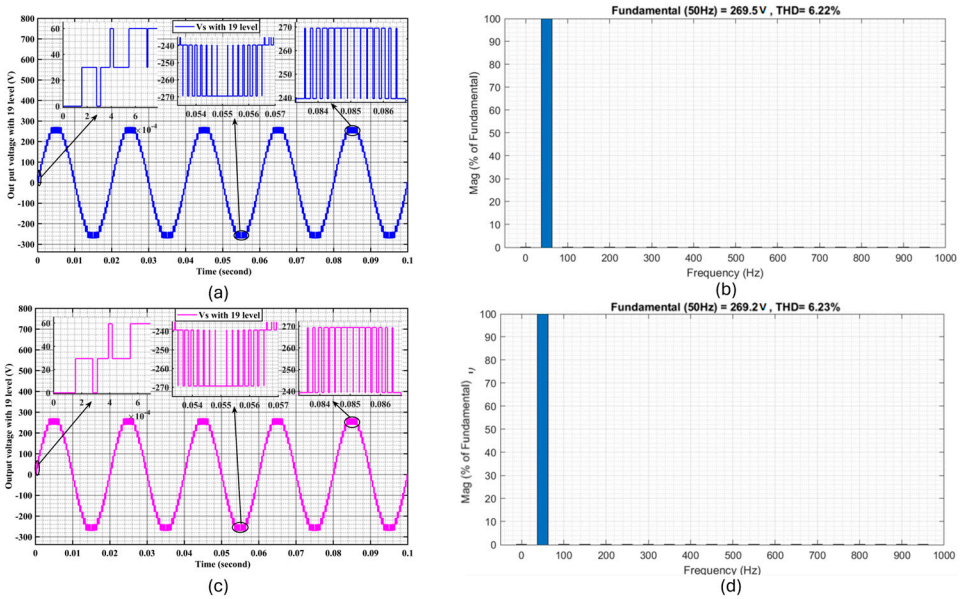


Figure 15. Comparison between the results of the 19-level inverter implemented with CHB and the 19-level inverter using our topology: output signal of CHB (**a**); THD% of CHB (**b**); output signal of the new topology (**c**); THD% of the new topology (**d**).

5.2. Improving Performance

In enhancing the output signal quality as referenced in [41,42], our strategy involves the incorporation of an LC output filter. When a single-phase converter is coupled with an LC output filter, as shown in Figure 16, it can be characterized by a set of differential equations. The fundamental principle underlying an LC low-pass filter mirrors that of an RC low-pass filter, albeit utilizing an inductor (L) and a capacitor (C).

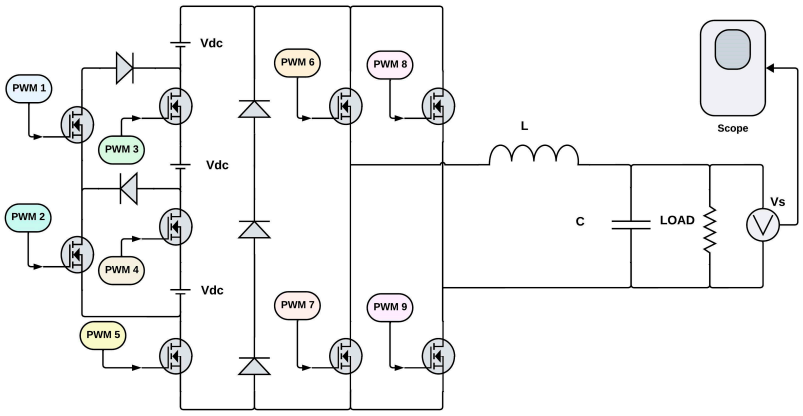


Figure 16. Our new technology with integrated LC filter.

Often referred to as a second-order low-pass filter, this configuration is commonly utilized for attenuating high-frequency components from a signal, thereby refining the overall output waveform fidelity and reducing unwanted noise interference.

$$Z_{RC} = \frac{Z_R * Z_C}{Z_R + Z_C} = \frac{R}{1 + j\omega RC} \tag{5}$$

$$Z_L = j\omega L \tag{6}$$

The signal can flow through the filter with little attenuation at low signal frequencies because the Zc capacitor's impedance is large in comparison to the ZL coil's impedance. However, the Zc capacitor's impedance decreases with increasing frequency, allowing the filter to block high-frequency signals.

$$\frac{V_s}{V_e} = \frac{Z_{RC}}{Z_{RC} + Z_L} = \frac{1}{1 + j\frac{\omega}{\omega_0}} \equiv \frac{\mathrm{A}}{1 + j\frac{\omega}{\omega_0}} \tag{7}$$

with

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{8}$$

In our proposal, we assume an ideal generator scenario where the generator is considered perfect. Specifically, we assume a resistance value of R = 50 Ω. In this context, the transfer function, a crucial aspect of system characterization, is frequently depicted in various representations for analytical purposes:

$$\frac{di^2}{dt^2} + \frac{Rdi}{Ldt} + \frac{1}{LC}i = 0 \tag{9}$$

Solution:

$$i(t) = [A\ cos(\omega st) + B\ sin(\omega st)]\ exp(-\mu t) \tag{10}$$

We suppose μ high oscillation in 1 ms:

Then,

$$L = \frac{RQ}{\omega_0} = 2\ *\ 10^{-2} H \tag{11}$$

and

$$C = \frac{1}{RQ\omega_0} = 2\ *\ 10^{-8} \tag{12}$$

where

- V_s is the filter output voltage.
- V_e is the filter input voltage.
- L is the inductance.
- C is the capacitance.
- R is the resistance.
- ω_0 is the natural angular frequency.
- ω is the angular frequency of the signal.
- Q is the quality factor.
- μ is the damping coefficient.
- i(t) is the current.

A continuous control law cannot be designed using the converter's discrete output signal, which has nineteen possible values. To resolve this issue and facilitate management of the system being examined, the average model of the proposed topology can be expressed in Figure 17.

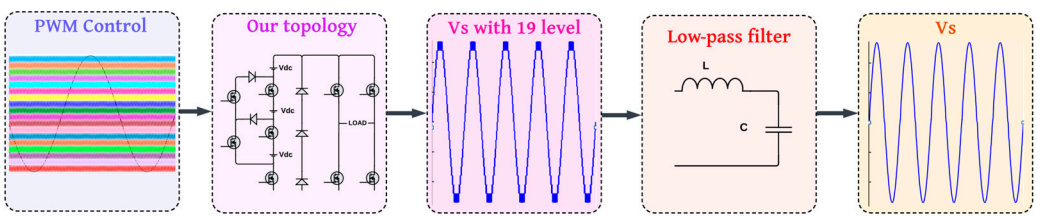
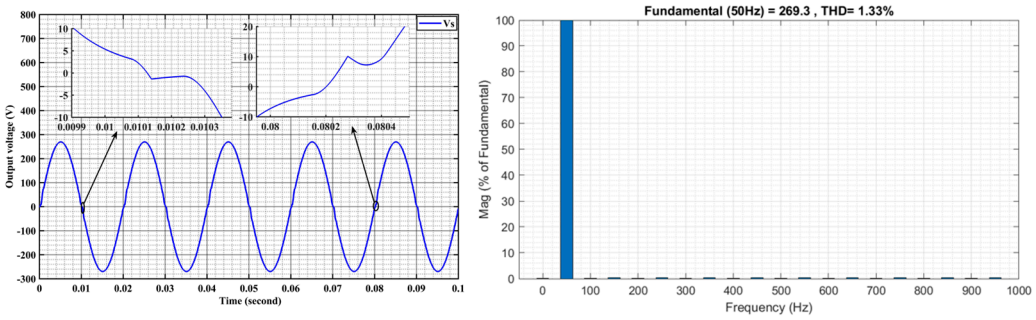


Figure 17. LC filter integration.

The considerable alteration observed in the percentage of total harmonic distortion (%THD) after the integration of an LC filter is clearly shown in Figure 18. This strategy proves both practical and rational for reducing harmonic content and improving the fidelity of the output signal.



(a) (b)

Figure 18. Output signal after low-pass filter integration (**a**); THD% (**b**).

5.3. Experimental Validation Using HIL with DSP F28379D

To validate the proposed 19-level inverter topology under realistic operating conditions, a hardware-in-the-loop (HIL) platform was employed using the Texas Instruments DSP TMS320F28379D (Texas Instruments, Dallas, TX, USA). This experimental setup enabled the testing of the PD-PWM control strategy and real-time performance analysis of the system while ensuring safety and flexibility in tuning the control parameters.

Figure 19 presents the experimental output waveform measured during the HIL. The blue curve represents the signal generated by the 19-level inverter and includes high-frequency components and slight irregularities, effectively simulating the real-world behavior of the converter. The red dashed line shows the ideal sinusoidal reference, used as a benchmark. As can be observed, the experimental signal closely follows the reference, reaching a peak amplitude of approximately 311 V, which confirms that the inverter produces a nearly ideal single-phase AC voltage.

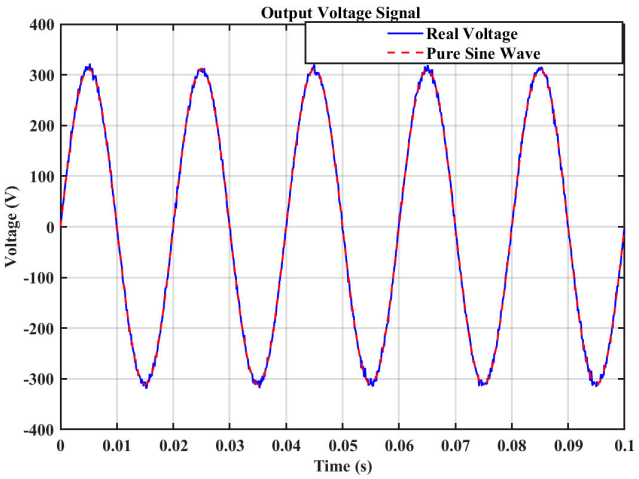


Figure 19. Experimental output waveform measured during the HIL.

Minor fluctuations around the waveform crest and trough are attributable to real-time switching events and measurement noise, which are typical in practical inverter operation. This behavior further confirms the effectiveness of the PD-PWM strategy, which was implemented on the DSP using Embedded Coder from MATLAB/Simulink and loaded via Code Composer Studio (CCS).

The HIL validation demonstrates

- The accurate tracking of the reference waveform with minimal deviation;
- The reliable generation of 19 discrete levels with proper voltage shaping;
- Realistic experimental behavior replicating practical inverter operation.

These results confirm that the proposed topology is not only functionally viable in simulation but also performs robustly when tested in a real-time embedded environment, achieving low total harmonic distortion (THD) and meeting voltage output quality standards.

To further evaluate the waveform quality, an FFT-based harmonic analysis was conducted on the output voltage captured during the HIL test. The spectrum revealed a strong fundamental component at 50 Hz, with an amplitude close to 269.3 V. Additional harmonics—primarily, the 3rd, 5th, and 7th—were present, reflecting typical switching-related distortions. The total harmonic distortion (THD) was calculated to be approximately 2.20% in Figure 20, confirming that the multilevel structure combined with the PD-PWM control technique successfully generates a high-fidelity voltage waveform suitable for power quality-sensitive applications. The comparison of simulation results (before and after the addition of an LC filter) with experimental data derived from the HIL platform with a DSP controller is summarized in Table 5. With only a minor increase in peak voltage, the data clearly demonstrates that the installation of an LC filter lowers the THD% from 6.2% to 1.3% in simulation. The THD% in the experimental setup is 2.2%, which is still quite near to the simulated value and validates the usefulness of the suggested topology and filtering approach to non-optimal parts and parasitic effects in the hardware.

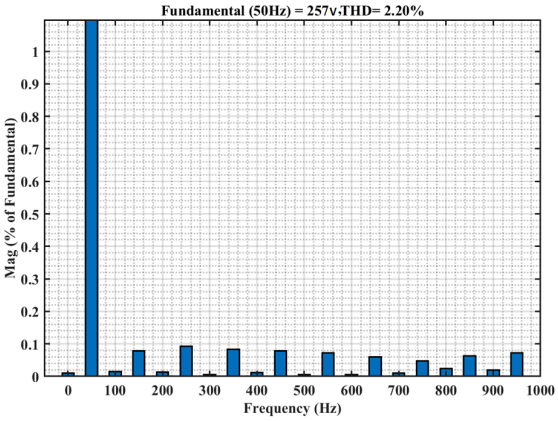


Figure 20. THD of experimental result.

Table 5. Simulated and experimental results (with and without LC filter) are compared.

Parameter to Be Compared	Before Adding an LC Filter	After Adding an LC Filter	Experimental Using HIL with DSP
THD%	6.2%	1.3%	2.2%
Peak (V)	269.2 V	269.3 V	257 V

Table 6 and Figure 21 compare and evaluate various multilevel converter topologies. This analysis clearly shows that our proposed topology is the best. With only a few switches required, it provides 19 levels. Clearly, when the number of levels is considerable, other topologies require many more components than the CHB, NPC, and FC topologies. That is why they are difficult, if not impossible, to implement, and for the NPC and FC topologies, we could not even run the simulation to compare them, given the large number of diodes, capacitors, and DC sources. Refs. [51,52,59,60] used almost the same number of switches, even though they had more components—our topology has the lowest THD%.

Our topology is therefore distinguished by the following features: very low THD (total harmonic distortion), even with many levels; optimal use of components, such as diodes and capacitors, limiting hardware requirements; and fewer switches, simplifying design and reducing costs. With its high efficiency and low harmonic distortion, the suggested multilevel inverter topology is especially ideal for new applications in plug-in hybrid electric vehicles (PHEVs) and electric vehicles (EVs), where system compactness and power quality are crucial needs [61].

Table 6. Comparison between different MLI topologies.

Topologies	N_{LEVELS}	N_{DC}	N_S	N_D	N_C	THD%
CHB-MLI	19	9	36	0	0	6.20%
NPC [4]	19	18	36	306	0	-
FC [5]	19	18	36	0	153	-
[51]	19	2	9	6	2	7.40%
[52]	19	2	8	4	0	7.19%
[62]	15	3	7	3	0	3.02%
[59]	19	3	13	0	0	3.89%
[60]	19	2	13	0	2	3.61%
[63]	17	2	12	0	4	4.83%
[64]	17	2	8	0	2	8.49%
[65]	15	4	12	0	0	5.50%
[66]	15	4	12	0	0	6.09%
[67]	7	1	8	1	2	5.68%
[68]	9	4	10	0	0	19.6%
[69]	11	1	12	0	2	-
[70]	21	4	12	0	0	12.64%
[71]	15	3	10	0	0	5.45%
[72]	21	3	10	0	0	3.49%
Proposed	**19**	**3**	**9**	**5**	**0**	**1.33%**

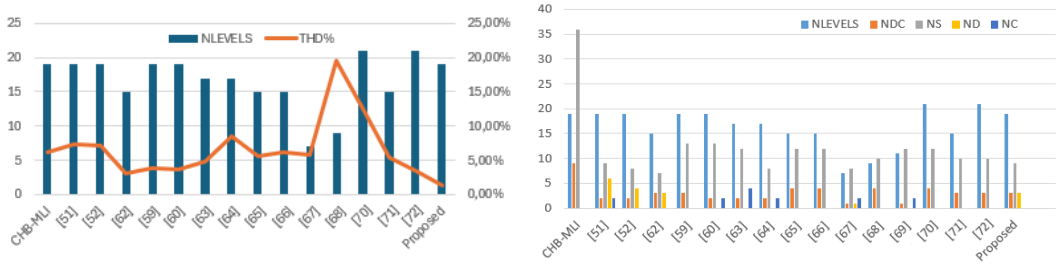


Figure 21. A graphical comparison of topology types [51,52,59,60,62–72].

6. Conclusion and Perspectives

This study presents a revolutionary multilevel converter architecture that can produce an output waveform with 19 levels. The suggested topology, which is managed by the PD-PWM technique, significantly reduces the total system complexity and the number of power switches needed, which lowers implementation costs and simplifies control. This novel converter's whole design and operation were thoroughly documented, and MATLAB Simulink simulations were used for rigorous validation. Additionally, the feasibility of implementing the suggested architecture in hardware was confirmed by experimental validation using HIL with DSP F28379D, which is a crucial step towards practical deployment. To further improve output voltage accuracy and system stability, future work will concentrate on creating a comprehensive closed-loop control system that can dynamically optimize converter settings in response to operating conditions. Overall, the study's findings show

that the suggested topology, which combines a lower component count, superior output, and outstanding adaptability for real-world uses, is a promising option for next-generation multilevel inverters.

Performance is further improved by adding a low-pass LC filter, which lowers the output voltage's THD to 1.33%.

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Abbreviations

PD-PWM	Phase-disposition pulse width modulation
CHB-MLI	Cascaded H-bridge multilevel inverter
THD	Total harmonic distortion
NPC	Diode-clamped multilevel inverter
CHB	Cascaded multilevel inverter
FC	Flying capacitor topology
ANPC	Active neutral-point-clamped
MLI	Multilevel inverter
PV	Photovoltaic

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