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Overlap Time Compensation and Characteristic Analysis for Current Source Photovoltaic Grid-Connected Inverter

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Abstract: In the current source photovoltaic grid-connected system, to prevent the DC-link inductor from incurring an opening circuit fault, it is necessary to include the overlap time in the switching signals. However, current error and serious harmonic distortion in the inverter-side and grid-side currents are generated, which will cause additional losses and reduce the power quality of the grid, so it is important to compensate for the current error caused by the overlap time. In this paper, the relationship between the nonlinear current errors caused by the overlap time and the AC-side voltage is analyzed. Then, the mathematical expression of the low-order harmonics with losses caused by the overlap time is derived. On this basis, a current error compensation method with a discrete filter of AC-side voltage is proposed. Finally, a simulation and experiment are carried out to verify the correctness and effectiveness of the theoretical analysis and compensation scheme presented in this paper. With an overlap time of 3 μs, the THD of the grid-side current decreases from 5.93% to 1.59% after compensation.

Keywords: current source inverter; overlap time; harmonic distortion; compensation scheme

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1. Introduction

Solar energy is widely used in the sustainable and environment-friendly power generation field [1]. Due to the simple structure and mature control technology, a voltage source inverter (VSI) is commonly adopted in the photovoltaic (PV) grid-connected system [2]. However, the VSI is a buck inverter, which requires the DC input voltage to be higher than the peak of the AC output voltage [3]. Therefore, on cloudy or rainy days, the output voltage of the PV cells reduces, the operation of the system stops, and the utilization rate decreases [4]. To address the problem that the input voltage is insufficient, the boost converter or the transformer needs to be added [5,6].

Compared with the VSI, the current source inverter (CSI) is a boost inverter [7,8], so only a single-stage CSI can realize the whole process of light utilization from weak to strong [9,10]. The DC-link inductor of CSI is series connected with the PV cells, so the input current is continuous and controllable, which is convenient in realizing maximum power point tracking (MPPT) [11,12]. The CSI is capable of overcurrent protection, so the reliability is higher than that of the VSI [10,13]. Meanwhile, the operation time of the CSI is longer than that of the VSI [14,15]. Based on the above advantages, CSI is more suitable for the PV grid-connected system [16].

To prevent the short circuit fault, the dead time needs to be added during the modulation process in the VSI [17,18]. Since the dead-time causes the distortion of the inverter output voltage and the gird-side current [19], many compensation schemes for VSI have been proposed to suppress the deadtime effect, such as pulse duration compensation [20], average voltage compensation [21], and adaptive harmonic compensation [22]. Different from VSI, the shoot-through is a normal switching state of the CSI, but the open circuit

state is not allowed to occur in the CSI; otherwise, high dv/dt will appear in the DC-link inductor and lead to a serious fault in the system. To prevent the open circuit fault in the CSI, it is imperative to introduce a turn-off delay into all switching signals. At this time, two switching signals remain in the on-state simultaneously, and this is named overlap time [23–25]. The nonlinear error of the inverter-side current is generated by the overlap time, which leads to the distortion in the grid-side current. However, the harmonic suppression schemes caused by the overlap time for CSI have rarely been reported. In [24], under the consideration of the influence of the snubber capacitor and the parasitic inductor, the dynamic commutation process of CSI during the overlap time is analyzed in detail, but no specific scheme to suppress the overlap time effect has been presented. According to the relations of the AC-side voltages, the positive and negative sawtooth waves are alternately adopted as the carrier wave in [25]; although the number of the overlapping time sequence can be reduced, the overlapping time effect has not been eliminated. Reference [23] proposes a compensation method for the dwell time of the current vectors according to the AC-side voltages. Reference [26] proposes a current feedforward compensation method in two-phase stationary coordinates. However, the above two methods require high voltage sampling accuracy; otherwise, error compensation may occur. In reference [27], an additional switching tube is parallel connected with the inverter bridge and is used to achieve the null vector; when it is turned on, the commutation action of the active vector is completed, so the overlap time can be eliminated. However, this modulation method is complex. For the current source rectifier, a diode is parallel connected with the rectifier bridge in reference [28], when the open circuit occurs during the commutation process, the additional diode can automatically provide a freewheeling circuit for the DC-link current. However, this topology is not suitable for the inverter occasion.

To effectively suppress the harmonic distortion caused by the overlap time, the following work has been completed. First, the relationship between the nonlinear error of the inverter-side current and the AC-side voltages is obtained during the overlap time. Then, the harmonic characteristics of the inverter-side current and the grid-side current are analyzed in detail. On this basis, the compensation method for the overlap time in the d–q axis is proposed. Finally, the simulation and experiment are carried out.

This paper is organized as follows. The overlap time generation mechanism for CSI is analyzed in Section 2. Then, the error and harmonics of the inverter-side current generated by the overlap time are derived in Sections 3 and 4, respectively, and a compensation scheme to suppress the overlap time effect is also proposed in Section 4. Finally, the simulation and experimental verifications are presented in Section 5. The conclusion is drawn in Section 6.

2. Topology, SVPWM Scheme and Overlap Time Generation of CSI

2.1. Topology of CSI

The topology of the current source PV grid-connected inverter is shown in Figure 1, where u_{dc} represents the output voltage of the PV cell, L_{dc} is the DC-link inductor and series connected with the PV cell, and i_{dc} is the current of L_{dc}. The inverter bridge is composed of the switching tubes S_1–S_6, and diodes D_1–D_6, C, L, R, and e represent the filter capacitance, inductance, resistance, and grid voltage, respectively. i_a, i_b, and i_c represent the three-phase inverter-side currents; u_a, u_b, and u_c represent the three-phase AC voltage of the inverter; and i_{ag}, i_{bg}, and i_{cg} represent three-phase grid-side currents.

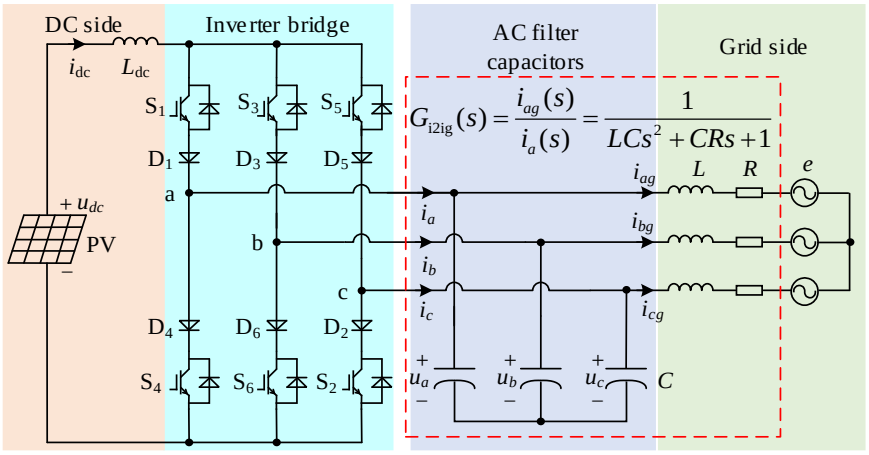

Figure 1. Topology of the current source PV grid-connected inverter.

2.2. SVM Scheme of CSI

The current vectors with corresponding switching states are shown in Figure 2. The space is divided into six sectors (I–VI) by the active vectors $\boldsymbol{I}_k$ (k = 1, 2, . . ., 6). In addition, there are three null vectors: $\boldsymbol{I}_7$, $\boldsymbol{I}_8$, and $\boldsymbol{I}_9$.

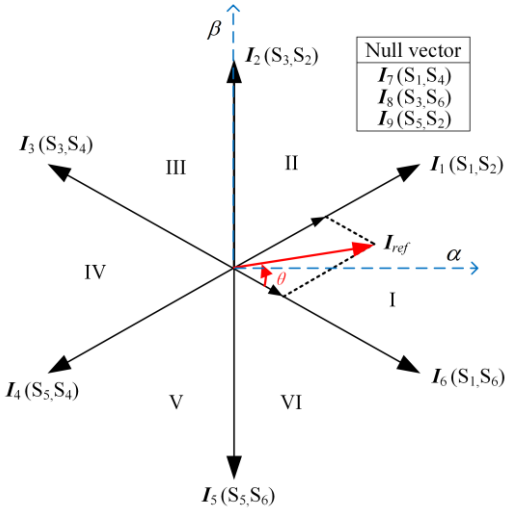

Figure 2. Current vectors and sectors.

Under the common seven-segment sequence SVM based on the triangular carrier wave, the inverter-side current is symmetrical, and the content of the low-order harmonic is less than that under other SVM schemes. If the target vector $\boldsymbol{I}_{ref}$ is located in sector I, $\boldsymbol{I}_{ref}$ is synthesized by the adjacent active vectors ($\boldsymbol{I}_1$ and $\boldsymbol{I}_6$) and null vector $\boldsymbol{I}_7$.

When $\boldsymbol{I}_{ref}$ is located in sector I, the switching signals diagrams are shown in Figure 3a, where m_a, m_b, and m_c are the compared values of the triple commutation time, and p_1–p_6 represent the switching signals of S_1–S_6, respectively. '0' represents off-state, and '1' represents on-state. At this time, all switching signals of the upper bridge arm (p_1, p_3, and p_5) remain '0' or '1' in a carrier period; commutation occurs among the switching tubes of the lower bridge arm (p_2, p_4 and p_6), and the total number of commutation times is six. t_1–t_6 represent the commutation comments. When $\boldsymbol{I}_{ref}$ is located in sector II, the switching signals diagrams are shown in Figure 3b, and the commutation occurs among the switching tubes of the upper bridge. The solid lines represent the actual signal waveform, and different color dashed lines are used to point out the commutation comments.

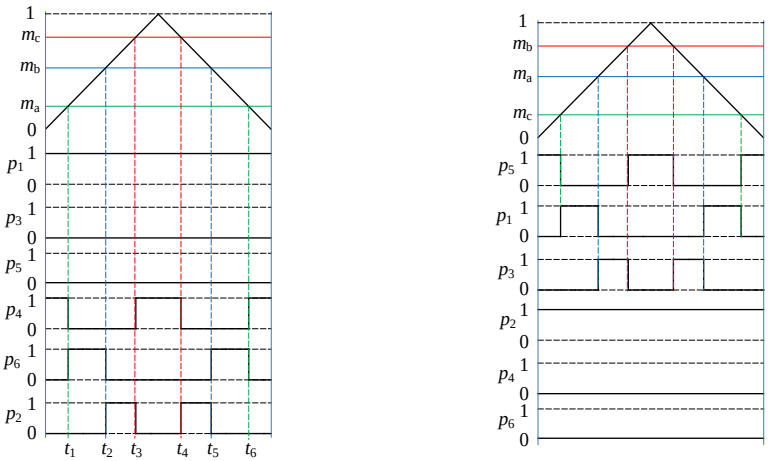

Figure 3. Switching signals diagrams in a carrier period under seven-segment SVM: (**a**) sector I; (**b**) sector II.

2.3. Overlap Time Generation Mechanism

In Figure 3, the moment of turn-on is consistent with that of turn-off. However, the delay phenomenon exists in the turn-on and turn-off process of the switching tube; if the delay process of turn-off is longer than that of turn-on, a brief open circuit state will appear in the inverter bridge, which will lead to a high dv/dt in the DC-link inductor. Therefore, turn-off delay should be introduced into all switching signals, at this time, the switching signals in the action of Sector I are shown in Figure 4. It can be seen that there are two switching signals in the on-state during t_{ov}; this is named the overlap time.

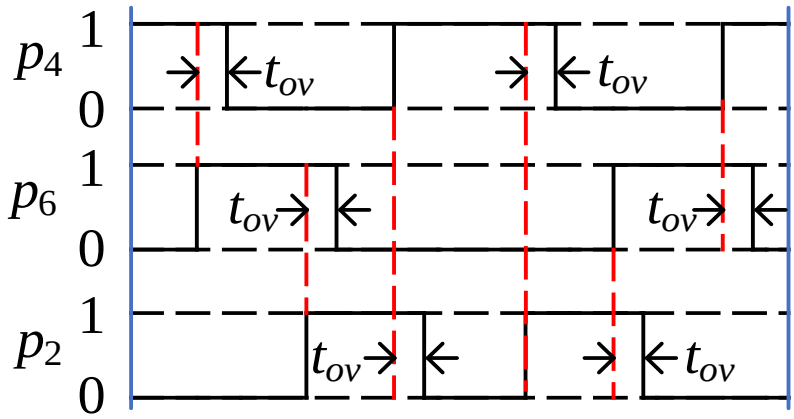

Figure 4. Switching signals diagrams with overlap time.

3. Analysis of Overlap Time Effect

In this section, the commutation characteristics during the overlap time are analyzed first; then, the inverter-side current error caused by the overlap time is analyzed.

3.1. Commutation Characteristics during the Overlap Time

Figure 5a shows the equivalent circuit during the overlap time in the commutation process from the null vector I_7 to the active vector I_1. At this time, both S_4 and S_6 are turned on simultaneously, but the flow path of i_{dc} depends on the relation of u_a and u_b.

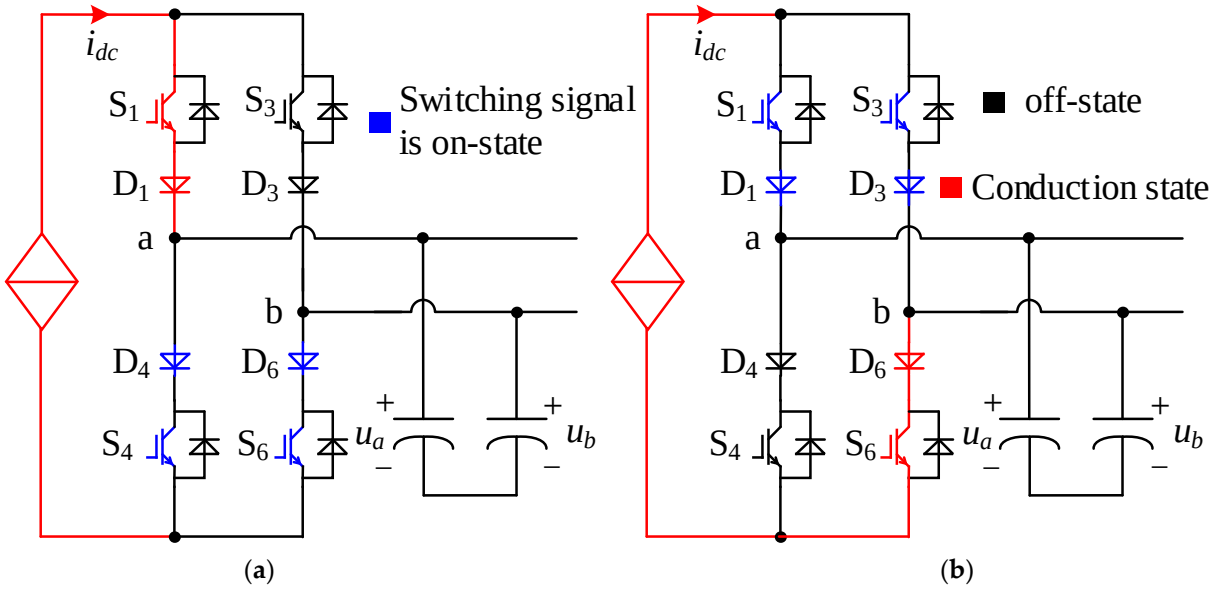

Figure 5. Equivalent circuit during the overlap time: (**a**) commutation from I_7 to I_1; (**b**) commutation from I_8 to I_1.

If $u_a > u_b$, D_4 remains in the conduction state, and D_6 withstands the reverse voltage; the generated current vector remains I_7, which leads to the nonlinear error on i_a and i_b.

If $u_a < u_b$, D_4 withstands the reverse voltage, D_6 changes to the conduction state, i_{dc} is switched from S_4 and D_4 to S_6 and D_6, and the generated current vector changes from I_7 to I_1; commutation can be achieved, and no nonlinear error is generated.

Figure 5b shows the equivalent circuit during the overlap time in the commutation process from the null vector I_8 to the active vector I_6. At this time, both S_1 and S_3 are turned on simultaneously, but the flow path of i_{dc} also depends on the relation of u_a and u_b.

If $u_a > u_b$, the forward voltage of D_3 is higher than D_1, so D_3 remains in the conduction state, and D_1 withstands the reverse voltage; the generated current vector remains I_8, which leads to the nonlinear error on i_a and i_b.

If $u_a < u_b$, D_3 withstands the reverse voltage, D_1 changes to the conduction state, i_{dc} is switched from S_3 and D_3 to S_1 and D_1, and the generated current vector changes from I_8 to I_6; no nonlinear error will occur.

The commutation characteristics during the overlap time can be summarized as follows:

1. When the target current vector is located in Sector I, III, or V, the commutation occurs among the lower bridge arms (S_4, S_6, and S_2). DC-link current only flows through the switching tube and diode whose phase voltage is higher, so the nonlinear current will not be generated if the sequence of commutation is from high voltage to low voltage;
2. When the target current vector is located in Sector II, IV, or VI, the commutation occurs among the upper bridge arms (S_1, S_3, and S_5). DC-link current only flows through the switching tube and diode whose phase voltage is lower, so the nonlinear current will not be generated if the sequence of commutation is from low voltage to high voltage.

3.2. Current Error Caused by the Overlap Time in a Carrier Period

According to the analysis of the commutation characteristics during the overlap time, combined in Figures 3 and 4, under all relationships of the AC voltage, the diagrams of the current error caused by the overlap time in sector I during a whole carrier period are shown in Figure 6. It can be seen that there are three stages in which the overlap time generates

current error in a carrier period, and the average three-phase inverter-side current error can be expressed as

$$\begin{cases} \Delta i_{\mathrm{x}} = -2 f_{\mathrm{s}} t_{\mathrm{ov}} i_{\mathrm{dc}} \\ \Delta i_{\mathrm{y}} = 0 \qquad\qquad u_{\mathrm{x}} > u_{\mathrm{y}} > u_{\mathrm{z}}, \\ \Delta i_{\mathrm{z}} = 2 f_{\mathrm{s}} t_{\mathrm{ov}} i_{\mathrm{dc}} \end{cases} \tag{1}$$

where f_{s} is the carrier frequency, Δi_{a}, Δi_{b}, and Δi_{c} represent the three-phase inverter-side current error, respectively, and x, y, and z belong to {a, b, c}.

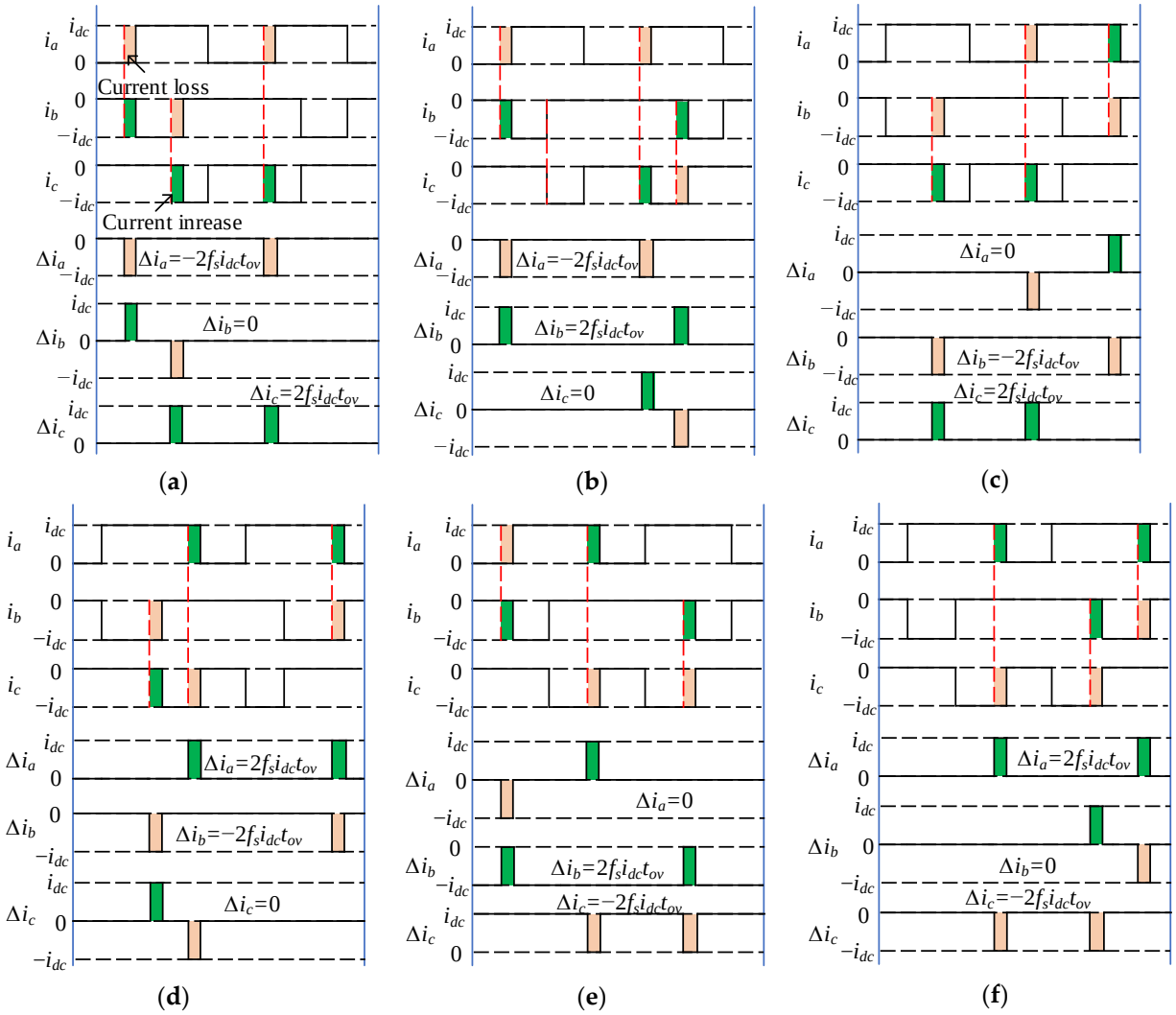

Figure 6. The diagrams of i_{a}, i_{b}, and i_{c} with their error caused by the overlap time in sector I: (**a**) $u_{\mathrm{a}} > u_{\mathrm{b}} > u_{\mathrm{c}}$; (**b**) $u_{\mathrm{a}} > u_{\mathrm{c}} > u_{\mathrm{b}}$; (**c**) $u_{\mathrm{b}} > u_{\mathrm{a}} > u_{\mathrm{c}}$; (**d**) $u_{\mathrm{b}} > u_{\mathrm{c}} > u_{\mathrm{a}}$; (**e**) $u_{\mathrm{c}} > u_{\mathrm{a}} > u_{\mathrm{b}}$; (**f**) $u_{\mathrm{c}} > u_{\mathrm{b}} > u_{\mathrm{a}}$.

When I_{ref} is located in sector II, under all relationships with the AC-side voltage, the diagrams of the current error caused by the overlap time in sector I during a whole carrier period are shown in Figure 7, where the red lines are used to indicate the moment of current error. It can be seen that the average three-phase current error can also be expressed by Formula (1), so the average current error caused by the overlap time in a whole carrier period is only related to the AC-side voltage and is independent of the sector where I_{ref} locates. The average current error under all relationships of the AC-side voltages can be summarized in Table 1.

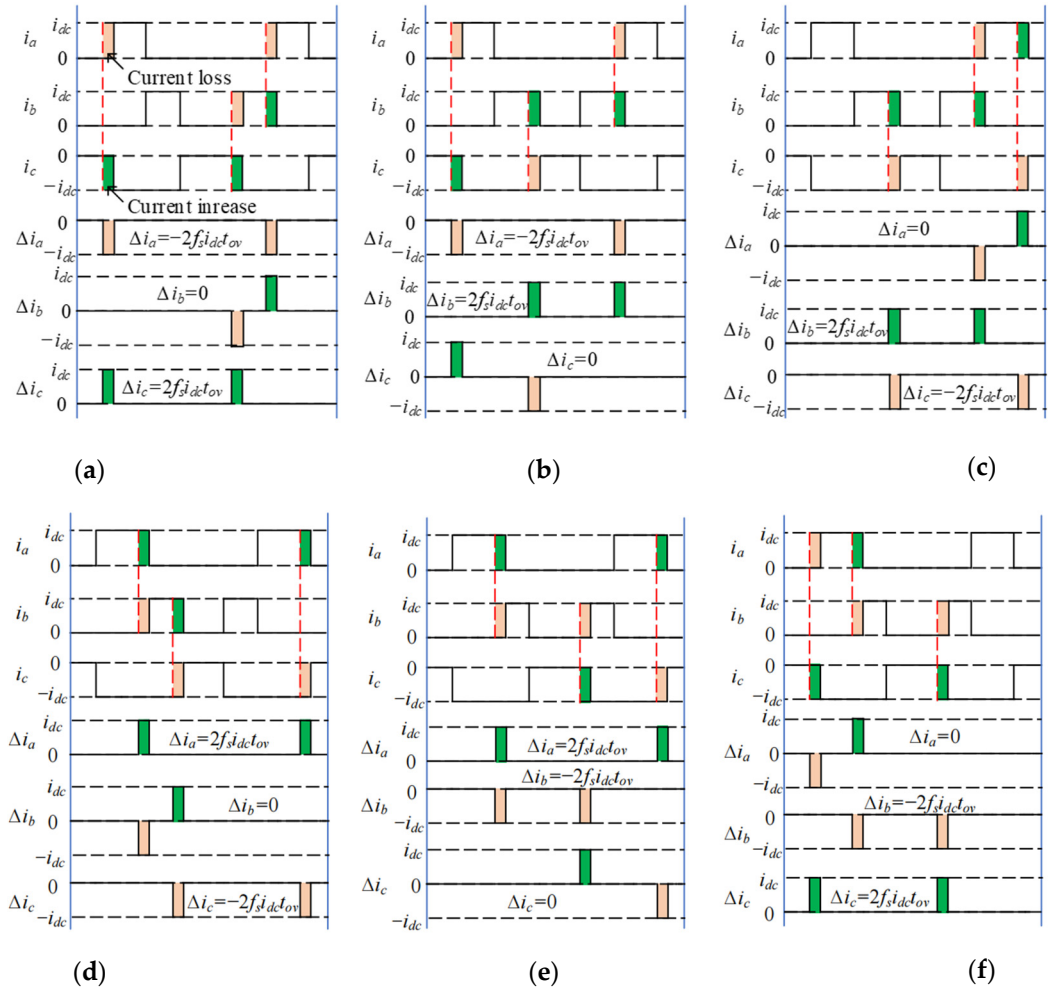

Figure 7. The diagrams of i_a, i_b, and i_c with their error caused by the overlap time in sector II: (**a**) $u_a > u_b > u_c$; (**b**) $u_a > u_c > u_b$; (**c**) $u_b > u_a > u_c$; (**d**) $u_b > u_c > u_a$; (**e**) $u_c > u_a > u_b$; (**f**) $u_c > u_b > u_a$.

Table 1. Average current error caused by the overlap time.

Relation of AC Voltage	Δi_a	Δi_b	Δi_c
$u_a > u_b > u_c$	$-2f_s t_{ov} i_{dc}$	0	$2f_s t_{ov} i_{dc}$
$u_a > u_c > u_b$	$-2f_s t_{ov} i_{dc}$	$2f_s t_{ov} i_{dc}$	0
$u_b > u_a > u_c$	0	$-2f_s t_{ov} i_{dc}$	$2f_s t_{ov} i_{dc}$
$u_b > u_c > u_a$	$2f_s t_{ov} i_{dc}$	$-2f_s t_{ov} i_{dc}$	0
$u_c > u_a > u_b$	0	$2f_s t_{ov} i_{dc}$	$-2f_s t_{ov} i_{dc}$
$u_c > u_b > u_a$	$2f_s t_{ov} i_{dc}$	0	$-2f_s t_{ov} i_{dc}$

4. Analysis of Harmonic Characteristics and Compensation Method for Overlap Time

4.1. Harmonic Characteristics for Overlap Time

According to Table 1, the waveform of Δi_a is shown in Figure 8, the initial phase of u_a is considered zero, and Δi_a can be expressed as

$$\Delta i_a = \begin{cases} 0 & (0 \le \omega t < \pi/6) \\ -2i_{dc} t_d f_s & (\pi/6 \le \omega t < 5\pi/6) \\ 0 & (5\pi/6 \le \omega t < 7\pi/6) \\ 2i_{dc} t_d f_s & (7\pi/6 \le \omega t < 11\pi/6) \\ 0 & (11\pi/6 \le \omega t < 2\pi) \end{cases}. \quad (2)$$

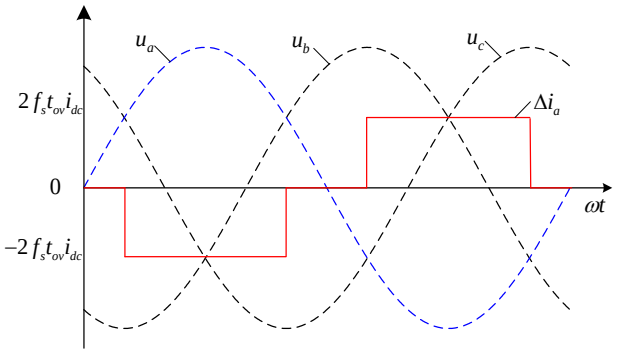

Figure 8. Waveform of Δi_a.

This is the symmetry of half wave and quarter wave, so Δi_a only contains the odd-order harmonics, Equation (2) is decomposed into Fourier series, and the harmonic expression of Δi_a can be obtained as

$$\Delta i_a = \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{\pi} \left\{ -\sin \omega t + (-1)^{k+1} \sum_{k=1}^{\infty} \left[\frac{1}{6k-1} \sin(6k-1)\omega t + \frac{1}{6k+1} \sin(6k+1)\omega t \right] \right\}. \quad (3)$$

Equation (3) shows that the overlap time introduces the $6k \pm 1$-order harmonics to the inverter-side current of CSI, and the amplitude of the harmonic is proportional to t_{ov} and i_{dc}.

4.2. Parameters Design for L, C, and R

Next, the harmonics of the grid-side current caused by the overlap time will be discussed. According to Figure 1 and reference [29], the transfer function $G_{i2ig}(s)$ from i_a to i_{ag} can be derived as

$$G_{i2ig}(s) = \frac{1}{LCs^2 + CRs + 1}. \quad (4)$$

The parameters of L, C, and R are determined by the Bode plots under different values. First, L and C remain unchanged. The Bode plots under different values of R are shown Figure 9a. The resonance peak decreases with the increase in R, but the efficiency of the system will decrease, so the value of R should be moderate. Meanwhile, the gain in the high-frequency range is independent of the value of R.

Then, L and R remain unchanged. The Bode plots under different values of C are shown Figure 9b. As the value of C increases, the high-frequency range gain increases, but the bandwidth of $G_{i2ig}(s)$ decreases.

Since there are abundant high-order harmonics in the inverter-side current near the switching frequency, to achieve good filtering performance, this paper stipulates that the gain of $G_{i2ig}(s)$ is less than 60 dB at the switching frequency of 10 kHz, so the values of L and C should be satisfied as

$$4\pi^2 LC > 10^{-5}. \quad (5)$$

Based on the above analysis, the parameters of L, C, and R are set as 4 mH, 66 μF, and 0.5 Ω, respectively. Substituting these parameters into Equation (4), the Bode plot of $G_{i2ig}(s)$ is shown in Figure 9c. To improve efficiency, the value of R is small, resulting in $G_{i2ig}(s)$ being an under-damped system.

There is a resonance peak in the magnitude–frequency characteristic curve of $G_{i2ig}(s)$, and $G_{i2ig}(s)$ will amplify the harmonics whose frequency belongs to the range [70 Hz, 400 Hz] in the inverter-side current. According to the expression of the harmonic caused by the overlap time, the frequencies of the fifth and seventh harmonics are 250 Hz and 350 Hz, and belong to the resonance region, which shows that the overlap time will introduce fifth and seventh harmonic distortion to the gird-side current of CSI.

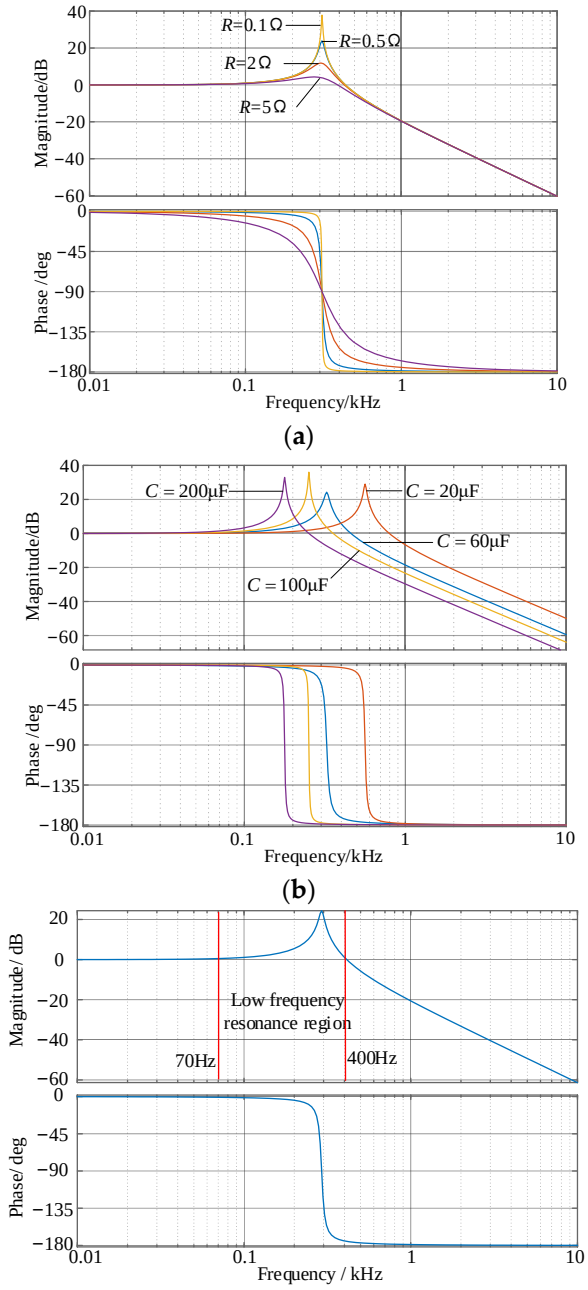

Figure 9. Bode plot of $G_{\mathrm{i2ig}}(s)$: (**a**) different R; (**b**) different C; (**c**) parameters determined in this paper.

4.3. Analysis of Harmonic Losses Caused by Overlap Time

Since the fundamental component of the current and switching action times have no change, the conduction and switching losses have no relationship with the overlap time. However, the harmonic components in the inverter-side current generate harmonic losses on resistors. Taking the fifth harmonic as an example, according to Equations (3) and (4), the amplitude of fifth harmonic component in grid-side current can be derived as

$$I_{ag5} = \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{5[\omega_5^2 C^2 R^2 + (LC\omega_5^2 - 1)^2]}, \tag{6}$$

where I_{ag5} is the amplitude of fifth harmonic component in i_{ag}, and ω_5 is the angular frequency of the fifth harmonic, being equal to 500π rad/s. The whole harmonic loss P_{h_loss} caused by the overlap time is expressed as

$$P_{h\_loss} = \frac{72 f_s^2 t_{ov}^2 i_{dc}^2 R}{25\left[\omega_5^2 C^2 R^2 + \left(LC\omega_5^2 - 1\right)^2\right]^2}. \tag{7}$$

4.4. Compensation Scheme of the Overlap Time

Figure 10 shows the control structure of the current source PV grid-connected inverter. It contains the conventional double-loop control scheme and the proposed overlap time compensation, where θ_g represents the grid voltage angle and is detected by the phase-locked loop, i_{dg} and i_{qg} represent the grid-side currents in d–q axis, and i_{dg}^* and i_{qg}^* represent the references of i_{dg} and i_{qg}, respectively. i_{dc}^* is the reference of the DC-link current and is determined by the MPPT principle. The PI controller is adopted to regulate the DC-link current; its output is i_{dg}^*, and i_{qg}^* is commonly set to zero. i_{dg} and i_{qg} are controlled by the PI controller with feedback decoupling and active damping, and the references of inverter-side currents in the d–q axis, i_d^* and i_q^*, are obtained.

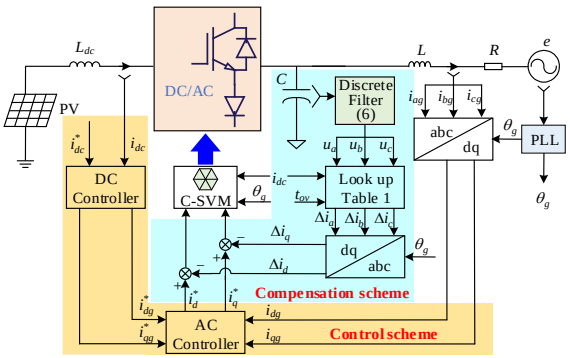

Figure 10. Control structure with compensation of the overlap time.

Before implementing the SVPWM algorithm, compensation is required to eliminate the current error caused by the overlap time. First, the three-phase AC-side voltages are sampled at each carrier period, so Δi_a, Δi_b, and Δi_c can be obtained by looking up Table 1. Then, Clarke and Park's transformations are performed, and the current errors of the inverter-side currents in the d–q axis, Δi_d and Δi_q, are obtained. Before SVPWM, Δi_d and Δi_q are subtracted from i_d^* and i_q^*, respectively.

According to Table 1, the proposed compensation scheme has a high requirement for AC voltage sampling accuracy. However, the filter capacitor absorbs the high-order harmonics of the inverter-side current, so there are significant ripples in the AC voltage, which seriously affect the sampling accuracy. If a low-pass filter is adopted, the phase delay will be generated, and the relations of the AC-side voltages will not be judged correctly. Therefore, a high-performance discrete filter is adopted to eliminate the ripple interference, its transfer function expression $G_R(z)$ in the z-domain is

$$G_R(z) = \frac{40\omega_n T_s (1 - z^{-2})}{\omega_n^2 T_s^2 + 40\omega_n T_s + 4 + 2(\omega_n^2 T_s^2 - 4)z^{-1} - (40\omega_n T_s - \omega_n^2 T_s^2)z^{-2}}, \tag{8}$$

where ω_n is the fundamental angle frequency and T_s is the sampling period. The performance of $G_R(z)$ under T_s = 1 ms is shown in Figure 11. The fundamental wave of u_a can be accurately extracted without phase shift under a low carrier ratio.

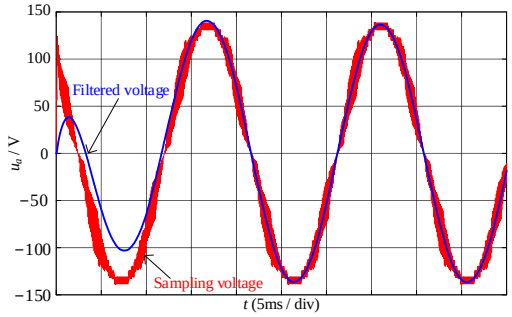

Figure 11. The waveforms of u_a before and after the discrete filter.

5. Simulation and Experimental Verification

5.1. Simulation Results and Analysis

In the environment of MATLAB 2022b/Simulink, the simulation models are established to verify the correctness of the analysis of the harmonic characteristics and the effectiveness of the proposed compensation method. The reference of the DC-link current is set as 15 A, f_s is set as 10 kHz, the simulations are carried out under t_{ov} = 0 µs and t_{ov} = 3 µs, and the simulation waveforms and FFT results are shown in Figures 12 and 13, respectively. Without the overlap time, it is obvious that there are very few harmonics in i_a and i_{ag}. However, after the overlap time of 3 µs is introduced, the fundamental amplitude of i_a, decreases from 9.90 A to 9.474 A, and the fifth harmonic, seventh harmonic, and total harmonic distortion (THD) significant increase. Affected by LC resonance, the harmonic distortion of i_{ag} is very significant; the ratios of the fifth harmonic and seventh harmonic are 4.52% and 3.56%.

To verify the correctness of the harmonic expression, the amplitude of the fundamental wave, fifth and seventh harmonics, and the THD of i_a under different overlap times are simulated and shown in Table 2.

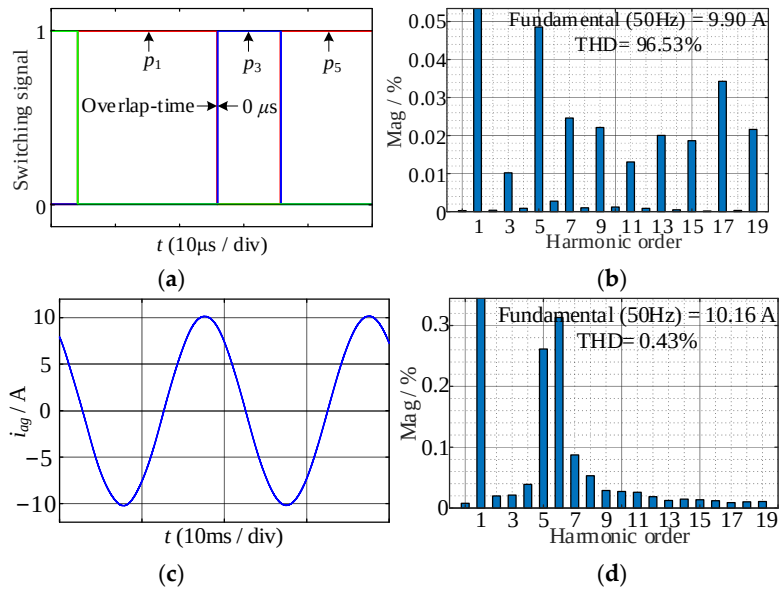

Figure 12. Simulation results without overlap time: (**a**) switching signals; (**b**) FFT results of i_a; (**c**) i_{ag}, (**d**) FFT results of i_{ag}.

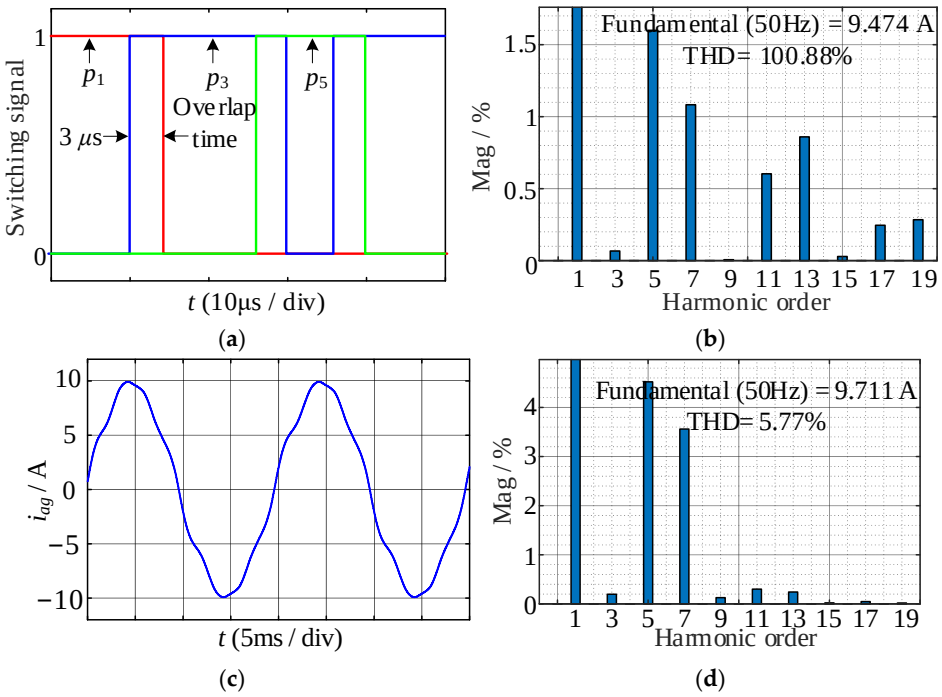

Figure 13. Simulation results with overlap time of 3 μs: (**a**) switching signals; (**b**) FFT results of i_a; (**c**) i_{ag}; (**d**) FFT results of i_{ag}.

Table 2. Average current error caused by the overlap time.

Overlap-Time (μs)	Fundamental Amplitude(A)	Fifth Harmonic Amplitude (A)	Seventh Harmonic Amplitude (A)	THD (%)
0	9.90	0.005	0.003	96.53
0.5	9.835	0.037	0.025	97.20
1	9.776	0.069	0.049	97.89
1.5	9.713	0.098	0.074	98.61
2	9.656	0.140	0.097	99.35
2.5	9.592	0.175	0.122	100.09
3	9.543	0.213	0.148	100.88

According to Equation (3), the fundamental of i_a is expressed as

$$i_{a1} = I_a \sin(\omega t - \varphi) - \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{\pi} \sin \omega t, \tag{9}$$

where I_a is the fundamental amplitude of i_a, φ is the phase of i_a lagging u_a, and is equal to 67°. In this operation, the amplitude loss of i_a related to the overlap time can be derived as

$$\Delta I_a = I_a - \sqrt{(I_a \sin \varphi)^2 + (I_a \cos \varphi - \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{\pi})^2}, \tag{10}$$

where ΔI_a is the fundamental amplitude loss of i_a. Since the contents of the fifth and seventh harmonics in i_a are very few without the overlap time, ΔI_{a5} and ΔI_{a7}, the amplitude increment of the fifth and seventh harmonics in i_a, are approximately derived as

$$\Delta I_{a5} = \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{5\pi}, \tag{11}$$

$$\Delta I_{a7} = \frac{4\sqrt{3} f_s t_{ov} i_{dc}}{7\pi} \tag{12}$$

Under different overlap times, ΔI_a, ΔI_{a5}, and ΔI_{a7}, shown in Table 2, are compared with Equation (7) to Equation (9), respectively, and the comparison results are shown in Figure 13. The amplitude errors of the fundamental wave and fifth and seventh harmonics in i_a are relatively close to the lines of Equations (7)–(9), which shows that the derived expression of the harmonic caused by the overlap time is theoretically correct.

Next, the proposed compensation model is introduced into the simulation, and the amplitude of the fundamental wave and fifth and seventh harmonics in i_a are obtained and shown in Table 3. Meanwhile, comparison results with no compensation are reflected in Figure 14; the amplitude errors of the fundamental wave and fifth and seventh harmonics in i_a, can be significantly reduced by the proposed compensation scheme. At this time, the simulation waveforms and FFT results of i_{ag} under t_{ov} = 3 μs are shown in Figure 15; compared to Figures 12 and 13, the low harmonic distortion caused by the overlap time can be suppressed by the current error compensation.

Table 3. The low harmonic characteristics of ia after the proposed compensation.

Overlap-Time (μs)	Fundamental Amplitude(A)	Fifth Harmonic Amplitude (A)	Seventh Harmonic Amplitude (A)	THD (%)
0.5	9.897	0.005	0.003	96.55
1	9.896	0.009	0.005	96.56
1.5	9.896	0.017	0.009	96.57
2	9.890	0.028	0.018	96.57
2.5	9.890	0.041	0.027	96.57
3	9.876	0.068	0.049	96.65
0.5	9.897	0.005	0.003	96.55

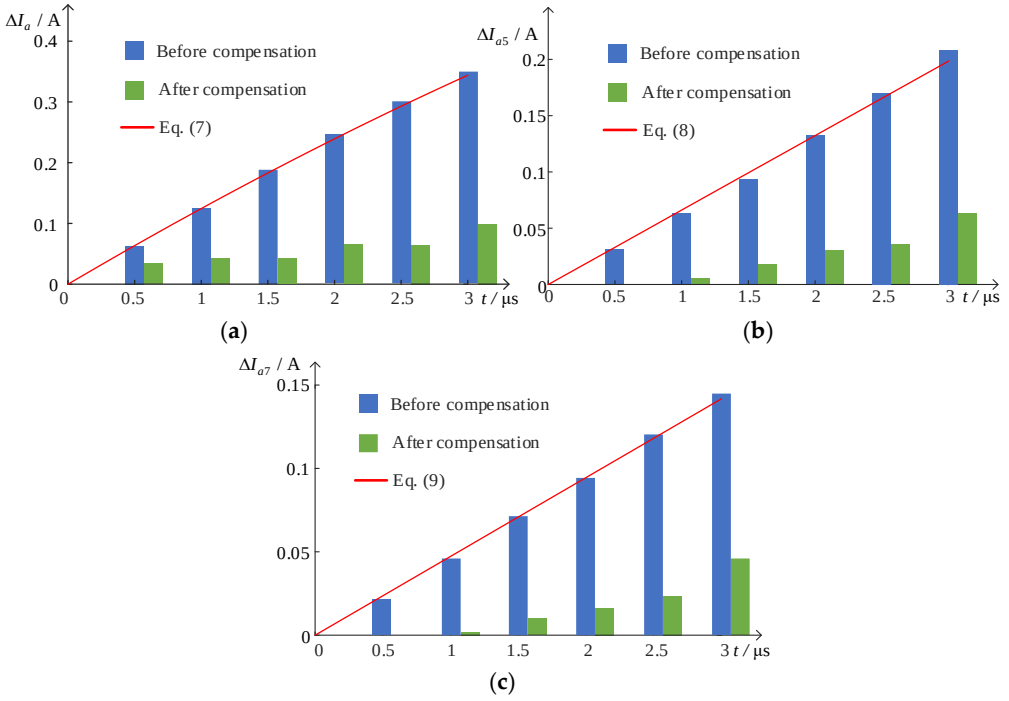

Figure 14. Comparison results of no compensation, proposed compensation, and derived harmonic expressions: (**a**) ΔI_a; (**b**) ΔI_{a5}; (**c**) ΔI_{a7}.

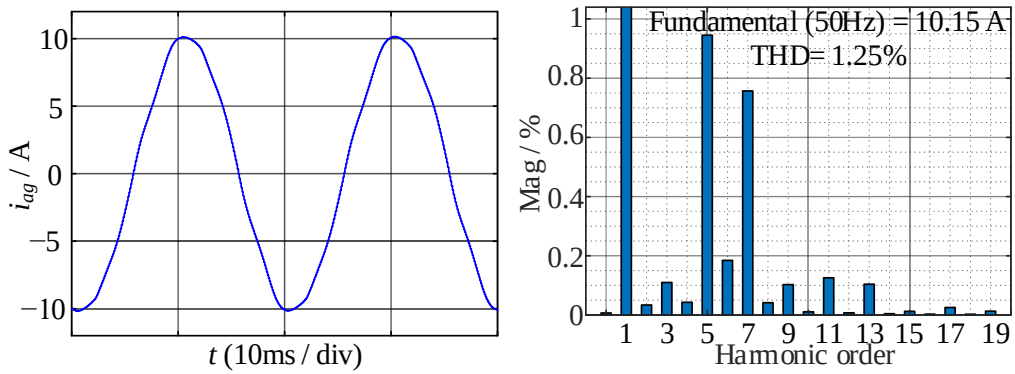

Figure 15. Simulation results after compensation under t_{ov} = 3 μs: (**a**) waveform of i_{ag}; (**b**) FFT results of i_{ag}.

5.2. Experimental Results and Analysis

To further verify the effectiveness of the overlap time compensation method proposed in this paper, a prototype of the CSI is established and shown in Figure 16, and the part numbers and parameters of each component are listed in Table 4.

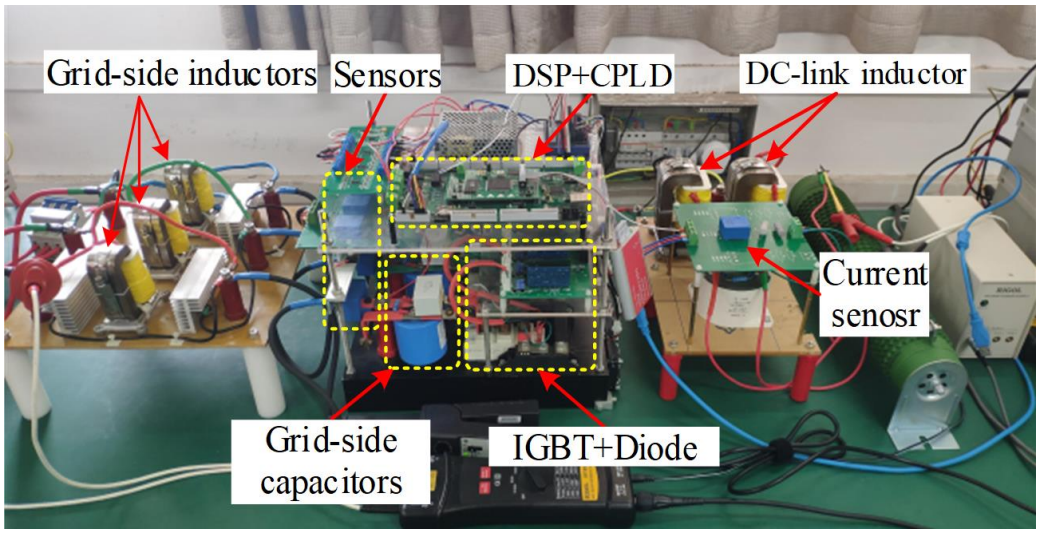

Figure 16. Experimental prototype of CSI.

Table 4. The part numbers and parameters of each component.

Category	Part Number	Parameter
AC voltage simulator	Chroma 61830	100 V
DC input voltage	DS1020	50 V
Controller	TMS320F28335 + CPLD	/
Voltage sensor	LV28-P	/
Current sensor	LA200-p	/
Switching tube	FF100R12RT4	/
Diode	MEA75-12DA	/
DC-link inductance	/	8 mH
AC-side inductance	/	4 mH
AC-side capacitance	/	66 μF
AC-side resistance	/	0.5 Ω

The operation of the experiment is the same as the simulation: i_{dc} = 15 A; f_s = 10 kHz; t_{ov} = 3 μs. Without compensation, the experimental waveform and FFT result of i_{ag} are

shown in Figure 17. Due to the overlap time effect and LC resonance, the obvious low-order harmonic distortion occurs in i_{ag}, where the amplitude of the fifth and seventh harmonics are 0.451 A and 0.356 A, respectively. It presents the same phenomenon as the simulation results shown in Figure 12.

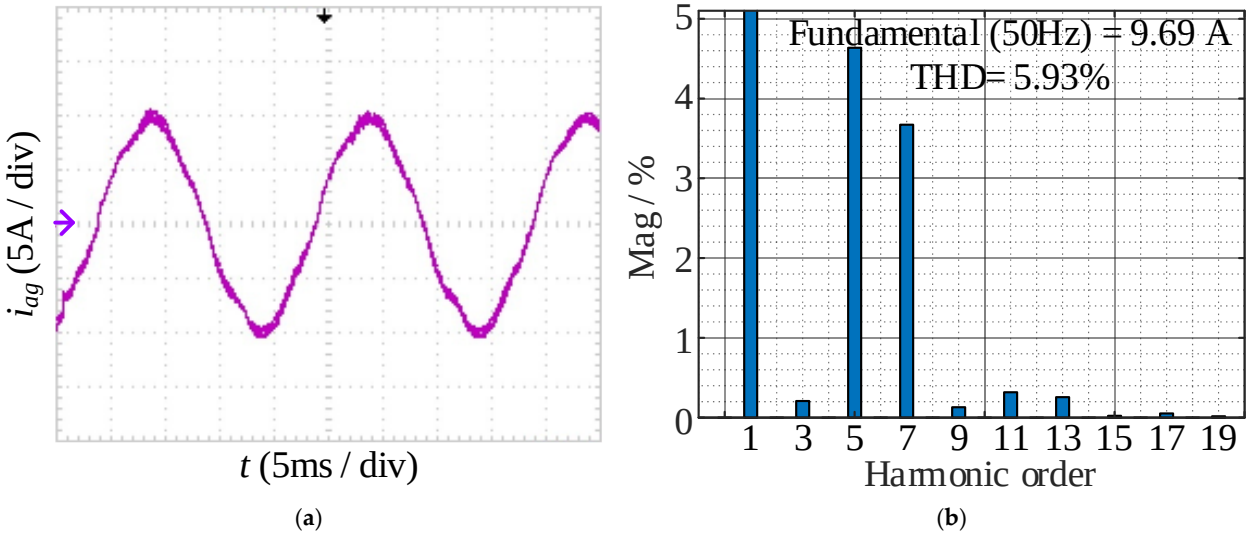

Figure 17. Experimental results without compensation under t_{ov} = 3 µs: (**a**) waveform of i_{ag}; (**b**) FFT result of i_{ag}. Purple arrow—the zero tick mark.

After the proposed current error compensation is introduced into the control algorithm, the experimental waveform and FFT result of i_{ag} are shown in Figure 18; after compensation, the fundamental amplitude increase from 9.69 A to 9.95 A, the amplitudes of the fifth and seventh harmonics are reduced to 0.119 A and 0.097 A, and the THD decreases from 5.93% to 1.95%.

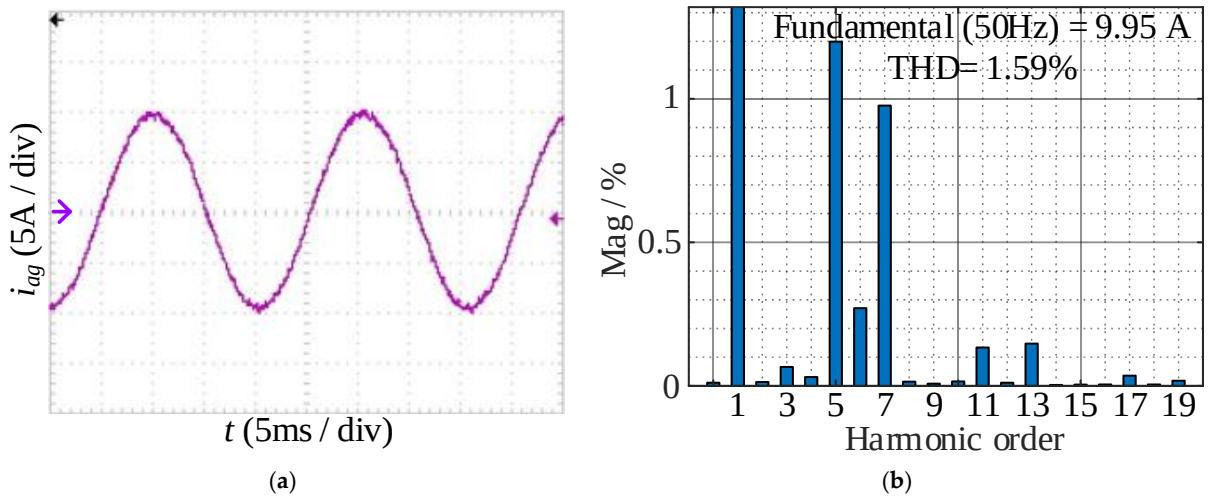

Figure 18. Experimental results with compensation under t_{ov} = 3 µs: (**a**) waveform of i_{ag}; (**b**) FFT result of i_{ag}. Purple arrow—the zero tick mark.

To demonstrate the necessity of the discrete filter Equation (9), Figure 19 shows the experimental waveform and FFT result of i_{ag} without a discrete filter. Due to the voltage sampling errors, the determination of the AC voltage relationships within a few carrier cycles is incorrect. Compared to Figure 18, although the fundamental amplitude can be compensated effectively, the suppression effect of the fifth and seventh harmonics is weaker

than those adopted the discrete filter. The THD of i_{ag} is 2.65%, and the amplitudes of the fifth and seventh harmonics are 0.178 A and 0.158 A, respectively.

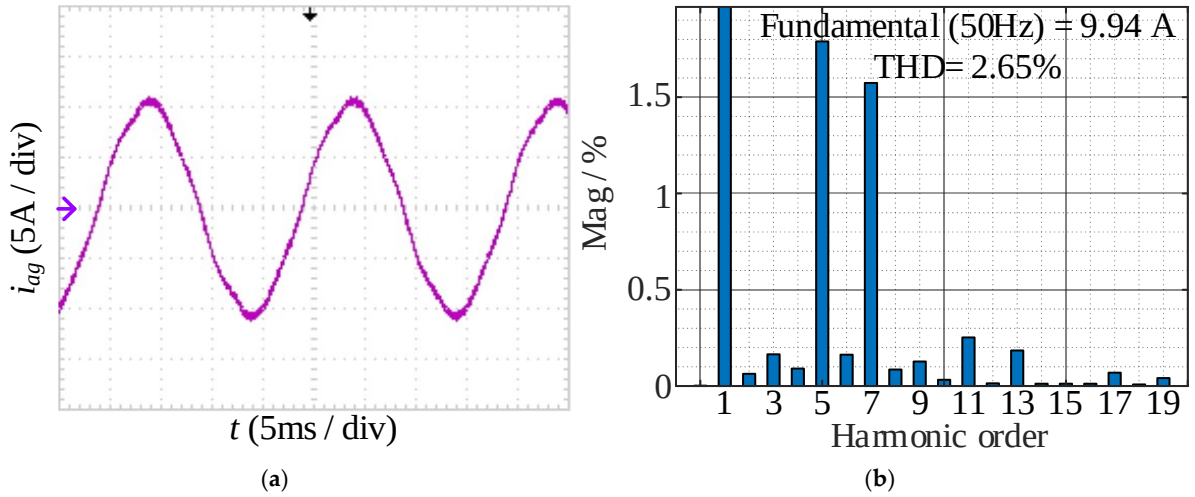

Figure 19. Experimental results with compensation and no discrete filter under t_{ov} = 3 µs.: (**a**) waveform of i_{ag}; (**b**) FFT results of i_{ag}. Purple arrow—the zero tick mark.

Figure 20 shows the comparison results of no compensation, compensation without discrete filter, and the proposed compensation under different overlap time, which shows that if the AC voltage relationship can be accurately obtained, the current error and harmonic distortion caused by the overlap time can be significantly compensated.

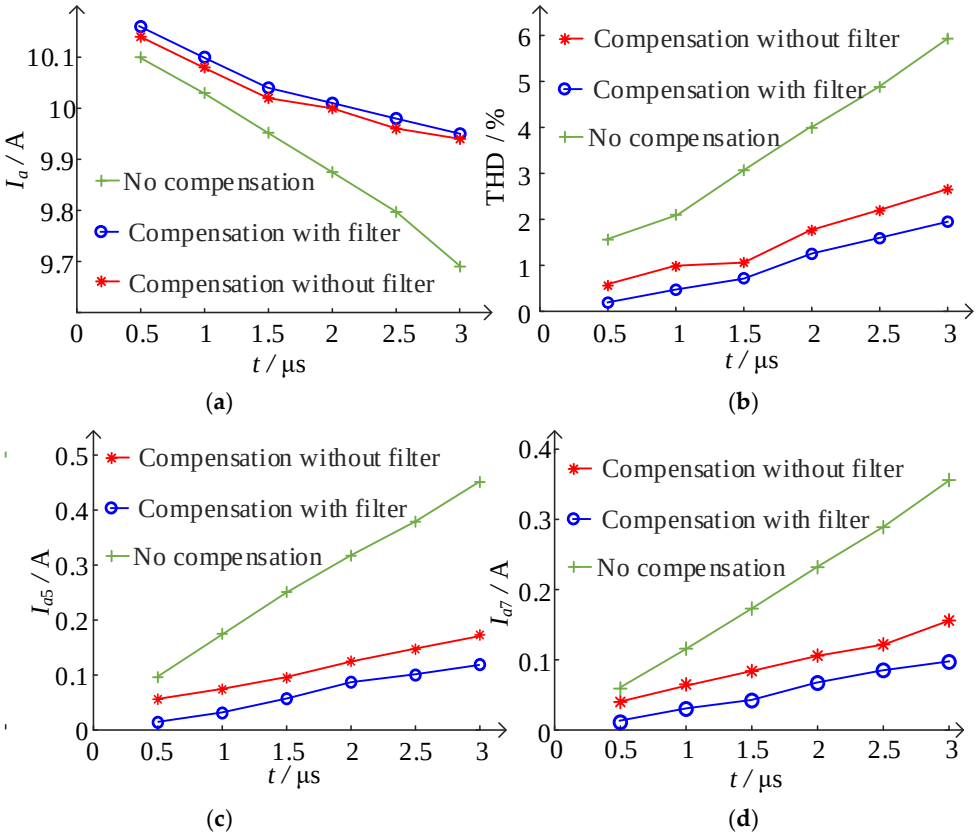

Figure 20. The comparison results of no compensation, compensation without discrete filter, and the proposed compensation under different overlap time: (**a**) fundamental amplitude; (**b**) THD; (**c**) amplitude of fifth harmonic; (**d**) amplitude of seventh harmonic.

6. Conclusions

To prevent an open circuit fault in the current source inverter, the switching signal needs to be delayed and turned off, resulting in overlap time and low-order harmonics appearing in inverter-side and grid-side currents. In this paper, based on analyzing the nonlinear error and harmonic characteristics caused by the overlap time, a current compensation method with an AC voltage discrete filter is proposed. Finally, the correctness and effectiveness of the theoretical analysis and compensation scheme are certified via simulation and experiment, and our conclusions are formed as follows:

(1) The current error during the overlap time is only determined by the relation of the AC-side voltage; it is not related to the sector of the target current vector.
(2) The overlap time leads to a decrease in the fundamental wave and an increase in the low-order odd harmonics in the inverter-side current. Due to the LC resonance, the fifth and seventh harmonics in the grid-side current will further increase.
(3) Since the AC-side voltage can be accurately obtained, the nonlinear errors caused by the overlap time can be significantly reduced by the proposed compensation scheme.
(4) The proposed approach is dependent on the sampling accuracy of the filter capacitor voltage. Further research can focus on the control system bandwidth design and active damping method to suppress the harmonic distortion caused by the overlap time, eliminating the need for the sampling of the voltage.

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