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Investigation of a 25 kV–50 Hz Railway-Substation Power Supply Based on a Back-to-Back Modular Multilevel Converter Topology

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Abstract: This paper presents a preliminary study of a 25 kV–50 Hz railway substation power supply system. The control of a back-to-back converter based on modular multilevel converter (MMC) technology was investigated to fit with the power quality requirements of the application. One of the main challenges is the presence of constraining load conditions, under which the train circulation variability, low-frequency harmonics and critical power transients can notably decrease the power quality and lead to instability. In order to address this, cascaded controllers based on resonant controllers are proposed to ensure the desired performance. Furthermore, balancing voltage algorithms are added to avoid stress phenomena and additional losses in the studied power conversion interface. The paper presents the design of the control stages and demonstrates the robust performance of the system using a realistic loading condition of a railway substation.

Keywords: MMC converters; back-to-back converter; power quality; railway station; harmonics

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1. Introduction

Railway systems around the world use diverse power supplies, as we can see with the example of Europe, where three main power supply modes are in use [1]. Indeed, the use of 3 kV DC, 15 kV AC at 16.7 Hz and 25 kV AC at 50 Hz necessitates the use of different rolling stocks (i.e., trains) or stocks that can endure changes in the power supply [2,3], which can lead to heavy rolling stocks. Even if we solve the issue by making rolling stocks versatile and able to operate in different electric traction systems, we also need to solve the static infrastructure issue. Having versatile rolling stocks means that they cannot be perfectly operated in every environment without making compromises, resulting in a drop in voltage quality. As shown in Figure 1, there are places in Europe that have up to three different power supply modes in a restricted area.

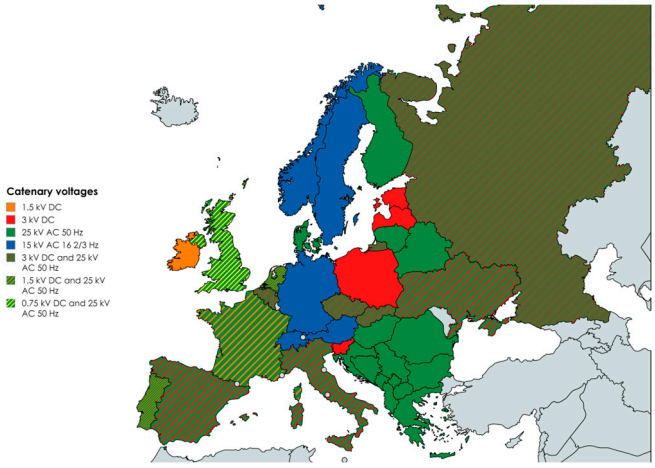

Figure 1. Electrification systems in Europe [4–6].

These places are the most sensitive, and with the development of decentralized microgrids, we have to be sure that the distribution systems are not polluted by high harmonics [7] that could lead to issues in the power grid. DC systems have a quite simple architecture: the catenary rectifier is directly connected to the three phases of the distribution system, providing a natural balance of the load on the network [8]. DC systems also allow rolling stocks to be lighter, reducing the amount of energy needed to power them. Unfortunately, the use of low voltage requires increasing the number of substations, making implementation difficult, especially in urban zones where they are the most used. Now, when considering AC power supply systems, we have to first make a distinction: either the catenary is powered with the same frequency as the distribution network, 50 Hz in Europe or 60 Hz in America, or the catenary is powered with a different frequency, typically 16.7 Hz, with or without a dedicated distribution network. The latter configuration requires an initial conversion step where both the frequency and voltage level are modified using stationary converters, motors or turbines if there is a dedicated power plant. This power supply architecture has been used historically [9] and is still used in Germany, for example. One of its unique characteristics is that it can have its own distribution network [10], making the public distribution network immune to power quality issues. However, in this case, doubling the infrastructure also doubles the need for maintenance and almost doubles the cost. Therefore, having the supply at the same frequency is the most advantageous, since there is no need for an additional conversion step. However, connections between substations and the distribution network are only made in two of the three phases, making a phase change necessary for each connection point. Even though this creates a relative equilibrium, imbalance persists because of distance-induced line inductance and capacitance, resulting in a small but still present balancing problem. All of these architectures are connected to transformers that are bulky and non-controllable, and can have magnetization issues and other complications [11,12].

This is where modular multilevel converters (MMC) become interesting: due to their versatility, they have a wide range of applications, such as speed drives [13–15], DC transmission lines [16–19], power conditioning (thanks to static compensators) [20–23] and battery energy storage systems [24,25]. Power conditioning can also be achieved with direct powering of the load to be compensated, thus MMCs can be used to power electric arc furnaces [26,27] that are particularly difficult loads to model [28,29], which makes tuning the control more difficult than for conventional loads. This application, in which power quality is regulated, can be applied to the railway field, as has been demonstrated in the past [30,31], but focused on either different frequency systems or parallel power conditioning [32] or with separated layers [33].

Looking at the research [34], we find that railway powering systems tend to use increasingly more power electronics to power the catenaries. However, few articles discuss

industrial constraints. Indeed, when designing these converters, it must be remembered that real insulated gate bipolar transistors (IGBTs) work within a specific range and do not have an unlimited voltage range. The following work was conducted while considering IGBTs that work under 1 kHz and have a rated voltage of 2.5 kV, resulting in the choice of a 320 Hz switching frequency for all IGBTs in both converters.

This paper provides a comprehensive analysis of the behavior of a complete power conversion chain for a realistic railway substation power supply application. The studied system is based on a back-to-back MMC converter that connects the main grid to power a railway catenary. On the load side, the power supply ensures grid-forming functionality by creating a point of common coupling of 25 kV–50 Hz. This system, with its control, was developed to meet both the energy quality standards on the grid side and railway standards on the load side. In order to achieve these objectives, we investigated the studied structure in three complementary parts: (i) analysis of controlling the grid-side AC/DC converter with a focus on the distributed capacitor voltage balancing algorithm; (ii) investigation of AC voltage regulation at the catenary side (this control is based on a proportional resonant controller without regard to the complex load model); and (iii) simulation-based analysis of the interaction between the two converters. As a preliminary study before further industrial investigation, a scenario employing one train at steady state and another with acceleration, steady-state and deceleration phases was performed to verify compliance of the proposed system with railway standards.

2. System Description

The full converter structure had a three-phase rectifier, a DC link and a single-phase inverter, as shown in Figure 2. The rectifier and inverter are based on MMC topology with half-bridge submodules.

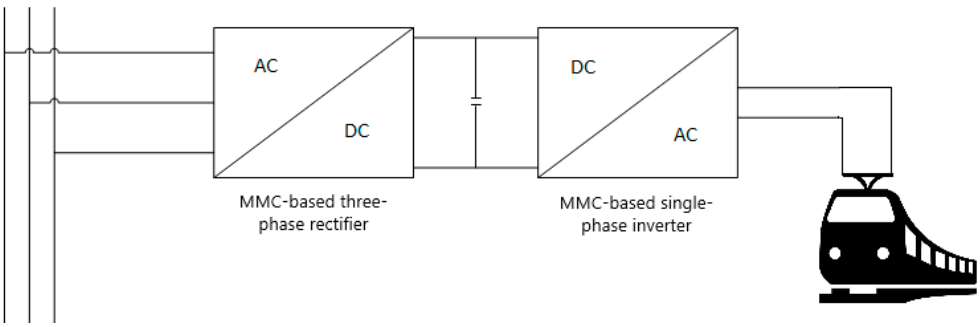

Figure 2. Overview of a railway-substation power supply based on MMC technology with a back-to-back topology.

In order to ease the comprehension of this work, we split this part into two axes concerning the rectifier part and the inverter part of the converter. Below we present the topology and control as well as simple results that can be used to assess the performance of our work.

The main objective of this converter is to provide 25 kV–50 Hz voltage to the catenary side while preventing disturbances on the grid side. The chosen capacitors have a rated voltage V_{SM} of 2500 volts, and the number of submodules is chosen based on this data. The DC link voltage between the two converters has a rated voltage V_{dc} of 70 kV, meaning that we must have a total of 28 submodules per arm, N_{SM}, as calculated by Equation (1):

$$N_{SM} = ceil\left(\frac{V_{dc}}{V_{SM}}\right) \tag{1}$$

Furthermore, capacitor capacity must be determined in order to provide and absorb enough power so as to not degrade performance. This criterion is described in [35,36] and is based on varying submodule energy ΔW_{SM}, described by Equation (2):

$$\Delta W_{SM} = \frac{2}{3}\frac{S}{kN\omega_0}\left(1 - \left(\frac{kcos(\varphi)}{2}\right)^2\right)^{\frac{3}{2}} \tag{2}$$

This allows us to determine the capacitor value by using Equation (3):

$$C = \frac{\Delta W_{SM}}{2\Delta V_{SM} U_c^2} \tag{3}$$

which leads to Equation (4):

$$C = \frac{S}{3kN\omega_0 \Delta V_{SM} U_c^2}\left[1 - \left(\frac{kcos(\varphi)}{2}\right)^2\right]^{\frac{3}{2}} \tag{4}$$

where S is the apparent power of the converter, k is the voltage modulation index, N is the number of SMs per arm, ω_0 is the fundamental frequency, ΔV_{SM} is the voltage ripple of the submodule, U_c is the mean value of the capacitor voltage and $\cos\varphi$ is the power factor.

3. Study of the Grid-Side Rectifier

On the rectifier side, we used a double-star structure, as is used in high-voltage direct current (HVDC) transmission. Here, the objective is the same: we need to maintain the value of the DC link and limit the effect of the load on the distribution grid. Therefore, we must control these parameters while preventing the divergence of submodule capacitors.

This part of the work was based on a double-star application where the DC and AC sides are decoupled and can be controlled separately; thus, the architecture was the same, with the converter connected to a 30 kV grid using 3.9 mH inductance and 24.5 mΩ resistance, as shown in Figure 3.

3.1. DC and AC Regulation

The main objective of this part is to balance the DC link, making sure it does not diverge and stays even over time. This part of the control is based on Equation (5):

$$i_{dc} = C * \frac{dV_{dc}}{dt} + i_{load} \tag{5}$$

where i_{dc} is the output current of the converter, V_{dc} is the DC link voltage, C is the DC link capacitor and i_{load} is the load current. This allows us to have an i_{dc} reference. This reference is then used to recreate a V_{dc} reference that will be added to the other regulation loops. Network current regulation is one of the key features that needs to be achieved; we have to make sure to minimize the effects of the converter and the load on the network.

To do so, we act on the current as it passes through the converter, controlling it in the same stationary frame as the DC link to ensure balance. The q component of the current reference is set at 0, and we calculate the d component. The DC component is then set to be coupled to the d-axis, leading to the i_d reference being defined by Equation (6):

$$i_{d_{ref}} = \left(K_{P_{d_{ref}}} + \frac{K_{i_{d_{ref}}}}{s}\right)\left(V_{DC_{ref}} - V_{arm_{ave}}\right) \tag{6}$$

where $i_{d_{ref}}$ is the d-axis current reference, $V_{DC_{ref}}$ is the rated voltage the converter has to achieve, $K_{p_{d_{ref}}}$ and $K_{i_{d_{ref}}}$ are the gains for the proportional controller and $V_{arm_{ave}}$ is the averaged sum of the six arm voltages as defined by Equation (7):

$$V_{arm\,ave} = \frac{1}{6}\sum_{j=1}^{6}\sum_{i=1}^{N} V_{SMij} \tag{7}$$

where V_{SMij} is the submodule voltage at position i in arm j. This reference is then used to generate voltage references using Equation (8):

$$V_{dq_{ref}} = \left(K_{p_{dq_{ref}}} + \frac{K_{i_{dq_{ref}}}}{s}\right)\left(i_{dq_{ref}} - i_{dq}\right) \tag{8}$$

where the subscript dq refers to either component d or q (for ease of expression) and $K_{p_{dq_{ref}}}$ and $K_{i_{dq_{ref}}}$ are the gains for the proportional controllers. $V_{d_{ref}}$ and $V_{q_{ref}}$ are calculated separately and then put back into the original reference frame, leading to $V_{ac_{ref}}$.

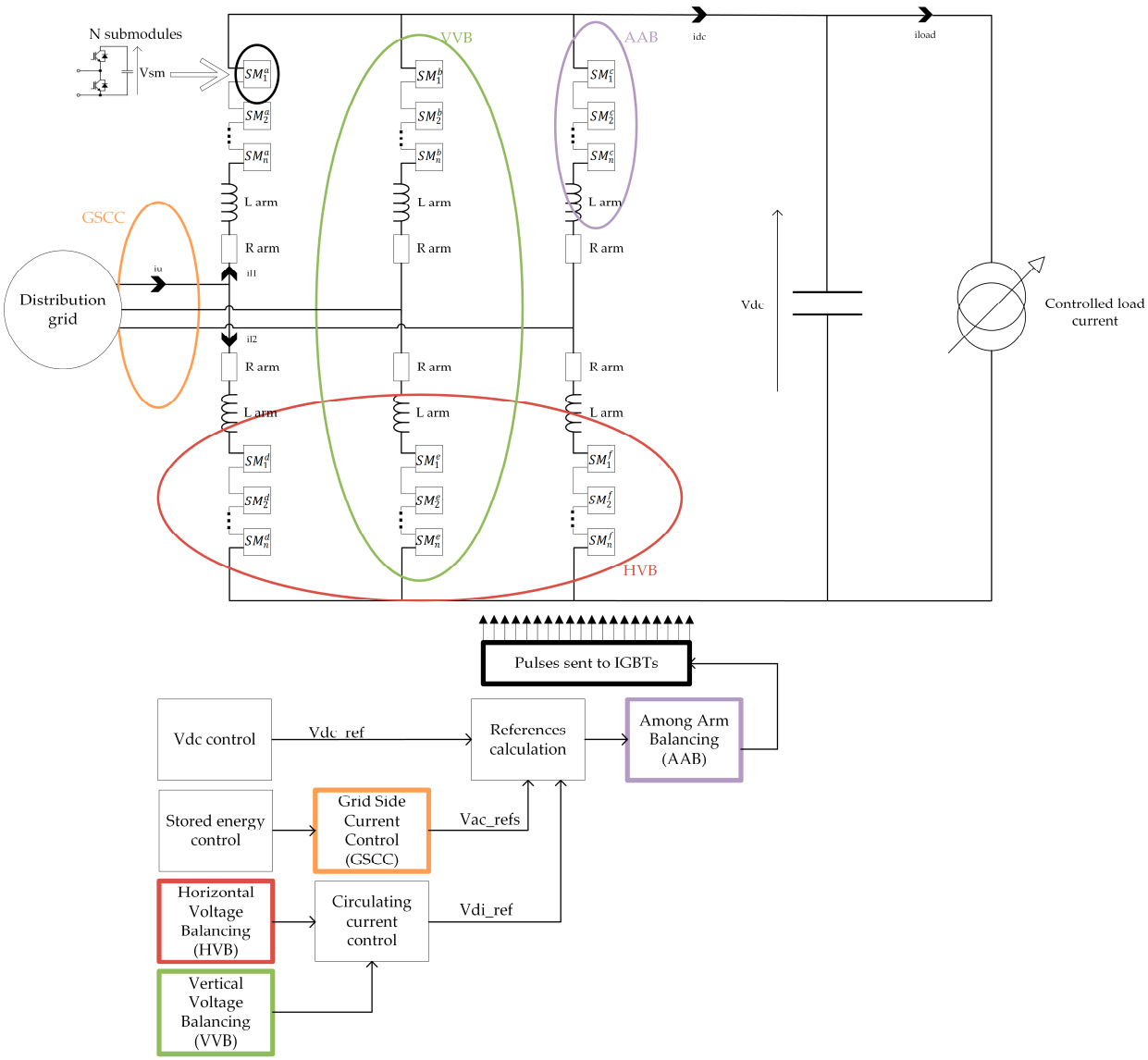

Figure 3. Grid-side Rectifier control scheme.

3.2. Internal Balancing

In addition, vertical and horizontal balancing is achieved, meaning that every block of N submodules will have the same global voltage, which will reduce the risk of circulating currents [36,37], hence reducing the losses in our system.

Horizontal voltage balancing (HVB) is achieved by comparing each pair of symmetric arms to the others to create a reference for the horizontal energy repartition. This command can be summarized by Equation (9)

$$i_{hor_{ref}} = \left(K_{p_{h_{ref}}} + \frac{K_{i_{h_{ref}}}}{s}\right)\left(\frac{1}{2}\left(v_{arm_{up}} + v_{arm_{down}}\right) - v_{arm_{ave}}\right) \tag{9}$$

where $i_{hor_{ref}}$ is the horizontal current reference, $K_{p_{h_{ref}}}$ and $K_{i_{h_{ref}}}$ are the gains for the proportional controller and $v_{arm_{up}}$ and $v_{arm_{down}}$ are the average voltage for each upper and lower arm, respectively. The associations are made for each phase.

Vertical voltage balancing (VVB) is achieved by controlling the zero, positive and negative sequence in the converter. These three components are calculated and then separately injected into a PI controller, as summarized by Equation (10):

$$x_{seq_{ref}} = \left(K_{pv_{ref}} + \frac{K_{iv_{ref}}}{s}\right)x_{seq} \tag{10}$$

where $x_{seq_{ref}}$ is the reference for the considered sequence (positive, negative or zero), $K_{pv_{ref}}$ and $K_{iv_{ref}}$ are the gains for the proportional controller and x_{seq} is the considered sequence. These references are then used to recreate two three-phase signals using dq transformation by Equation (11):

$$\begin{cases} \left(positive_{seq_{ref}} \middle| negative_{seq_{ref}}\right) * P^{-1} = abc_{ref1} \\ \left(zero_{seq_{ref}} \middle| 0\right) * P^{-1} = abc_{ref2} \end{cases} \tag{11}$$

where P^{-1} is the inverse Park transform, and abc_{ref1} and abc_{ref2} are the two three-phase reference signals. These two signals are then compared to create the reference for vertical energy repartition and are denoted as $i_{ver_{ref}}$.

The two references, $i_{ver_{ref}}$ and $i_{hor_{ref}}$, are then added to produce a circulating reference for each phase, which is compared to circulating current i_{circ}, which is calculated by Equation (12) [38,39]:

$$i_{circ} = \frac{i_{up} \pm i_{low}}{2} \tag{12}$$

where i_{up} and i_{low} are the current in the upper and lower arm, respectively. This current is compared to the average circulating current $i_{circ_{ave}}$, defined by Equation (13):

$$i_{circ_{ave}} = \frac{1}{6}\sum_{i=1}^{6} i_i \tag{13}$$

where i_i is the current in arm i. The difference between the two circulating currents is then compared to the reference produced by the HVB and VVB controllers.

From all of these regulation loops, we combine the various references into a new reference to use for PWM generation. This combination is presented in Equation (14):

$$V_{n_{ref}} = \frac{V_{dcref} \pm \left(V_{acref} - V_{acref_{av}}\right) - V_{diref}}{\sum V_{SMarm}} \tag{14}$$

where $V_{n_{ref}}$ is the normalized reference used for PWM generation, V_{dcref} is the reference from the DC link control, V_{acref} is the reference from the current grid-side control and

$V_{acref_{av}}$ is the averaged value of the previous one, V_{diref} is the reference from the balancing process and $\sum V_{SMarm}$ is the sum of all capacitor voltages in one arm.

3.3. Capacitors Balancing

Reference $V_{n_{ref}}$ is then injected into an algorithm that provides near level control of each capacitor's voltage [40], allowing decentralized control and reducing computing time when compared to other methods [41,42]. The operating mode of this sorting method can be summarized by Equation (15):

$$\tilde{V_{n_{ref}}} = V_{n_{ref}} + \left(\frac{(V_{SM_n} - V_{SM\ average})}{V_{SM\ ref}} * sign(i_{arm}) \right) \tag{15}$$

Where $\tilde{V_{n_{ref}}}$ is the reference used for PWM generation once voltage balancing is achieved, V_{SM_n} is the voltage of capacitor n, $V_{SM\ average}$ is the average capacitor voltage in one arm, $V_{SM\ ref}$ is the desired capacitor voltage and $sign(i_{arm})$ is the sign of the current passing through the converter's arm. This algorithm balances voltage across an arm, meaning the effect is not apparent from the macroscopic point of view, but it must be noted that this algorithm works better when the switching frequency is not a multiple of the network frequency.

To verify the good behavior of the rectifier, we connected the DC link to a current source to provide continuous current. This allowed us to look at grid currents, arm capacitor voltages and DC link voltages, which are the main variables we need to control.

3.4. Rectifier's Simulation

To validate the rectifier's behavior in the IGBT model, we ran the following simple scenario using a Matlab r2014 and PLECS 3.3.7 environment. We applied a varying current load to the converter to simulate a load variation that emulates trains. The initial current was set at 1100 amperes (phase 1), and after 2 seconds it was gradually increased to 2300 amperes (phase 2), emulating acceleration. After 1.5 seconds of steady state (phase 3), deceleration occurred at the same rate as acceleration (phase 4), and the current was returned to 1100 amperes (phase 5). This case is depicted in Figure 4.

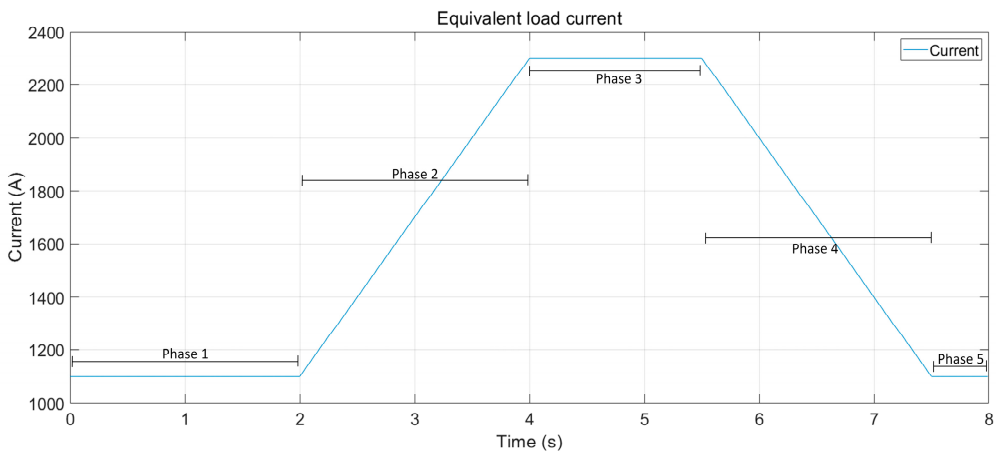

Figure 4. Current applied to the rectifier's DC link.

One of the main purposes of the inverter is to provide a stable voltage source. Therefore, it is critical to monitor the DC link voltage and ensure that any deviation during transitional states is inconsequential. The DC link voltage and the chosen reference are shown in Figure 5.

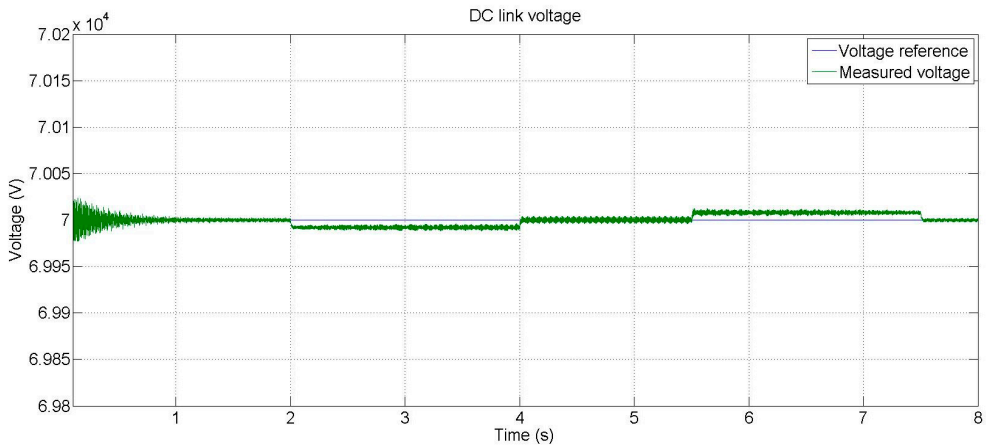

Figure 5. Rectifier's DC link voltage.

We can observe a very small deviation during the transient state. This deviation can be measured, and is shown in Figure 6.

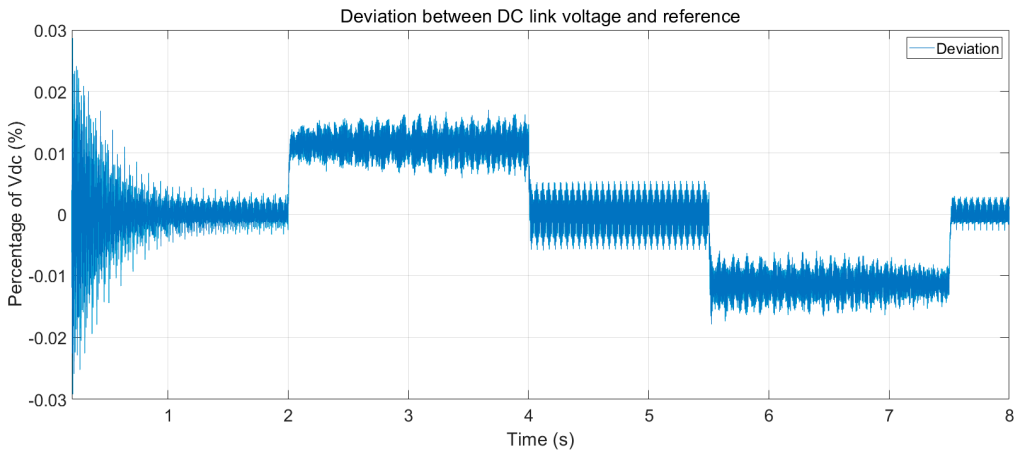

Figure 6. DC link voltage deviation.

As shown in Figure 6, the maximum deviation, excluding initialization, is around 10 volts, which is negligible for a 70 kV DC link. This very low deviation is partially due to the capacitor balancing. The outcome is shown in Figures 7 and 8.

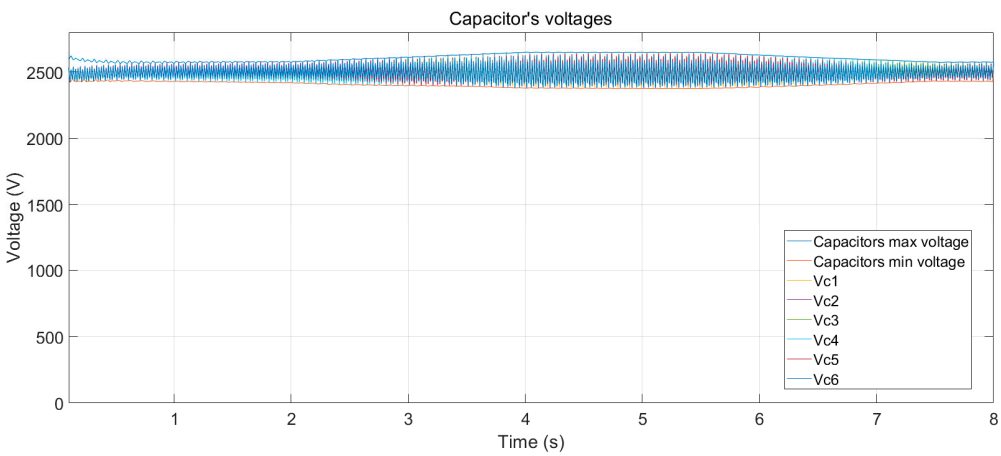

Figure 7. Capacitor voltages for one arm.

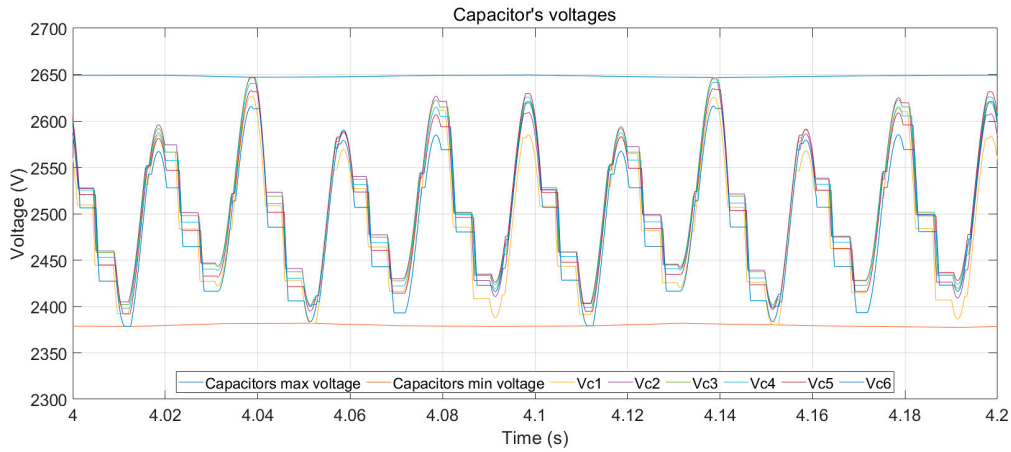

Figure 8. Capacitor voltages for one arm (zoomed-in view).

Minimum and maximum capacitor voltages from Figures 7 and 8 were calculated from the maximum and minimum voltages of all arm capacitors, allowing us to see whether a significant voltage drop occurred without printing all 28 curves. The displayed curves show that they all are balanced and have limited fluctuations.

While the converter must ensure a steady DC link voltage, the other critical feature of this converter is that it ensures good current quality on the grid side. This is why current waveform and THD are measured. Network currents are shown in Figure 9 with zoomed-in views.

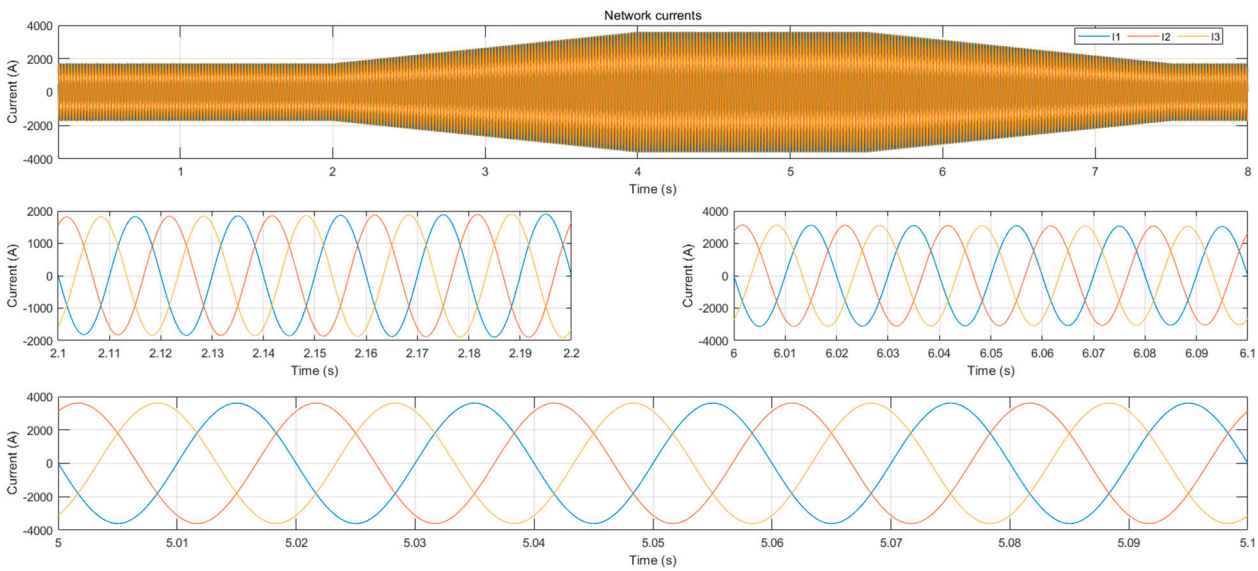

Figure 9. Network currents.

As can be observed, the three phases are well balanced and the measured THD does not exceed 0.5% even during transient phases, which prevents distortion on the grid side and proves the good performance of the system. It is also noted that on the dq-axis, the current components are well aligned with their references, as shown in Figure 10.

All of these results prove the good behavior of the inverter structure when under stress and during transient phenomena. In the next section, the inverter is studied.

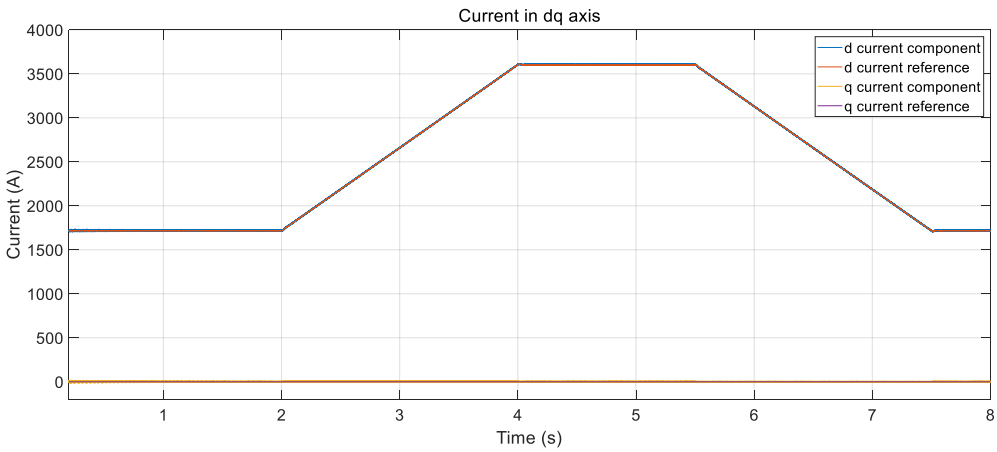

Figure 10. Grid currents in dq-axis.

4. Study of the Catenary-Side Inverter

On the load side, a single-phase MMC inverter is used. This inverter, as shown in Figure 11, connects the load through an output LC filter. This power stage is called a grid-forming inverter, in which the amplitude and frequency can be adapted to the specified power supply of any medium-voltage alternating current (MVAC) railway station.

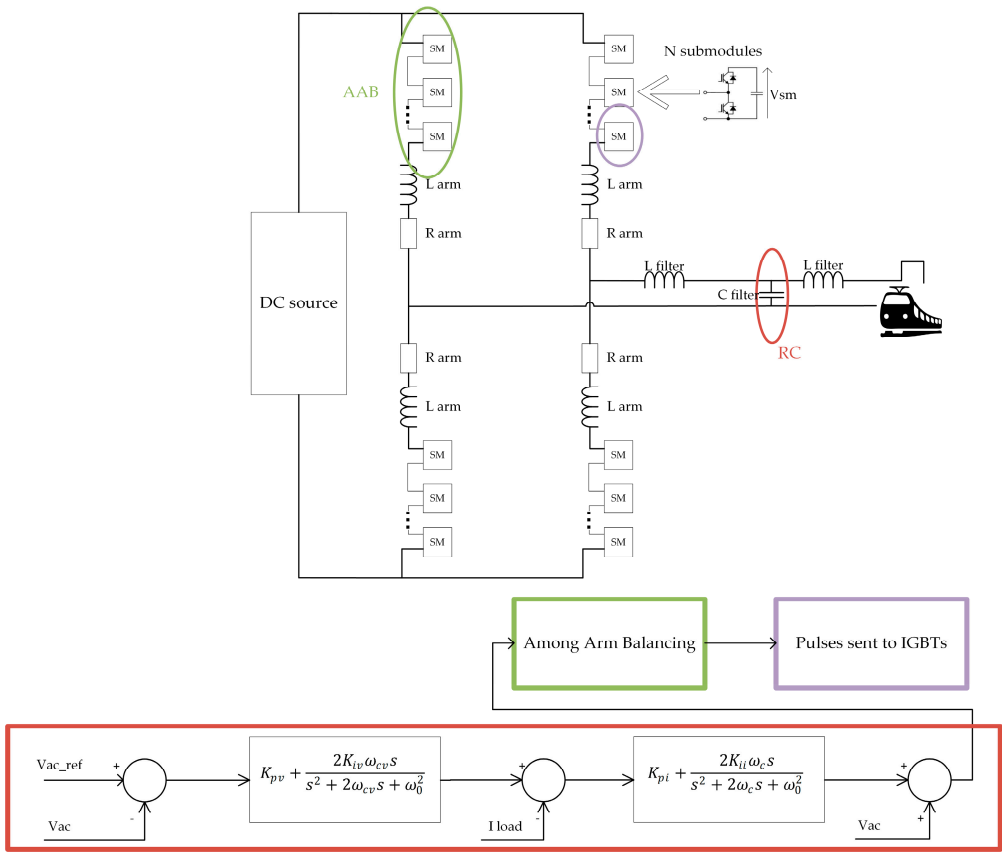

Figure 11. Catenary side with emphasis on resonant controller structure.

The proposed controller is based on imbricated loops, with an external output voltage loop and an inner current loop. The balancing voltage algorithm described in the previous section ensures voltage equilibrium inside the structure. The controllers are based on PR controllers, the transfer function of which is given in Equation (16):

$$G(s) = K_p + \frac{2K_i\omega_c s}{s^2 + 2\omega_c s + \omega_0^2} \tag{16}$$

where K_p is the proportional gain, K_i is the integral gain, ω_0 is the desired frequency around which the system will work and ω_c is the bandwidth of the system.

The transfer functions of inner current and outer voltage loops are expressed in Equations (17) and (18). For the voltage loop, the hypothesis is that the current loop gain is equal to one when the sizing is made. Note that the connection line to the load is not accounted for in order to achieve a robust control law in the presence of uncertainties.

$$H_i(s) = \frac{s^2K_{pi} + s\left(2\omega_{ci}\left(K_{pi} + K_{ii}\right)\right) + K_{pi}\omega_0^2}{Ls^3 + s^2\left(2L\omega_{ci} + K_{pi}\right) + s\left(L\omega_0^2 + 2\omega_{ci}\left(K_{pi} + K_{ii}\right)\right) + K_{pi}\omega_0^2} \tag{17}$$

$$H_v(s) = \frac{s^2K_{pv} + s\left(2\omega_{cv}\left(K_{pv} + K_{iv}\right)\right) + K_{pv}\omega_0^2}{Cs^3 + s^2\left(2C\omega_{cv} + K_{pv}\right) + s\left(C\omega_0^2 + 2\omega_{cv}\left(K_{pv} + K_{iv}\right)\right) + K_{pv}\omega_0^2} \tag{18}$$

where C is the capacitor of the filter, L is the inductance of the filter, K_{pi} and K_{ii} are the gains of the current controller, ω_{ci} is the bandwidth of the current controller, K_{pv} and K_{iv} are the gains of the voltage controller and ω_{cv} is the bandwidth of the voltage controller. The voltage bandwidth is set to be ten times lower than the current bandwidth ($\omega_{cv} = \omega_{ci}/10$) to avoid interaction issues between the two loops. The current loop bandwidth is set to $\omega_{0c} = f_{sw}/5$ to achieve appropriate disturbance rejection and f_{sw} is the apparent switching frequency of the MMC inverter.

Inverter Simulation

As noted in [43,44], railway trains generate significant harmonic content during their journeys, which is a challenge to control and compensate. In order to emulate a railway system, the choice was made to use current sources connected to the output of the LCL filter. The approach is similar to that in [45] with harmonic datasets used as the current source. As stated in [8], the rated power of a TGV is around 8.8 MW, and can be up to 20 MW for a train with multiple units. That is why the power consumption of the next simulation varied from 9.3 to 27.8 MW. The assumption was made that all harmonics would increase proportionally when the current consumption increased, which may not be true with certain configurations [46] but will suffice for this work. Since the data were obtained by measuring at a distribution point, we assumed that the resonance phenomena that could happen in the catenary already happened the moment the measurements were made. The measured current was formatted in the order of frequency rank, amplitude and phase, allowing us to calculate both active and reactive power.

Using the same scenario as the one used for the rectifier, the simulation started with a single train at steady state, and a second train was added at 2 seconds and gradually rose to its steady state, and after 2.5 seconds, deceleration began, leaving the first train alone and at steady state. The global appearance of the operation is depicted in Figure 12.

The current waveform from measurements on thyristor trains explains the highly distorted current with a THD of around 25%, as can be seen in Figure 13.

The catenary voltage was set to achieve an RMS voltage of 25 kV. We measured a significant drop in THD, reaching 2.3%, and the odd harmonics disappeared, complying with the requirements in [47], even during the transient phenomenon, as can be seen in Figure 14.

This current profile combined with the catenary voltage results of the power measurement can be seen in Figure 15.

Since the train's current has harmonics and is not in phase with the voltage, a high reactive power value can be observed. The impact of this reactive power must be limited to the catenary side and must not reach the distribution grid.

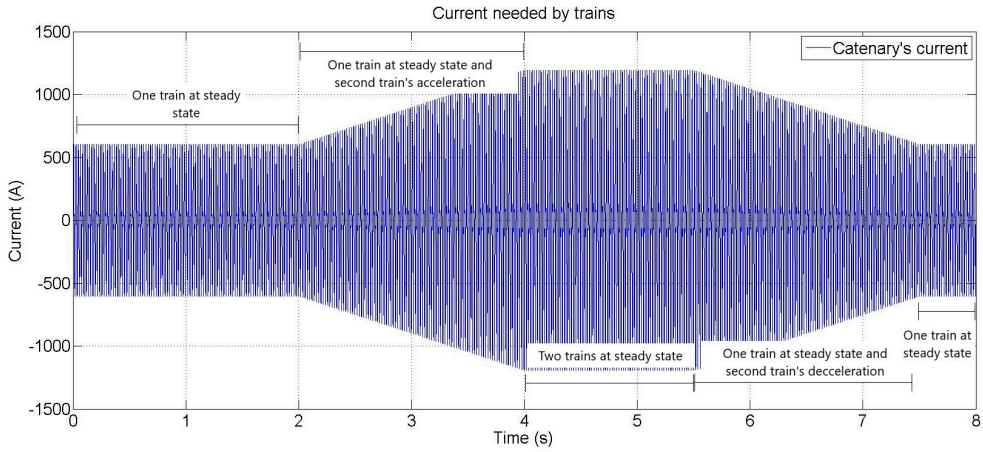

Figure 12. Catenary current with different phases.

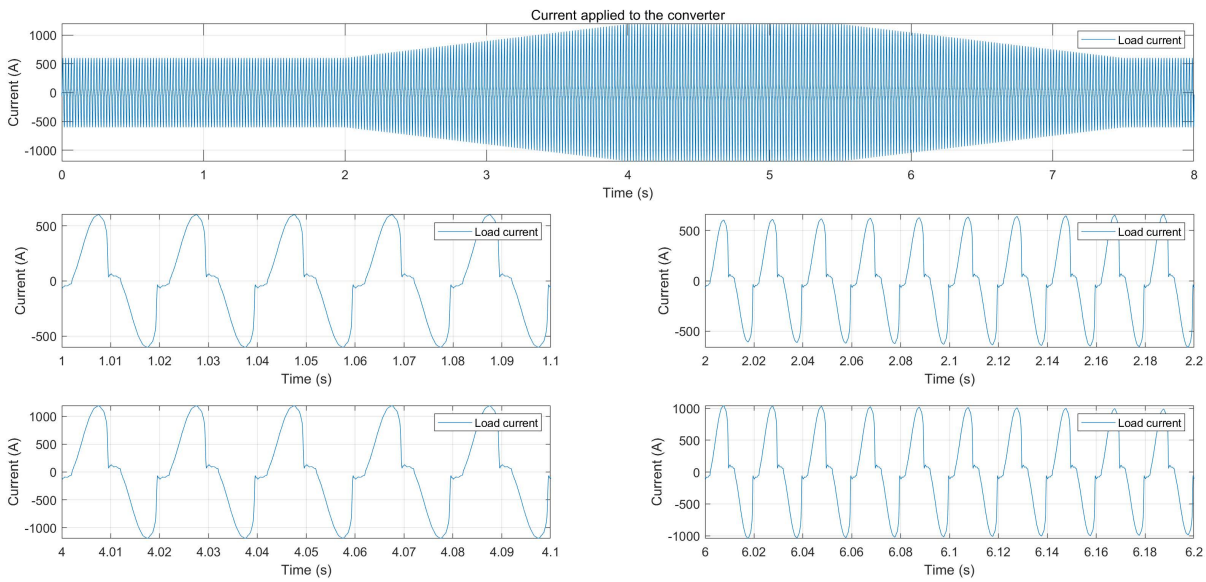

Figure 13. Current applied to catenary in different phases.

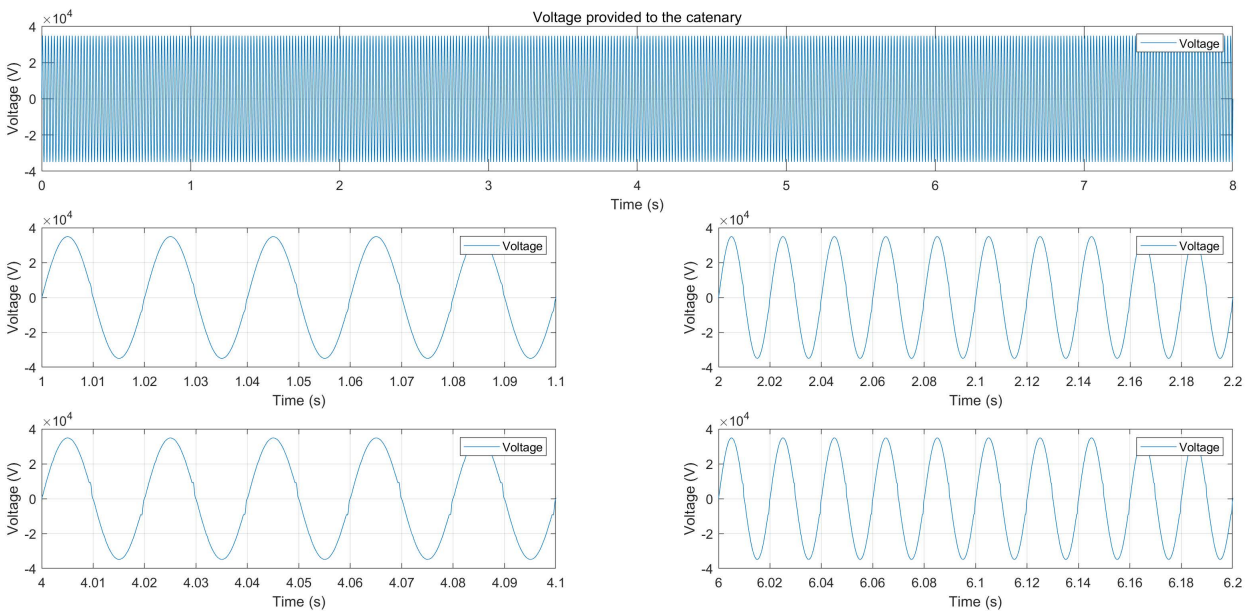

Figure 14. Catenary voltage during different phases.

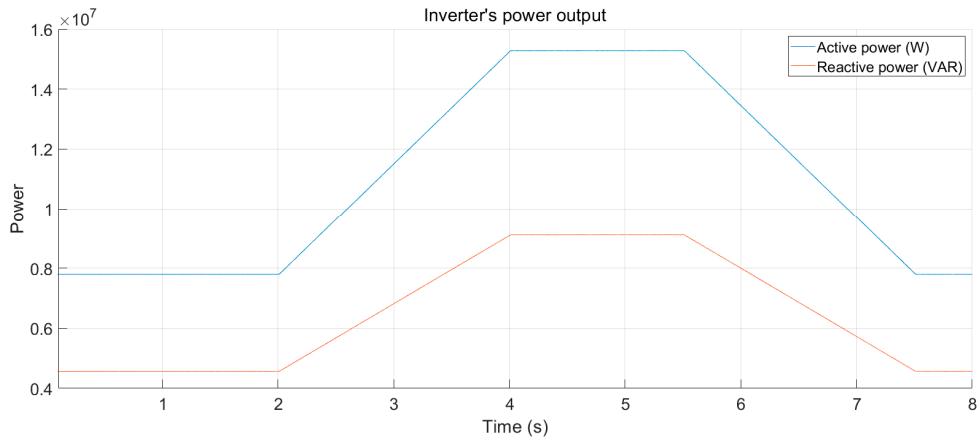

Figure 15. Power output on inverter side.

Capacitor voltages also need to be monitored to ensure that the balancing method provides adequate performance. This requirement is validated, as shown in Figure 16, even though the mean value of voltage is not exactly 2500 volts.

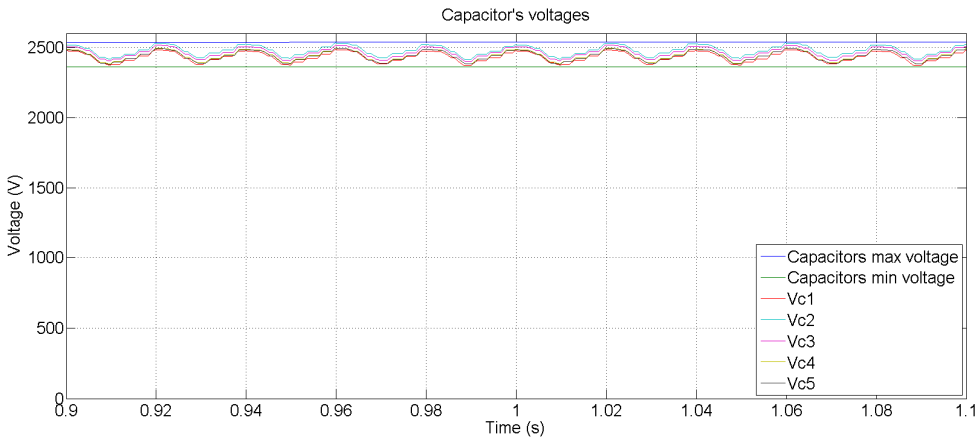

Figure 16. Capacitor voltages.

These results show the good performance of the inverter, even when it has to provide high harmonic currents while preserving good voltage quality on the catenary side.

5. Back-to-Back Structure Using the Simplified Topology

Both converters work in a satisfying range of performance; however, the most important part of the back-to-back structure is that it has to be in a back-to-back configuration and has to be validated in this configuration. To do so, we must connect the converters using the DC link. However, previous work involved significant simulation time, making it difficult to tune the control of both converters while they were connected. To solve this issue, a simplified model for each converter is proposed and compared to the complete models.

To reduce the simulation time and ease the testing of different configurations and loads, a simplified averaged model is used in the rest of this paper. The control structure remains the same as before; the only change is in the converter part of the structure. Each arm of the converter is replaced by the components presented in Figure 17.

This architecture implies that the internal arm voltage balance is strong enough to get rid of voltage information from each capacitor. Before the back-to-back simulation is carried out, the behavior of the converters is compared.

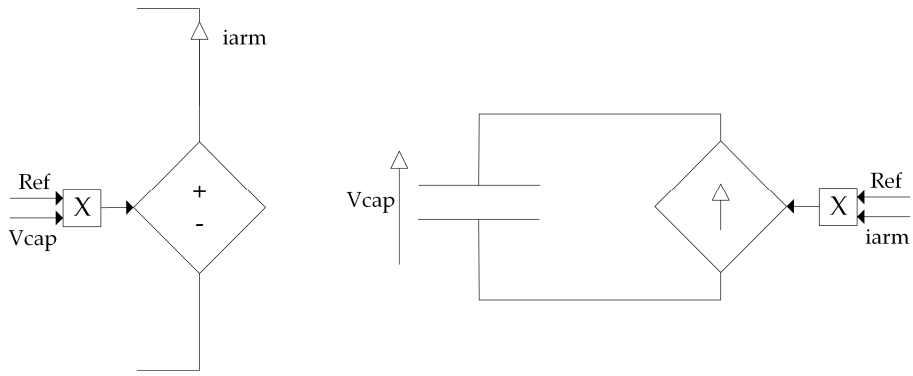

Figure 17. Simplified arm model.

5.1. Simulation of Simplified Rectifier

First, we must ensure that the simplified rectifier produces the same results as the IGBT model. The main aspects to be monitored are the arm voltage, the DC link voltage and the grid-side current.

Even if the capacitors are not included in this simplified model and therefore cannot be monitored, arm voltage control is still implemented and must be taken into account when validating the model's operation. Both arm voltages are shown in Figure 18.

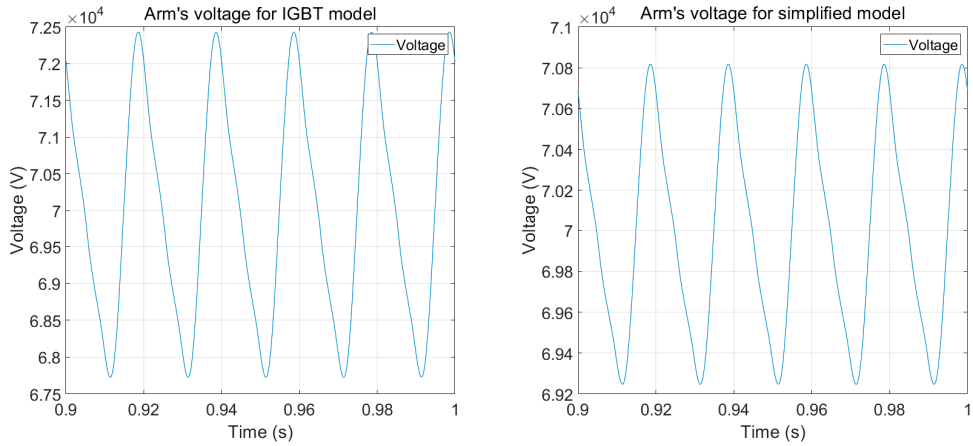

Figure 18. Arm voltage for IGBT model and simplified model.

A difference in the ripple magnitude can be observed between the models, but they share the same ripple frequency and their average value is the same, which is the main concern for a simplified and averaged model. The second observed component is a direct link to the arm voltage, similar to the DC link voltage. Maintaining a stable DC link voltage is crucial when interfacing the rectifier with an inverter or a long cable. That is why it is important to ensure that this part is working as it should. Both models are shown in Figure 19.

In steady state, both models produce identical results, with a difference of less than 1 volt.

Finally, the grid-side currents are analyzed, as shown in Figure 20.

Once again, the results for the converters are similar, with a low THD and similar values, validating the average behavior of the simplified rectifier and making it suitable for the rest of the study.

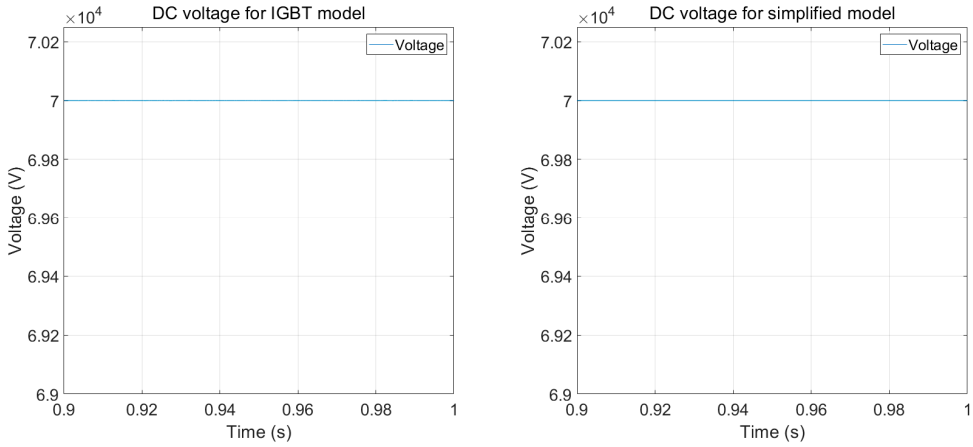

Figure 19. DC link voltage for both models.

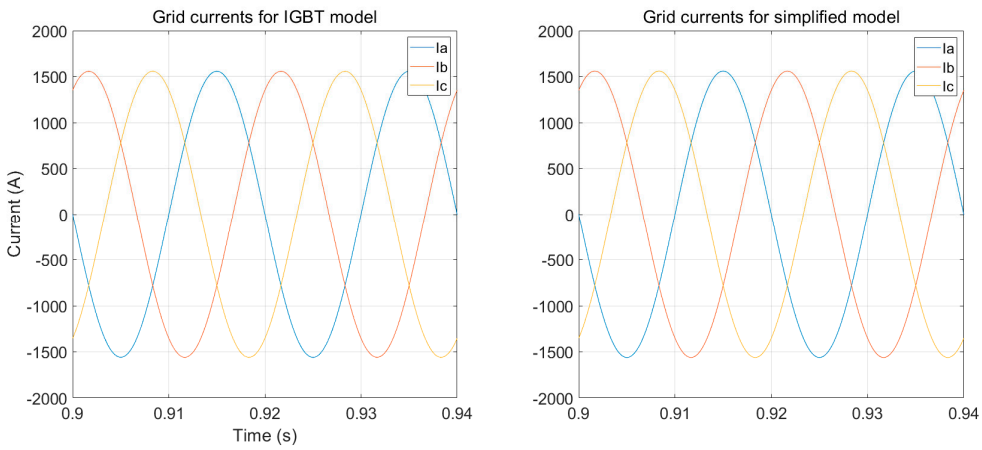

Figure 20. Grid side-current for both models.

5.2. Simulation of Simplified Inverter

For this part of the converter, the main concern is the catenary voltage, which must remain at an RMS value of 25 kV during the main time period to ensure the required performance of the rolling stock. The second concern is common for the rectifier, as it concerns the capacitor voltage or, more precisely, the arm voltage, which must be close to the IGBT model, if not the same. Both of these voltages are presented in Figure 21.

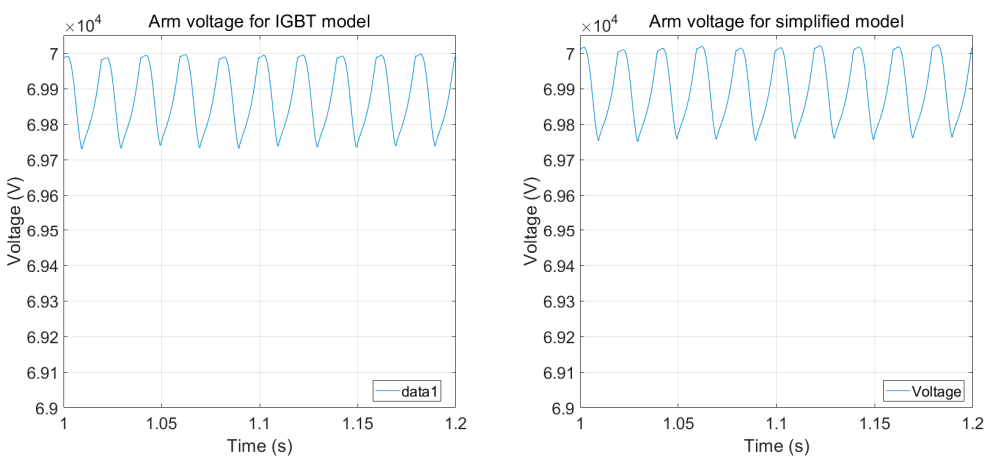

Figure 21. Arm voltage for both models.

As it can be observed in the figure above, arm voltages are way closer than they were in the rectifier model. In the same way that in happened in the previous comparison, their ripple follows the same frequency, now have the same amplitude and consequently have the same average value.

The last round of comparison is made between the two catenary voltages in Figure 22.

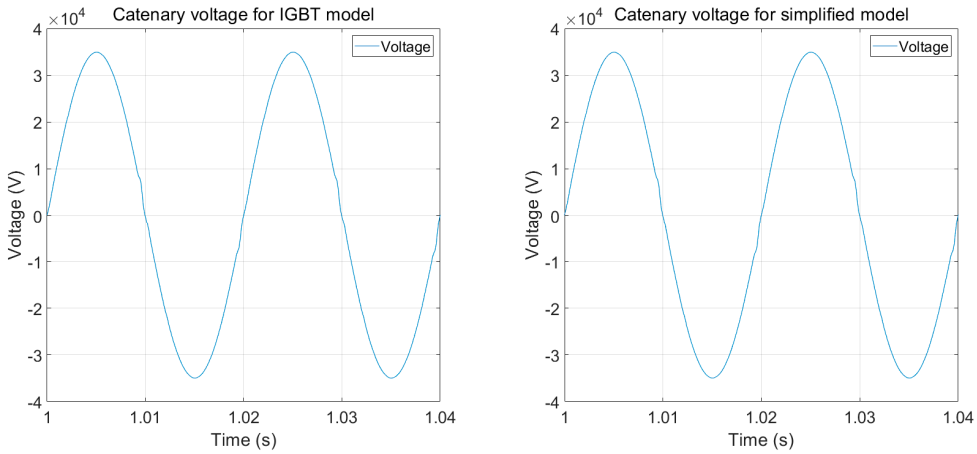

Figure 22. Catenary voltage for both models.

The simplified model provides the same voltage as the model with the IGBTs, with similar THD and RMS, proving the validity of the model for the desired application.

Further results are shown in Table 1, comparing both models at steady state using their average values, where the voltage offset is defined as the mean value of the difference between the regulation and the output of the system.

Table 1. Comparison between models.

	IGBT	Simplified	Error
	Rectifier side		
Arm voltage (V)	69,833.1	70,061.5	228.4 (0.3%)
DC link current (A)	80.1	80.09	0.009 (0.012%)
Voltage offset (V)	11.84	11.7	0.14 (1.18%)
THD network currents (%)	0.003	0.001	0.002 (200%)
	Inverter side		
THD catenary (%)	0.01	0.01	0 (0%)
Voltage offset (V)	7.01	−4.63	11.64 (166%)

As both averaged converters have precise behavior regarding static and dynamic states, they can be used to build a back-to-back averaged model by connecting them.

5.3. Back-to-Back with Railway-like Loads

The same current profile, as depicted in Figure 14, is used in the simplified back-to-back converter; therefore, we can use the same comparison basis to validate the back-to-back system. First, we make sure that the catenary's side voltage remains the same as it was when the inverter was operating alone.

From Figure 23, it can be seen that the voltage is similar, with a slight decrease in THD from 2.3% to 1.7%. This might be due to the lack of commutations, especially since the system with IGBTs commutes at the relatively low frequency of 320 Hz. The THD is even lower when we investigate the rectifier side and grid currents, which tend to be around 0.5% for the three of them, as shown in Figure 24.

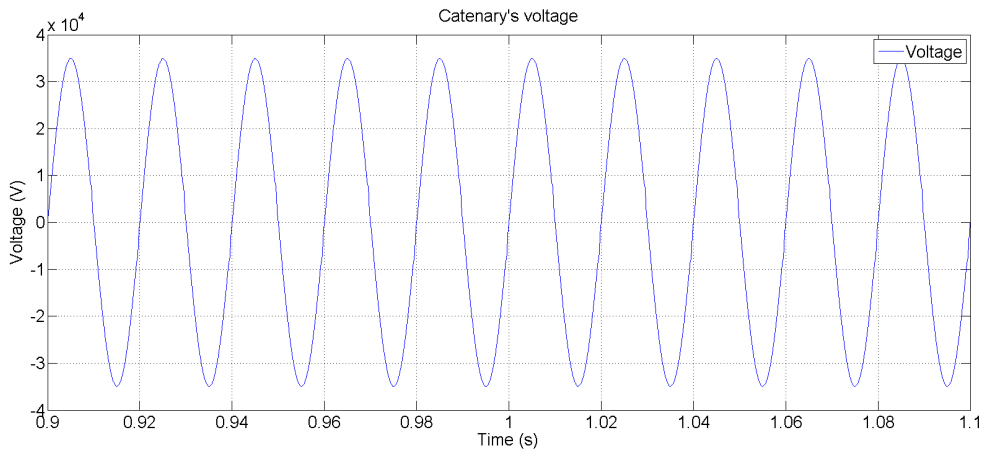

Figure 23. Catenary voltage for simplified model.

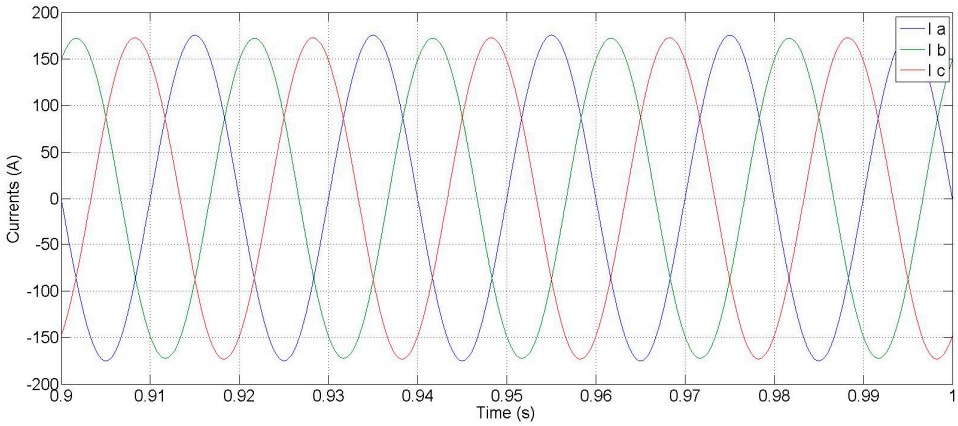

Figure 24. Grid-side currents for simplified model.

Regarding a performance review, input current and output voltage must be studied to ensure they comply with the requirements, such as those in [47] for the inverter side and [48] for the grid side.

Regarding the grid side, IEEE Standard 519 states that harmonic currents should be, in the worst case, less than the values given in Table 2.

Table 2. Current distortion limits for systems rated 120 V through 69 kV.

Maximum Harmonic Current Distortion, % of I_L					
Individual harmonic order					
$2 \leq h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h < 50$	TDD
4	2	1.5	0.6	0.3	5

To compare these values with the value from our model, we use a discrete Fourier transformation. The main frequency is set to 50 Hz, as this is the catenary frequency we want. The vector obtained is then normalized using the component at the desired frequency, here 50 Hz. These values are then converted to percentages, resulting in a moving THD, as in [46,49], with substation measurements, allowing us to compare them with the values in Table 2.

Comparing the measured values to the standard ones, it can be seen that none of the harmonics are over the threshold and that higher distortion occurs during the load increase, as can be observed in Figure 25.

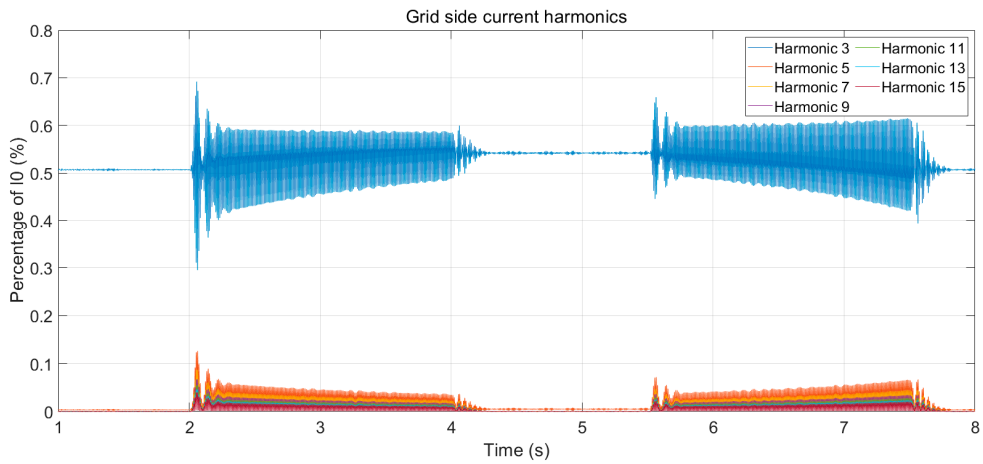

Figure 25. Harmonic distortion for grid currents.

As shown in Figure 25, one curve is not grouped with the others—the curve corresponding to the third-rank harmonic, which oscillates around 0.5%—while the others never go over 0.3%, completely complying with IEE 519, and this is the case for the three phases. It can then be concluded that the rectifier part of the converter works satisfactorily, preventing the propagation of harmonics created by the load and reducing the impact on the power grid.

For the catenary side, the studied standard is IEC 62498-1 [47], which indicates the amount of harmonics that is tolerated for equipment compatibility. The harmonic percentages are given in Table 3.

Table 3. Compatibility levels of harmonic components.

Compatibility Levels of Odd Harmonic Components													
Order of harmonic	3	5	7	9	11	13	15	17	19	21	23	25	>25
Percentage of nominal line voltage	15	8	7	6	5	4.5	4.5	4	4	4	3.5	3.5	$5\left(\frac{11}{h}\right)^{\frac{1}{2}}$
Compatibility levels of even harmonic components													
Order of harmonic	2	4	>6										
Percentage of nominal line voltage	3	1.5	1										

It should be noted that these are not the values that are imposed on the catenary voltage; rather, they are the values under which the equipment must perform as specified. Therefore, these values can be defined as the maximum reachable values, since they have no impact on the equipment. With that information in mind, the voltage harmonics are calculated the same way as the current harmonics, as shown in Figure 26.

Similar to the current spectrum, the only voltage harmonic over 1% is the third-rank harmonic, which goes up to 0.68%, considerably below the 15% of the standard. The RMS value of the voltage also must be considered, as it cannot have variation higher than 20%. The results of the simulation have a variation of 0.12%, which fits the requirements.

Finally, we can look at the power coming from the grid and the power needed by the trains to ensure improved power quality. Both sides of the system are depicted in Figure 27.

As can be observed from Figure 27, the reactive power generated by the trains is almost brought to zero on the rectifier side, protecting the grid from power fluctuations induced by thyristor trains.

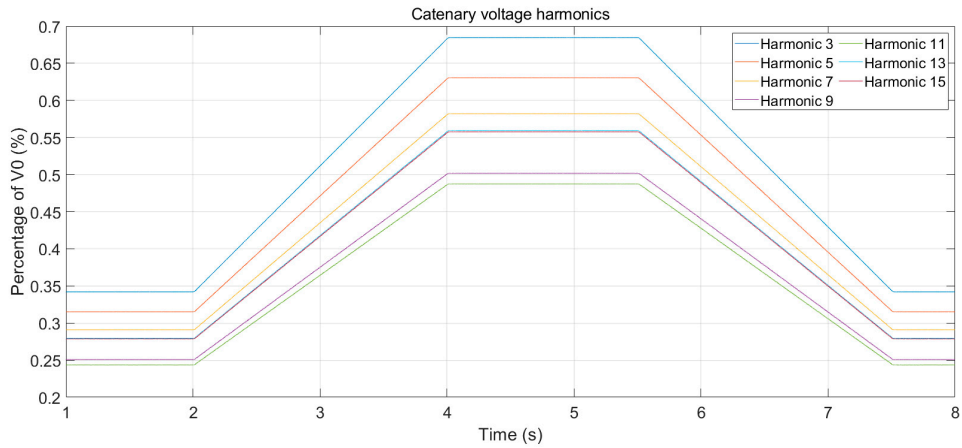

Figure 26. Harmonic distortion for catenary voltage.

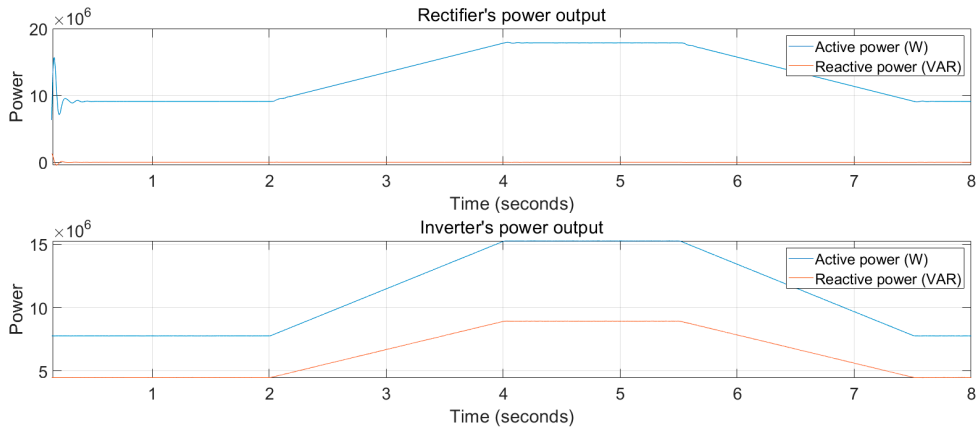

Figure 27. Power flows for both sides.

6. Conclusions

This paper evaluates the feasibility of using a back-to-back converter to power 25 kV–50 Hz railway electrical networks with industrial constraints. We demonstrate that both parts of the converter work separately and provide satisfactory results for grid current and catenary voltage. The connection of the two converters allows the creation of a back-to-back converter that combines the benefits of both architectures.

The last part of this work shows promising results for power quality improvement of railway electrical networks. Eliminating harmonic components can indeed increase the reliability of the installation and reduce the impact on the distribution grid, thus improving the implementation of decentralized means of production. It also shows that this topology can support high power variations, which can be a key point in places where multiple trains are powered at the same time, such as train stations.

It should be noted that the performance can be improved since the model does not take into account the switching frequency of the IGBTs, since improving their switching frequency also increases the power quality as well as losses. Therefore, further research must be conducted to find a compromise between the gain coming from the power quality improvement and the increased losses. It would then be possible to study only a part of the converter using a full model while using a simplified model for the other part. This configuration would allow us to focus on specific events such as a drop in grid voltage, resonance issues, short circuits on the catenary side or even submodule faults in one side of the converter or in another converter connecter through the catenary, the grid or both.

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