energies

MDPI

Article

Novel Single-Stage Electrolytic Capacitor-Less Buck-Boost Inverter

Youn-Ok Choi [1] and Khai M. Nguyen [2,*]

[1] Department of Electrical Engineering, Chosun University, Gwangju 61452, Republic of Korea; yochoi@chosun.ac.kr
[2] Department of Electrical and Electronics Engineering, Ho Chi Minh City University of Technology and Education, Ho Chi Minh City 700000, Vietnam
* Correspondence: khainm@hcmute.edu.vn

Abstract: Nowadays, single-phase, single-stage, buck-boost power inverters are mostly considered to be used for renewable energy source applications due to their wide range of capabilities. This article introduces a novel, single-phase, single-stage, buck-boost inverter with a wide range of input DC voltage. In addition, the introduced inverter does not use the electrolytic capacitor, which enhances the lifetime and volume reduction in the inverter, avoids the high equivalent series resistance, and reduces the inrush current of electrolytic capacitors in the introduced inverter. Moreover, the introduced inverter exhibits a reduced switch voltage rating, and the novel PWM control strategy with the half-cycle of the sinusoidal is derived to reduce the switching loss of power switches, thus improving the inverter's efficiency. The operation states, theoretical analysis, and design of components are fully discussed. A comparative study of the introduced inverter with other buck-boost inverter topologies is also reported. Finally, the 500 W laboratory prototype is set up for simulation and experimental verification. The experimental results verify the correctness of operating analysis and simulation.

Keywords: buck-boost inverter; single-phase inverter; transformer-less PV inverter; single-stage

check for updates

Citation: Choi, Y.-O.; Nguyen, K.M. Novel Single-Stage Electrolytic Capacitor-Less Buck-Boost Inverter. *Energies* **2024**, *17*, 6191. https://doi.org/10.3390/en17236191

Academic Editor: José Gabriel Oliveira Pinto

Received: 24 October 2024
Revised: 30 November 2024
Accepted: 4 December 2024
Published: 8 December 2024

Copyright: © 2024 by the authors. Licensee MDPI, Basel, Switzerland. This article is an open access article distributed under the terms and conditions of the Creative Commons Attribution (CC BY) license (https://creativecommons.org/licenses/by/4.0/).

1. Introduction

Recently, renewable energy sources have emerged as a promising option for adopting clean and pollution-free energy solutions. Compared with other renewable sources, solar energy technology has become a good solution due to its numerous advantages of sufficient reserves, friendly environment, and easy improvement [1–3]. As the core component of distributed generation, the grid-connected inverter has become the research hotspot of many researchers. In addition, renewable energy sources are connected to the grid system by adding power electronics inverters. In general, a series connection of solar photovoltaic panels is used to deliver a high direct current (DC) bus feed to an inverter. Based on the galvanic isolated characteristics of the transformer, the common-mode leakage current is successfully eliminated in the isolated inverter. Although the transformer-based inverter can offer isolation and protection, it has the disadvantages of the transformer, such as its heavy weight, high cost, difficult installation, and decreased efficiency of the overall system [4,5]. Alternatively, the transformer-less inverter can reduce the inverter's price and mass and improve efficiency. The voltage-source inverter is considered for use between solar photovoltaic panels and the grid. Various structures, including an H-bridge with five switches (H5) [6], a modified H5 [7], a family of H6 [8], and a HERIC inverter structure [9], can be considered to replace the conventional full-bridge topology.

In addition, the conventional voltage source inverter only performs the buck function in the DC–AC inverter, where the output voltage amplitude should be lower than the DC bus voltage [10–13]. In some partial operation conditions, the DC bus voltage is significantly degraded and there is not enough voltage to maintain grid-connected operation. This leads

to a wider range of output of solar photovoltaic systems. Then, the boost function of the power inverters is required to solve this problem, and an additional boost converter is connected before the voltage-source inverter to handle the boost function [14–16]. This means the system has two-stage power conversion for controlling the step-up or step-down of the input DC bus voltage. However, the disadvantages of the two-stage structure topologies include low efficiency, high price, and difficulty with control in each stage. On the other hand, the single-stage structures with both boosting and bucking abilities are flexible enough to be controlled with a wide range of input voltage. The single-stage configuration has some advantages such as small volume, a lower number of components, low cost, and efficiency improvement [17,18], helping it to overcome a two-stage structure. From this perspective, single-stage buck-boost structures are present in the literature [19–29].

In [22], an active buck-boost inverter was introduced by using the full-bridge inverter unit. Nevertheless, this topology is not effective because many power switches are used, and high conduction loss occurs. The single-stage boost inverter including two boost modules [23] is proposed to provide a buck-boost function. However, it uses many passive components. The Z-source inverter was developed with an X-shape of inductors and capacitors in the first stage. For the second stage of the Z-source inverter, the full H-bridge circuit provides a shoot-through state for buck-boost operation with a single stage [24]. The dual-boost DC–AC inverter is proposed in [25], which uses a half-cycle modulation scheme to address the high loss of inductors because of the high circulating current in the boost inductors. This topology can provide high efficiency because the dual switch is switched at a high frequency. Despite these improvements, this structure has the disadvantage of using many inductors. To reduce the size of magnetic devices, a Manitoba buck-boost inverter [26] was recently introduced. In this structure, two inductors are operated for the buck-boost function and reduce the high-frequency switching device of the grid side. However, the drawback of the Manitoba buck-boost inverter is that it requires eight semiconductor switches, and all inductors require a high current rating. In addition, differential boost converters with split inductors were proposed in [27]. However, this structure gives higher switching and conduction losses. The virtual-ground buck-boost inverter [28] was proposed with low common-mode voltage. However, this inverter requires seven power switches and two output filter capacitors. The novel dual buck and boost inverter is also proposed in [29] by adding two more switches to the two buck-boost modules. Different from the conventional buck-boost inverter, this inverter can work in the pure full-bridge mode and reduce the current flow through two capacitors. Nevertheless, many power switches are used to utilize dual-mode time sharing, which increases the loss of switching devices.

This article introduces the new single-stage, single-phase, buck-boost inverter (S^2B^2I) to offer the buck-boost ability in single-stage power conversion. The half-cycle modulation strategy is derived to decrease the losses of power switches and generate the half-sinusoidal waveform on the capacitors. Then, the small-film capacitors can be employed in the proposed S^2B^2I to enhance the lifetime of the inverter without the inrush current using electrolytic capacitors in traditional inverters. The remainder of this article is structured as follows: Section 2 outlines the new structure and the derived PWM control scheme of the proposed S^2B^2I, along with detailed descriptions of its operating modes. Section 3 discusses component selection. Section 4 provides a comparative analysis. Section 5 presents extensive simulations. Section 6 details the experiments that validate the operating principles of the introduced S^2B^2I. Finally, Section 7 concludes the article.

2. Proposed S^2B^2I

2.1. Topology

The proposed S^2B^2I is shown in Figure 1. It is composed of eight switches (S_1–S_8), two inductors (L_1, L_2), two leg capacitors (C_1, C_2), and one output capacitor (Co). Capacitors C_1 and C_2 are used for filtering and snubbing. The introduced S^2B^2I features a symmetrical design that incorporates two buck-boost modules. Module A on the right side seen from the input voltage V_i, is built by switches S_1–S_4, inductor L_1, and capacitor C_1. Similarly,

module B on the left side, seen from the input voltage V_i, is formed by switches S_5–S_8, inductor L_2, and capacitor C_2. The proposed S^{2}B^{2}I also uses a dual-mode control method. More specifically, the switches of module A operate at a high frequency during the positive half of the output cycle, while the switches of module B operate at a high frequency during the negative half of the output cycle.

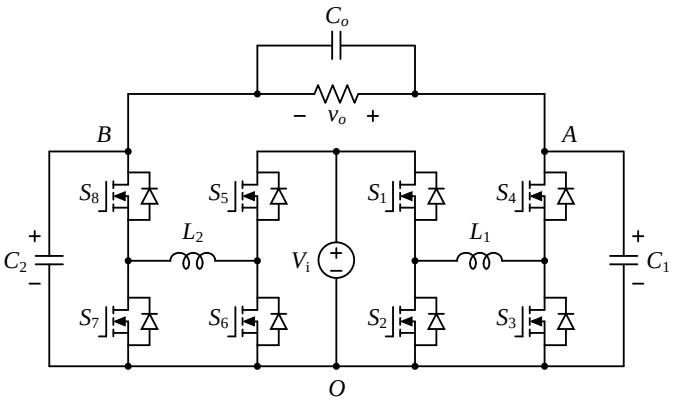


Figure 1. Proposed S^{2}B^{2}I.

2.2. Derived PWM Strategy

The PWM switching strategy of the proposed S^{2}B^{2}I is shown in Figure 2. The main purpose of this control strategy is to generate a positive voltage with a half-sinusoidal waveform on capacitors C_1 and C_2 for modules A and B, respectively. The peak of the output voltage of the modules is the same in amplitude, but the phase angle of module B is shifted 180° compared to module A, which means that the four switches of module B are controlled by the phase shift of 180° from the four switches of module A.

In the interval of ($0 < \omega t \leq \pi$), switches S_1–S_4 work at a high frequency and do not change the switching state in ($\pi < \omega t \leq 2\pi$), while switches S_5–S_8 operate at a high frequency in the negative half of the output cycle ($\pi < \omega t \leq 2\pi$). Thus, the four switches of modules A and B just operate at high switching in half of the output sinusoidal waveform. The output voltage of module A and module B can be expressed as follows:

$$v_A(t) = \begin{cases} V_o \sin(\omega t), & 0 < \omega t \leq \pi \\ 0, & \pi < \omega t \leq 2\pi \end{cases} \quad (1)$$

$$v_B(t) = \begin{cases} 0, & 0 < \omega t \leq \pi \\ V_o \sin(\omega t - \pi), & \pi < \omega t \leq 2\pi \end{cases} \quad (2)$$

where $V_o = 2V_m$ and ω are the peak inverter output voltage and the output voltage line frequency, respectively.

The output voltage can be achieved by finding the difference between v_A and v_B:

$$v_o(t) = v_A(t) - v_B(t) = V_o \sin(\omega t) \quad (3)$$

The proposed S^{2}B^{2}I operates in boost mode when the output voltage amplitude is greater than the input DC voltage V_i. In contrast, the inverter operates in step-down mode when the output voltage amplitude is below V_i. It can be seen that the two modules are similar, so the following analysis will focus on module A. In addition, when the output voltage of module A is higher than V_i, module A operates in boost mode from t_1 to t_2, as shown in Figure 2. In this case, switches S_3 and S_4 work at a high frequency, while S_1 is ON and S_2 is OFF. When the output voltage of module A is less than V_i, the operation of module A is in buck mode from 0 to t_1 and t_2 to 2π, as shown in Figure 2. Switches S_1 and S_2 work at a high frequency, while S_3 is OFF and S_4 is ON.

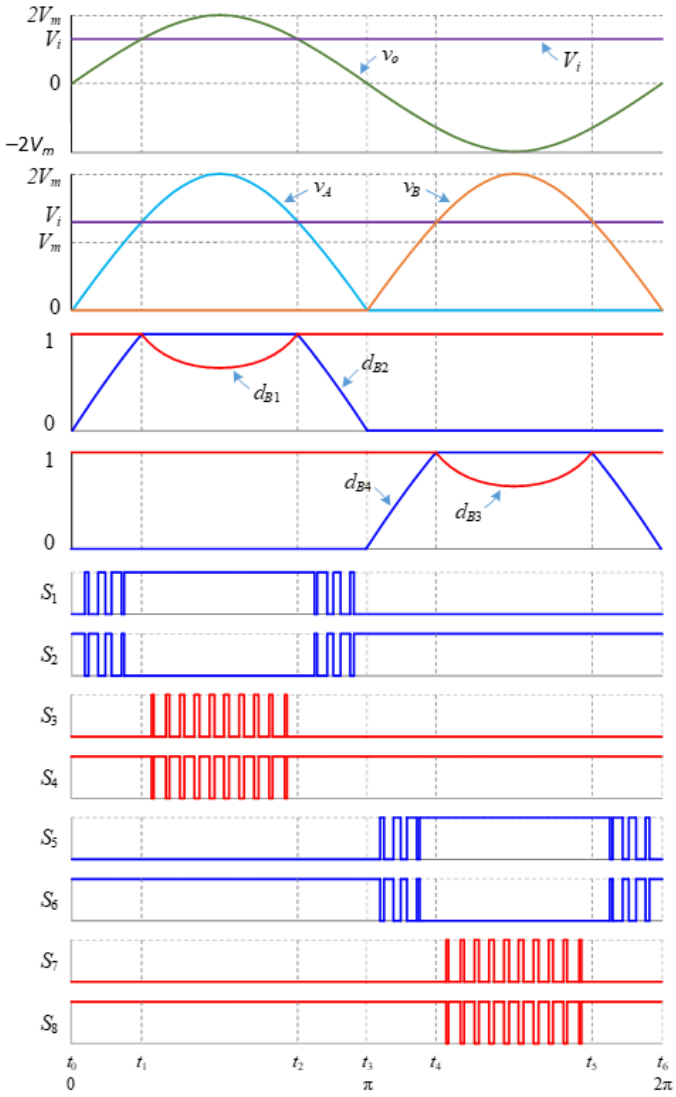


Figure 2. Derived PWM switching scheme of the proposed S^2B^2I.

Based on the difference between the output voltage of module A and V_i, the operation partition of the boost and buck modes is determined as follows:

Boost mode:

$$m_A(t) > 1,\ t_1 < t \leq t_2 \tag{4}$$

Buck mode:

$$m_A(t) \leq 1,\ \begin{cases} t_0 < t \leq t_1 \\ t_2 < t \leq t_3 \end{cases} \tag{5}$$

where m_A is the modulation factor, which is well-defined as the ratio between the output voltage of module A and the input voltage and given by

$$m_A(t) = \frac{v_A(t)}{V_i} \tag{6}$$

PWM signals in boost mode and buck mode are controlled with the duty cycle of d_{B1} and d_{B2}, respectively, and can be derived from

$$d_{B1}(t) = \begin{cases} \frac{1}{G\sin(\omega t)},\ t_1 < t \leq t_2 \\ 1,\ t_0 < t \leq t_1 \ and\ t_2 < t \leq t_6 \end{cases} \tag{7}$$

$$d_{B2}(t) = \begin{cases} G\sin(\omega t),\ t_0 < t \le t_1 \text{ and } t_2 < t \le t_3 \\ 1,\ t_1 < t \le t_2 \end{cases} \tag{8}$$

$$t_1 = \frac{1}{\omega}\sin^{-1}\left(\frac{1}{G}\right) \tag{9}$$

$$t_2 = \frac{1}{\omega}\left[\pi - \sin^{-1}\left(\frac{1}{G}\right)\right] \tag{10}$$

Similar to module A, the operating modes of module B are controlled with the duty cycle of d_{B3} and d_{B4} and are given by

$$d_{B3}(t) = \begin{cases} \frac{1}{G\sin(\omega t - \pi)},\ t_4 < t \le t_5 \\ 1,\ t_0 < t \le t_4 \text{ and } t_5 < t \le t_6 \end{cases} \tag{11}$$

$$d_{B4}(t) = \begin{cases} G\sin(\omega t - \pi),\ t_3 < t \le t_4 \text{ and } t_5 < t \le t_6 \\ 1,\ t_4 < t \le t_5 \end{cases} \tag{12}$$

where G is the voltage gain, which is defined as the output voltage amplitude V_o to the input voltage V_i:

$$G = \frac{V_o}{V_i} \tag{13}$$

2.3. Operating Mode

As shown in Figure 2, once the input voltage is higher than the output voltage, more specifically the input voltage is higher than the voltage on capacitor C_1 and capacitor C_2, the buck mode of the proposed S^2B^2I starts. The proposed inverter has four operating modes in this mode, as shown in Figure 3a,b,d,e. Modes 1 and 2, as shown in Figure 3a,b, are the operating modes in buck mode when $v_o > 0$. Modes 4 and 5, as shown in Figure 3d,e, are the operating modes in buck mode when $v_o < 0$.

When the input voltage is lower than the output voltage, the boost mode of the proposed S^2B^2I starts. Modes 2 and 3, as shown in Figure 3b,c, are the operating modes in boost mode when $v_o > 0$. Modes 5 and 6, as shown in Figure 3e,f, are the operating modes in boost mode when $v_o < 0$.

Mode 1 (Figure 3a): switches S_2, S_4, S_6, and S_8 are ON and S_1, S_3, S_5, and S_7 are OFF; L_1 and C_1 discharge to load through S_6, S_8, and L_2. The inductor current L_1 decreases as

$$\frac{di_{L1}(t)}{dt} = \frac{v_A}{L} \tag{14}$$

where L is the inductance of L_1 and L_2.

Mode 2 (Figure 3b): switches S_1, S_4, S_6, and S_8 are ON and S_2, S_3, S_5, and S_7 are OFF. V_i and L_1 charge C_1 and supply power to the load through S_6, S_8, and L_2. The slope of the inductor current L_1 in terms of V_i and V_A can be expressed as

$$\frac{di_{L1}(t)}{dt} = \frac{V_i - v_A}{L} \tag{15}$$

Mode 3 (Figure 3c): switches S_1, S_3, S_6, and S_8 are ON and S_2, S_4, S_5, and S_7 are OFF. L_1 stores energy from V_i and C_1 discharges to load through S_6, S_8, and L_2. The inductor current L_1 increases as

$$\frac{di_{L1}(t)}{dt} = \frac{V_i}{L} \tag{16}$$

Modes 4–6: These modes are technically identical to Modes 1, 2, and 3. Switches S_5–S_8 in module B operate at a high frequency, while switches S_1, S_3, and S_2, S_4 in module A are OFF and ON, respectively.

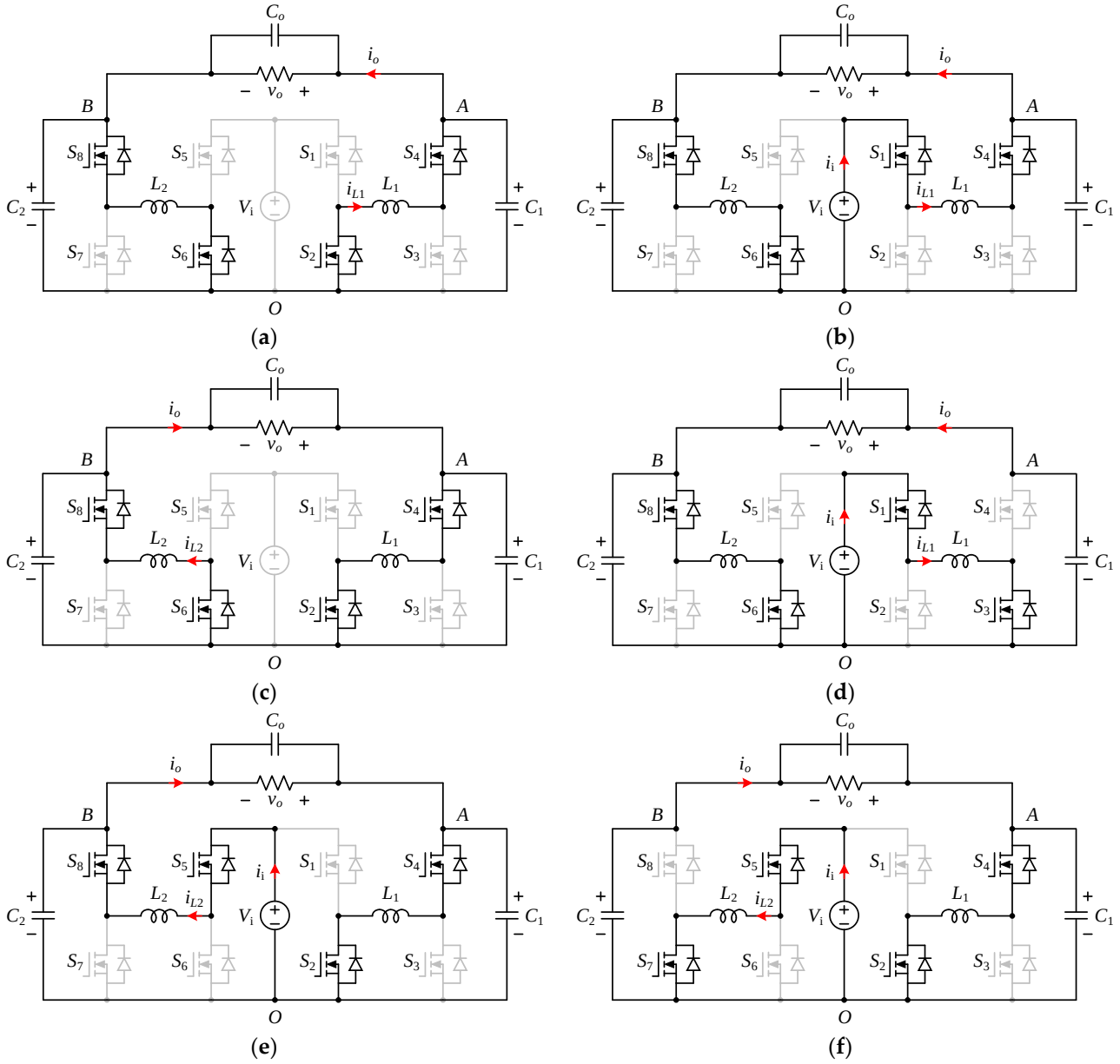


Figure 3. Operational modes of the proposed S^{2}B^{2}I. (**a**) Mode 1. (**b**) Mode 2. (**c**) Mode 3. (**d**) Mode 4. (**e**) Mode 5. (**f**) Mode 6.

3. Components Design Guideline

3.1. Inductance Selection

Assuming I_o is the peak value of the load current of the proposed S^{2}B^{2}I, the equation for the output current is

$$i_o(t) = I_o \sin(\omega t + \theta) \tag{17}$$

where θ is the phase angle of the output voltage and load current.

The current inductor waveform is a non-sinusoidal waveform during step-up operation ($G > 1$). The maximum current inductor is obtained as

$$i_L(t) = I_o G \tag{18}$$

The current ripple of the inductor is defined by

$$\Delta i_{L\max} = (1 - d_{Bo_\max}) \frac{V_i}{L f_{sw}} = \left(1 - \frac{1}{G}\right) \frac{V_i}{L f_{sw}} \tag{19}$$

In step-down operation ($G < 1$), the inductor current waveform is sinusoidal and the same as the output current. However, there is a high-frequency component when the current through the inductors is positive; this ripple value is given by

$$\Delta i_{L\max} = \frac{V_i}{4Lf_{sw}} = \frac{V_i}{4Lf_{sw}} \tag{20}$$

Rearranging (14) and (15), inductors L_1 and L_2 can be calculated by

$$L = \begin{cases} \left(1 - \frac{1}{G}\right) \frac{V_i}{\Delta i_{L\max} f_{sw}}, \; G > 1 \\ \frac{V_i}{4\Delta i_{L\max} f_{sw}}, \; G \leq 1 \end{cases} \tag{21}$$

In the abovementioned equation, $\Delta i_{L\max} = x\% \times I_L$. Based on this value, inductor L can be determined as

$$L = \begin{cases} \left(\frac{G-1}{G^2}\right) \frac{V_i}{x\% \cdot I_o \cdot f_{sw}} & (G > 1) \\ \frac{V_i}{4x\% \cdot I_o \cdot f_{sw}} & (G \leq 1) \end{cases} \tag{22}$$

3.2. Capacitance Selection

The capacitor voltage ripple is different in the boost and buck modes. The voltage ripple of the capacitor is defined by

$$\Delta V_{C\max} = \begin{cases} (1 - d_{Bo_\max}) \frac{I_o}{C \cdot f_{sw}} = \left(1 - \frac{1}{G}\right) \frac{I_o}{C \cdot f_{sw}} \; (G > 1) \\ \frac{\Delta i_{L\max}}{8.C.f_{sw}} = \frac{V_i}{32L \cdot C \cdot {f_{sw}}^2} \; (G < 1) \end{cases} \tag{23}$$

We choose the limit of the maximum voltage ripple $\Delta V_{C\max} = y\% \times V_o$. The minimum value of C_1 and C_2 is needed to achieve $\Delta V_{C\max}$

$$C = \begin{cases} \left(1 - \frac{1}{G}\right) \frac{I_o}{y\% \cdot V_o \cdot f_{sw}} \; (G > 1) \\ \frac{V_i}{32y\%.V_o \cdot L \cdot {f_{sw}}^2} \; (G < 1) \end{cases} \tag{24}$$

3.3. Switching Devices

The voltage stresses of the switches are

$$\begin{cases} V_{S_1} = V_{S_2} = V_{S_5} = V_{S_6} = V_i \\ V_{S_3} = V_{S_4} = V_{S_7} = V_{S_8} = V_o, \end{cases} \tag{25}$$

The current stresses of the switches are

$$\begin{cases} I_{S_1} = I_{S_3} = I_{S_4} = I_{S_5} = I_{S_7} = I_{S_8} = I_o G \\ I_{S_2} = I_{S_6} = I_o, \end{cases} \tag{26}$$

The switching device selection is based on the expected relevant peaks of its voltage and current and the availability of the switching devices. With 400 V maximum DC input voltage and 220 Vrms output voltage, a switching voltage rating of 600 V is recommended.

3.4. Power Loss Analysis

The power loss of the proposed S^2B^2I is analyzed in detail in the following subsections. The total power loss of the inverter consists of the switch loss, inductor loss, and capacitor loss.

3.4.1. Power Loss of Power Switches

The total power loss of the switches is equal to the sum of the conduction losses and switching losses, given by:

$$P_{S_tot} = P_{S_con} + P_{S_sw} \tag{27}$$

$$P_{S_con} = 2\sum_{i=1}^{4} R_{dsi} I_{Si.rms}^2 \tag{28}$$

$$P_{S_sw} = 2\sum_{i=1}^{4} V_{Si} I_{Si.avg} \left(t_{ri} + t_{fi}\right) f_s \tag{29}$$

where R_{dsi}, t_{ri}, and t_{fi} are the on-state drain-source resistance and the turn-on and turn-off delay times of each MOSFET, respectively.

The average and R.M.S. current values through the switches are calculated as

$$\begin{cases} I_{S1.avg} = \frac{1}{2\pi}\left[2\int_0^{t_1} i_{L1}(t) d_{B2}(t) d(\omega t) + \int_{t_1}^{t_2} i_{L1}(t) d(\omega t)\right] \\ I_{S1.rms} = \sqrt{\frac{1}{2\pi}\left[2\int_0^{t_1} {i_{L1}}^2(t) d_{B2}(t) d(\omega t) + \int_{t_1}^{t_2} {i_{L1}}^2(t) d(\omega t)\right]} \end{cases} \tag{30}$$

$$\begin{cases} I_{S2.avg} = \frac{1}{2\pi}\left[2\int_0^{t_1} i_{L1}(t) d_{B2}(t) d(\omega t) + \int_0^{\pi} i_{L1}(t) d(\omega t)\right] \\ I_{S2.rms} = \sqrt{\frac{1}{2\pi}\left[2\int_0^{t_1} {i_{L1}}^2(t) d_{B2}(t) d(\omega t) + \int_0^{\pi} {i_{L1}}^2(t) d(\omega t)\right]} \end{cases} \tag{31}$$

$$\begin{cases} I_{S3.avg} = \frac{1}{2\pi}\left[\int_{t_1}^{t_2} i_{L1}(t) d_{B1}(t) d(\omega t)\right] \\ I_{S3.rms} = \sqrt{\frac{1}{2\pi}\left[\int_{t_1}^{t_2} {i_{L1}}^2(t) d_{B1}(t) d(\omega t)\right]} \end{cases} \tag{32}$$

$$\begin{cases} I_{S4.avg} = \frac{1}{2\pi}\left[\int_{t_1}^{t_2} i_{L1}(t) d_{B1}(t) d(\omega t) + \int_{t_2}^{2\pi} i_{L1}(t) d(\omega t)\right] \\ I_{S4.rms} = \sqrt{\frac{1}{2\pi}\left[2\int_0^{t_1} {i_{L1}}^2(t) d_{B1}(t) d(\omega t) + \int_{t_2}^{2\pi} {i_{L1}}^2(t) d(\omega t)\right]} \end{cases} \tag{33}$$

3.4.2. Power Loss of Inductors

The power loss in the inductors includes the core loss and the copper loss. The inductor loss is defined as

$$P_{D_sw} = 2 \cdot k \cdot B^{\beta} \cdot f_s^{\alpha} \cdot A_e \cdot l_e + 2 r_L I_{L1.rms}^2 \tag{34}$$

where B is the AC magnetic flux; f_s is the frequency; A_e is the core cross-sectional area; l_e is the core mean magnetic path length; $I_{L1.rms}$ and $I_{L2.rms}$ are RMS currents of the inductors; and r_L is wire resistance. k, α, and β can be found from the manufacturer's datasheet.

RMS values $I_{L1.rms}$ and $I_{L2.rms}$ can be calculated as

$$I_{L1.rms} = I_{L2.rms} = \sqrt{\frac{1}{2\pi}\left(2\int_0^{t_1} {i_o}^2(t) d(\omega t) + \int_{t_1}^{t_2} \left[\frac{i_o(t)}{1 - d_{B1}(t)}\right]^2 d(\omega t)\right)} \tag{35}$$

3.4.3. Power Loss of Capacitors

The power loss of capacitors is calculated as

$$P_C = r_{C1} I_{C1.rms}^2 + r_{C2} I_{C2.rms}^2 \tag{36}$$

where r_{C1} and r_{C2} are the equivalent series resistance (ESR) of the C_1 and C_2 capacitors, respectively; $I_{C1.rms}$ and $I_{C2.rms}$ are the RMS capacitor currents and are calculated as

$$\begin{cases} I_{C1.rms} = \sqrt{\frac{1}{2\pi}\left(\int_{t_1}^{t_2} {i_o}^2(t) d_{B1}(t) d(\omega t) + \int_{\pi}^{2\pi} \left[I_{in} - i_{L2}(t) - i_o(t)\right]^2 d(\omega t)\right)} \\ I_{C2.rms} = \sqrt{\frac{1}{2\pi}\left(\int_{\pi}^{2\pi} \left[I_{in} - i_{L2}(t)\right]^2 d_{B1}(t) d(\omega t) + \int_{\pi}^{2\pi} {I_{in}}^2 [1 - d_4(t)] d(\omega t)\right)} \end{cases} \tag{37}$$

The parameters for the power loss calculation are presented in Table 1. Figure 4 depicts the power loss distribution of the proposed CGBBI when V_{in} = 50 V and 200 V, v_o = 110 Vrms, and P_o = 500 W.

Table 1. Parameters for power loss analysis.

Parameters		Values
Inductors L_1, L_2	Core	CM777125 (142 nH/N^2)
	Parasitic Resistor	40 mΩ
Capacitors	ESR of C_1 and C_2	49 mΩ
MOSFETs		IPW60R045CPA (600 V, 60 A, R_{dson} = 45 mΩ)

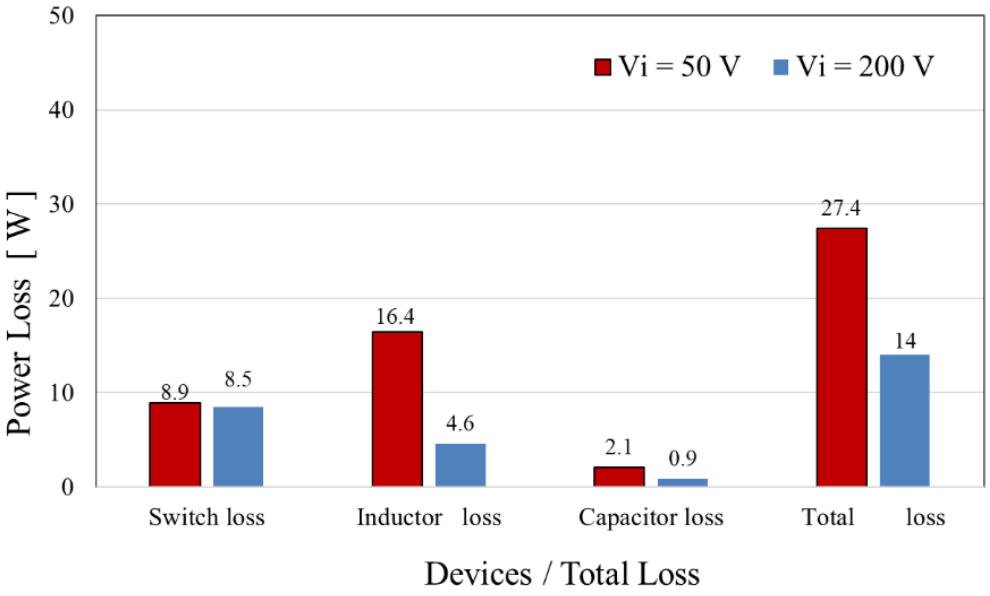


Figure 4. Power loss distribution of the proposed the proposed S^{2}B^{2}I.

4. Comparative Study

Amplification Ratio and Component Count

Table 2 provides a comparison between other buck-boost inverters and the proposed S^{2}B^{2}I, encompassing the power switch count, diodes, inductors, capacitors, high switching frequency switches in the positive and negative periods, switching frequency, number of DC sources, single-stage characteristics, power rating, boosting voltage, and reported efficiency. Compared with other buck-boost inverters in [23,25,26], the inverters in [12,13,24,27] and the proposed S^{2}B^{2}I use more power switches. However, the inverters in [13,24] and the proposed S^{2}B^{2}I did not use any power diodes in the inverter system. In terms of passive component comparison, the proposed S^{2}B^{2}I uses fewer inductors and capacitors. Note that the proposed S^{2}B^{2}I only uses film capacitors. This can improve the reliability and lifetime of the inverter. According to the input voltage reference, the switching time of each power switch of the proposed S^{2}B^{2}I can be changed, the total switching time of switches in the half cycle is not changed, and the high switching frequency switches of the proposed S^{2}B^{2}I can estimate two in the half cycle. For the operating input voltage range, the proposed S^{2}B^{2}I is the widest among the inverters in Table 2. In terms of the measured efficiency comparison, the proposed S^{2}B^{2}I has high efficiency in lower input voltage operation when compared with other inverters. Hence, the proposed S^{2}B^{2}I is a good solution compared with other inverters.

Table 2. Comparison between the proposed S^2B^2I and other buck-boost inverters.

Topologies	[12]	[13]	[25]	[26]	[27]	[28]	[29]	**S^2B^2I**
No. of switches & Voltage stress	4 × [V_i] 4 × [V_o]	4 × [V_i] 4 × [V_i + V_o]	4 × [V_i + V_o] 2 × [V_o]	4 × [V_i + V_o] 4 × [V_o]	2 × [V_i + V_o] 2 × [V_i + V_o]	3 × [V_i + V_o] 2 × [V_o]	4 × [V_i] 4 × [V_o]	4 × [V_i] 4 × [V_o]
No. of diodes & Voltage stress	2 × [V_i] 2 × [V_o]	0	0	0	2 × [V_i + V_o] 2 × [V_i + V_o]	2 × [V_o]	2 × [V_i] 2 × [V_o]	0
No. of inductors & reported inductance	2 × [0.6 mH] 1 × [0.4 mH]	1 × [0.3 mH]	2 × [0.5 mH]	2 × [0.78 mH]	2 × [50 µH] 2 × [0.3 mH]	1 × [0.7mH]	2 × [1.2 mH]	2 × [0.25 mH]
No. of capacitors & reported capacitance	2 × [5 µF]	1 × [6.8 µF]	2 × [20 µF]	1 × [6.8 µF]	2 × [3 µF] 1 × [6.8 µF]	2 × [6µF]	1 × [2µF]	2 × [4 µF] 1 × [2 µF]
High freq. switches at +,− half cycles	4, 4	2, 2	2, 2	1, 1	2, 2	1, 1	2, 2	2, 2
Switching freq.	50 kHz	30 kHz	20 kHz	20 kHz	50 kHz	50 kHz	40 kHz	50 kHz
No. of DC source	2	1	1	1	1	1	1	1
Single-stage system	No	No	Yes	Yes	Yes	Yes	Yes	Yes
Power rating	1500 W	500 W	500 W	400 W	500 W	500 W	550 W	500 W
V_i * → V_o(rms)	116 → 210	85 → 110	80 → 110	60 → 110	77 → 110	84 → 110	100 → 110	50 → 110
Reported efficiency at P_o with V_i * (%)	96.4%	94.7%	91.1%	91.1%	95.6%	95.6%	96.4%	94.3%
Range of V_i (V)	-	85–200	-	60–200	77–200	84–200	100–200	50–200
Peak measured efficiency	97.6%	96.8%	92.6%	95.7%	96.5%	97%	96.6%	97%

* DC input voltage.

5. Simulation Results

For the theoretical verification, the proposed S^2B^2I is examined through PSIM 9.1 simulation software analysis, as shown in Figure 5. A 500 W inverter with the following specifications was used: v_o = 110 Vrms, L_1 = L_2 = 0.25 mH, C_1 = C_2 = 4 µF, C_0 = 2 µF, f_o = 50 Hz, and f_{sw} = 50 kHz.

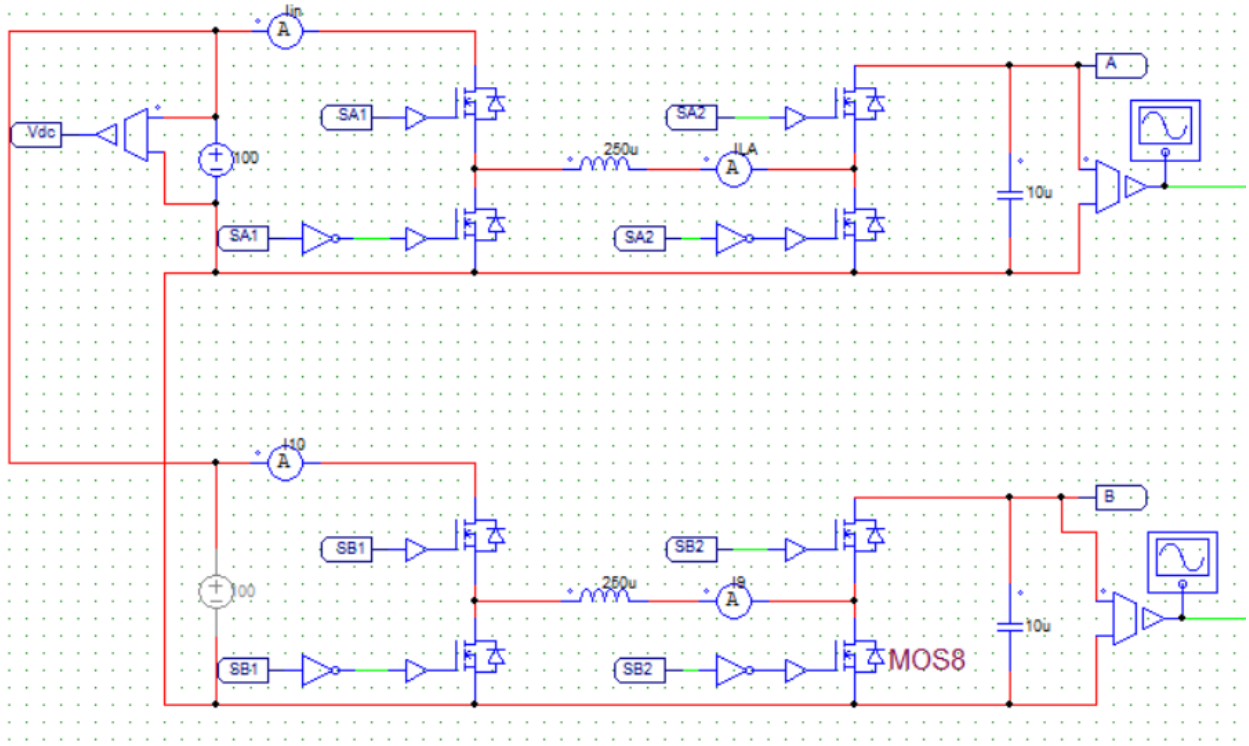


Figure 5. Simulation circuit of the proposed S^2B^2I.

Figures 6 and 7 show the simulation results of the proposed inverter. Figure 6a shows the simulation results for the worst case when the input voltage is stepped up instantly from 50 V to 155 V with the G = 3.1. The peak voltage across the capacitors is equal to the output peak voltage of 155 V. The peak current of the inductor is about 20 A, which is equal to the theoretical values calculated from (13). The inductors and capacitors are designed according to the case $G > 1$ and satisfied in (17) and (19), where a 15% maximum peak-to-peak current ripple and a 10% peak-to-peak maximum voltage ripple are considered. Figure 6b shows the voltage stress on switches S_1, S_2, S_3, and S_4 for module A. It can be seen that the voltage stress of the two S_1 and S_2 switches is equal to the input voltage of 50 V, while the voltage stress of the two S_3 and S_4 switches is equal to the peak output voltage of 155 V. This is also the same in module B.

Similarly, the simulated results for buck mode are shown in Figure 7 when the input voltage is 200 V. The input, output, capacitors C_1 and C_2, voltages, and inductor L_1 and L_2 currents are presented in Figure 7a. The voltage stress on switches S_1–S_4 is described in Figure 7b. As shown in Figure 7, the output voltage amplitude is lower than the DC input voltage. The capacitor voltage is the same as that in boost mode because the output voltage has not changed. The simulated waveforms are corrected to the theory in Section 2.

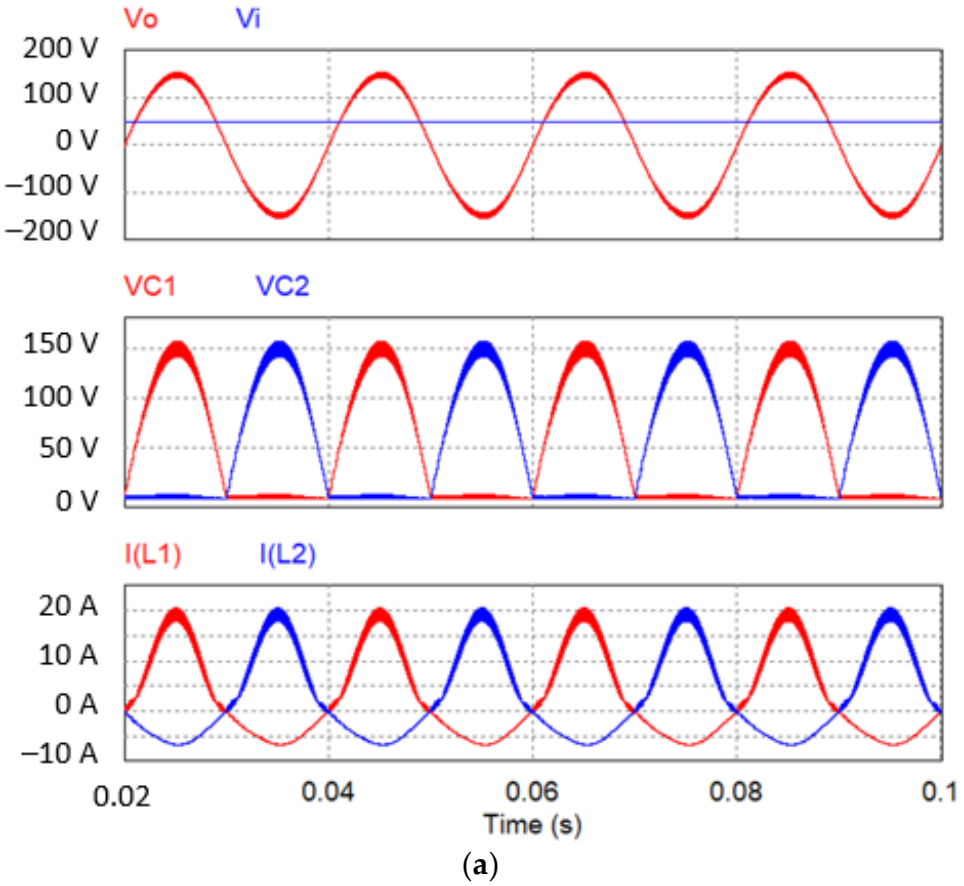
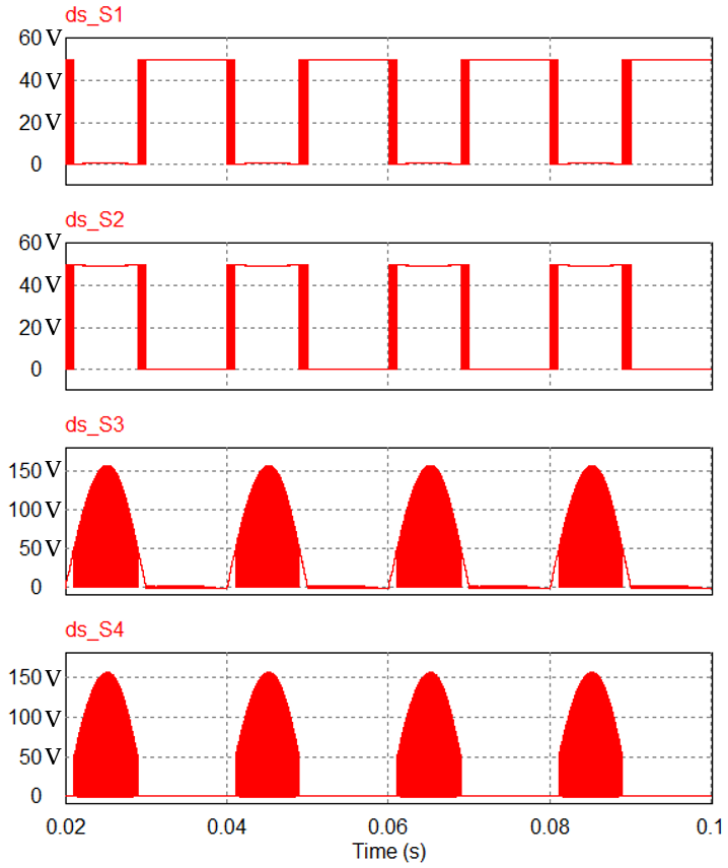
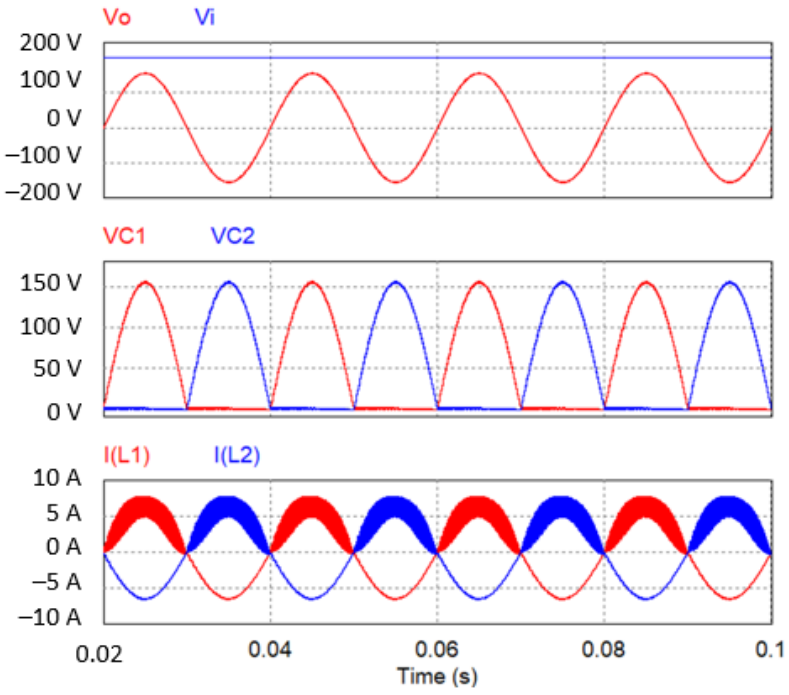


Figure 6. *Cont.*



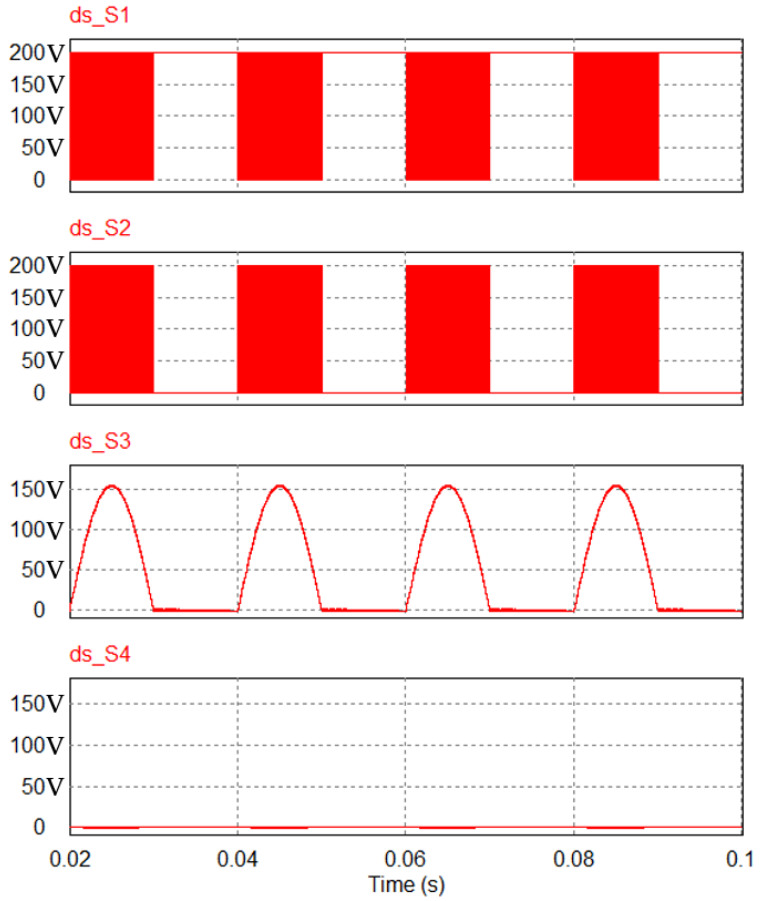
(**b**)

Figure 6. The waveforms of simulation results in boost operation when G = 3.1. (**a**) Input and output voltages, capacitor C_1 and C_2 voltage, and currents of inductors L_1 and L_2. (**b**) Voltage stress on switches S_1–S_4.



(**a**)

Figure 7. *Cont.*



(**b**)

Figure 7. The waveforms of simulation results in buck operation when $G = 0.78$. (**a**) Input and output voltages, capacitor C_1 and C_2 voltage, and currents of inductors L_1 and L_2. (**b**) Voltage stress on switches S_1–S_4.

6. Experimental Results

To validate the achievability of the proposed S^2B^2I, a hardware prototype of the proposed S^2B^2I is set up to prove the effectiveness of the derived strategy. The testing parameters and selection of experimental devices are included in Table 3. It is noted that the 600 V devices we used are based on the availability of the device in the laboratory. With the specs in Table 3, the 300 V or 400 V switching devices can be used. Because the prototype is not well-designed, a small voltage spike will appear when the switch is turned off. A photo of the inverter prototype is shown in Figure 8.

Table 3. Simulation and experiment specifications.

Parameters		Values
Input voltage		50~200 V
Output phase voltage		110 Vrms
Output frequency		50 Hz
Power rating		500 W
Inductors $L_1 = L_2$		0.25 mH
Capacitors	$C_1 = C_2$	4 µF
	C_0	2 µF
Switches		IPW60R045CPA (600 V, 60 A, 45 mΩ)
Switching frequency		50 kHz

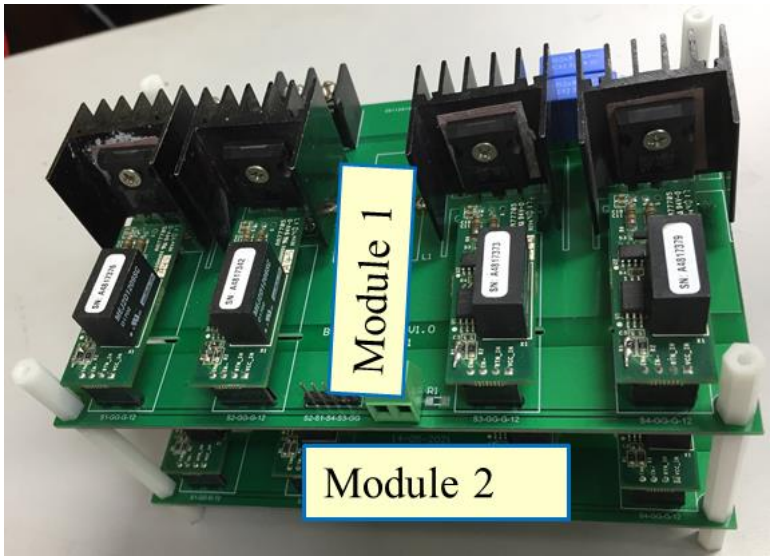
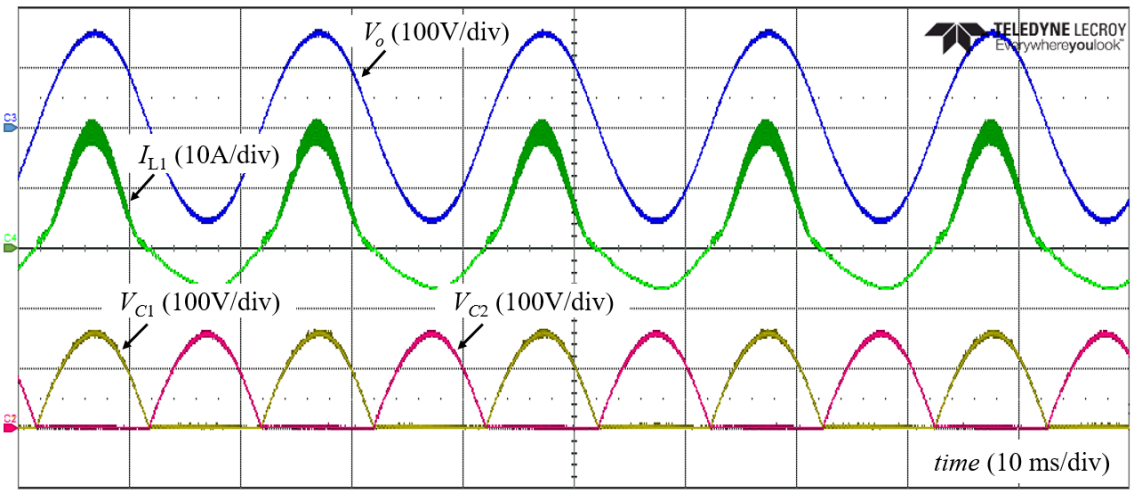


Figure 8. A photo of the S^2B^2I prototype.

Figure 9 shows the testing waveforms of the introduced S^2B^2I in step-up operation (V_i = 50V, v_o = 110 Vrms). In Figure 9a, the output voltage amplitude is 156 V and the peak current of inductor L_1 is around 20 A, which is consistent with the calculated and simulated values at G = 3.1. The measured peak value of the output current is 6.5 A. Capacitor voltages V_{C1} and V_{C2} are half sinusoidal and have the same peak voltage in each half-cycle, respectively. The voltage ripples on capacitors C_1 and C_2 are low. Figure 9b presents the PWM signals of switches S_1, S_3, and S_4, which are corrected to the derived PWM method in Section 2. Figure 9c shows the voltage stress on switches S_1, S_3, and S_4. It can be seen that switch S_1 is operated in line frequency and the voltage stress is equal to the input voltage. In addition, the two S_3 and S_4 switches are switched at high frequency in a half-cycle, and those voltage stresses are equal to the peak output voltage.



(**a**)

Figure 9. *Cont.*

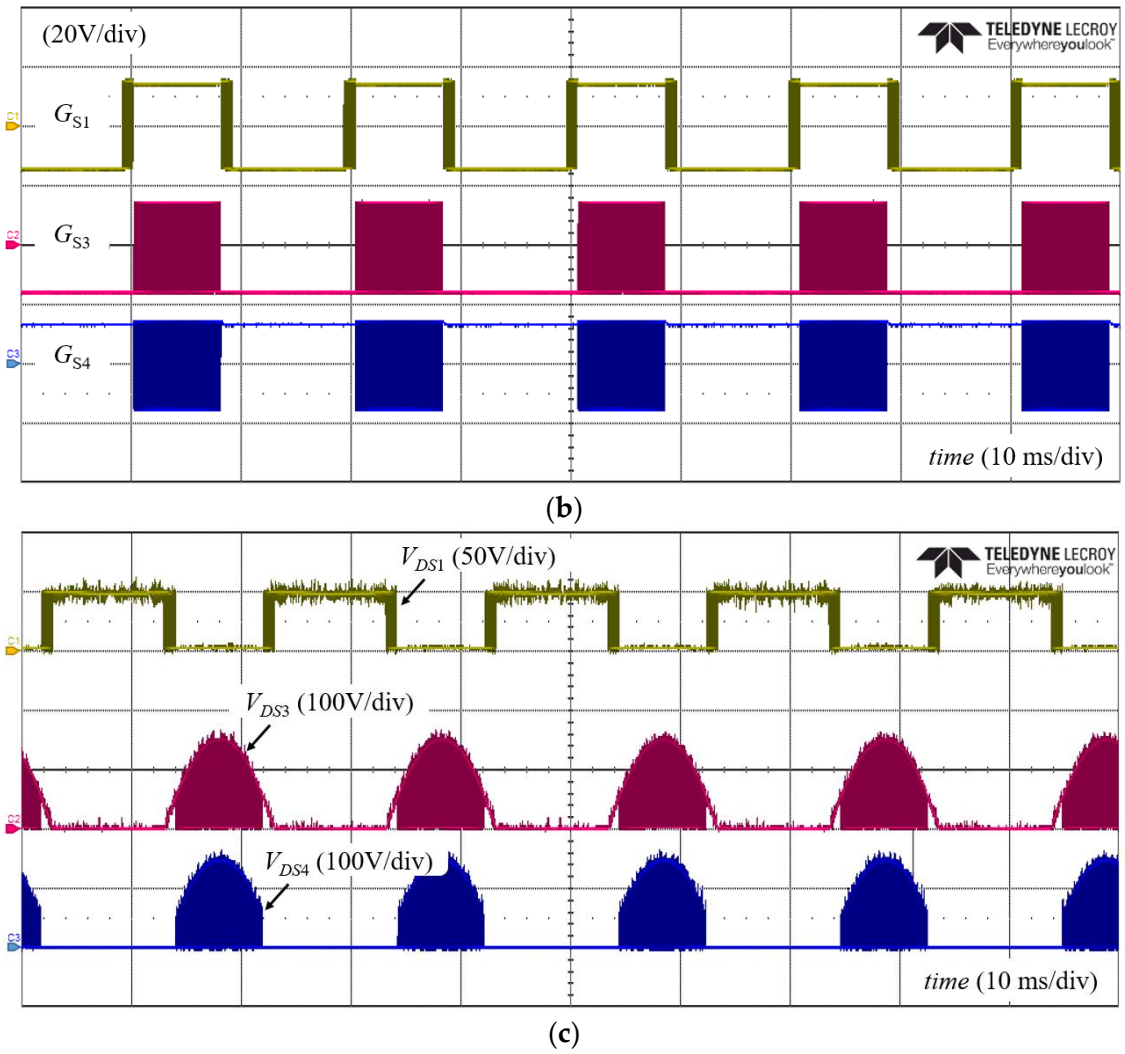


Figure 9. The waveforms of experimental results in boost operation when G = 3.1. (**a**) Output voltage, current of inductor L_1, and voltages of capacitors C_1 and C_2. (**b**) PWM signals of switches S_1, S_3, and S_4. (**c**) Voltage stress on switches S_1, S_3, and S_4.

Figure 10 presents the experimental waveforms of the proposed S^2B^2I in step-down operation (V_i = 200 V, v_o = 110 Vrms). From Figure 10a, the output voltage has a peak value of 156 V and the inductor current is similar to the output current. The difference is that the inductor current in the positive half-wave has a high-frequency ripple, which is caused by the high-frequency operation of switches S_1 and S_2. Capacitor voltages V_{C1} and V_{C2} are the same. Figure 10b shows the PWM signals of switches S_1, S_3, and S_4, which are similar to the simulation results. The PWM control signal for switch S_1 is indicated in Figure 10b. Figure 10c shows the voltage stress on switches S_1, S_3, and S_4.

From the experimental validation, the total harmonics distortion (THD) of the output current is measured at different power ratings and shown in Figure 11a when the output voltage is kept at 110 Vrms. The THD of output current i_o of the proposed S^2B^2I is lower than 3% when the G = 3.1 and also lower than 2.5% when the G = 0.78. The efficiency of the proposed S^2B^2I is also computed at different power ratings and compared with the different gains, as shown in Figure 11b. The efficiency in Figure 11 is measured by using the power meters at the both input and output sides of the inverter. It can be clearly seen from Figure 11b that the proposed S^2B^2I has higher efficiency in G = 0.78 compared to G = 3.1. The highest efficiency of the proposed S^2B^2I achieved 97% at G = 0.78. When G = 3.1, the maximum efficiency achieved by the inverter was 94.5%. This is because voltage gain increased and switches S_3 and S_4 in module A and S_7 and S_8 in module B operated with a

higher switching frequency. In addition, the conduction loss of inductors also increased due to the increase in the inductor current in boost mode.

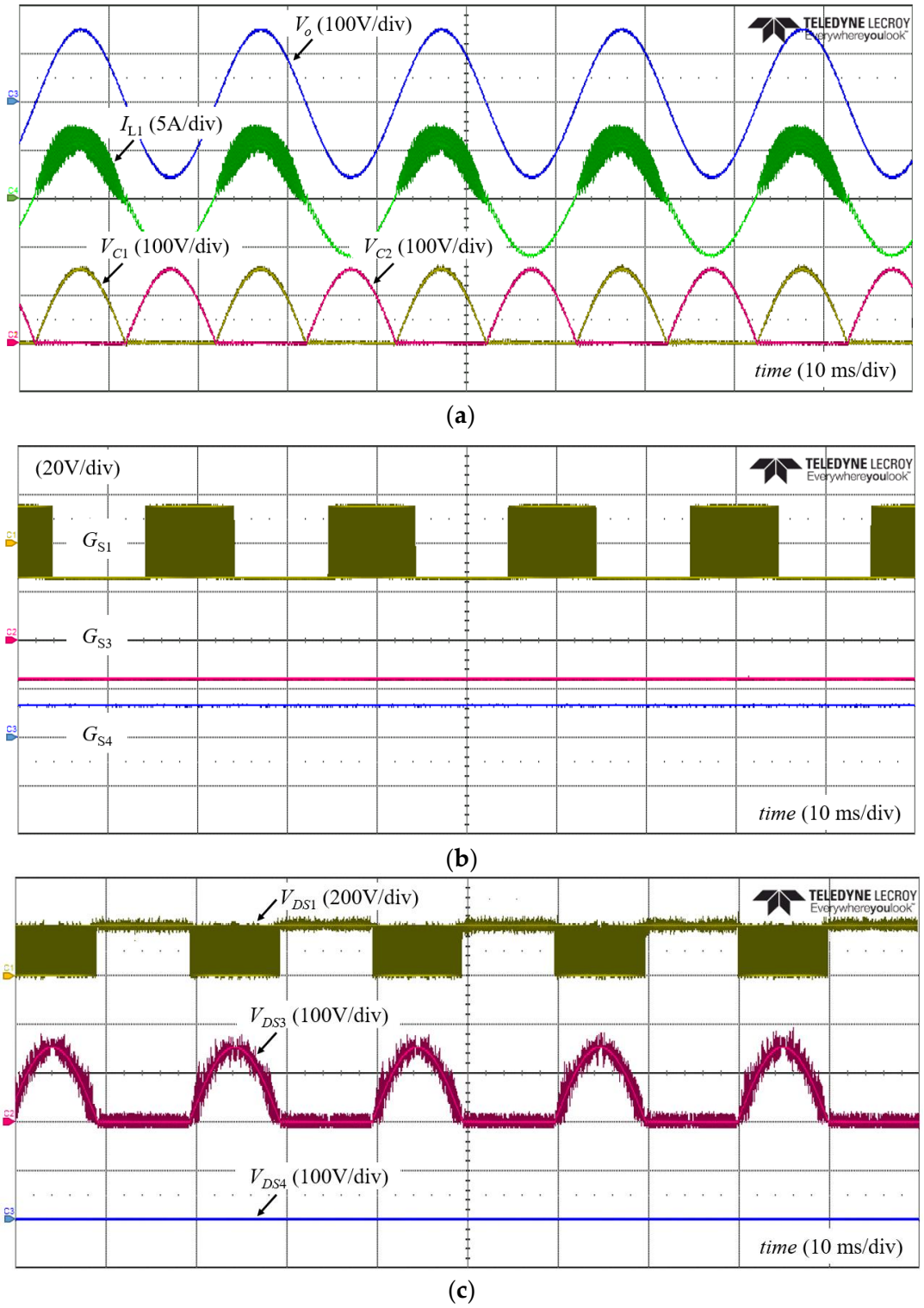


Figure 10. The waveforms of experimental results in buck operation when G = 0.78. (**a**) Output voltage, current of inductor L_1, and voltages of capacitors C_1 and C_2. (**b**) PWM signals of switches S_1, S_3, and S_4. (**c**) Voltage stress on switches S_1, S_3, and S_4.

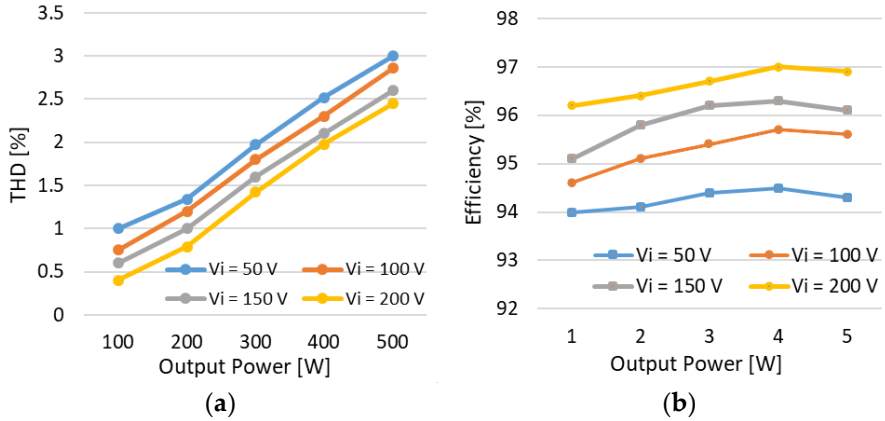


Figure 11. Measurements of the proposed S^2B^2I. (**a**) THD of output current; (**b**) efficiency.

7. Conclusions

A new S^2B^2I with a non-electrolyte capacitor is described in this article, which provides a buck-boost function in single-stage power conversion. One of the characteristics of the proposed S^2B^2I structure is a wide range of input voltage. As a result, the voltage rating of switching devices can be significantly reduced. In addition, half of the power switch in each module is operated in line frequency by using the derived PWM control method, and then the efficiency of the proposed S^2B^2I is improved. The proposed S^2B^2I structure does not use an electrolytic capacitor, so the proposed S^2B^2I can improve the life of the inverter and has certain significance for the solar photovoltaic distributed generation system.

Author Contributions: Y.-O.C. determined topology, data analysis, and original draft preparation. K.M.N. contributed to propose configuration, analysis, review, and editing. All authors have read and agreed to the published version of the manuscript.

Funding: This study was supported by research funds from Chosun University (2021).

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Meneses, D.; Blaabjerg, F.; Garcıa, O.; Cobos, J.A. Review and comparison of step-up transformerless topologies for photovoltaic ac-module application. *IEEE Trans. Power Electron.* **2013**, *28*, 2649–2663. [CrossRef]
2. Barater, D.; Lorenzani, E.; Concari, C.; Franceschini, G.; Buticchi, G. Recent advances in single-phase transformer-less photovoltaic inverters. *IET Renew. Power Gener.* **2016**, *10*, 260–273. [CrossRef]
3. Duong, D.T.; Nguyen, M.K.; Nguyen, T.T.; Cha, H.; Lim, Y.C.; Choi, J.H. Switching-Cell Structure Based Generic Five-Level Current Source Inverter. *IEEE Trans. Ind. Electron.* **2023**, *70*, 5696–5706. [CrossRef]
4. Zhang, N.; Zhang, G.; See, K.W.; Zhang, B. A single-switch quadratic buck–boost converter with continuous input port current and continuous output port current. *IEEE Trans. Power Electron.* **2018**, *33*, 4157–4166. [CrossRef]
5. Zhang, L.; Sun, K.; Feng, L.; Wu, H.; Xing, Y. A family of neutral point clamped full-bridge topologies for transformerless photovoltaic gridtied inverters. *IEEE Trans. Power Electron.* **2013**, *28*, 730–739. [CrossRef]
6. Victor, M.; Greizer, F.; Bremicker, S.; Hubler, U. Method of Converting a Direct Current Voltage from a Source of Direct Current Voltage, More Specifically from a Photovoltaic Course of Direct Current Voltage, into an Alternating Current Voltage. U.S. Patent 2005 286 281 A1, 29 December 2005.
7. Xiao, H.; Xie, S.; Chen, Y.; Huang, R. An optimized transformer-less photovoltaic grid-connected inverter. *IEEE Trans. Ind. Electron.* **2011**, *58*, 1887–1895. [CrossRef]
8. Ji, B.; Wang, J.; Zhao, J. High-efficiency single-phase transformer-less PV H6 inverter with hybrid modulation method. *IEEE Trans. Ind. Electron.* **2013**, *60*, 2104–2115. [CrossRef]
9. Ketterer, J.; Schmidt, H.; Siedle, C. Inverter for Transforming a DC Voltage into an AC Current or an AC Voltage. European Patent 1 369 985 A2, 13 May 2003.
10. Kerekes, T.; Teodorescu, R.; Rodríguez, P.; Vázquez, G.; Aldabas, E. A new high-efficiency single-phase transformerless PV inverter topology. *IEEE Trans. Ind. Electron.* **2011**, *58*, 184–191. [CrossRef]

11. Ray, O.; Mishra, S. Boost-derived hybrid converter with simultaneous dc and ac outputs. *IEEE Trans. Ind Appl.* **2014**, *50*, 1082–1093. [CrossRef]
12. Dutta, S.; Chatterjee, K. A buck and boost based grid connected PV inverter maximizing power yield from two PV arrays in mismatched environmental conditions. *IEEE Trans. Ind. Electron.* **2018**, *65*, 5561–5571. [CrossRef]
13. Khan, U.A.; Park, J.W. Full-bridge single-inductor-based buck–boost inverters. *IEEE Trans. Power Electron.* **2021**, *36*, 1909–1920. [CrossRef]
14. Duong, T.D.; Nguyen, M.K.; Tran, T.T.; Choi, J.H.; Lim, Y.C. Transformerless High Step-Up DC DC Converters with Switched-Capacitor Network. *Electronics* **2019**, *8*, 1420. [CrossRef]
15. Duong, T.D.; Tai, T.T.; Nguyen, M.K.; Lim, Y.C.; Choi, J.H. Transformer-less switched-capacitor quasi-switched boost DC-DC converter. *Energies* **2022**, *14*, 6591. [CrossRef]
16. Nguyen, M.K.; Duong, T.D.; Lim, Y.C. Switched-capacitor-based dual-switch high-boost dc-dc converter. *IEEE Trans. Power Electron.* **2018**, *33*, 4181–4189. [CrossRef]
17. Khan, M.N.H.; Forouzesh, M.; Siwakoti, Y.P.; Li, L.; Kerekes, T.; Blaabjerg, F. Transformerless inverter topologies for single-phase photovoltaic systems: A comparative review. *IEEE J. Emerg. Sel. Top. Power Electron.* **2020**, *8*, 805–835. [CrossRef]
18. Tran, T.T.; Nguyen, M.K.; Duong, T.D.; Lim, Y.C.; Choi, J.H. A Switched-Capacitor-Based Six-Level Inverter. *IEEE Trans. Power Electron.* **2022**, *37*, 4804–4816. [CrossRef]
19. Vo, D.V.; Nguyen, M.K.; Duong, T.D.; Tran, T.T.; Lim, Y.C.; Choi, J.H. A novel single-stage common-ground transformerless Buckboost inverter. *Electronics* **2022**, *11*, 829. [CrossRef]
20. Husev, O.; Matiushkin, O.; Roncero-Clemente, C.; Blaabjerg, F.; Vinnikov, D. Novel family of single-stage buck-boost inverters based on unfolding circuit. *IEEE Trans. Power Electron.* **2019**, *34*, 7662–7676. [CrossRef]
21. Kurdkandi, N.V.; Husev, O.; Matiushkin, O.; Vinnikov, D.; Siwakoti, Y.; Lee, S.S. Novel family of flying inductor-based single-stage buck-boost inverters. *IEEE J. Emerg. Sel. Top. Power Electron.* **2022**, *10*, 6020–6032. [CrossRef]
22. Tang, Y.; Dong, X.; He, Y. Active buck-boost inverter. *IEEE Trans. Ind. Electron.* **2014**, *61*, 4691–4697. [CrossRef]
23. Khan, A.A.; Cha, H.; Khan, U.A.; Kim, H.-G. Four-switch buck-boost inverter for stand-alone and grid-connected single-phase PV systems. In Proceedings of the IEEE 3rd International Future Energy Electronics Conference and ECCE Asia, Kaohsiung, Taiwan, 4–7 June 2017; pp. 460–465.
24. Peng, F.Z. Z-source inverter. *IEEE Trans. Ind. Appl.* **2003**, *39*, 504–510. [CrossRef]
25. Tang, Y.; Bai, Y.; Kan, J.; Xu, F. Improved dual boost inverter with half cycle modulation. *IEEE Trans. Power Electron.* **2017**, *32*, 7543–7552. [CrossRef]
26. Ho, C.N.M.; Siu, K.K.M. Manitoba Inverter—Single Phase Single-Stage Buck-Boost VSI Topology. *IEEE Trans. Power Electron.* **2019**, *34*, 3445–3456. [CrossRef]
27. Khan, A.A.; Lu, Y.W.; Eberle, W.; Wang, L.; Khan, U.A.; Cha, H. Single-phase split-inductor differential boost inverters. *IEEE Trans. Power Electron.* **2020**, *35*, 107–120. [CrossRef]
28. Akbar, F.; Cha, H.; Kim, H.-G. Novel Virtual-Ground Single-Stage Single Inductor Transformerless Buck-Boost Inverter. *IEEE Trans. Ind. Electron.* **2021**, *68*, 6927–6938. [CrossRef]
29. Wang, H.; Wu, W.; Zhu, J.; Koutroulis, E.; Chung, H.S.-H.; Blaabjerg, F. A novel dual buck and boost transformer-less single-phase grid-tied inverter. *IEEE Trans. Power Electron.* **2022**, *37*, 4211–4224. [CrossRef]

Disclaimer/Publisher's Note: The statements, opinions and data contained in all publications are solely those of the individual author(s) and contributor(s) and not of MDPI and/or the editor(s). MDPI and/or the editor(s) disclaim responsibility for any injury to people or property resulting from any ideas, methods, instructions or products referred to in the content.