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Multisampling with Sigma-Delta ADCs for Medium-Voltage Cascaded H-Bridge Converters

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Abstract: The control of medium-voltage cascaded H-bridge (CHB) converters demands precise, high-bandwidth, low-latency, and isolated measurements. Traditional analog-to-digital converters (ADCs) can facilitate multisampling methods to meet these requirements but do not provide the high-voltage galvanic isolation that may be necessary in a system operating at medium voltage. Sigma-Delta ADCs (SD-ADCs) present a promising alternative due to their superior noise rejection capabilities and direct integration with the optical fiber interface. However, the inherent latency associated with SD-ADCs, stemming from their operating principles, poses challenges when integrating them with multisampling methods. This paper analyzes the integration of multisampling techniques with SD-ADCs for medium-voltage CHB converter control. First, the impact of SD-ADC-induced delays on the control system is elucidated from the passivity perspective. Second, the practical implementation of multisampling with SD-ADCs is discussed in detail. Finally, experimental results from a 2400 Vrms medium-voltage CHB converter are presented to validate the analysis and illustrate the effectiveness of the proposed implementation.

Keywords: cascaded h-bridge converters; multilevel converters; multisampling; sigma-delta converters; stability; passivity



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1. Introduction

Multilevel converters (MLCs) enhance the efficiency and reduce the size of modern high-power electronics systems by enabling direct connection to medium-voltage networks. Among existing MLC topologies, the cascaded H-bridge (CHB) converter is especially promising and has been adopted for solid-state transformers (SST), static synchronous compensators (STATCOM), medium-voltage motor drives, and battery energy storage systems [1–4].

Commonly, the CHB converter operates under phase-shifted pulse-width modulation (PS-PWM), which can effectively reduce the output current ripple [5,6]. With modern PS-PWM implementation on digital signal processors (DSPs), analog-to-digital converters (ADCs) are used to sample the current and voltage at the peak or valley of the triangular carriers. This method, which keeps the sampling frequency the same as the carrier frequency, is called single sampling (SS). Despite being widely used due to its simplicity, SS has an inherent delay that compromises the system passivity, which can adversely affect the stability and dynamic response of the CHB converter [7,8].

To mitigate this issue, multisampling methods are proposed in the literature to reduce the delay by sampling at a frequency higher than the switching frequency [9–14]. The simplest multisampling method is double sampling (DS), which samples the signal at both the peak and valley of the carriers, making the sampling frequency twice the carrier frequency. In [15,16], it is shown that the sampling frequency of a CHB converter can be increased by a factor equal to the number of modules without introducing a high-frequency switching

ripple in the measurement signals. Further increasing the sampling frequency beyond this limit results in high-order switching noise and nonlinear behavior [17–20]. In addition, multisampling reduces the time available for computation, requiring more powerful DSPs.

As an alternative to traditional ADCs, Sigma-Delta ADCs (SD-ADCs) have emerged as a promising solution for medium-voltage multilevel converters (MLCs), effectively addressing the noise coupling and isolation challenges associated with conventional ADCs. The core principle of SD-ADC involves sampling the signal at a much higher frequency using a Sigma-Delta modulator, which converts it into a single-bit digital stream. This stream is then transmitted and processed by a low-pass decimation filter to remove quantization and high-frequency noise, thereby reconstructing the equivalent measurement signal.

In addition to offering exceptional high-frequency noise rejection by effectively averaging the signal over time, SD-ADCs provide a distinct advantage in medium-voltage applications due to their compatibility with digital signal transmission over optical fibers [21–23]. Medium voltage converter applications typically require an isolated sensor system to prevent electrical interference between high-voltage components and low-voltage control circuitry. This isolation is typically achieved using sensors, transformers, or optical communication links designed to meet galvanic isolation requirements. While ADCs themselves do not provide galvanic isolation, they play a crucial role in integrating analog signals from sensors into digital control systems. SD-ADCs can simplify this integration by enabling direct digital signal transmission over optical fibers, significantly reducing the complexity of achieving galvanic isolation. By contrast, traditional ADC solutions require separate isolation mechanisms, such as signal transformers or additional optoisolators, which add complexity and delay. These features make SD-ADCs particularly advantageous for medium-voltage MLC systems, where robust galvanic isolation and reliable digital transmission are critical.

Integrating the multisampling technique with SD-ADCs combines the benefits of both methods to optimize medium-voltage converter performance. This approach can minimize system delay, enhance passivity, and expand the control bandwidth, while also improving noise immunity through the advanced noise-rejecting capabilities of SD-ADCs. However, it presents several challenges, which have not been fully explored in the literature. First, the SD-ADC's inherent filtering, which operates like a moving average, introduces a delay effect that depends on its parameters [24,25]. Second, the computational burden associated with multisampling in conjunction with SD-ADC must be considered, as SD-ADC requires a measurement window to effectively average the signal [26] while multisampling reduces the computation time by a factor of the number of samples.

To address the above challenges, in this paper, we investigate the integration of multisampling and the SD-ADC sensing techniques by analyzing the SD-ADC's hardware setup, parameter configuration, and delay effect for a medium-voltage CHB converter. The main contributions of the paper include the following:

- The SD-ADC's practical delay effect is analyzed, and its impact on the CHB converter's passivity is analyzed.
- The integration of multisampling with SD-ADCs is discussed, and a practical implementation regarding the system and SD-ADC parameters is given.
- The proposed multi-sampling implementation with SD-ADC is verified with a 2400 Vrms medium-voltage CHB converter.

The rest of the paper is organized as follows: In Section 2, the CHB converter and its control are introduced. In Section 3, the sampling methods for CHB converters are discussed. In Section 4, the SD-ADC sensing for the CHB converter is discussed. In Section 5, simulation results and hardware experiment results based on a 2400 Vrms medium-voltage CHB converter are presented. Section 6 concludes the paper.

2. Cascaded H-Bridge Converter with Grid-Side Current Control

The N -level single-phase CHB is a type of MLC composed of N H-bridge cells connected in series (see Figure 1). This paper examines a single-phase configuration, and a

similar analysis can be performed on three-phase applications in a stationary reference frame. In this configuration, each cell is equipped with its own isolated DC–DC converter, which connects to a common DC bus, enabling the direct conversion from DC to medium-voltage AC. In this paper, we focus on the grid-side control of the CHB converter by assuming that the H-bridge cells' DC voltage is tightly regulated by the DC–DC converters. Details on the implementation and control strategies for the CHB and DC–DC converters can be found in [27].

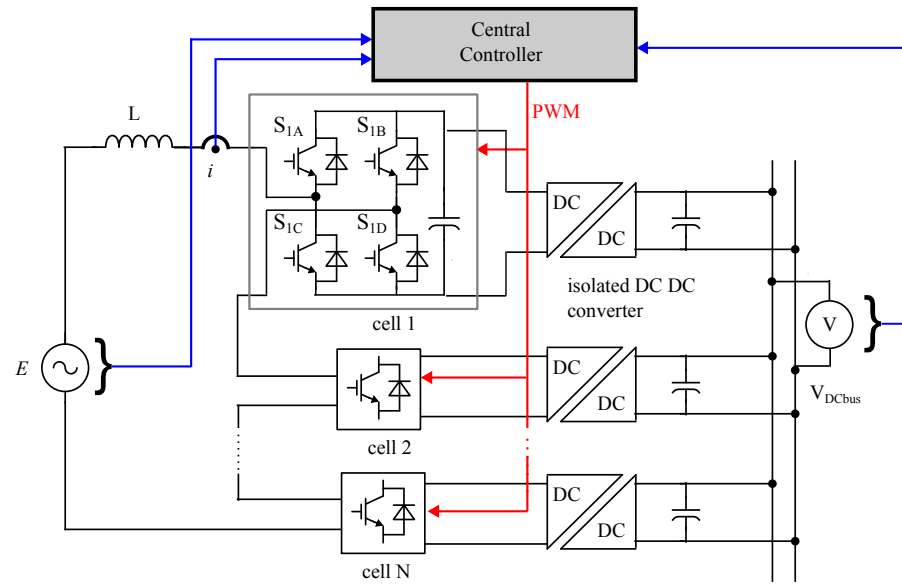


Figure 1. System diagram of the N-cell single-phase CHB, showing values sensed by the central controller: grid voltage (E), grid current (i), and shared DC bus voltage (V_{DCbus}).

While various grid-side control methods are available, this paper focuses on grid-following control, which regulates the grid current and is widely employed in various CHB applications. Grid-forming control with virtual inertia, however, is not considered in this study. The simplified model of the single-phase grid-tied CHB converter with grid-following current control is presented in Figure 2a. Using Kirchhoff's voltage law, the current i through the output inductor L is given by the following:

$$i = \frac{1}{sL}(v - E) = G_p(s)(v - E) \quad (1)$$

where v is the output of the CHB converter, E is the grid phase voltage, and $G_p = 1/sL$ is the transfer function of the output filter.

To regulate the grid current, closed-loop current control is implemented as illustrated in Figure 2b. The control input for the system can be modeled as follows:

$$v = G_c(s)(i_{ref} - iG_s(s)) + E' \quad (2)$$

where $G_c(s)$ is the controller transfer function, $G_s(s)$ is the sensor delay and E' is the feedforward term of the grid phase voltage.

The resulting transfer function for the grid current becomes

$$i(s) = \frac{G_c(s)G_{dp}(s)G_p(s)}{1 + G_c(s)G_{dp}(s)G_s(s)G_p(s)}i_{ref} - \frac{G_p(s)}{1 + G_c(s)G_{dp}(s)G_s(s)G_p(s)}E \quad (3)$$

where $G_{dp}(s)$ represents the control and modulation delay.

The current control loop transfer function can be further simplified into the following form, where G_{cl} is the closed loop transfer function and Y_o is the output admittance of the VSC as shown in Figure 2c.

$$G_{cl} = \frac{G_c(s)G_{dp}(s)G_p(s)}{1 + G_c(s)G_{dp}(s)G_s(s)G_p(s)}, \quad Y_o = \frac{G_p(s)}{1 + G_c(s)G_{dp}(s)G_s(s)G_p(s)} \quad (4)$$

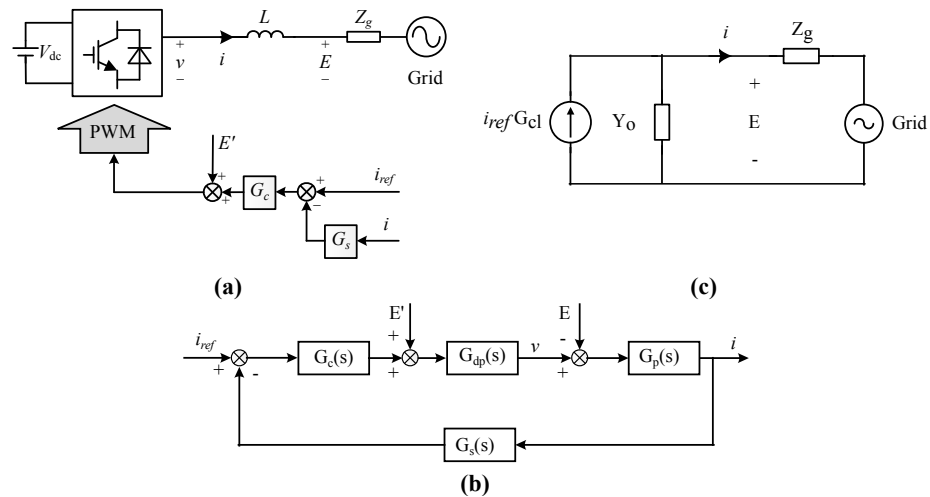


Figure 2. (a) Simplified control diagram for grid-side current control of the CHB, (b) current closed-loop control feedback model, (c) Norton equivalent circuit.

The controller chosen for this analysis is a Proportional-Resonant (PR) controller, which is commonly employed in single-phase systems. The PR controller incorporates a single resonant component tuned to the fundamental angular frequency $\omega_o = 2\pi \times 60$ Hz. The parameter ζ represents the damping factor. The transfer function of the PR controller is given by

$$G_c(s) = K_p + \frac{K_r s}{s^2 + 2\zeta\omega_o s + \omega_o^2} \quad (5)$$

It is worth noting that the PR controller's resonant frequency can also be tuned to other frequencies to suppress the harmonics. The value of the gain K_p of the controller can be used to determine the current control bandwidth (BW) according to [28]:

$$K_p = 2\pi \text{ BW } L \quad (6)$$

Control Delay and Passivity

Digital controllers are the preferred method for implementing control for the CHB converter. However, digital control introduces inherent delays due to factors such as A/D conversion, pulse-width modulation (PWM) actuation, and processing time [29].

The sources of digital delay can be categorized into three main components: T_{smpd} , which represents the sampling delay; t_{ctrl} , the control delay, defined as the processing time on digital controllers that spans the interval between the sampling and the update to the PWM register and T_{DPWM} , the digital modulation delay, defined as the time between updating the PWM register and actuation of the output voltage. The control and modulation delay can be combined into T_d and modeled with the following:

$$G_{dp}(s) = e^{-st_{ctrl}} e^{-sT_{DPWM}} = e^{-sT_d} \quad (7)$$

With the above definition, the time available for control algorithm computation is $t_{ctrl} - T_{smpd}$. As a result, the sampling delay is critical in determining the t_{ctrl} , and therefore, T_d , particularly when using multisampling with a reduced processing time.

Power electronic systems that exhibit passive characteristics have been proposed to countermeasure the potential oscillations [30,31]. This is based on the idea that if each connected subsystem is passive, the whole system is passive, and therefore, stable. The passivity of a converter is ensured when the real part of the output admittance Y_o is nonnegative [30], i.e., the phase of Y_o is within $[-90^\circ, 90^\circ]$.

For the grid-connected converter model presented in the previous subsection, Y_o depends greatly on the delay T_d . To demonstrate the relationship between Y_o and T_d , the Bode plots of Y_o with different delays are shown in Figure 3.

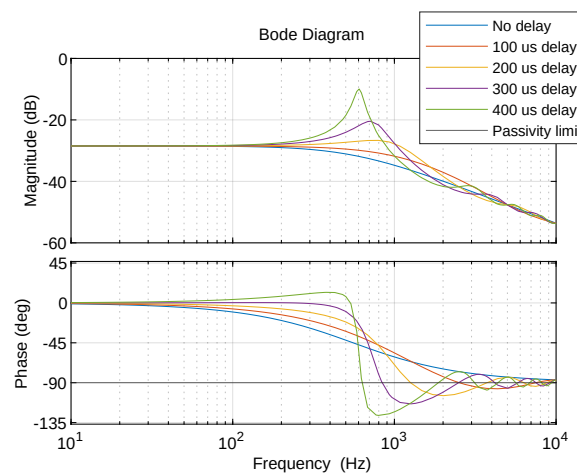


Figure 3. Bode plot of the output admittance of the CHB for different control delays.

The dissipative region associated with passivity is defined by the frequency range up to the point where the phase plot crosses the -90° threshold. From the expression for Y_o in (4), the dissipative region is derived as $f_{dissipative} = (0, \frac{1}{4T_d})$. As shown in Figure 3, the delay significantly impacts this region, with larger delays leading to a reduction in the dissipative frequency range.

Since digital control delay and sensor delay are major contributors to the overall system delay and thus to its passivity, in the following sections we will examine the delay effect caused by different sampling techniques and SD-ADCs in the context of medium-voltage CHB converters.

3. Sampling with Traditional ADCs

Figure 4 shows a traditional ADC sensing solution commonly employed in modern power electronics converters. In this setup, an analog low-pass filter (LPF) reduces high-frequency signal noise and an optional isolation amplifier may be used to provide galvanic isolation. All these components have an associated delay that we combine into t_{ADC} . The ADC conversion is conducted internally by the DSP. A major challenge with this configuration is the complexity of the analog circuit design, as it must account for the entire signal loop to achieve the noise rejection capability.

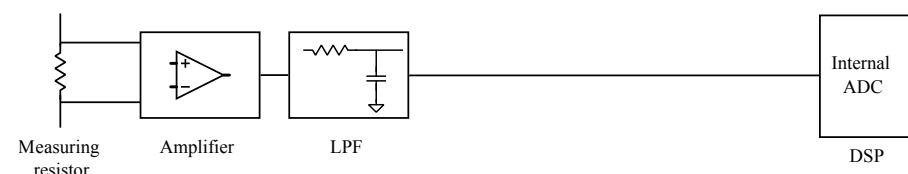


Figure 4. Current sensing using a traditional ADC.

3.1. Unipolar and Bipolar Modulation

The most widely used modulation scheme for the CHB converter is PS-PWM which has two variants: unipolar and bipolar modulation. An example of PS-PWM for $N = 2$ is shown

in Figure 5 for both variants. The phase shift between carriers is given by $\phi_{BM} = 2\pi/N$ for bipolar modulation and $\phi_{UM} = \pi/N$ for unipolar modulation. The modulation signal m is shown in red and its negative in green. The expected voltage output for cells 1 and 2 are $v_1(t)$ and $v_2(t)$, respectively, and their sum gives the total voltage $v(t)$.

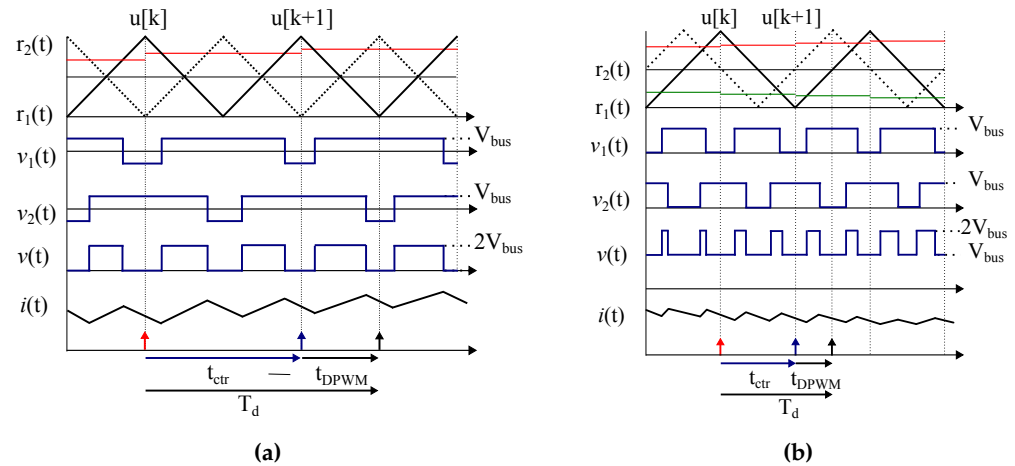


Figure 5. Expected waveforms illustrating interleaved modulation for a CHB with $N = 2$: (a) Bipolar modulation with single sampling; (b) unipolar modulation with double sampling. Key instants: $\uparrow$ sampling, $\uparrow$ modulation update, $\uparrow$ update effect.

Figure 5 shows that the PS-PWM makes the effective switching frequency of the converter $f_{effsw} = Nf_{sw}$ for bipolar modulation and $f_{effsw} = 2Nf_{sw}$ for unipolar modulation [5]. The increase in effective switching frequency also entails an equal increase in the current ripple frequency.

3.2. Single Sampling and Double Sampling

For a single-phase CHB, there are two basic sampling options: single sampling (SS) and double sampling (DS), as illustrated in Figure 5 for a CHB with $N = 2$. The figure shows the modulation signal, the voltage output, and the sampling instants. The carrier signals $r_1(t)$ and $r_2(t)$ are also shown, with a switching period of T_s .

For SS in Figure 5a, the sampling occurs once per cycle, either at the peak or valley of the carrier r_1 , where the instantaneous current matches the average current, reducing high-frequency ripple. The total delay is $T_d = 1.5T_s$. In DS in Figure 5b, sampling occurs at both the peak and valley with a total delay of $T_d = 0.75T_s$.

Sampling with traditional ADCs tends to have noise, especially in the high EMI environments typical of high-power converters. This problem is compounded in MLC because of the increased chances of a sampling event in the vicinity of a switching event. Noise rejection can be implemented with either digital or analog filters, but both introduce a delay.

4. Sampling with Sigma-Delta ADCs

4.1. Sigma-Delta Sensing and Its Delay Effect

To address the challenges of traditional ADCs, Figure 6 presents the diagram of a typical SD-ADC sensing setup. An optional analog LPF can be used to reduce high-frequency noise before the signal enters the SD-ADC modulator. The SD-ADC modulator converts the signal into a digital stream that can be transmitted via an optical fiber interface to the DSP's digital input, providing isolation and physical separation. In the DSP, a low-pass decimation filter is used to remove quantization and high-frequency noise and reconstruct the equivalent measurement signal.

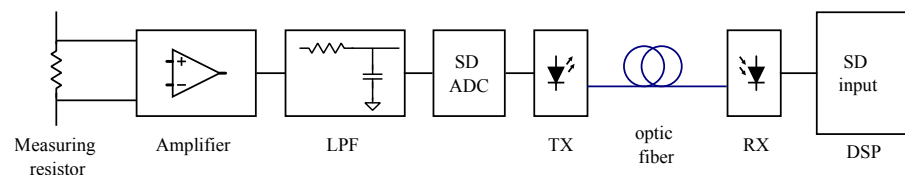


Figure 6. Current sensing using an SD-ADC with optical isolation.

For time-critical applications, the most common decimation filter is the sinc^K filter, characterized by three key parameters, i.e., the modulator frequency f_{mod} , the filter order K , and the oversampling ratio (OSR). Its discrete transfer function is given by the following:

$$H(z) = \left[\frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} \right]^K \quad (8)$$

The sinc^K filter has the frequency response of the sinc function to the power of K [32], as shown by the following equation:

$$H_{\text{sinc}}(f) = \left(\frac{\sin(f \times \pi \times \text{OSR} / (2f_{\text{mod}}))}{f \times \pi \times \text{OSR} / (2f_{\text{mod}})} \right)^K \quad (9)$$

The implementation of the sinc^K SD-ADC on the DSP produces new data at a fixed frequency of $f_{\text{SDoutput}} = f_{\text{mod}} / \text{OSR}$. The decimation filter averages the data over K cycles, resulting in the SD-ADC averaging window defined by

$$t_{\text{SDperiod}} = \frac{K}{f_{\text{SDoutput}}} = \frac{\text{OSR} \times K}{f_{\text{mod}}} \quad (10)$$

Table 1 presents two configurations to illustrate the impact of a shorter versus longer SD-ADC averaging window (t_{SDperiod}), achieved by adjusting the oversampling ratio (OSR) and modulation frequency (f_{mod}) in each case. The magnitude Bode plot in Figure 7a compares their frequency responses. The sinc filter's behavior, influenced by SD-ADC parameters and t_{SDperiod} , lacks an analytical gain-to-delay solution because the sinc function is non-invertible. Figure 7b shows the relationship between the SD-ADC averaging window and cutoff frequency (-3 dB) for sinc^K filters for $K = 3$.

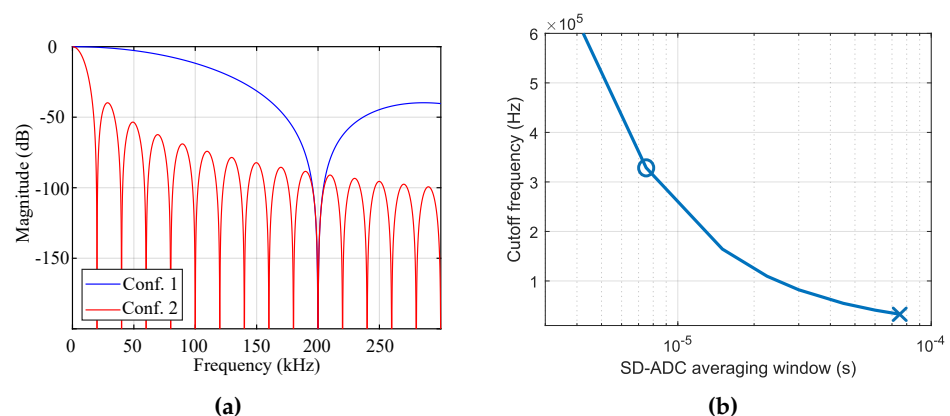


Figure 7. (a) Sinc filter Bode magnitude plot for Configuration 1 ($k = 3$, $\text{OSR} = 50$, $f_{\text{mod}} = 10$ MHz) and Configuration 2 ($k = 3$, $\text{OSR} = 250$, $f_{\text{mod}} = 5$ MHz). (b) Cutoff frequency versus SD-ADC averaging period, with markers for Configuration 1 (o) and Configuration 2 (x).

Table 1. Comparison of SD-ADC parameters for Configurations 1 and 2.

Parameter	Symbol	Configuration 1	Configuration 2
Modulation Frequency	f_{mod}	10 MHz	5 MHz
Order of Sinc Filter	K	3	3
Oversampling Ratio	OSR	50	250
Cutoff Frequency (−3 dB)	f_{cutoff}	330 kHz	33 kHz
SD-ADC Averaging Window	$t_{SDperiod}$	15 μ s	150 μ s

4.2. Single and Double Sampling with Sigma-Delta ADCs

The equivalent sampling instant occurs at the midpoint of the SD-ADC averaging window, and the processed data become available after a delay of $t_{SDdelay} = t_{SDperiod}/2$, which we define as the effective delay introduced by the SD-ADC sensing.

To achieve regular sampling, the equivalent sampling instants of SD-ADC must be aligned with the controller's sampling period (T_{samp}). This alignment requires synchronizing the modulation clock (f_{mod}) with the DSP clock (f_{DSP}), which in turn, requires an additional clock signal from the DSP to the SD-ADC modulator.

Figure 8 compares the sampling delays of traditional ADC sampling and regularly sampled SD-ADC, for both SS and DS. The traditional ADC sampling aims to accurately sample at the point $u[k]$; to conduct this, a start-of-conversion signal is activated before the intended sampling time to account for the propagation delay. The ADC data are ready after the ADC conversion delay t_{ADC} , making the effective available control time $t'_{ctrl} = t_{ctrl} - t_{ADC}$.

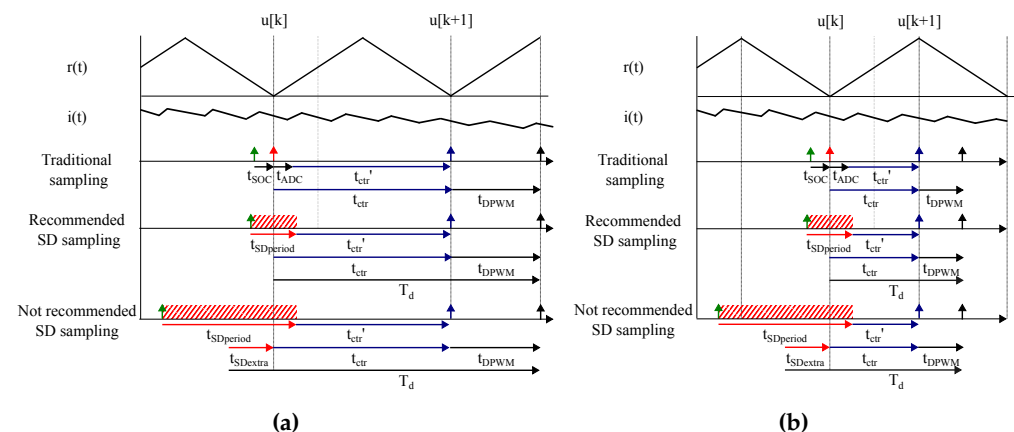


Figure 8. Implementation of different sampling methods with SD-ADCs: (a) single sampling and (b) double sampling. Key instants: $\uparrow$ start of conversion, $\uparrow$ sampling, $\uparrow$ modulation update, $\uparrow$ update effect, $///$ SD-ADC sampling window.

The SD-ADC samples multiple times around the intended sampling instant. Here, the center of the sampling window, $t_{SDperiod}$, represents the “instant” of interest, as shown in the red area in Figure 8. Data from the SD-ADC become available after a delay of $t_{SDdelay}$, which is half of $t_{SDperiod}$, resulting in an effective control time of $t'_{ctrl} = t_{ctrl} - t_{SDdelay}$.

In Figure 8, the total delay is labeled as T_d , which consists of the SD-ADC delay $t_{SDdelay}$, computational delay t'_{ctrl} , and the effective delay from the PWM T_{DPWM} . Importantly, if the parameters of the SD-ADC are correctly selected, there is no additional delay introduced to the system, which is shown as the recommended SD sampling in Figure 8.

In contrast, Figure 8 also shows an example of a non-recommended $t_{SDperiod}$ that exceeds the sampling period T_s . This extended $t_{SDperiod}$ cannot align with the intended sampling point $u[k]$. As an alternative, the middle of the SD sampling window is aligned with the middle point of the carrier before $u[k]$, which ensures the sampling of the average current. However, this results in a measurement with an effective delay $t_{SDextra}$. Such a

configuration would negatively impact both the bandwidth and passivity of the system as we will show in the simulation and hardware tests.

When using SD-ADCs, the sampling window of SS can be larger than that with DS, leading to a slightly better averaging effect than that of DS. SS allows for more time for control algorithm computation. However, the processing time delay t_{ctrl} of SS is twice as much as that of DS. In a generic case of multisampling with more than two samples in a carrier period, to avoid additional sensing delays, the recommended $t_{SDperiod}$ should only be a small fraction of the sampling period, allowing enough time for the necessary calculations. If the α ($0 < \alpha < 1$) portion of the sampling period, i.e.,

$$\alpha = \frac{t'_{ctrl}}{T_{samp}} \quad (11)$$

is reserved for calculation; the $t_{SDperiod}$ constraint is

$$(1 - \alpha)T_{samp} = \frac{1 - \alpha}{f_{samp}} = \frac{t_{SDperiod}}{2} = \frac{OSR \times K}{2f_{mod}} \quad (12)$$

However, (12) shows that this may become difficult for multisampling as the sampling frequency increases. Therefore, the following process is recommended to implement multisampling with SD-ADC:

1. Profile the program to find t'_{ctrl} required for control algorithm computation.
2. Determine the sampling frequency according to the desired multisampling method. In conservative designs, it is recommended to have $\alpha \approx 0.6$ in (11) to have a good trade-off between the SD-ADC averaging effect and the multisampling frequency.
3. Choose the OSR, f_{mod} , and K according to (10) for the SD-ADCs.

5. Simulation and Experimental Results

5.1. Simulation Results

To verify the analysis and proposed implementation, PLECS software version 4.7.5 was used to simulate a CHB Converter with grid-side current control, following the overall system diagram shown in Figure 2a. The system parameters are given in Table 2. The grid voltage is simulated as a sum of an ideal 60 Hz fundamental component and 3rd-, 5th-, 7th-, and 13th-order harmonics,

$$E = V_{grid} \sin(\omega_o t) + \sum_{n \in \{3, 5, 7, 11, 13\}} V_n \sin(n\omega_o t) \quad (13)$$

The harmonic components V_n were extracted from the experimental grid voltage waveform and used for the simulation. In the CHB converter, PR controllers (5) with resonant components for the fundamental, third, and fifth harmonic components are implemented to enhance current control performance under distorted grid voltage conditions.

Table 2. System Parameters.

Parameter	Value	Symbol
Number of modules	6	N
Grid voltage	2400 Vrms	E
Total inductance	12 mH	L
Rated power	300 kW	P_{rated}
Shared DC bus voltage	300 V	V_{DCbus}
CHB cell bus voltage	1000 V	V_{CHBbus}
Fundamental frequency	60 Hz	f_o
Switching frequency	5 kHz	f_{sw}
Effective switching frequency	60 kHz	$f_{sw,eff}$

We implemented two SD-ADC configurations for comparison, i.e., Configurations 1 and 2 listed in Table 1. To compensate for the additional delay in Configuration 2, which originates from the SD-ADC sensor, the control bandwidth is adjusted to maintain stability and achieve a similar phase margin. The simulations use a bandwidth of 750 Hz for Configuration 1 and 500 Hz for Configuration 2 by varying the proportional gain K_p according to (6).

First, we adopt the method in [7] to measure the CHB output impedance Y_o and assess the impact of SD-ADC's delay on the passivity of the CHB converter. To be more specific, we use a single variable-frequency voltage source E as a disturbance and measure the current response of the CHB. Multiple simulations were conducted at varying disturbance frequencies ω_{dis} to obtain diverse datapoints. The output admittance Y_o was calculated based on the current i and the disturbance voltage E .

Figure 9 shows the Bode plot of the simulated output admittance for the CHB model, compared with theoretical values from (4), for SD-ADC Configurations 1 and 2 (Table 1). As illustrated in Figure 9, the measured impedance aligns closely with the values derived from the theoretical equations for both SD-ADC configurations. This agreement confirms the accuracy of the analysis of the SD-ADC delay presented in Section 4.

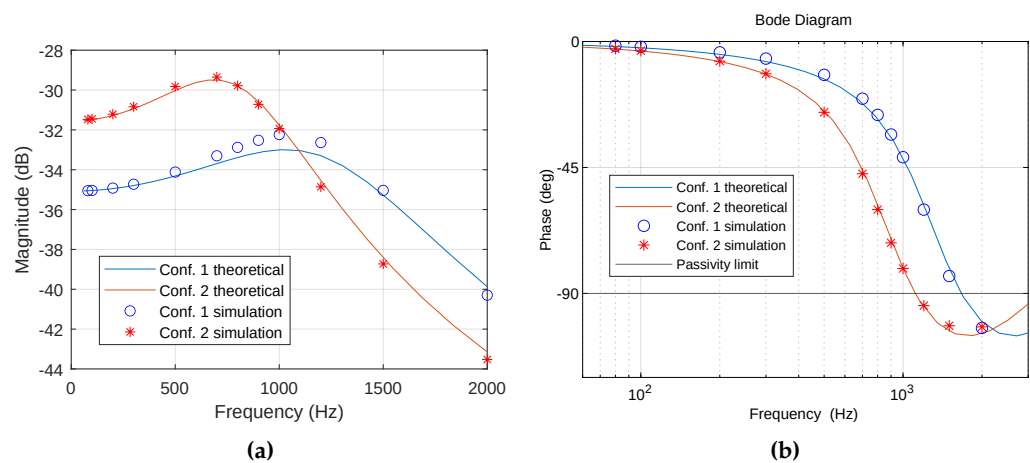


Figure 9. Bode plots of the output admittance of the CHB converter: (a) magnitude (b) phase, with SD-ADC Configurations 1 and 2 are given in Table 1.

Additionally, it can be observed from Figure 9b that the CHB output impedance Y_o with SD-ADC Configuration 1 exhibits a larger passivity region than with Configuration 2. This is because the averaging window $t_{SDperiod}$ of Configuration 2 (150 μ s) is larger than that of Configuration 1 (15 μ s), resulting in an increased effective delay and reduced passivity region. This shows the impact of SD-ADC configuration on the converter's passivity characteristics.

Next, the CHB converter is connected to the grid to examine the impact of ADC configurations on the current control performance. With the DS strategy, the current waveform results are shown in Figure 10. It can be observed that Configuration 1 has lower harmonic content than Configuration 2 due to the reduced delay, and therefore, increased control bandwidth.

Finally, additional simulations were performed using both traditional and SD-ADC sensing methods, testing under SS and DS strategies with different current control bandwidths, as shown in Table 3. For SS, a lower bandwidth was selected to account for the increased control delay. In contrast, DS strategies demonstrated a lower total harmonic distortion (THD) compared to SS strategies. With proposed Configuration 1, the SD-ADC achieved a similar THD to that of traditional ADCs.

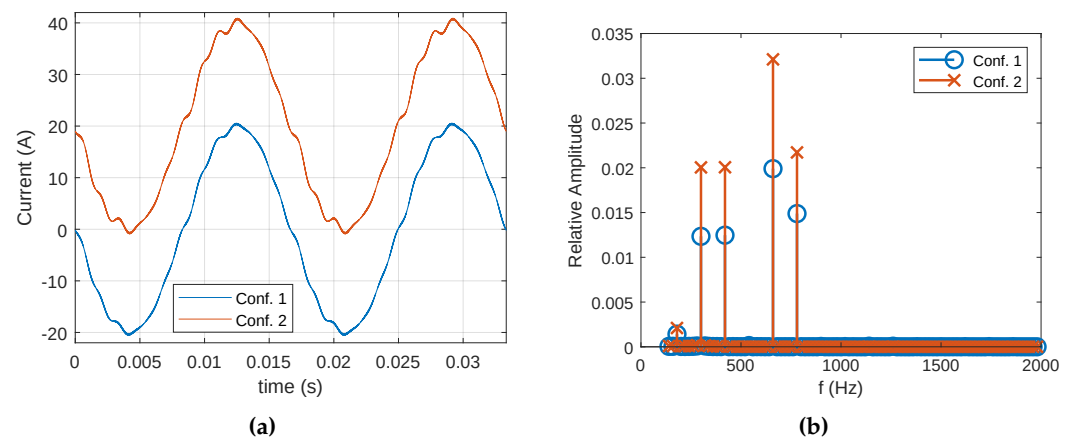


Figure 10. Simulation results for the two SD-ADC configurations in Table 1: (a) current waveforms; (b) harmonic spectrum of the current waveforms.

Table 3. Comparison of simulation results for different sampling strategies.

Simulation with Different Sampling Strategies	BW (Hz)	THD (%)	Harmonic Content (%)				
			3rd	5th	7th	11th	13th
SS Traditional	500	6.8	0.2	2.0	2.4	5.1	3.2
SS SD-ADC (Conf 1)	500	7.0	0.2	2.1	2.5	5.4	3.1
SS SD-ADC (Conf 2)	500	8.2	0.2	2.2	3.2	6.8	2.5
DS Traditional	750	3.0	0.1	1.2	1.2	1.9	1.4
DS SD-ADC (Conf 1)	750	3.1	0.1	1.2	1.2	2.0	1.5
DS SD-ADC (Conf 2)	750	4.3	0.2	1.3	1.4	2.9	2.6
DS SD-ADC (Conf 2)	500	4.8	0.2	2.0	2.0	3.2	2.2

5.2. Experimental Results

Figure 11 shows the experimental setup which includes a 6-cell single-phase CHB to test different SD-ADC configurations for measuring current. A utility transformer steps up the grid voltage to supply 2400 Vrms medium-voltage AC input to the CHB, and a solid-state breaker (SSB) is positioned between the transformer and CHB for fast disconnection. The control cabinet, housing the central controller along with grid current and voltage sensors, is situated at the bottom of the CHB rack. The top-left insert of Figure 11 shows a single CHB cell, which includes an H-bridge converter and an isolated DC–DC converter using a dual active bridge (DAB) topology. Each cell has a local controller for DAB control, while the central controller manages the H-bridge converters, as well as the CHB’s overall operation and protection. The controller is TMS320F28379D, and the SD-ADC modulator is AMC1306M25, both are from Texas Instruments (Dallas, TX, USA). The current sensor is LF 210-S from LEM (Geneva, Switzerland).

The parameters used for the tests are given in Table 2. The system was operated with phase-shifted unipolar PWM making the effective switching frequency 12 times higher than the switching frequency. We tested the two configurations of SD-ADC parameters shown in Table 1 to evaluate their effect on converter performance. Similar to the simulation setup, PR controllers with resonant components for the fundamental, third, and fifth harmonic components are implemented. In addition, the control bandwidth is designed to be 750 Hz for Configuration 1 and 500 Hz for Configuration 2, by varying the proportional gain K_p .

To compare their frequency responses, Figure 12 shows the open-loop Bode plot of the current transfer function, defined as

$$G_{ol} = G_c(s)G_{dp}(s)G_s(s)G_p(s) \quad (14)$$

As shown in Figure 12, the Bode plot confirms that both configurations have a similar phase margin, although they have different control bandwidths. In other words, to achieve

the same stability margin, the control bandwidth of Configuration 2 has to be reduced due to the additional delay originating from the SD-ADC.

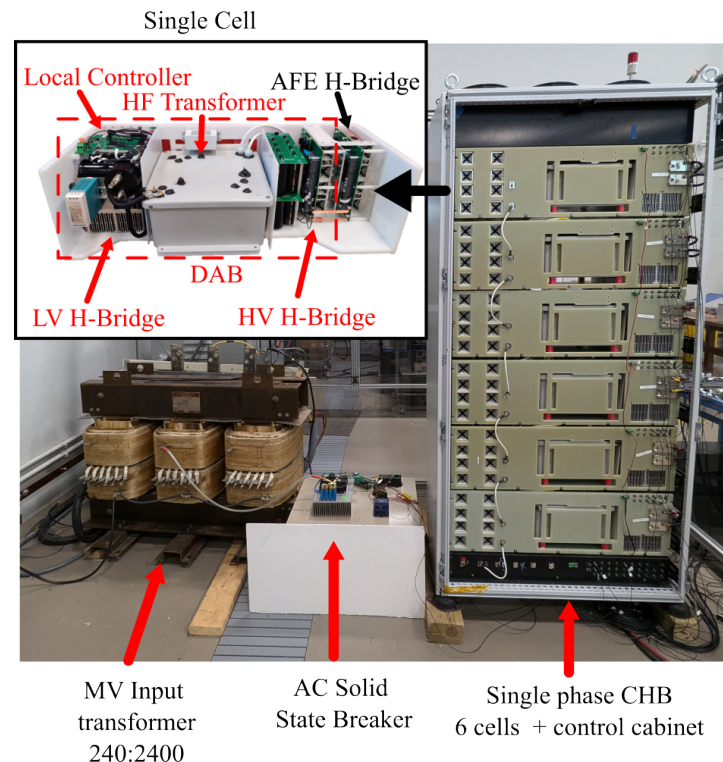


Figure 11. Experimental setup: the control cabinet is located at the bottom of the rack that houses the six cells of the CHB. The top-left insert shows details of a single cell.

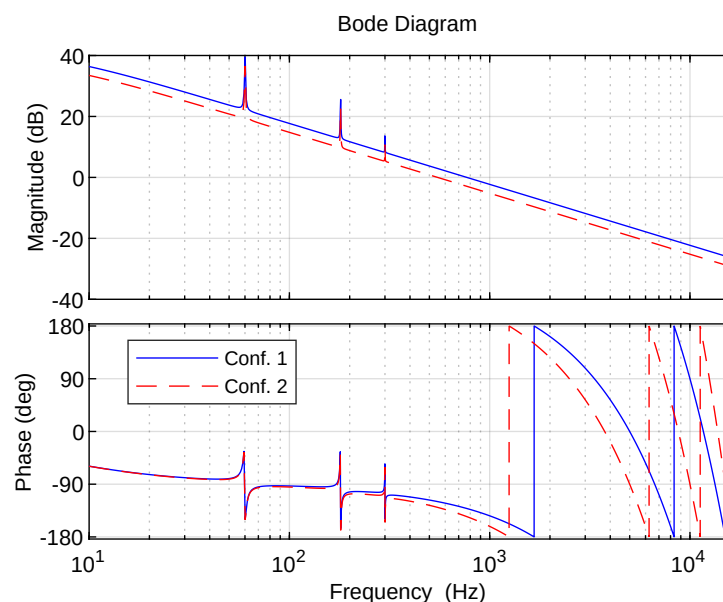


Figure 12. Open-loop Bode plot of the current transfer function for Configurations 1 and 2.

Figure 13 shows the measured grid voltage. The most significant harmonic voltages are the 3rd, 5th, 7th, 11th, and 13th. Figure 14 shows the experimental current waveforms and their harmonic spectra for Configurations 1 and 2, highlighting an improved harmonic response in Configuration 1. Configuration 1 has a better THD because of the decreased delay and increased bandwidth, with measured THD values of 4.5% for Configuration 1 and 5.5% for Configuration 2. Notably, the 11th harmonic component, which is significant

in Configuration 2, was significantly reduced in Configuration 1. The 11th harmonic shows the strongest difference in attenuation because the bandwidth in Configuration 1 extends beyond its frequency, allowing for greater attenuation. The harmonic contents for the grid voltage and currents under Configurations 1 and 2 can be found in Table 4.

Table 4. Experimental results for THD and harmonic content.

Hardware Tests Waveforms	BW (Hz)	THD (%)	Harmonic Content (%)				
			3rd	5th	7th	11th	13th
Grid Voltage	-	2.2	0.7	1.1	0.3	0.6	0.4
DS SD-ADC (Conf 1)	750	4.5	1.4	1.3	0.9	2.2	1.8
DS SD-ADC (Conf 2)	500	5.5	1.5	1.5	1.3	3.3	2.8

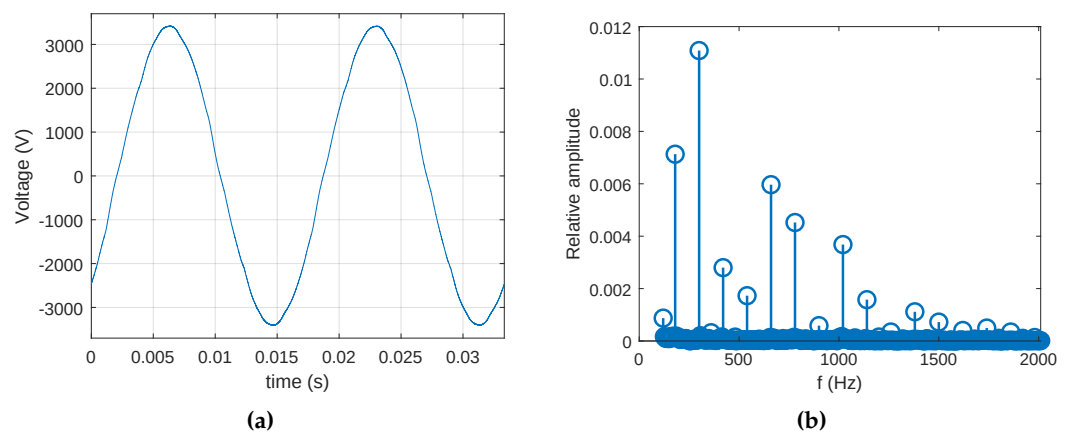


Figure 13. (a) Measured grid voltage waveform (b) harmonic spectrum.

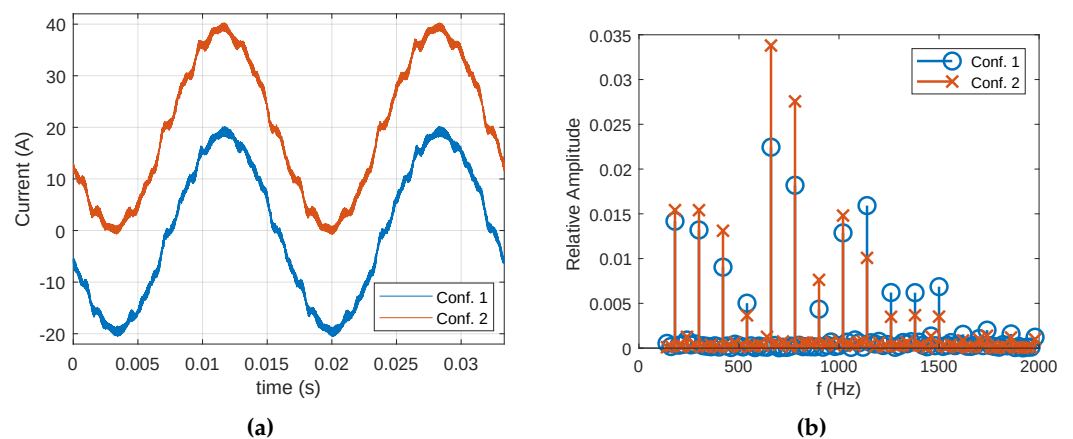


Figure 14. (a) Experimental current waveform results. Configuration 2 is plotted with a +20 A offset. (b) Experimental harmonic spectrum of the current waveform for Configurations 1 and 2.

Figure 15 displays the experimental waveforms of the grid current and shared DC bus voltage specifically for Configuration 1. The shared DC bus voltage tracks a nominal value of 300 V with a ripple of 15 V_{pp} at 120 Hz, caused by the power oscillation of the single-phase voltage output. The voltage output is connected to a resistive load, with the load rated at 30 kW.

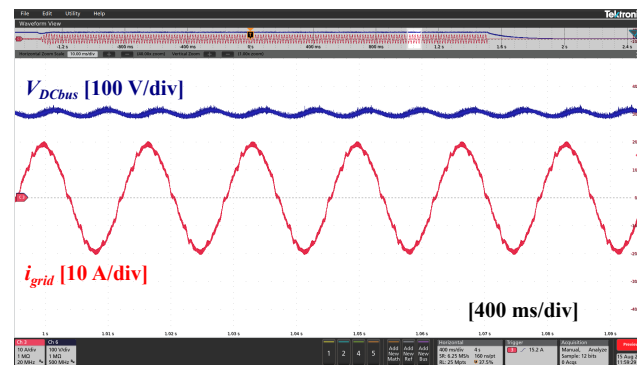


Figure 15. Experimental results for Configuration 1 showing the shared DC bus voltage tracking.

5.3. Discussion

The results from both the simulation and experimental analysis show consistent trends, demonstrating the effectiveness of the proposed SD-ADC configurations in medium-voltage CHB converters. As seen in Figure 14, experimental results confirm the simulation findings, with Configuration 1 showing a better harmonic response than Configuration 2 due to its increased bandwidth and reduced delay.

The simulation and experimental results also confirm that, with properly selected parameters, SD-ADC-based multisampling performs as well as traditional sampling. This makes SD-ADC a practical alternative, offering benefits such as reduced hardware complexity and improved control resolution while maintaining system stability and performance.

6. Conclusions

This work investigated the integration of multisampling techniques with SD-ADCs in medium-voltage CHB converters, addressing key challenges related to delay and passivity. The findings demonstrate that SD-ADC sensing, when combined with multisampling strategies, effectively balances the trade-offs between delay minimization, control bandwidth, and system stability. Through detailed simulations and hardware experiments on a 2400 Vrms CHB converter, the proposed approach was validated, showcasing its practicality and performance advantages.

Key contributions of this work include the analysis of SD-ADC-induced delay effects on converter passivity, the development of guidelines for parameter selection, and the successful implementation of multisampling with SD-ADC sensing. Test results highlight that shorter averaging windows and precise parameter tuning allow SD-ADCs to achieve comparable or superior performance to traditional ADCs while offering additional benefits such as simplified hardware design for galvanic isolation.

These findings underscore the potential of SD-ADCs as a viable alternative for high-performance converter control in medium-voltage applications, enabling improved stability, reduced THD, and higher control bandwidth.

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