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A Novel High-Gain Multi-Stage Switched-Capacitor-Based DC-DC Boost Converter with Closed-Loop Control

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Abstract: In this manuscript, a direct current (DC) boost converter based on a switched-capacitor circuit with closed-loop control, tailored for applications with high-voltage gain, is introduced. The converter utilizes a network with switching capacitors to enhance voltage gain without relying on inductors, making it ideal for high-voltage scenarios. An active disturbance rejection control (ADRC)-based control scheme is used to maintain output voltage stability in the presence of disturbances. The proposed converter's functionality and performance are assessed through simulations and experimental tests under various load conditions. A loss analysis, considering the losses from switches and diodes, is provided to determine the net efficiency. The results from both simulations and experiments show that the proposed converter achieves a high-voltage gain, excellent load regulation, and rapid transient response, highlighting its potential for applications that require a high-voltage boosting operation.

Keywords: SC-BC; DC-DC converter; duty ratio; voltage gain; volt–sec balance; ADRC; observer; controller

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1. Introduction

In recent times, there has been a significant increase in the use of energy storage devices in conjunction with renewable energy sources like fuel cells and photovoltaics (PVs). The DC characteristics of such energy sources are the major cause of increasing interest in DC microgrids. In order to maintain a steady supply of energy and balance variations in generation and demand, energy storage electrical systems stores the abundant energy for later use. They are essential for grid stability, backup power, renewable energy systems, and electric vehicles (EVs) [1]. However, these devices frequently produce low voltage, which prompts for high-gain converters to raise it to levels that are usable. Also, the energy produced by PV panels generally have low voltage due to various factors such as partial shading, dirt, lower light intensity, and lower designed efficiency of around 20%, and thus the demand for high-gain DC-DC converters is increasing to optimize the flow of power [2]. The voltage can only be increased by around two to three times the input voltage using a traditional boost converter [3]. If its duty cycle further increases to achieve a higher gain, the system tends towards instability and also, at higher duty cycles, the controller may fail to stabilize the converter. Additionally, using a converter at very high duty cycles (0.9 or above) or very low duty cycles (near 0.1) causes unfavorable nonlinear behavior and decreased efficiency [4–7]. This issue is addressed and solved in [8] by designing a Luo super-lift-based converter consisting of many switches. However, this converter has significantly increased switching losses and could achieve a voltage gain of up to around 10 only. Some authors have used a transformer in the circuit of the converter to achieve a higher gain, as in the flyback converter explained in [9]. Their circuit becomes bulky and

costly with the use of a transformer, Also, the converter's overall efficiency decreases due to the presence of leakage inductance in the transformer.

Researchers attempted to achieve higher gains by eliminating the transformers using non-isolated inductors in [10,11]. In [10], the efficiency of the converter is claimed to be around 92%. Also, the cost of the converter is high due to the presence of two high-frequency inductors. This problem is also faced by the converter in [11] as it has two coupled inductors. Also, this converter has an efficiency of around 92.7%. Some authors have achieved high gains by cascading various individual converter stages [12–14]. However, with the cascading phenomenon, the losses increase, resulting in reduced efficiency. In the literature, switched-capacitor-based boost converters (SC-BCs) are receiving tremendous attention from researchers for harvesting energy with a high-voltage gain from non-conventional sources [15,16]. These are hybrid types of converters that do not contain bulky transformers and give much-improved efficiency [16–20]. The main aim of the design of hybrid SC-BC converters is to multiply the input voltage with a network consisting of some switches and capacitors and then feed this voltage to a boost converter, thereby increasing the voltage gain to a larger value. The author in [21] developed a model of a high-gain switched-capacitor-based boost converter without the need of any inductor. However, due to the absence of an inductor, the input current rises instantly during the transient phase. This leads the input source to enter a constant current mode. This may be harmful to the devices connected at the output of this converter. In [22], the author proposed a model of a switched-capacitor-based boost converter consisting of many diodes and MOSFETs. The above-said circuit is further modified by replacing all the diodes with the MOSFETs to eliminate the voltage drops in the diodes [23]. However, this modified circuit contains many switches, that may result in poor efficiency at higher switching frequencies (due to switching losses in the MOSFETs). In [24], a switched-capacitor-based boost converter circuit was designed by the author for high-voltage gain applications with three duty ratios and an efficiency of 93.4%. Nonetheless, the use of three duty ratios makes the controllability of the said converter quite complex.

It has been seen that authors in the previously reported works have focused on the design of switched-capacitor-based converters to achieve a higher gain without considering their closed-loop control. However, it is impossible to achieve a fixed DC voltage at the output of the converter in the presence of unwanted disturbances (varying load, varying input, noise, etc.). Designing control laws for SC-BC converters is a great challenge to researchers, as these circuits are highly nonlinear and exhibit inverse response characteristics. In the present manuscript, a novel switched-capacitor-based boost converter consisting of three diodes, five MOSFETs, three capacitors, an inductor, and a load resistor is proposed. The key advantage of the designed converter is that a substantial voltage gain can be obtained by operating the switches together with two different duty ratios. This concept of two-duty ratios facilitates the user to achieve a substantially high gain without the use of an extreme duty ratio. Furthermore, the active disturbance rejection control (ADRC) is applied to the proposed converter to achieve its stable closed-loop operation. ADRC is an advanced control technique that estimates the disturbances as a separate variable and suppresses them in real time [25–29]. The robustness of the proposed controller towards variations in the reference voltage, input signal, and load resistance is verified through simulations and experiments. The main contributions of this work are therefore summarized as follows:

- A novel switched-capacitor-based boost converter is proposed that provides a high-voltage gain.
- The gain of the proposed converter is calculated and found to be higher than a conventional boost converter and the converters in [10,11,24].
- The recommended converter is controlled using an ADRC technique to achieve a stable and fixed DC under varying loads and environmental conditions increasing its suitability for renewable energy applications.
- Loss analysis for the circuit is performed for four different loads and efficiencies of more than 94% are achieved.

This paper has been organized in the following way. Section 2 describes the principle of operation of the proposed converter. A brief description of the mathematical modeling for the converter is given in Section 3. The performance characteristics are explained in Section 4. Section 5 describes the design and tuning method for the ADRC-based controller. Section 6 describes the results obtained from the simulation and experimental setups. Furthermore, a loss analysis is also performed which is analyzed in Section 7. The conclusion is derived in Section 8.

2. Proposed Circuit

The complete structure of the proposed switched-capacitor (SC)-based boost converter circuit is shown in Figure 1a. This is a hybrid structure consisting of a switched-capacitor circuit and a boost-converter circuit arranged in a cascaded manner. With the aid of the capacitors, the first stage of the circuit, which consists of a network of switched capacitors, doubles the input voltage. The second stage then increases the input voltage and transfers the energy to the load side with an enhanced output voltage. In the switched-capacitor circuit, there are four MOSFETs (T_1, T_2, T_3, and T_4), two diodes ($d1$ and $d2$), and two capacitors (C_1 and C_2). The boost converter circuit has an inductor (L_b), a capacitor (C_b), a MOSFET (T_b), a diode (d_b), and a load resistance (R_L). The diode voltage drop is denoted by v_D which is approximately 0.7 V. There is no such voltage drop in the case of the MOSFETs. There are three different modes in which the circuit can function:

The time span of the first mode is zdT_s, where z is the charging duty cycle of the switched-capacitor circuit over the span dT_s. The duration of the second and third modes are $(1-z)dT_s$ and $(1-d)T_s$, respectively. The circuit diagram of the first mode of operation is depicted in Figure 1b. In this mode, MOSFETs T_2, T_4, and T_b are switched ON while MOSFETs T_1 and T_3 are kept OFF. The voltage across both the capacitors C_1 and C_2 keeps rising. In the meantime, the load voltage is supplied by the capacitor C_b, which discharges through the load resistance R_L. In the second stage, as depicted in Figure 1c, the MOSFETs T_1, T_3, and T_b are switched ON while keeping the MOSFETs T_1 and T_3 OFF. This mode charges the inductor with a voltage three times the input voltage by connecting the voltages across the capacitors and the source in series. On the load side, the capacitor still discharges through the load as in the first stage. In the third stage, only the MOSFET T_b is switched OFF keeping the other circuit conditions as they were in the second stage. Here, the stored energy in the capacitors combined with the stored energy in the inductor and voltage source is plunged to the capacitor C_b, so that the output voltage is increased in comparison with the input voltage depending on the duty ratio of T_b. Also, the load resistor R_L is supplied by the load current through the input source.

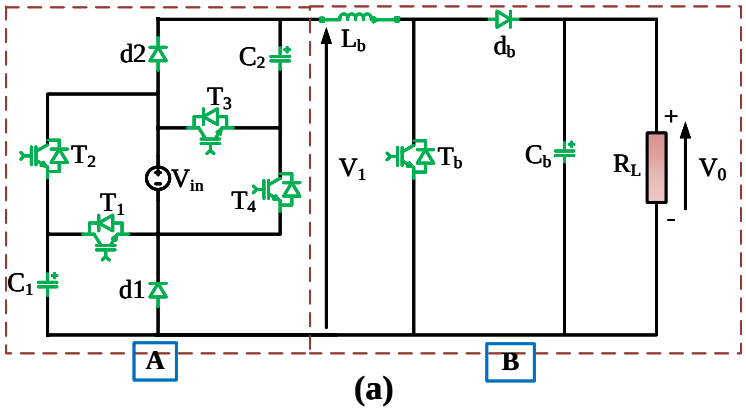


Figure 1. *Cont.*

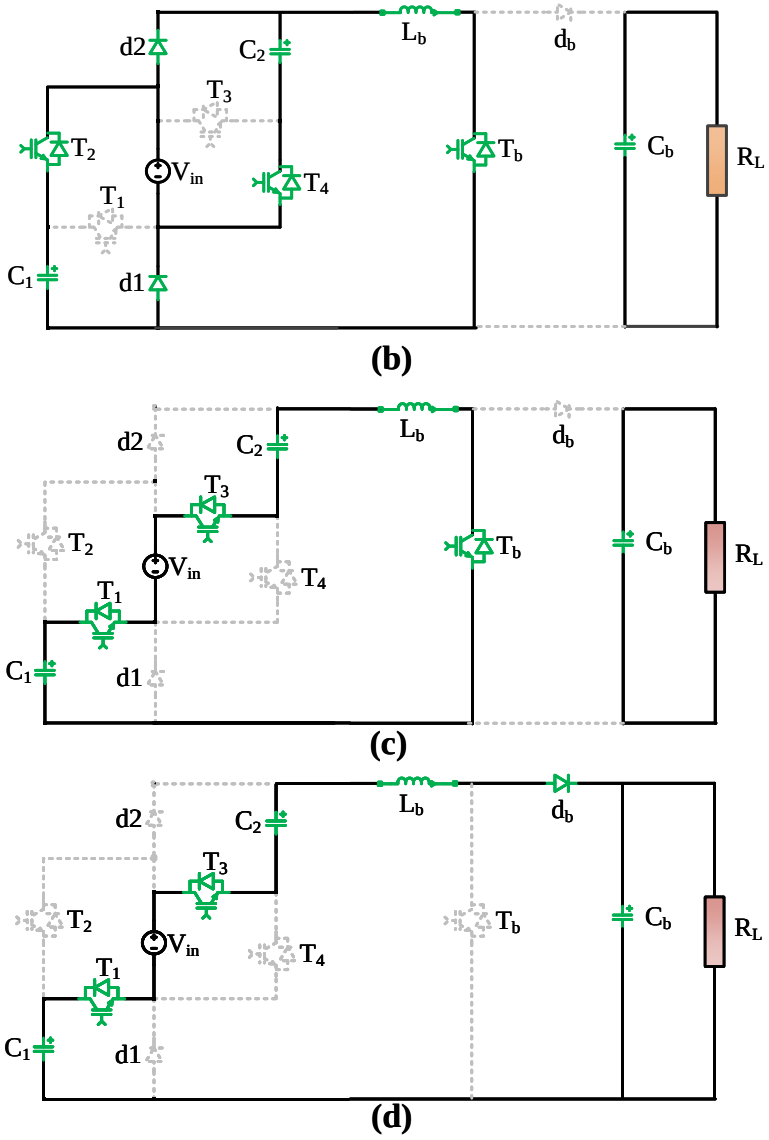


Figure 1. Proposed SC-based DC-DC converter. (**a**) Complete circuit diagram. (**b**) Mode 1 operation (time interval (zd)*T_s: C_1, C_2, C_3, and L_b are being charged). (**c**) Mode 2 operation (time interval $(1-\text{z})\text{d}T_s$: capacitors are connected in series and L_b is charged to higher voltage). (**d**) Mode 3 operation (time interval $(1-\text{d})T_s$ L_b: is discharged and output voltage is boosted).

3. Mathematical Modeling of Proposed Converter

As mentioned in the previous section, the SC-BC has three modes of operation. The differential equations are obtained independently in these three modes of operation. To obtain the combined differential equation, the state-space averaging technique is used. The diode voltage drop is considered to be 0.7 V. The internal resistance of the source voltage (V_{in}) is designated R_{in} while that of the inductor is designated R_{L_b}. The internal resistance of MOSFET is very small and is neglected. The value of the capacitances in the switched-capacitor circuit is equal and can be denoted by C. Also, the voltage across these capacitors will be equal and is denoted by v_C.

3.1. Mode 1

The differential Equations (1)–(3) represent the state variables in this mode:

$$\frac{dv_C}{dt} = \frac{1}{2CR_{in}}v_{in} - \frac{1}{2C}i_{L_b} - \frac{1}{2CR_{in}}(v_C + v_D) \tag{1}$$

$$\frac{di_{L_b}}{dt} = \frac{v_C - v_D}{L_b} - \frac{R_{L_b}}{L_b} i_{L_b} \tag{2}$$

$$\frac{dv_o}{dt} = -\frac{v_o}{R_L C_b} \tag{3}$$

3.2. Mode 2

Equations (4)–(6) corresponding to this mode are as follows:

$$\frac{dv_C}{dt} = -\frac{1}{C} i_{L_b} \tag{4}$$

$$\frac{di_{L_b}}{dt} = \frac{1}{L_b} v_{in} - \frac{2}{L_b} v_C - \frac{(R_{in} + R_L)}{L_b} i_{L_b} \tag{5}$$

$$\frac{dv_o}{dt} = -\frac{v_o}{R_L C_b} \tag{6}$$

3.3. Mode 3

The differential Equations (7)–(9) defining this mode are as follows:

$$\frac{dv_C}{dt} = -\frac{1}{C} i_{L_b} \tag{7}$$

$$\frac{di_{L_b}}{dt} = \frac{1}{L_b} v_{in} - \frac{2}{L_b} v_C - \frac{(R_{in} + R_L + R_{L_b})}{L_b} i_{L_b} - \frac{1}{L_b} v_o \tag{8}$$

$$\frac{dv_o}{dt} = \frac{1}{C_b} i_{L_b} - \frac{1}{R_L C_b} v_o \tag{9}$$

To combine the three modes in a complete interval the state-space averaging technique is used such that the three modes are summed up by multiplying with zd, $(1-z)d$, and $(1-d)$, respectively. The averaged Equations (10)–(12) are given as follows:

$$\frac{dv_C}{dt} = \frac{zd}{2CR_{in}} v_{in} - \frac{zd}{2CR_{in}} v_C - \frac{zd}{2CR_{in}} v_D - \frac{(2-zd)}{2C} i_{L_b} \tag{10}$$

$$\begin{aligned} \frac{di_{L_b}}{dt} =& \frac{(1-zd)}{L_b} v_{in} + \frac{(3zd-2)}{L_b} v_C - \frac{zd}{L_b} v_D + \\ & \frac{((zd-1)R_{in} - R_{L_b} + (d-1)R_L)}{L_b} i_{L_b} - \frac{(1-d)}{L_b} v_o \end{aligned} \tag{11}$$

$$\frac{dv_o}{dt} = \frac{(1-d)}{C_b} i_{L_b} - \frac{1}{R_L C_b} v_o \tag{12}$$

Small signal analysis can be carried out by introducing a small perturbation on all the state variables. However, in order to develop the model, smaller perturbations are ignored, keeping only the average values of the variables such as $zd \Rightarrow ZD$, $v_{in} \Rightarrow V_{in}$, $v_C \Rightarrow V_C$, $i_{L_b} \Rightarrow I_{L_b}$, $v_D \Rightarrow V_D$, and $v_o \Rightarrow V_o$.

Hence, these changes are substituted into Equations (10)–(12) to obtain a large signal model in Equations (13)–(15) written below as follows:

$$\begin{aligned} \frac{dV_C}{dt} =& \frac{ZD}{2CR_{in}} V_{in} - \frac{ZD}{2CR_{in}} V_C - \frac{ZD}{2CR_{in}} V_D - \\ & \frac{(2-ZD)}{2C} I_{L_b} \end{aligned} \tag{13}$$

$$\frac{dI_{L_b}}{dt} = \frac{(1-ZD)}{L_b}V_{in} + \frac{(3ZD-2)}{L_b}V_C - \frac{(1-D)}{L_b}V_o + \frac{((ZD-1)R_{in} - R_{L_b} - (1-D)R_L)}{L_b}I_{L_b} - \frac{ZD}{L_b}V_D \tag{14}$$

$$\frac{dV_o}{dt} = \frac{(1-D)}{C_b}I_{L_b} - \frac{1}{R_L C_b}V_o \tag{15}$$

Under steady-state conditions, the above time derivatives may be equated to zero. Therefore, we have the following (16):

$$\frac{dV_C}{dt} = \frac{dI_L}{dt} = \frac{dV_o}{dt} = 0 \tag{16}$$

Substituting (16) into (13)–(15), we obtain the following:

$$V_0 = \frac{N_1^r}{D^r}V_{in} + \frac{N_2^r}{D^r}V_D \tag{17}$$

where $N_1^r = (2ZD-1)ZD(1-D)R_o$, $N_2^r = (4-4ZD)(1-D)ZDR_o$, and $D^r = (9ZD - 4 - 4Z^2D^2)R_{in} + (2ZD - 3ZD^2 + ZD^3)R_o + ZDR_L$.

The diode voltage drop may be nullified by replacing diodes with MOSFETs.

3.4. Small Signal Modeling of the Developed Converter

The three modes of the converter are explained by assuming the duty ratio of all three modes as D_1, D_2, and $1-(D_1+D_2)$, respectively. The timing diagram depicting all the modes is shown in Figure 2. This figure also depicts the ON and OFF times of each switch and diode. Neglecting the diode voltage drop, the averaged model of the suggested converter using Equations (1)–(9) in terms of D_1 and D_2 is given as follows:

$$\begin{bmatrix} \frac{dv_C}{dt} \\ \frac{di_{L_b}}{dt} \\ \frac{dv_o}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{D_1}{2CR_{in}} & \frac{D_1-2}{2C} & 0 \\ \frac{3D_1-2}{L_b} & -\frac{R_x - D_1(R_{in}+R_L) - D_2R_{L_b}}{L_b} & \frac{-(1-D_1-D_2)}{L_b} \\ 0 & \frac{(1-D_1-D_2)}{C_b} & -\frac{1}{C_b} \end{bmatrix} \begin{bmatrix} v_C \\ i_{L_b} \\ v_o \end{bmatrix} + \begin{bmatrix} \frac{D_1}{2CR_{in}} \\ \frac{1-D_1}{L_b} \\ 0 \end{bmatrix} v_{in} \tag{18}$$

where $R_x = R_{in} + R_L + R_{L_b}$. The small signal model could be derived by perturbing each of the variables in Equation (18). The perturbed variables could be depicted as $d_1 = D_1 + \hat{d}_1; d_2 = D_2 + \hat{d}_2; v_C = V_C + \hat{v}_C; i_{L_b} = I_{L_b} + \hat{i}_{L_b}; v_o = V_o + \hat{v}_o; v_{in} = V_{in} + \hat{v}_{in}$.

The above perturbations are substituted in Equation (18) and the steady-state parts are removed. Hence, the small signal model of the designed converter is obtained as follows:

$$\begin{bmatrix} \dot{\hat{v}}_C \\ \dot{\hat{i}}_{L_b} \\ \dot{\hat{v}}_o \end{bmatrix} = \begin{bmatrix} -\frac{D_1}{2CR_{in}} & \frac{D_1-2}{2C} & 0 \\ \frac{3D_1-2}{L_b} & -\frac{R_x - D_1(R_{in}+R_L) - D_2R_{L_b}}{L_b} & \frac{-(1-D_1-D_2)}{L_b} \\ 0 & \frac{(1-D_1-D_2)}{C_b} & -\frac{1}{C_b} \end{bmatrix} \begin{bmatrix} \hat{v}_C \\ \hat{i}_{L_b} \\ \hat{v}_o \end{bmatrix} + \begin{bmatrix} \frac{I_{L_b}+R_{in}I_{L_b}-V_C}{2CR_{in}} \\ \frac{3V_C+(R_{in}+R_L)I_{L_b}-V_o-V_{in}}{L_b} \\ -\frac{I_{L_b}}{C_b} \end{bmatrix} \hat{d}_1 + \begin{bmatrix} 0 \\ \frac{R_{L_b}I_{L_b}-V_0}{L_b} \\ -\frac{I_{L_b}}{C_b} \end{bmatrix} \hat{d}_2 + \begin{bmatrix} \frac{D_1}{2CR_{in}} \\ \frac{1-D_1}{L_b} \\ 0 \end{bmatrix} v_{in} \tag{19}$$

This equation can be written in simplified form as follows:

$$\begin{bmatrix} \dot{\hat{v}}_C \\ \dot{\hat{i}}_{L_b} \\ \dot{\hat{v}}_o \end{bmatrix} = A \begin{bmatrix} \hat{v}_C \\ \hat{i}_{L_b} \\ \hat{v}_o \end{bmatrix} + B_1\hat{d}_1 + B_2\hat{d}_2 + B_3 v_{in} \tag{20}$$

where the matrices A, B_1, B_2, and B_3 are stated in Equation (19). This equation may be used to obtain the transfer function of the circuit in the terms of different variables such as d_1, d_2, and V_{in} independently.

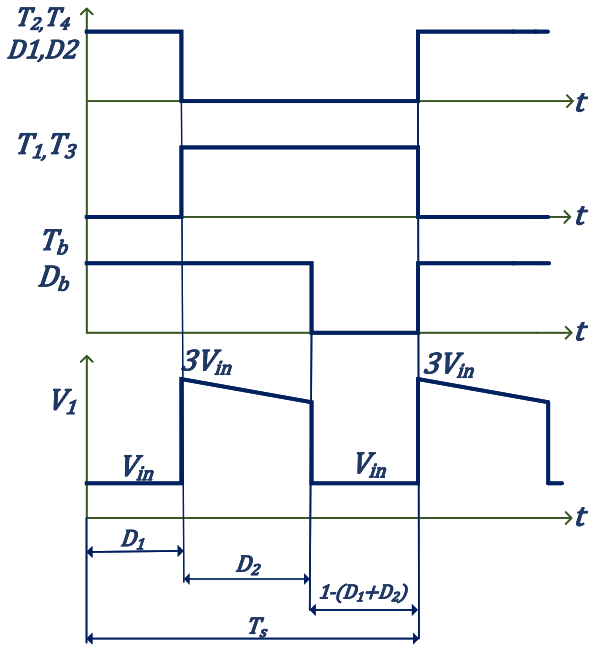


Figure 2. Timing diagram depicting all the modes.

3.5. Gain Calculations by Volt–Sec Balance of Inductor

The differential equation of the inductor current with respect to time is written for all three modes and, finally, the volt–sec balance is applied over a time period.

Mode 1: Consider that mode 1 operates for a period of D_1T_s, where D_1 is the duty cycle of the switches corresponding to the first mode. Kirchhoff's voltage law (KVL) is applied to the loop containing the inductor which results in the following:

$$\frac{di_{L_b}}{dt} = \frac{v_{in}}{L_b} \tag{21}$$

Mode 2: Mode 2 is assumed to occur for a period of D_2T_s, where D_2 is the duty cycle of the switches corresponding to the second mode. Hence, applying the KVL across the inductor results in the following equation:

$$\frac{di_{L_b}}{dt} = \frac{v_{in}}{L_b} + \frac{v_{C_1}}{L_b} + \frac{v_{C_2}}{L_b} \tag{22}$$

Mode 3: The third mode occurs for a time span of $1-(D_1+D_2)T_s$. The KVL equation for the inductor is given by the following:

$$\frac{di_{L_b}}{dt} = \frac{v_{in}}{L_b} + \frac{v_{C_1}}{L_b} + \frac{v_{C_2}}{L_b} - \frac{v_0}{L_b} \tag{23}$$

The volt–sec balance equation across the inductor for the complete time period T_s is given by the following:

$$\int_0^{D_1} \left(\frac{di_{L_b}}{dt}\right)^{I} dt + \int_0^{D_2} \left(\frac{di_{L_b}}{dt}\right)^{II} dt + \int_0^{1-(D_1+D_2)} \left(\frac{di_{L_b}}{dt}\right)^{III} dt = 0 \tag{24}$$

Therefore,

$$D_1 v_{in} + D_2(v_{in} + v_{C_1} + v_{C_2}) + (1 - (D_1 + D_2))(v_{in} + v_{C_1} + v_{C_2} - v_0) = 0 \quad (25)$$

It is presumable in the steady condition that $v_{C_1} = v_{C_2} = v_{in}$. Hence, the voltage gain equation is calculated as follows:

$$\frac{v_0}{v_{in}} = \frac{3 - 2D_1}{1 - (D_1 + D_2)} \quad (26)$$

4. Comparison of the Proposed Converter's Performance

Equation (25) provides the introduced converter's voltage gain. The gain depends on D_1 as well as D_2. The effect of D_1 and D_2 on the gain is observed by varying D_2 for a fixed value of D_1 and the response hence obtained is plotted as depicted in Figure 3. Here, different values of D_1 are selected and, at these values, the effect of varying D_2 is studied on the gain. As the value of D_1 increases, the curve shifts from right to left. A few alternative converters shown in [10,11,24] are compared with the proposed converter's various performance attributes. A gain of 46 is achieved at $D_1 = 0.35$ and $D_2 = 0.6$ while, for $D_1 = 0.6$, $D_2 = 0.25$, and $D_3 = 0.1$, the converter in [24] produces a gain of 31. The converter presented in [10] attains its maximum gain of around 35 while the proposed converter achieves its highest gain of 95. Figure 4 displays the gain's comparison of the various converters and proves that the presented converter achieves the highest gain. Table 1 compares the voltage gain, voltage stress, and several other components of the proposed converter with those of existing converters. On comparing with the other converters, it is found that the suggested converter is capable of achieving much higher gain for the same values of duty ratios. The voltage stress on the diodes and switches is comparable to that of the converter in [10] and lower than that of the traditional boost converter. Also, fewer inductors are needed to generate a comparably larger gain. Furthermore, the theoretical efficiencies of the various converters are also compared and listed in Table 1. The efficiency of the developed converter is calculated in Section 7. The advocated converter's theoretical efficiency is around 96 % and is higher than the converters in [10,11,20].

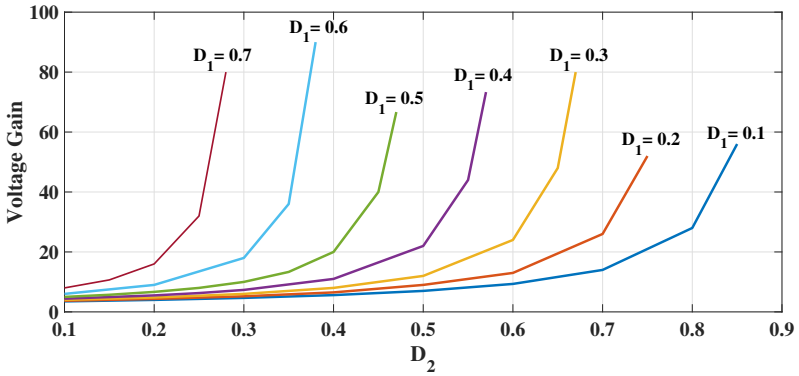


Figure 3. Plot for voltage gain vs D_2 with different D_1.

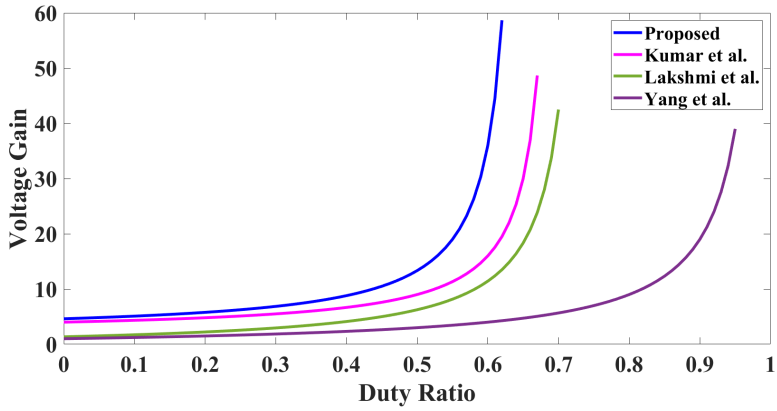


Figure 4. Comparison of gain of proposed topology and topologies in [10,11,24].

Table 1. Comparison of presented and existing converters.

Technical Information	Proposed Converter	Converter in [24]	Converter in [10]	Converter in [11]
Voltage gain	$\frac{v_0}{v_{in}} = \frac{3-2D_1}{1-(D_1+D_2)}$	$\frac{v_0}{v_{in}} = \frac{3-2D_1-D_2}{1-D_1-D_2-D_3}$	$\frac{v_0}{v_{in}} = \frac{1-D_1}{1-(D_1+D_2)}$	$\frac{v_0}{v_{in}} = \frac{1+D}{1-D}$
Quantity of diodes	3	3	2	0
Quantity of switches	5	5	3	3
Quantity of inductors	1	1	2	2
Quantity of capacitors	3	3	1	1
Diode's voltage stress	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$
Voltage stress on switches	$V_{T_1,s} = V_{T_3,s} = v_{in}$ $V_{T_2,s} = V_{T_4,s} = v_{in}$ $V_{T_b,s} = v_0$	$V_{T_1,s} = V_{T_3,s} = v_{in}$ $V_{T_2,s} = V_{T_4,s} = v_{in}$ $V_{T_b,s} = v_0$	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$	$V_{D1,s} = V_{D1,s} = v_{in}$ $V_{D_b,s} = v_{in} + v_0$
Theoretical efficiency	96%	93.4%	92%	92.7%

5. ADRC-Based Control of the Proposed Converter

For practical applications, there is a need for regulated output from the converter. In order to obtain the intended output from the converter, a closed-loop control framework is required. All robustness and stability requirements are met by the active disturbance rejection control approach. The disturbance variable's estimation and its real-time suppression or rejection form the basis of the ADRC approach [29,30]. The fundamental block diagram of the closed-loop ADRC control structure is shown in Figure 5.

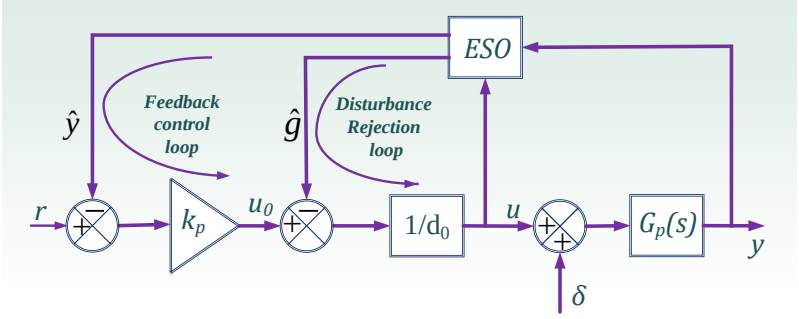


Figure 5. A closed-loop ADRC control block schematic diagram.

In this figure, y is the obtained output, $\hat{y}$ is the output estimate, $\hat{g}$ is the estimate of the disturbance comprising the unmodeled dynamics and external and internal distur-

bances, and r is the reference. The controller's gain is denoted by k_p. Furthermore, $G_p(s)$ corresponds to the transfer function of the developed converter, the external disturbance is denoted by δ, and u is the final control signal. The extended state observer (ESO) differentiates the output and the disturbance signal, and estimates them separately. Further, the disturbance is canceled by the selection of a proper controller.

The modeling of the converter's section B is conducted independently in order to use the control approach on the converter in an appropriate manner. The control signal provided by the controller drives the switch (T_b). The transfer function of section B of the converter is derived and formulated by Equation (27):

$$\frac{v_0}{d} = \frac{-R_L L_b I_{L_b} s + R_L d V_0}{R_L L_b C_b s^2 + L_b s + R_L d^2} \tag{27}$$

5.1. Controller Design

Equation (28) represents the conversion of the transfer function of the converter derived from Equation (27) into the time domain:

$$\ddot{y} = (-c_1 \dot{y} - c_0 y + \delta(t) - d_1 \dot{u} + \Delta d_0 u) + d_0 u \tag{28}$$

where d_0 and d_1 are the numerator's coefficients, indicating the dynamics of the zeroes, and c_0 and c_1 are the denominator's coefficients in the real transfer function, showing the pole dynamics. The system's gain is denoted by d_0, and any inaccuracy in the presumption of d_0 is represented by Δd_0. $\delta(t)$ represents the external disturbances. Equation (28) can be summarized by Equation (29) as follows:

$$\ddot{y} = g(y, \dot{y}, \delta, u, \dot{u}) + d_0 u \tag{29}$$

where

$$g(\cdot) = (-c_1 \dot{y} - c_0 y + \delta(t) - d_1 \dot{u} + \Delta d_0 u) \tag{30}$$

Equation (31) represents the bifurcation of the total disturbance g as follows:

$$g = g_1 + g_2 \tag{31}$$

In Equation (31), the pole dynamics are represented by $g_1 = -c_0 y - c_1 \dot{y}$, whereas all the disturbances and unmodeled dynamics are represented by g_2. Once more, g may be expressed as in Equation (32):

$$g = -c_0 y - c_1 \dot{y} + g_2 \tag{32}$$

The differentiation of g results in Equation (33):

$$\dot{g} = -c_0 \dot{y} - c_1 \ddot{y} + \dot{g}_2 \tag{33}$$

Since $\ddot{y} = g + d_0 u$, $\dot{g}$ can be given by Equation (34):

$$\dot{g} = -c_0 \dot{y} - c_1 (g + d_0 u) + \dot{g}_2 \tag{34}$$

Now, assume $x_1 = y$, $x_2 = \dot{y}$, $x_3 = g(\cdot)$ and $\dot{x}_3 = \dot{g}_2(\cdot) = \beta$. Hence, the derivative of g is given by Equation (35) as follows:

$$\dot{g} = -c_0 x_2 - c_1 x_3 - c_1 d_0 u + \beta \tag{35}$$

With the aforementioned presumptions, the state-space Equation (36) is constructed as follows:

$$\begin{aligned} \dot{x} &= A_H x + B_H u + H_H \beta \\ y &= C_H x \end{aligned} \tag{36}$$

where $A_H = \begin{bmatrix} 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & -c_0 & c_1 \end{bmatrix}$, $B_H = \begin{bmatrix} 0 \\ d_0 \\ -c_1 d_0 \end{bmatrix}$, $C_H = \begin{bmatrix} 1 & 0 & 0 \end{bmatrix}$, and $H_H = \begin{bmatrix} 0 \\ 0 \\ 1 \end{bmatrix}$ are the state matrices of the proposed high-gain converter.

The observer is intended for the system described above, as seen in Equation (37):

$$\begin{aligned} \dot{z_H} &= A_H z_H + B_H u + M_H(y - \hat{y}) \\ \hat{y} &= C_H z \end{aligned} \tag{37}$$

Here, the observer's state variable is denoted by $z_H = \begin{bmatrix} z_1 & z_2 & z_3 \end{bmatrix}^T$, $M_H = \begin{bmatrix} \alpha_{1H} & \alpha_{2H} & \alpha_{3H} \end{bmatrix}^T$ is the observer's gain, and 'T' stands for the matrix's transposition.

The third-order observer's characteristic equation may be constructed with poles assigned to $-\omega_o$. This would lead to Equation (38) as follows:

$$|sI - (A_H - M_H C_H)| = (s + \omega_o)^3 = 0 \tag{38}$$

Comparing the terms in Equation (38) results in Equations (39)–(41):

$$\alpha_{1H} = 3\omega_o - c_1 \tag{39}$$

$$\alpha_{2H} = 3\omega_o^2 - (c_0 - c_1\alpha_{1H}) \tag{40}$$

$$\alpha_{3H} = \omega_o^3 - (c_0\alpha_{1H} + c_1\alpha_{2H}) \tag{41}$$

A proportional derivative type controller is selected to reject the disturbance term in real time as given by Equation (42) as follows:

$$u = \frac{K_{pH}(R_H - z_H)}{d_0} \tag{42}$$

where $R_H = \begin{bmatrix} r & 0 & 0 \end{bmatrix}^T$ and $K_{pH} = \begin{bmatrix} k_{1H} & k_{2H} & 1 \end{bmatrix}$.

The characteristic equation of a controller may be constructed with poles assigned to $-\omega_c$. This would lead to Equation (43) as follows:

$$\left|sI - (A_H - B_H K_{pH})\right| = (s + \omega_c)^3 = 0 \tag{43}$$

The above equation results in $k_{1H} = \omega_c^2$ and $k_{2H} = 2\omega_c$. Equation (44) provides the controller's transfer function as follows:

$$G_c(s) = \frac{\omega_c^2}{(s + \omega_c)^2} \tag{44}$$

5.2. Frequency Domain Analysis and Parameter Tuning

Stability analysis can be performed for the closed-loop system by using Equations (36), (37), and (42) as given by Equation (45):

$$\begin{bmatrix} \dot{x} \\ \dot{z}_H \end{bmatrix} = \begin{bmatrix} A_H & -\tilde{B}_H k_{pH} \\ M_H C & A - M_H C - \tilde{B}_H k_{pH} \end{bmatrix} \begin{bmatrix} x \\ z_H \end{bmatrix} + \begin{bmatrix} \tilde{B}_H & H_H \\ \tilde{B}_H & 0 \end{bmatrix} \begin{bmatrix} \tilde{r} \\ \beta \end{bmatrix} \tag{45}$$

where $\tilde{B}_H = B_H/d_0$ and $\tilde{r} = k_{pH}r$. Now, using an equivalence transformation $\begin{bmatrix} \tilde{x} & \tilde{z}_H \end{bmatrix}^T = Q\begin{bmatrix} x & z_H \end{bmatrix}^T$, where $Q = Q^{-1}$, the state estimation Equation (45) is now given by Equation (46):

$$\begin{bmatrix} \dot{\tilde{x}} \\ \dot{\tilde{z}}_H \end{bmatrix} = \begin{bmatrix} A_H - \tilde{B}_H k_{p_H} & -\tilde{B}_H k_{p_H} \\ 0 & A_H - M_H C_H \end{bmatrix} \begin{bmatrix} \tilde{x} \\ z_H \end{bmatrix} + \begin{bmatrix} \tilde{B}_H & H_H \\ 0 & H_H \end{bmatrix} \begin{bmatrix} \tilde{r} \\ \beta \end{bmatrix} \quad (46)$$

To fulfill the criteria of BIBO stability, the eigen values of Equation (46) must be in the left half plane. Here, the scaled reference $\tilde{r}$ and β are always bounded and the condition of stability is only dependent on $\beta = \dot{g}_2$, which means that g_2 should be differentiable [31].

The selection of tuning parameters is a crucial part of the closed-loop performance of the system. The author of [31,32] gave specific guidelines for the selection of the controller's and observer's bandwidths. Based on this, the controller's and observer's bandwidths were selected as $\omega_c = 900$ rad/s and $\omega_o = 3600$ rad/s. Accordingly, the values of the controller's and observer's gains were calculated.

The closed-loop system's stability can be proved by drawing the Bode plot as shown in Figure 6. This figure clearly demonstrates that the closed-loop system is stable with gain and phase margins at 20.1 dB and 71.9 degrees respectively.

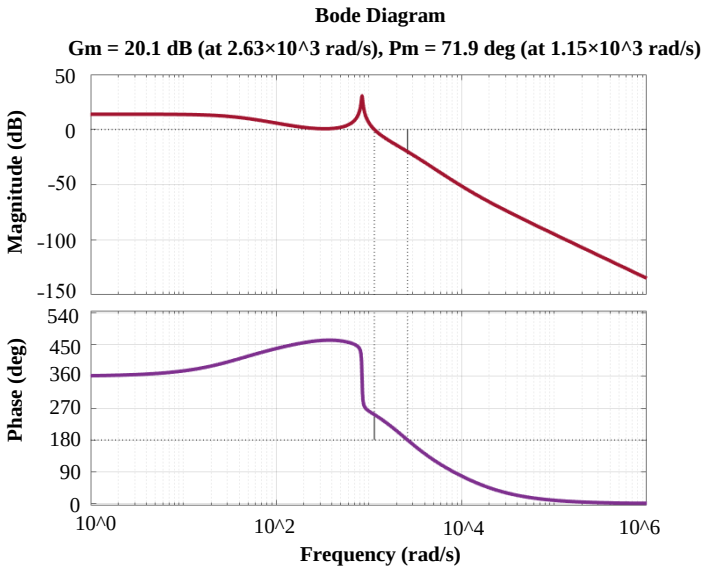


Figure 6. Bode plot of the closed-loop system.

6. Simulation and Experimental Results

To analyze the servo and regulatory performances, simulations and experimental verifications are carried out. Additional research is conducted on the regulatory performance in relation to the input voltage and load resistance fluctuations.

6.1. Simulation Results

The simulation was carried out by utilizing the Simscape power system toolkit and the MATLAB/Simulink 2021a platform. Table 2 displays the circuit's specs.

The discrete mode of operation was used for the control system design. The simulation study is performed under various scenarios consisting of input voltage and load fluctuations.

Figure 7 shows the diagram for the output voltage, input voltage, load current, and duty cycle following a momentary variation in the reference voltage. In this case, the input voltage is set to 5 V and a 100 Ω fixed resistor is used. The variation in reference voltage is performed in various steps as 12 V-15 V-20 V and then back to 20 V-15 V-12 V. The response from Figure 7 shows that the output voltage adjusts to match the reference voltage as it fluctuates due to the adjustment of the duty ratio provided by the controller with a settling time of 0.02 s. The output current also settles to a new value with the settlement of the

output voltage. Here, it can be noticed that the output of 20 V is obtained at a duty ratio of 0.4 proving the converter exhibits high gain.

Table 2. Specifications for the developed converter's circuit.

Components	Specifications
Switching frequency	100 kHz
V_{in}	5 V
V_0	20 V
L_b	130 mH
C_b	1000 µF
C_1, C_2	100 µF
R_L	100 Ω

The responses obtained using simulation for varying input are presented in Figure 8. In this case, the reference voltage is set to 20 V and a 100 Ω load resistor is used. Two steps are taken to vary the input voltage. Initially, it is settled at 5 V, then it is changed to 8 V and back to 5 V at certain instants of time as shown in Figure 8. The output response displayed by Figure 8 may be used to assess how the controller can swiftly and effectively regulate the output while suppressing disturbances such as sudden fluctuations in input voltage. ADRC uses the ESO to identify the variations in the states of the converter due to the fluctuations in input voltage. After that, it uses error feedback to dynamically modify the duty cycle in order to keep the output voltage steady. Even when input voltage fluctuates unpredictably, this method guarantees strong, adaptive control.

Furthermore, the load resistance is varied while the setpoint and the input voltages remain fixed at 20 V and 5 V, respectively. A 50 Ω load resistor is utilized initially but, after a short while, it is abruptly changed to 100 Ω and then back to 50 Ω. Figure 9 displays the responses under this load variation. Since the load current is lower, the response of the current is multiplied by 20 and plotted thereafter for improved visibility, which explains the variation in the load. The output voltage settles to the reference voltage right away and has a very small ripple magnitude. The resulting response demonstrates decisively the controlled system's capacity to reject disturbances under various load conditions. The variables like output voltage and inductor current are continually monitored by the ESO. These parameters are changed by an abrupt change in load, and the ESO records this as a disturbance in its state estimations. After that, the state error feedback produces a duty cycle according to the disturbance estimates and error. Hence, it provides a robustness against the varying loads.

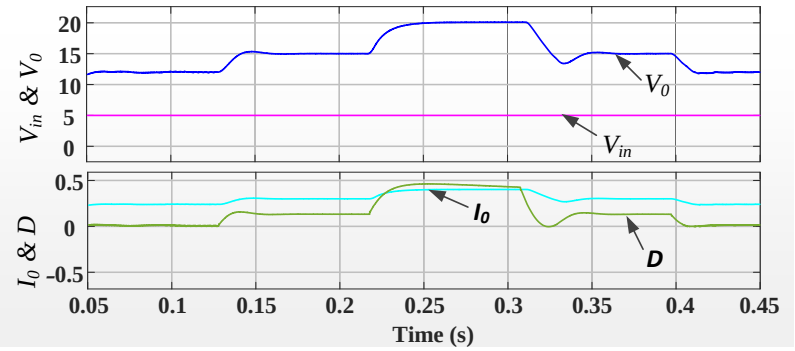


Figure 7. Output voltage response for varying reference.

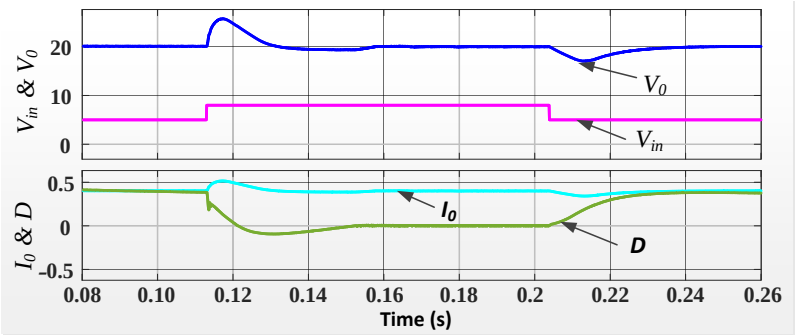


Figure 8. Response of the output voltage to varying input.

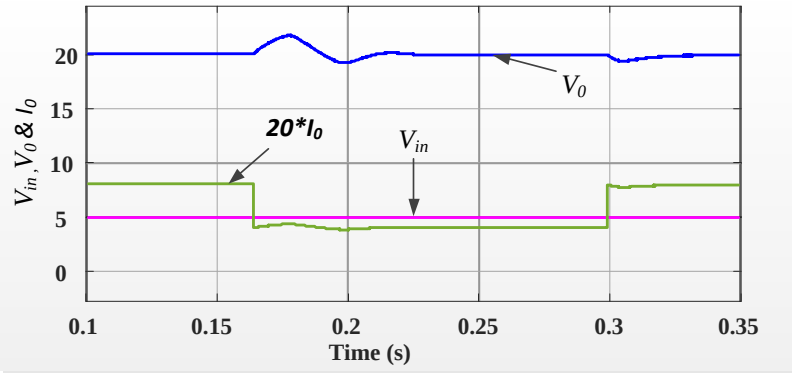


Figure 9. Response of the output voltage to varying load.

6.2. Hardware Results

The complete experimental setup is depicted in Figure 10. A 200 watt prototype is developed for the proposed circuit. In the experimental setup, MOSFET-IXFH80N65X2 designed by IXYS company from Milpitas, CA, USA and Diode-SL80F040 manufactured by SL Power Electronics, a company based in the Calabasas, CA, USA were used. A gate driver circuit is used to feed the control signal to the MOSFET's gate terminal.

The gate driver circuit enhances the PWM pulse generated by microcontroller TMS320F 28379D designed by Texas Instruments (TI), a company based in the Dallas, TX, USA is programmed by the MATLAB code composer studio. The gate pulse fed to various MOSFETs is shown in Figure 11. Here, the numbers '0' to '4' beside the pulses represents the switching pulses for the switches T_1, T_2, T_3, T_4 and T_b respectively as labelled in the Figure 11. An LV-55P voltage sensor developed and manufactured by LEM (Liaisons Electroniques et Mécaniques), a company based in Pfäffikon, Switzerland is used to sense the output voltage and feed it to the microcontroller that ultimately supplies the controller feedback structure. An APCSMP09 source designed by APC Instruments, a company based in India is used for supplying ±15 V to the sensor. A programmable DC source is used as the input voltage to the circuit. The waveforms are recorded on a multiport DSO with the help of current and voltage probes. To verify the servo performance of the system, the reference is varied similarly to that in the simulation and the response obtained is depicted in Figure 12. From the figure, it is determined that the system has a good reference tracking ability and the experimental and simulation results match satisfactorily.

Disturbance rejection abilities can be inferred from Figures 13 and 14. This shows that the effect of disturbance owing to load and input voltage variations on the output voltage is suppressed immediately by the controller. The load variations are performed by varying the resistance from 100 Ω to 50 Ω to 100 Ω, keeping the reference and input voltages at 20 V and 5 V, respectively. The output voltage remains constant in spite of variations in the load. However, the load affects the load current. Similarly, no effect is seen on the output voltage when the input voltage is varied from 5 V to 8 V to 5 V, keeping the reference at 20 V and load at 100 Ω.

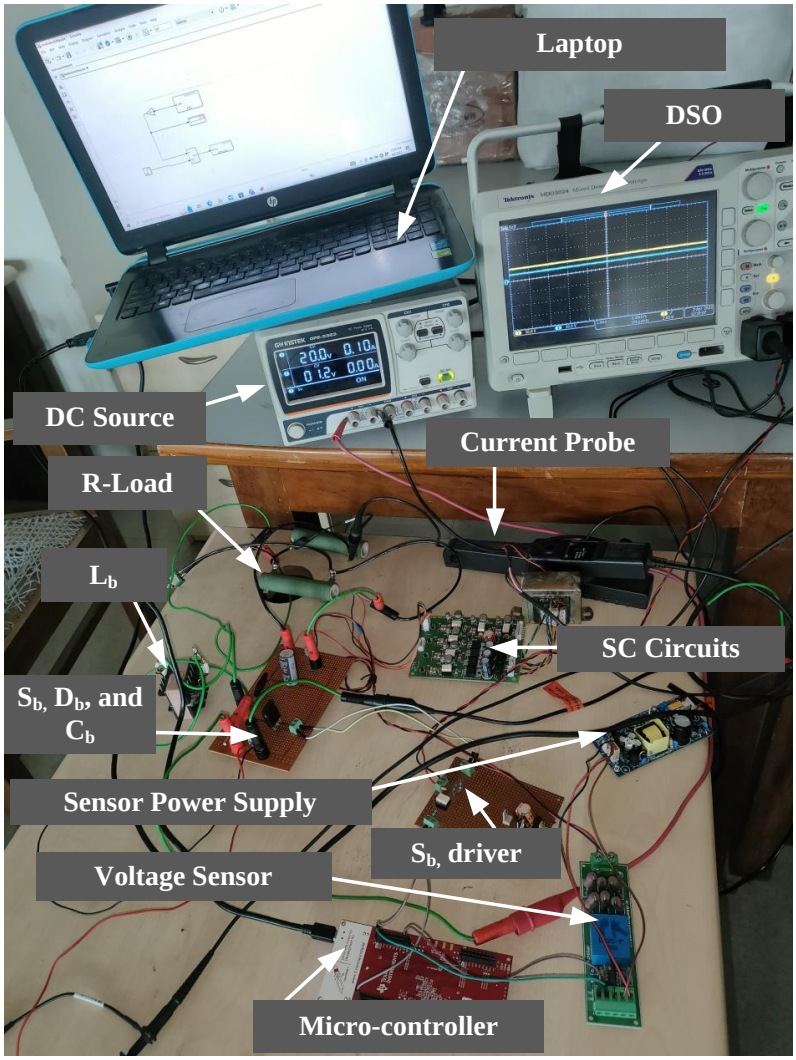


Figure 10. Experimental prototype.

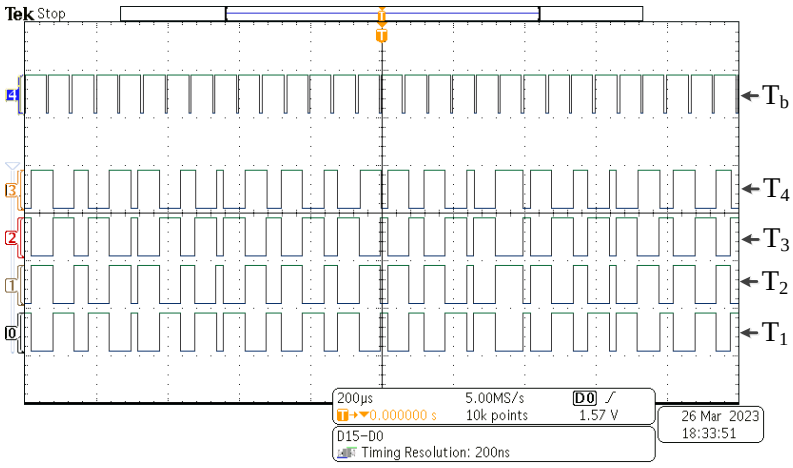


Figure 11. Gate pulses for different switches.

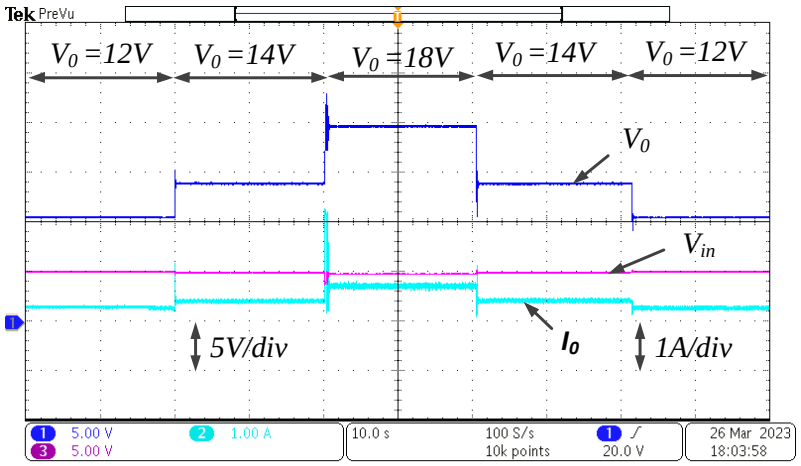


Figure 12. Responses obtained for variation in reference.

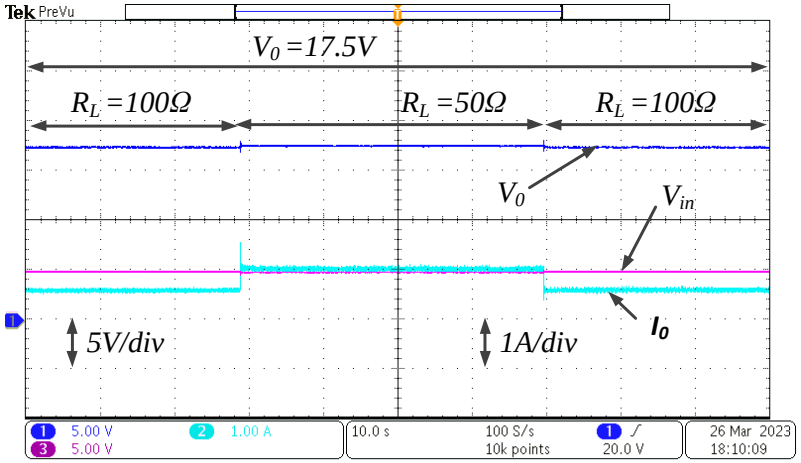


Figure 13. Responses obtained for variation in load.

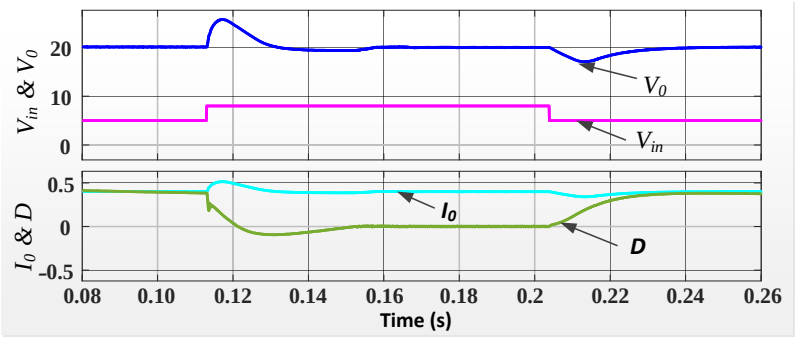


Figure 14. Responses obtained for variation in input.

7. Loss Analysis for the Proposed Converter

Using the model that the author developed in [33], the detailed loss calculations are performed by taking into account the losses occurring in the switches (switching (P_{sw}) + conduction losses (P_{con})) and diodes (conduction losses (P_{con})). These losses are computed for ON-state voltage drops and energy factors with the help of quadratic curves. A curve-fitting tool is used for obtaining these curves with the help of datasheets of the switches

and diodes. In this work, the datasheet of MOSFET IXFH80N65X2 is used for the respective calculations. The corresponding Equations (47)–(51) are given as follows:

$$V_{DS} = -20 \times 10^{-8} I_{SW}^2 + 0.001 I_{SW} + 0.966 \quad (47)$$

$$V_D = -10 \times 10^{-8} I_D^2 + 0.0024 I_D + 0.779 \quad (48)$$

$$K_{SW-on} = 80 \times 10^{-8} I_{SW}^2 - 0.0024 I_{SW} + 4.01 \quad (49)$$

$$K_{SW-off} = 30 \times 10^{-8} I_{SW}^2 - 0.0011 I_{SW} + 3.15 \quad (50)$$

$$K_{Diode-rev} = -70 \times 10^{-8} I_D^2 + 0.004 I_D + 6.654 \quad (51)$$

Here, V_{DS} and V_D are the ON-state voltage drops of the MOSFET and diode, respectively. I_{SW} is the current through the switch and I_D is the current through the diode. K_{SW-on} and K_{SW-off} are the energy factors of the MOSFET in the ON and OFF states, respectively. The OFF-state energy factor for the diode is denoted by $K_{Diode-off}$. Equations (47)–(51) are used to calculate the losses according to the procedure explained in [33–35]. From Equation (52), the efficiency for the developed converter may be obtained as follows:

$$\eta_{SCBC} = \frac{P_{out-SCBC}}{P_{in-SCBC}} = \frac{P_{out-SCBC}}{P_{out-SCBC} + losses} \quad (52)$$

where $P_{out-SCBC}$ and $P_{in-SCBC}$ are the output and input powers of the converter, respectively. The calculated losses and efficiencies are summarized in Table 3. The table summarizes the losses of each switch and diode calculated during four different rated power outputs and the efficiencies are calculated accordingly. From the table, it can be seen that maximum efficiency is obtained at 96.6% when the rated power is 111 watts. The experimental efficiencies are also calculated for the proposed circuit and it is found to be lower than the theoretical efficiency. The full load experimental efficiency for the proposed circuit is calculated to be 94.07%. The efficiency value decreases both above and below the full load.

Table 3. An evaluation of the proposed converter's efficiency.

Diodes and Switches	**Rated Output Power (P_{out})**			
	111 W	**142.9 W**	**200 W**	**333 W**
	$P_{sw} + P_{con}$	$P_{sw} + P_{con}$	$P_{sw} + P_{con}$	$P_{sw} + P_{con}$
T_1	0.120	0.164	0.255	0.524
T_2	0.474	0.671	1.009	2.098
T_3	0.120	0.164	0.255	0.524
T_4	0.474	0.671	1.009	2.098
T_b	0.445	0.605	0.935	1.908
d_b	0.179	0.242	0.369	0.744
$d1$	1.049	1.453	2.204	4.518
$d2$	1.049	1.453	2.204	4.518
Total Loss	3.913	5.472	8.242	16.93
Efficiency (η)	96.6%	96.34%	96.04%	95.17%

8. Conclusions

The presented converter makes use of a switched-capacitor network to meet the requirement of a significantly high-voltage gain for renewable energy applications. The switches are operated with two individual duty ratios, providing a very-high-voltage gain. The availability of two duty ratios makes it easier for the user to attain large gains without utilizing a single duty ratio at higher values. The variations in the voltage gain with respect to duty cycles are demonstrated graphically. In the proposed converter, the

voltage stress on the switches is lower as compared to those obtained in [22,23]. Both switching and conduction losses are taken into account for calculating the converter's efficiency. The efficiency of the designed converter for various loads is found to be above 95%. The closed-loop control strategy utilizing the ADRC controller is implemented on the proposed converter by selecting the controller's and observer's bandwidths as 900 rad/s and 3600 rad/s, respectively. Both simulation and experimental outcomes validate that the newly developed converter along with the ADRC control attains an elevated voltage gain, effective load regulation, and rapid transient response that make the converter suitable for microgrid applications. Other advanced control techniques such as sliding mode control, adaptive control, model predictive control, etc. may be implemented on the newly constructed converter.

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