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Modeling and Analyzing of CMOS Cross-Coupled Differential-Drive Rectifier for Ultra-Low-Power Ambient RF Energy Harvesting

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Abstract: This paper models and analyzes the Complementary Metal Oxide Semiconductor (CMOS) cross-coupled differential-drive (CCDD) rectifier for Ultra-Low-Power ambient radio-frequency energy harvesters (RFEHs) working in the subthreshold region. In this paper, two closed-form equations of CCDD rectifier output voltage and input resistance in the subthreshold region were derived based on BSIM4 models of NMOS and PMOS. The model give insight to specify circuit parameters according to different inputs, transistor sizes, threshold voltages, numbers of stages, load conditions and compensation voltages, which can be used to optimize the rectifier circuit. There is a good agreement between the simulation results and these models, and these models have a maximum deviation of 10% in comparison with the simulation results in the subthreshold region. The measurement results of a single-stage CCDD rectifier reported in a previous paper were adopted to verify the model. The output voltage and input resistance predicted by these models provide excellent consistency with corresponding measurement results. The model can be employed to optimize the CCDD rectifier without expensive calculation in the design stage.

Keywords: RF energy harvesting; cross-coupled differential-drive rectifier; optimization; power conversion efficiency; subthreshold region

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1. Introduction

Due to the elimination of batteries and lifetime limitations, radio-frequency energy harvesting (RFEH) is becoming a viable solution to substitute batteries and scale down sensors' cost and size [1,2]. The major weaknesses of RFEH in CMOS implementation are the restricted amount of energy that can be scavenged from ambient RF sources [3–6] and the low power conversion efficiency (PCE) of rectifiers at low input power levels [7–9]. The available RF energy in free space is confined due to the limited maximum allowed transmitted signal strength, the rapid attenuation of signals over distances, and the limited size of receiver antennas [4]. A previous study performed outdoor dynamic measurements in core areas of Montreal, Canada, to study the ambient RF power density. This study concluded that the power available to the RF energy harvester in each frequency band is small and the GSM/LTE 850M cellular communication band has the highest average power level in Downtown Montreal, which is −35.50 dBm. This low voltage value at the input of the RF energy harvesters, even boosted by the impedance-matching networks, is not high enough to produce large overdrive voltage for CMOS transistors. These transistors all operate in the subthreshold region, resulting in high conduction losses; therefore, the efficiency of CMOS rectifiers is low at low input power levels [7].

The dominating rectifier topologies commonly employed are Dickson and CCDD, and they can be realized by discrete components or CMOS transistors. For RFEH, the main advantageous component is the Schottky diode due to its low forward voltage drop, low power losses, and high switching speed [8]. However, it has a bulky size and cannot be

integrated into a CMOS chip. The CMOS CCDD rectifier is a more popular choice for RFEH compared to Dickson because it provides dynamic threshold compensation to reduce dead zones, which severely decrease the PCE when input voltage amplitudes are low [10–13]. To increase the efficiency of these rectifiers, some gate biasing techniques were utilized to compensate Vth and reduce the ON resistance of transistors by changing the gate-source or gate-drain voltage of transistors in CMOS rectifiers [14–18]. Some other papers studied the body biasing of PMOS transistors integrated into a CCDD rectifier, which allows PMOS transistors to have a scalable Vth [19–21]. Using zero-threshold or low-threshold transistors is another method to reduce dead zones. Regrettably, these transistors are very sensitive to process variations and their leakage current is high, making them unfit for integration with digital blocks [22,23]. Due to the nonlinear behavior of the rectifier, optimization of this circuit and making a good tradeoff among all parameters for RFEH are challenging. An iterative numerical method can be used to optimize it, but computationally expensive simulation is needed [16,24]. On the other hand, we can optimize this circuit by using an exact analytical model for this rectifier to make optimum choices of parameters to achieve the required gain [25,26]. However, the comprehension of CCDD topology is still deficient, and no exact and practical analytical mathematical model or optimization guidelines are available in previous papers.

The first compact mathematical model of CCDD rectifiers in the subthreshold region was proposed in [27]. However, this model was based on several assumptions, such as the characteristics of this circuit being ideally symmetrical, which is not realistic, especially with low input RF voltage swing, and the sizes of transistors were set to given values. These assumptions also caused the ranges of variables (W/L and threshold voltages) to be constrained, which affected the optimization of these rectifiers. In addition, there were some flaws in the model. Firstly, they allege that $V_{sd} = V_a \cos wt - V_{DC}$, but the common-mode voltage V_{CM} generated by a rectification operation acts as a static gate biasing voltage, compensating Vth to increase the drain current of PMOS and NMOS in CCDD rectifiers [28]. The effect of V_{CM}, which plays an important role in improving sensitivity in low input RF voltage swing, is not taken into account in the analytical derivation process in [27]. Secondly, they suppose that the rectifier's resistance $R_{in} = R_S = 50\ \Omega$, but this assumption is in contradiction to [29]. Post-layout simulations in [29] show that the rectifier input resistance R_{in} increases greatly at low V_{in} as transistors enter the subthreshold region. Refs. [16,24] also support the results of [29]. Thirdly, they conceive that the (I_{S0}/W) of the device in the adopted process is 4.7686 μA/μm and the width is 50 μm. Thus, I_{S0} is 238.43 μA, which is much larger than the same parameter in [16] and is in contradiction to the application scenario. Another analytical model was presented in [16]. It models the behavior of a CCDD rectifier connected to two square-wave signals in opposite phases and employs an analogy method to rewrite the equation of output DC voltage, which can be made between sinusoidal signals and square-wave signals according to [30]. The analogy method presented in [30] was based on a half-wave rectifier using Shockley diodes, and the feasibility of the analogy in [16] was not verified by experiments. Furthermore, the proposed model also assumed the characteristics of the circuit were ideally symmetrical. The other analytical model is proposed in [31]. However, the authors assumed that NMOS and PMOS had the same absolute threshold voltage. Obviously, this assumption does not hold in reality. Moreover, the V_{DC} is given in integral form, which is more complex and the model should be further simplified. There are also some other analytical models [32] based on the Dickson charge pump; nevertheless, the model of the Dickson charge pump cannot be directly applied to a CCDD rectifier.

In addition, compensation voltages used in CCDD rectifiers were not modeled and analyzed in previous papers. The sensitivity of rectifiers was strongly dominated by Vth, and several Vth compensation techniques have been proposed by changing the gate-source voltage to increase the efficiency of CCDD rectifiers at low input power levels. Although the effect of the compensation voltage in Dickson rectifiers was taken into account in [33], the model of Dickson rectifiers cannot be applied to the CCDD rectifier directly. The

effect of the compensation voltage in CCDD rectifiers was mentioned in [16], but the static compensation voltage was confused with the dynamic compensation voltage and no more detailed analysis was conducted. Beyond that, what would be an optimum compensation voltage for specified transistors to provide the highest efficiency at low input power levels is unclear. Also, IoT sensors work in duty-cycled mode [16,33] in practice, which means the harvester circuit has a large capacitor to store the RF energy, and once the voltage of the capacitor reaches a pre-specified threshold value, the harvester circuit starts to operate and discharges the capacitor in a short time. Consequently, the load connected to the output of the rectifier is only a voltage sensor during the energy charging and accumulating time, and its current consumption is in the order of several 100 nA. Therefore, to analyze and design a harvester circuit for ambient RFEH, a model that characterizes the CCDD rectifier's operation behavior with a heavy load at very low input powers should be built, which is not mentioned in previous works. Furthermore, previous papers modeled the drain current of transistors using the weak inversion expressions of long-channel devices. Therefore, the small-geometry effects, such as short-channel effects and quantum effects, were not included in them. The mainstream CMOS processes for RFEH sensors are in deep submicron sizes (0.13 µm, 90 nm, and 65 nm), and all deep submicron MOSFETs suffer the conventional short-channel effects [34].

In this paper, an analysis model of a CCDD CMOS rectifier with dynamic and static compensation voltages is proposed to accurately predict the output voltage and input resistance. The model made substantial improvements compared to previous studies, which can be summarized as follows:

- The model is based on few assumptions. The previous papers were based on several assumptions, such as NMOS and PMOS having the same absolute threshold voltage, which is not realistic. The model is based on the charge conservation principle and the BSIM4 current model flowing through the PMOS and NMOS transistors of the CMOS CCDD rectifier at a steady state. There are no presumptions in the mathematical derivation of the model except that transistors were working in the subthreshold region. Therefore, the adaptability of this model is enhanced.
- Some overlooked phenomena of NMOS and PMOS working in the subthreshold region were discovered and some new insights were put forward from them. For instance, the rectifier input resistance R_{in} working in the subthreshold region is much larger than that working in the strong inversion region. As another example, the load connected to the output of the rectifier is often heavy during the energy charging and accumulating time in duty-cycled mode. Therefore, the accuracy of this model is improved.
- The detailed effect of the compensation voltage on the output voltage and the input resistance of the CCDD rectifier was precisely modeled. We define the dynamic compensation voltage as the bias voltage generated by the cross-coupled differential circuit to automatically minimize the turn-on voltage in forward-bias conditions and increase the turn-on voltage in reverse-bias conditions. V_{CM} in this paper is dynamic compensation voltage. Other bias voltages relying on voltages at nodes of the rectifying chain or external circuits and distributed to other gate terminals were classified as static compensation voltages. The static compensation voltage and the dynamic compensation voltage were first differentiated and described in this paper. Consequently, the most popular circuits to compensate for the Vth of the CCDD rectifier proposed in recent papers can be modeled and evaluated.

The rest of the paper is organized as follows: Section 2 presents our scheme of the CCDD rectifier with four external compensation voltages. The detailed mathematical derivation of output voltage is proposed in Section 3 and the derivation of input resistance is proposed in Section 4. Sections 5 and 6 present the simulation results and measurement results of some rectifiers alongside the derived outputs from the model. Section 7 presents a brief discussion of the model and finally, Section 8 provides the main conclusions of this work.

2. CCDD Rectifier with Compensation Voltages

Figure 1 shows the CMOS CCDD rectifier, which consists of two *n*-channel primary MOSFETs and two *p*-channel primary MOSFETs. In this schematic, an RF signal or power flows across the transistors differentially to decrease the dead-zone area, and these gates of transistors are dynamically biased by a differential mode signal. When the voltage at V_{RF+} is positive, the voltage at V_{RF-} is negative. Then, the gate of M_{P1} connects to a negative voltage, and its source connects to a positive voltage, so M_{P1} is ON in this case. Concurrently, the gate of M_{N2} connects to a positive voltage, and its source connects to a negative voltage, so M_{N2} is ON too. In this case, a loop appears in the circuit, and the input power is rectified and charges the output capacitor. Equally, when the circuit operates in the negative cycle, M_{N1} and M_{P2} are ON and these two transistors form another loop to charge the output capacitor. The DC components of gate voltages, V_X and V_Y, are both probably half of the output DC voltage V_{DC} under the steady-state condition, which acts as a kind of static gate bias voltage or compensation threshold voltage [5].

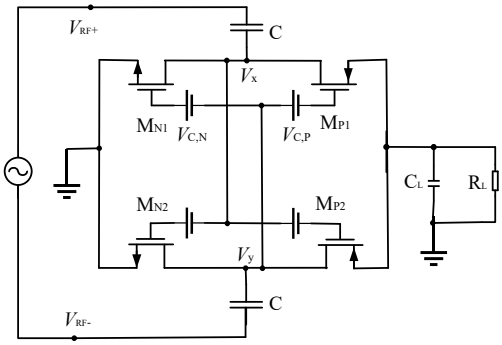


Figure 1. Schematic of the CCDD rectifier with compensation voltages.

In order to further reduce the forward voltage dropping across the transistor, a static DC bias offset V_C at the gate of the transistor can be performed to compensate Vth, such as in [14–16]. In addition, such compensation technology can be ideally implemented by supplying a static bias offset V_C between the gate and drain terminals of transistors. So, four battery symbols are added to the gate terminal of these primary four transistors to compensate Vth. By adding these static voltages ($V_{C,N(P)}$) to the bias of these four primary transistors, the effective turn-on voltage decreased, reducing the forward dropping voltage across the corresponding transistor, at the expense of increasing the reverse current and creating more chip areas.

3. Output Voltage Model of CMOS CCDD Rectifier with Compensation Voltages

The transistors in the CCDD CMOS rectifier at low input power levels all operate in weak inversion, and current mainstream CMOS processes are deep submicron for RFEH. Therefore, the BSIM4 MOSFET model is adopted in our model [35]. The drain current equation in the subthreshold region for NMOS and PMOS is expressed as (1) and (2):

$$I_{Dsub,N} = u_N \frac{W_N}{L_N} \sqrt{\frac{q\varepsilon_{si} NDEN}{2\Phi_s}} V_T^2 e^{\frac{-V_{th,N}-V_{off,N}}{nV_T}} e^{\frac{v_{GS}}{nV_T}} \left[1 - e^{-\frac{v_{DS}}{V_T}}\right] \quad (1)$$

$$I_{Dsub,P} = u_P \frac{W_P}{L_P} \sqrt{\frac{q\varepsilon_{si} NDEP}{2\Phi_s}} V_T^2 e^{\frac{V_{th,P}-V_{off,P}}{nV_T}} e^{\frac{v_{SG}}{nV_T}} \left[1 - e^{-\frac{v_{SD}}{V_T}}\right] \quad (2)$$

$\mu_{N(P)}$ is the mobility of the charge carrier of N(P)MOS. $W_{N(P)}$ and $L_{N(P)}$ are the N(P)MOS' width and length of the channel, respectively. q represents the elementary charge, and $\varepsilon_{si} = 11.7\varepsilon_0$ is the dielectric constant of silicon. NDEN(P) represents the channel doping concentration at the depletion edge for zero body bias of N(P)MOS, and Φ_s is the surface potential coefficient. Vth$_{,N(P)}$ is the threshold voltage of N(P)MOS. V_T is the thermal

voltage defined by kT/q, and n is the slope factor, which is commonly approximated as 1. V_{off} is the offset voltage, which determines the channel current at $\upsilon_{GS} = 0$. Obviously, the bias voltage applied to the gate of the transistor (υ_G) was the sum of its DC (V_G) and AC (υ_g) components.

We defined the following:

$$I_{S,N} = u_N \sqrt{\frac{q\varepsilon_{si} NDEN}{2\Phi_s}} V_T^2 e^{\frac{-V_{th,N} - V_{off,N}}{nV_T}} \tag{3}$$

$$I_{S,P} = u_P \sqrt{\frac{q\varepsilon_{si} NDEP}{2\Phi_s}} V_T^2 e^{\frac{V_{th,P} - V_{off,P}}{nV_T}} \tag{4}$$

Therefore, $I_{\mathrm{Dsub,N(P)}}$ can be given by

$$I_{Dsub,N} = I_{S,N} \frac{W_N}{L_N} e^{\frac{v_{GS}}{nV_T}} \left[1 - e^{-\frac{v_{DS}}{V_T}}\right] \tag{5}$$

$$I_{Dsub,P} = I_{S,P} \frac{W_P}{L_P} e^{\frac{v_{SG}}{nV_T}} \left[1 - e^{-\frac{v_{SD}}{V_T}}\right] \tag{6}$$

When the circuit in Figure 1 is in steady state, these equations hold according to [28]:

$$Q_{\mathrm{F_MN1}} - Q_{\mathrm{R_MN1}} = Q_{\mathrm{F_MP1}} - Q_{\mathrm{R_MP1}} = Q_1 \tag{7}$$

$$Q_{\mathrm{F_MN2}} - Q_{\mathrm{R_MN2}} = Q_{\mathrm{F_MP2}} - Q_{\mathrm{R_MP2}} = Q_2 \tag{8}$$

$$Q_1 + Q_2 = I_{Load} T \tag{9}$$

where $Q_{\mathrm{F_MN1}}$, $Q_{\mathrm{F_MN2}}$, $Q_{\mathrm{F_MP1}}$, and $Q_{\mathrm{F_MP2}}$ are the number of charges transferred in the forward direction through $\mathrm{M_{N1}}$, $\mathrm{M_{N2}}$, $\mathrm{M_{P1}}$, and $\mathrm{M_{P2}}$ during one unit period T, respectively. Here, $Q_{\mathrm{R_MN1}}$, $Q_{\mathrm{R_MN2}}$, $Q_{\mathrm{R_MP1}}$, and $Q_{\mathrm{R_MP2}}$ are the number of charges transferred in the reverse direction through $\mathrm{M_{N1}}$, $\mathrm{M_{N2}}$, $\mathrm{M_{P1}}$, and $\mathrm{M_{P2}}$ during the same period T, respectively. Q_1 and Q_2 are the number of charges transferred in the forward direction through the top path composed of $\mathrm{M_{N1}}$ and $\mathrm{M_{P1}}$ and the bottom path composed of $\mathrm{M_{N2}}$ and $\mathrm{M_{P2}}$, respectively. Equation (9) expresses that the total number of charges transferred in the forward direction is equal to charges flowing to the output load. The DC voltages of V_{X}, V_{Y} and V_{DC} converge to hold these equations.

We assume the top path and bottom path are ideally matched, and that V_{X} and V_{Y} are equal and are the same as the common-mode voltage V_{CM}. Meanwhile, Q_1 equals Q_2, and they are defined as Q.

$$Q_1 = Q_2 = Q = \frac{I_{Load} T}{2} \tag{10}$$

It is proposed in [28] that if the characteristics of NMOS and PMOS are ideally symmetrical, the DC voltages of V_{X} and V_{Y} become just half of V_{DC} in the steady state. But in fact, this statement does not always hold in the subthreshold region, which is beyond the scope of [28]. The DC voltages of V_{CM} and V_{DC} are shown in Figure 2. The measurement was carried out with P_{in} at −25 dBm; there is an evident difference between V_{DC} and $2V_{\mathrm{CM}}$.

To model the circuit behavior, we analyze the voltage waveforms of the rectifier circuit, which is shown in Figure 3. The input voltage is connected to a sinusoidal waveform, expressed as $V_{\mathrm{in}} = V_{\mathrm{a}} cos(wt)$, where V_{a} is the amplitude of the sinusoidal input voltage. V_{DC} is the output voltage across the capacitor C_{L} and the load R_{L}. Generally speaking, V_{DC} is smaller than V_{a}. The current waveform of the rectifier is show in Figure 4.

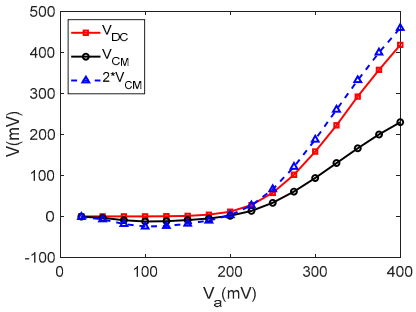


Figure 2. Output voltage and common-mode voltage of the rectifier in the subthreshold region.

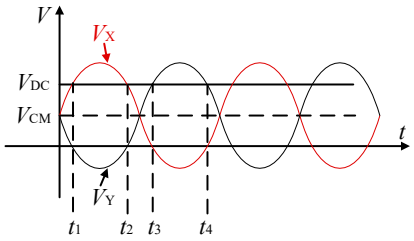


Figure 3. Voltage waveform of CCDD rectifier in subthreshold region.

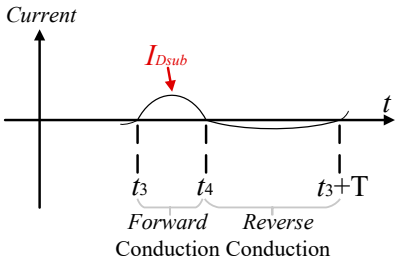


Figure 4. Current waveform of CCDD rectifier in subthreshold region.

We first analyze the M_{N1} path, at $t = t_3$, $V_{in}(t) = V_{DC}$, and V_{DS} of the transistor is equal to zero. Hence, the transistor's current is also equal to zero. After that, in the interval between t_3 and t_4, the input voltage is higher than the output voltage. We call the forward current in the subthreshold region $I_{Dsub,N1fw}$. The drain-source current of the transistor in the interval ($[t_3, t_4]$) is shown in Figure 5. The gate-source and drain-source voltages of the transistor in this interval are as follows:

$$v_{GS} = V_{C,N} + 2V_a \cos(\omega t) \tag{11}$$

$$v_{DS} = V_a \cos(\omega t) - V_{CM} \tag{12}$$

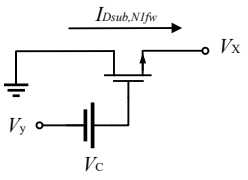


Figure 5. Subthreshold forward conduction of M_{N1}.

We can obtain the current of the transistor in $[t_3, t_4]$, which works in the subthreshold region according to (11) and (12):

$$I_{Dsub,N,fw} = I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N} + 2V_a \cos(\omega t)}{nV_T}} \left[1 - e^{-\frac{V_a \cos(\omega t) - V_{CM}}{V_T}} \right] \tag{13}$$

After t_4, in the interval between t_3 + T, the input voltage is larger than the output voltage and the source and drain terminus of the transistor switch for it. Therefore, the transistor begins to conduct in the reverse direction. Then, the $I_{\mathrm{Dsub,N1}rv}$ flows in the reverse direction, as shown in Figure 6. Thus, in [t_4, t_3 + T], the gate-source and drain-source voltages are

$$v_{GS} = V_{C,N} + V_{CM} + V_a \cos(\omega \mathrm{t}) \tag{14}$$

$$v_{DS} = V_{CM} - V_a \cos(\omega \mathrm{t}) \tag{15}$$

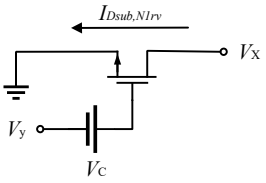


Figure 6. Subthreshold reverse conduction of $\mathrm{M_{N1}}$.

The transistor also works in the subthreshold region; the reverse current can be written as

$$I_{Dsub,N,rv} = I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N}+V_{CM}+V_a \cos(\omega \mathrm{t})}{nV_T}} \left[1 - e^{-\frac{V_{CM}-V_a \cos(\omega \mathrm{t})}{V_T}}\right] \tag{16}$$

Based on the transistor's current equations in both forward and reverse conductions, the charge conservation principle is adopted to analyze the circuit. Charges delivered by transistors in both top and bottom paths in the forward direction to the load capacitor $\mathrm{C_L}$ are equal to charges delivered by these transistors in the reverse direction and charges flowing through the load. For one transistor, charges delivered in the forward direction are equal to charges delivered in the reverse direction and one-half of the charges flow through the load. Both of them are calculated by integrating the corresponding current:

$$\int_{t_3}^{t_4} I_{Dsub,N,fw} dt = \int_{t_3}^{t_3+T} \frac{I_{Load}}{2}\, dt + \int_{t_4}^{t_3+T} I_{Dsub,N,rv} dt \tag{17}$$

The transistors currents can be substituted by (13) and (16). The resulting equation is

$$\begin{aligned} &\int_{t_3}^{t_4} I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N}+2V_a \cos(\omega \mathrm{t})}{nV_T}} \left[1 - e^{-\frac{V_a \cos(\omega \mathrm{t}) - V_{CM}}{V_T}}\right] dt = \\ &\int_{t_4}^{t_3+T} I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N}+V_{CM}+V_a \cos(\omega \mathrm{t})}{nV_T}} \left[1 - e^{-\frac{V_{CM}-V_a \cos(\omega \mathrm{t})}{V_T}}\right] dt + \int_{t_3}^{t_3+T} \frac{I_{Load}}{2} dt \end{aligned} \tag{18}$$

After some manipulation, the above equation is

$$\int_{t_3}^{t_3+T} I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N}}{nV_T}} \left[e^{\frac{2V_a \cos(\omega t)}{nV_T}} - e^{\frac{V_a \cos(\omega t)+V_{CM}}{nV_T}}\right] dt = \int_{t_3}^{t_3+T} \frac{I_{Load}}{2} dt \tag{19}$$

Because the interval in (19) constitutes a full period, we can calculate the integrals over [0, T] instead of [t_3, t_3 + T]. Fortunately, the result is irrelevant to the actual value of t_3 and t_4. Working out (19) for V_{CM}, we can obtain

$$V_{CM} = nV_T ln \frac{I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load} / \left(2I_{S,N} \frac{W_N}{L_N} e^{\frac{V_{C,N}}{nV_T}}\right)}{I_0\left(\frac{V_a}{nV_T}\right)} \tag{20}$$

I_0 is the zero-th order modified Bessel function of the first kind, defined as

$$I_0(x) = \frac{1}{\pi}\int_0^{\pi} e^{xcos(\theta)}d\theta \tag{21}$$

Also, we analyze the M_{P1} path following the above method and obtain

$$V_{DC} = V_{CM} + nV_T ln\frac{I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}\right)}{I_0\left(\frac{V_a}{nV_T}\right)} \tag{22}$$

Substituting (20) into (22), we can obtain

$$V_{DC} = nV_T ln\left[\frac{[I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}\right)][I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}\right)]}{[I_0\left(\frac{V_a}{nV_T}\right)]^2}\right] \tag{23}$$

Consequently, the output voltage of an N-stages CCDD CMOS rectifier V_{OUT} is given as $V_{\mathrm{OUT}} = NV_{\mathrm{DC}}$.

4. Input Resistance Model of CMOS CCDD Rectifier with Compensation Voltages

To analyze the input resistance of the rectifier, we analyze and calculate the power dissipation of each transistor first. For a single stage, the drain-source voltage and the transistor current are multiplied in both forward and reverse directions for these four transistors. Then, each voltage–current product is integrated into its interval. Therefore, the sum of these two integrals divided by the period T is the average consumed power dissipation in a single stage.

$$P_{d1} = 2(P_{MP1} + P_{MN1}) \tag{24}$$

$$P_{MP1} = \frac{1}{T}\left(\int_{t1}^{t2} V_{SD,P,fw}I_{Dsub,P,fw}dt + \int_{t2}^{t1+T} V_{SD,P,rv}I_{Dsub,P,rv}dt\right) \tag{25}$$

$$P_{MN1} = \frac{1}{T}\left(\int_{t3}^{t4} V_{DS,N,fw}I_{Dsub,N,fw}dt + \int_{t4}^{t3+T} V_{DS,N,rv}I_{Dsub,N,rv}dt\right) \tag{26}$$

The voltages and currents in the above equations are already obtained. The result is

$$P_{d1} = 2I_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}V_a\left[I_1\left(\frac{2V_a}{nV_T}\right) - e^{\frac{V_{DC}-V_{CM}}{nV_T}}I_1\left(\frac{V_a}{nV_T}\right)\right] + 2I_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}V_a[I_1\left(\frac{2V_a}{nV_T}\right) - e^{\frac{V_{CM}}{nV_T}}I_1\left(\frac{V_a}{nV_T}\right)] - V_{DC}I_{Load} \tag{27}$$

The power dissipation of the N-stage rectifier P_{dN} is obtained by the power dissipation in the single-stage P_{d1} multiplied by N. The power derived from the input AC source P_{inN} equals the power dissipated in the N-stage rectifier P_{dN} added to the load power consumption P_{Load}.

$$P_{\mathrm{inN}} = NP_{d1} + P_{\mathrm{Load}} \tag{28}$$

Also, the load voltage V_{DC} and the load current I_{Load} are multiplied to obtain P_{Load}. Then, we obtain

$$P_{inN} = 2NI_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}V_a\left[I_1\left(\frac{2V_a}{nV_T}\right) - \frac{I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}\right)}{I_0\left(\frac{V_a}{nV_T}\right)}I_1\left(\frac{V_a}{nV_T}\right)\right] + 2NI_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}V_a[I_1\left(\frac{2V_a}{nV_T}\right) - \frac{I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}\right)}{I_0\left(\frac{V_a}{nV_T}\right)}I_1\left(\frac{V_a}{nV_T}\right)] \tag{29}$$

To obtain the maximum possible power from the AC source antenna, the input impedance of the rectifier should be matched to the output impedance of the antenna. Unfortunately, the impedance of the rectifier circuit is affected by the parameters of this circuit and the input power. Firstly, a closed-form equation of the input resistance is proposed. Based on the basic power formula, the input power and the amplitude of the input signal are used to calculate the input resistance:

$$P_{inN} = \frac{{V_a}^2}{R_{inN}} \tag{30}$$

So, we have

$$R_{inN} = \frac{V_a I_0\left(\frac{V_a}{nV_T}\right)}{2NI_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}\left[I_0\left(\frac{V_a}{nV_T}\right)I_1\left(\frac{2V_a}{nV_T}\right) - [I_0\left(\frac{2V_a}{nV_T}\right) - I_{Load}/\left(2I_{S,P}\frac{W_P}{L_P}e^{\frac{-V_{C,P}}{nV_T}}\right)]I_1\left(\frac{V_a}{nV_T}\right)\right] + 2NI_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}[I_0\left(\frac{V_a}{nV_T}\right)I_1\left(\frac{2V_a}{nV_T}\right) - [I_0\left(\frac{2V_a}{nV_T}\right) - \frac{I_{Load}}{\left(2I_{S,N}\frac{W_N}{L_N}e^{\frac{V_{C,N}}{nV_T}}\right)}]I_1\left(\frac{V_a}{nV_T}\right)]} \tag{31}$$

As analyzed in [16], the input capacitance of the rectifier (C_{in}) is mainly composed of various parasitic capacitances, the input coupling capacitors (C_{co}), and the gate capacitance of N(P)MOS transistors ($C_{\text{GN(P)}}$). These capacitances are connected in series. To avoid any significant RF voltage dropping over C_{co} and transfer the full RF signal to the gate of the transistors, high-capacity capacitances are generally selected to be the input coupling capacitors, which are much higher than the gate capacitance. According to the series capacity formula of capacitors, the effect of C_{co} in the input capacitance can be neglected. So, we approximate the input capacitance of the rectifier as

$$C_{\text{inN}} = NC_{\text{in1}} + C_{\text{PAR}} \tag{32}$$

where C_{PAR} is the total parasitic capacitance connected to each of the RF inputs. The authors of [16] presented that the value of C_{inN} in post-layout simulations was much higher than the value in schematic simulations, which indicated that the total input capacitance C_{inN} was dominated by parasitic capacitance C_{PAR}. Therefore, when we design the impedance matching network, the value of C_{inN} obtained in post-layout simulations should be seriously considered to maximize the power transferred from the antenna to the input of the rectifier.

5. Simulation Results

5.1. Simulation Setup

Cadence Spectre simulation results with single- and N-stage COMS CCDD rectifiers configured with various specifications in the TSMC standard 65 nm CMOS process are used to verify the model. In order to enable low-power and low-leakage IoT applications, the low-power (LP) process portfolio is adopted. These four transistors are both high-threshold transistors. The threshold voltage V_{th0} of NMOS when the body bias is zero is 420 mV, and the threshold voltage V_{th0} of PMOS is −370 mV, which are both retrieved from Spectre library files. We focus on comparison between the deduction results of the output voltage model and input resistance model and simulation results. Some parameters of our model are determined based on the BSIM4 4.8.2 MOSFET Model User's Manual [30,31], such as $V_{\text{T}} = 26$ mV, $\mu_{\text{N}} = 240.734$ cm^2/(V·s), $\mu_{\text{P}} = 101.835$ cm^2/(V·s), $\Phi_{\text{s,N}} = 0.9743$ V, $\Phi_{\text{s,P}} = 0.9738$ V, $V_{off,\text{N}} = -103.68$ mV, $V_{off,\text{P}} = -68.06$ mV, $NDEN = 6.5 \times 10^{17}$, and $NDEP = 6.3687 \times 10^{17}$.

These input capacitors C are set to 1pF and load capacitors C_{L} are set to 1pF, the same as other papers. As mentioned in the Introduction, the mode describes the CCDD rectifier's duty-cycled behavior with a heavy load at very low input powers. Therefore, R_{L} is set to 0.45 MΩ, 1 MΩ, 5 MΩ, and 20 MΩ.

5.2. The Single-Stage Rectifier

Figure 7 shows a comparison between the model [16,27] and the simulation results for the output voltage at different RF power levels when the operating frequency is set to 915 MHz and the load R_L is set to 0.45 MΩ, 1 MΩ, 5 MΩ, and 20 MΩ. The peak voltage is still below the threshold of the adopted process, upholding subthreshold operation. It can be seen that the model and [16] are in accordance with the simulation results, and the model has the smallest deviation from the simulation results, especially with heavy loads. The maximum deviation is less than 10%.

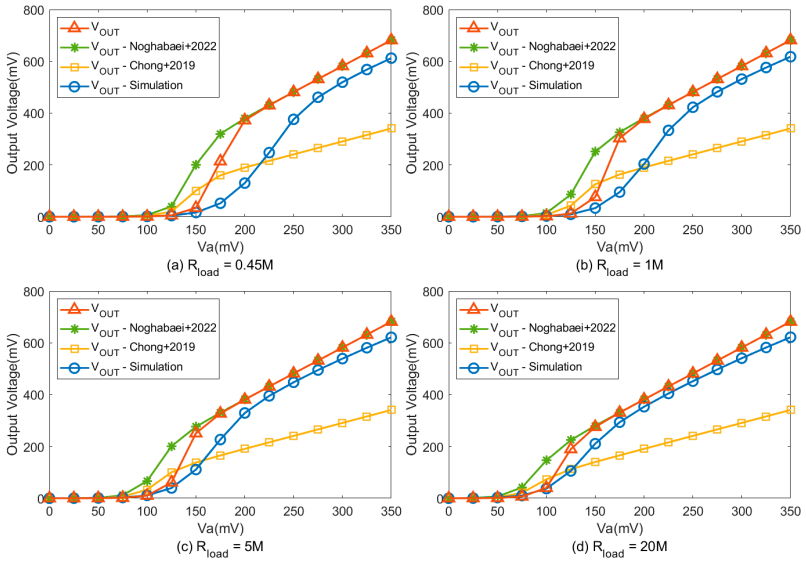


Figure 7. Output voltage of a single-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; (**a**) R_{Load} = 0.45 MΩ [16,27]; (**b**) R_{Load} = 1 MΩ [16,27]; (**c**) R_{Load} = 5 MΩ; [16,27] and (**d**) R_{Load} = 20 MΩ [16,27].

Figure 8 shows output voltages as a function of the input power with two compensation voltages from extra circuitries. $V_{C,N}$ is set to 100 mV and $V_{C,P}$ is set to −150 mV. It can also be seen that the model and [16] are in accordance with the simulation results, and our model has the smallest deviation from the simulation results, especially with heavy loads.

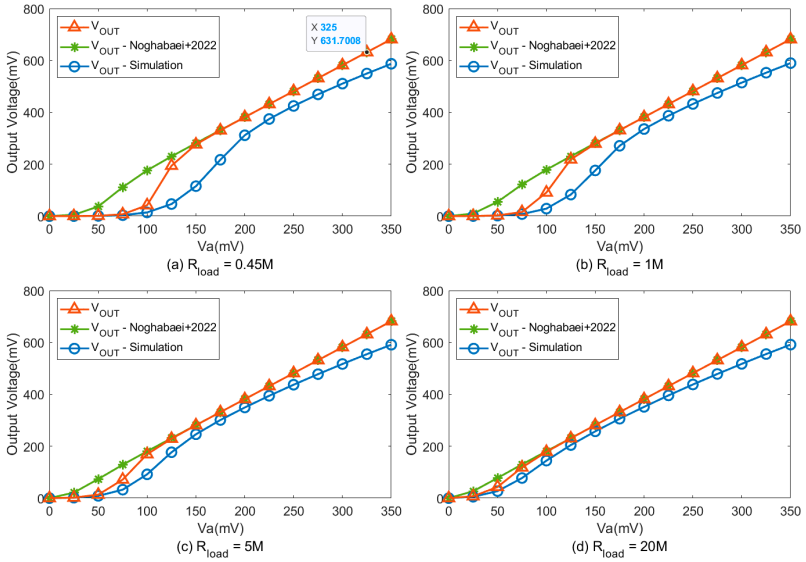


Figure 8. Output voltage of a single-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 100 mV; $V_{C,P}$ = −150 mV; (**a**) R_{Load} = 0.45 MΩ [16]; (**b**) R_{Load} = 1 MΩ [16]; (**c**) R_{Load} = 5 MΩ [16]; and (**d**) R_{Load} = 20 MΩ [16].

5.3. The N-Stage Rectifier

The number of stages is set to 10. Figure 9 shows output voltages as a function of the input power of a 10-stage rectifier when R_L was set to 0.45 MΩ, 1 MΩ, 5 MΩ, and 20 MΩ without compensation voltages. Figure 10 shows output voltages as a function of the input power of a 10-stage rectifier with compensation voltages. These yielded similar conclusions.

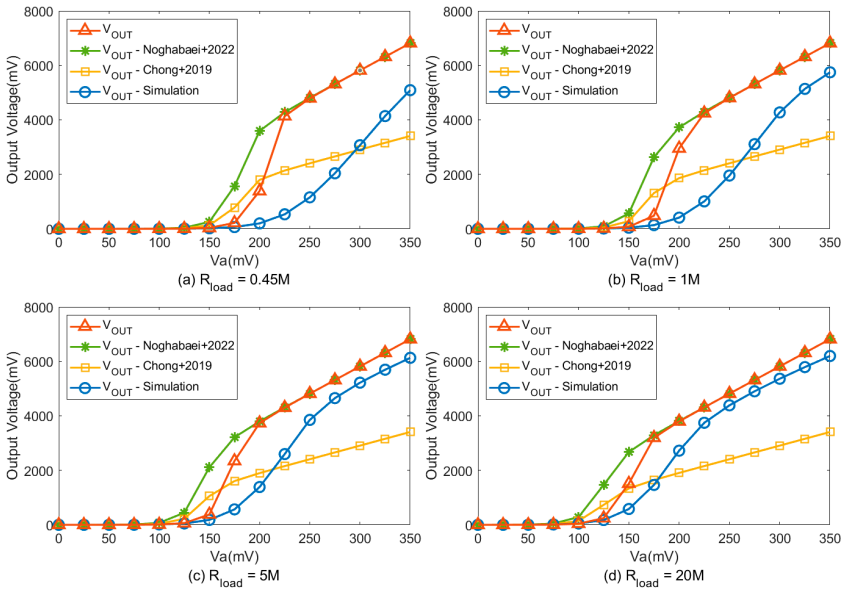


Figure 9. Output voltage of 10-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0 mV; $V_{C,P}$ = 0 mV; (**a**) R_{Load} = 0.45 MΩ [16,27]; (**b**) R_{Load} = 1 MΩ [16,27]; (**c**) R_{Load} = 5 MΩ [16,27]; and (**d**) R_{Load} = 20 MΩ [16,27].

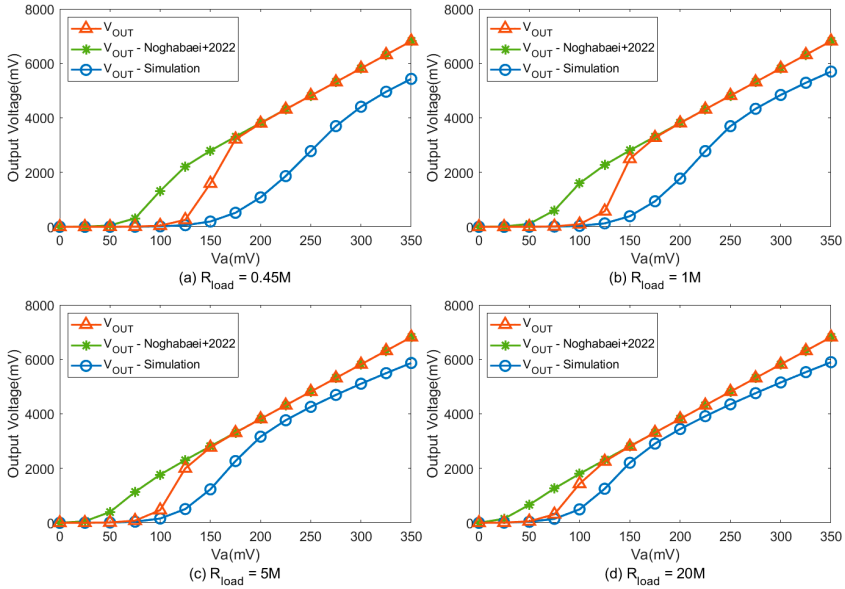


Figure 10. Output voltage of 10-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 100 mV; $V_{C,P}$ = −150 mV [16]; (**a**) R_{Load} = 0.45 MΩ [16]; (**b**) R_{Load} = 1 MΩ [16]; (**c**) R_{Load} = 5 MΩ [16]; and (**d**) R_{Load} = 20 MΩ [16].

Figure 11 is the comparison results of the input resistance between the model [16] and the simulation results at different RF power levels when the operating frequency was set to 915 MHz and the load R_L was set to 0.45 MΩ, 1 MΩ, 5 MΩ, and 20 MΩ. The peak voltage is still below the threshold voltage of the adopted process, holding subthreshold operation.

It can be seen that the model is in accordance with simulation results. Although [16] shows good agreement when the input is relatively large, the deviation increases when the input is small. Meanwhile, this result is consistent with the conclusion of [29] that the rectifier's input resistance R_{in} increases greatly at low V_{in} as transistors enter the subthreshold region. Because compensation voltages make no difference to input resistance, the results of input resistances with compensation voltages are not mentioned.

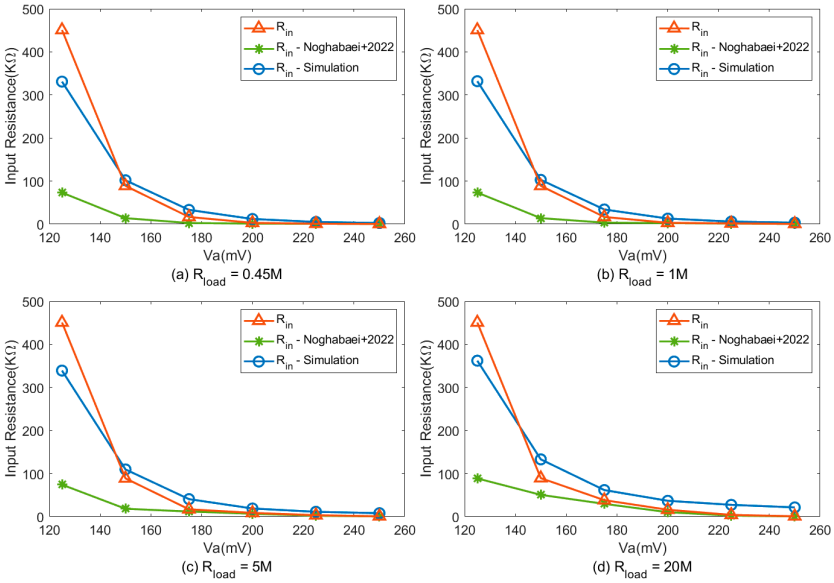


Figure 11. Input resistance of 10-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; (**a**) R_{Load} = 0.45 MΩ [16]; (**b**) R_{Load} = 1 MΩ [16]; (**c**) R_{Load} = 5 MΩ [16] and (**d**) R_{Load} = 20 MΩ [16].

5.4. PVT Variation Effects

PVT is an acronym for process, voltage, and temperature. Chip designers model chips at various process, voltage, and temperature corners in order to make them function after manufacturing in all scenarios or conditions. PVT variations are mostly considered, and most other variation is swallowed up in the process part. In the rectifier, the supply voltage is supplied from an antenna with a matching network. The incident RF power of the antenna is unpredictable and has a large dynamic range. So, Va is taken into account in our simulations, and other factors causing supply voltage variation are ignored. For process corners, we run simulations at FF, SS, and TT corners. For temperature, we run simulations at 0 °C, 25 °C, and 70 °C.

Figure 12 shows output voltages as a function of the input power of a single rectifier when T was set to 0 °C, 25 °C, and 70 °C, respectively, without compensation voltages. u_N, u_P, $V_{th,N}$, $V_{off,N}$, $V_{th,P}$, and $V_{off,P}$ were set according to different temperatures. Temperature variations have a certain influence on the differences between the model and simulation results, but this influence was in an acceptable range. Figure 13 shows input resistances as a function of the input power of a single rectifier when T was set to 0 °C, 25 °C, and 70 °C, respectively, without compensation voltages. Temperature variations have a certain influence on the differences between the model and simulation results, but this influence was in an acceptable range. When the process is set to TT, the effects are minimal.

Figure 14 shows output voltages as a function of the input power of a single rectifier when *process* was set to FF, TT, and SS, respectively, without compensation voltages. Figure 15 shows input resistances as a function of the input power of a single rectifier when *process* was set to FF, TT, and SS, respectively, without compensation voltages. We obtain the same results.

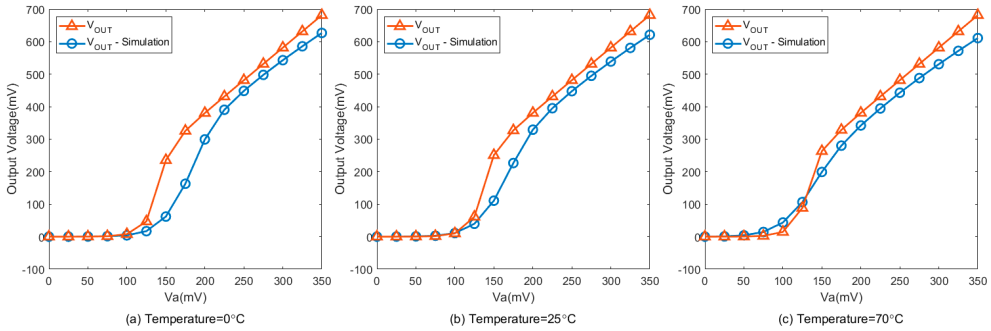


Figure 12. Output voltage of a single-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; R_{Load} = 5 MΩ; process is TT; (**a**) T = 0 °C; (**b**) T = 25 °C; (**c**) T = 70 °C.

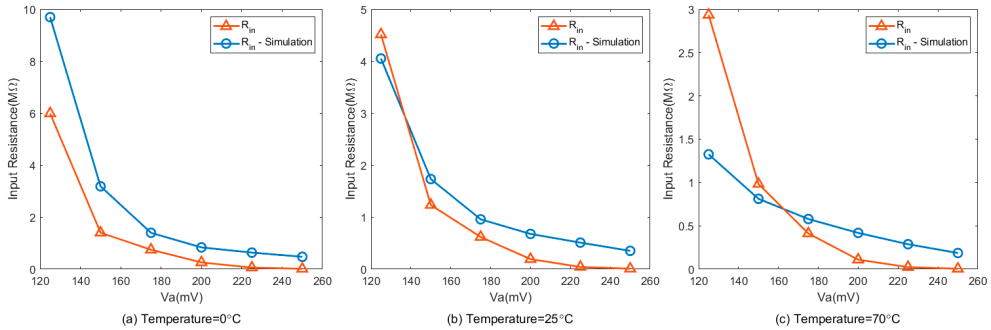


Figure 13. Input resistance of a single-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; R_{Load} = 5 MΩ; process is TT; (**a**) T_0 = 0 °C; (**b**) T_0 = 25 °C; (**c**) T_0 = 70 °C.

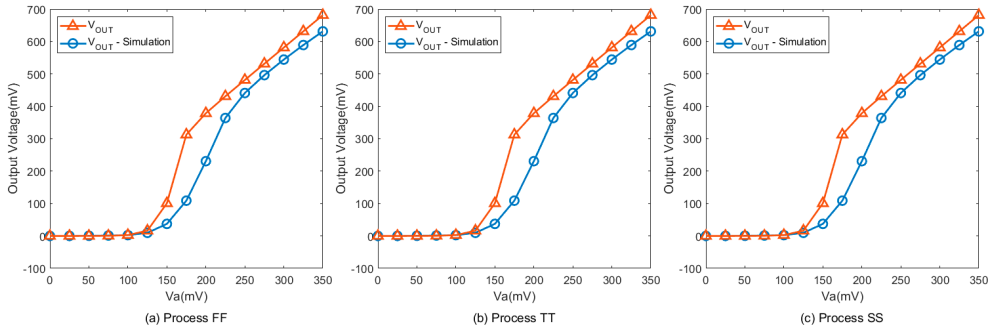


Figure 14. Output voltage of a single-stage rectifier vs. input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; R_{Load} = 5 MΩ; temperature = 25 °C; (**a**) *process* is FF; (**b**) *process* is TT; (**c**) *process* is SS.

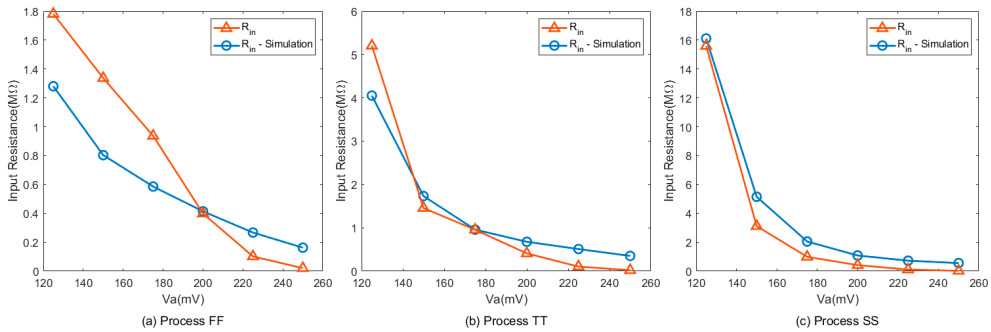


Figure 15. Input resistance of a single-stage rectifier vs input voltage. W_N = 960 nm; L_N = 60 nm; W_P = 960 nm; L_P = 60 nm; $V_{C,N}$ = 0; $V_{C,P}$ = 0; R_{Load} = 5 MΩ; temperature = 25 °C; (**a**) *process* is FF; (**b**) *process* is TT; (**c**) *process* is SS.

6. Measurement Results

The CCDD rectifier was fabricated in the 65 nm standard CMOS technology by the authors of [15] and the measurement results were reported in [15]. Rectifier transistors are low-threshold transistors, and the rectifier was optimized separately for its optimum performance. In this experiment, W_N is set to 1480 nm, L_N is set to 180 nm, W_P is set to 4000 nm, L_P is set to 100 nm, frequency is set to 433 MHz, and the load R_L is set to 0.1 MΩ, according to [15]. The measurement setup consists of a vector network analyzer and a digital multimeter. A GSGSG differential prober with a reference plane set to the on-chip pads of the rectifier's input is used to probe and sweep the chip. When the output RF power of the vector network analyzer is swept, the corresponding S-parameters and output voltage at the load are recorded. The instantaneous input power delivered to the rectifier is calculated by subtracting the transmission and the reflection losses from the RF power. The measurement setup is popular and commonly utilized in related articles, and a block diagram of the measurement setup is given in Figure 16. So, these measurement results are adopted to verify the model. Meanwhile, we use the proposed model and the model of [16] to predict the output voltages and input resistance.

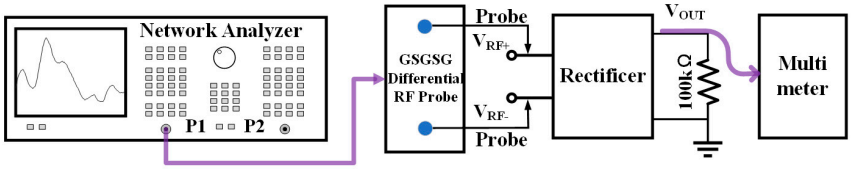


Figure 16. The block diagram of the measurement setup used in [15].

Figure 17 shows the measured output DC voltages of [15] and results predicted by the proposed model and the model of [16] versus the input powers. The threshold voltage of NMOS is around 379 mV and the threshold voltage of PMOS is around −429 mV. Both of them are found in simulation data. The measured results, predicted results of the model, and predicted results of [16] are consistent where the input powers are below −25 dBm (the peak voltage is still below the threshold of the adopted process). Furthermore, the proposed model matches the measured results better than the model of [16] in the subthreshold range.

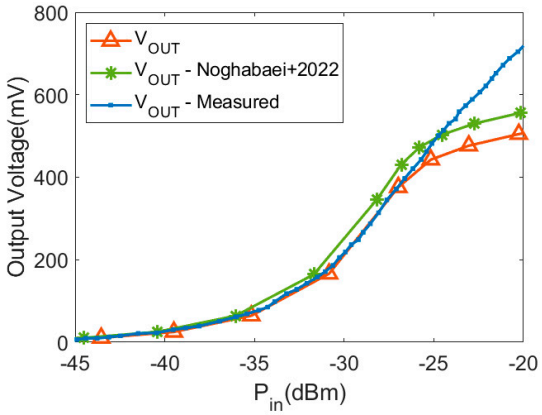


Figure 17. Measurement output voltages and predicted output voltages by the proposed model and the model of [16].

Due to the lack of input resistance data in [15] and input resistance being reflected from PCE according to the derivation process, the PCE results of [15] are adopted to verify the model. Figure 18 shows the measured PCE of [15], and the PCE predicted by our model and the model of [16] versus the input powers. The measured results, predicted results of the model, and predicted results of [16] are consistent where the input powers are below −25 dBm. Furthermore, the proposed model matches the measured results better than the model of [16].

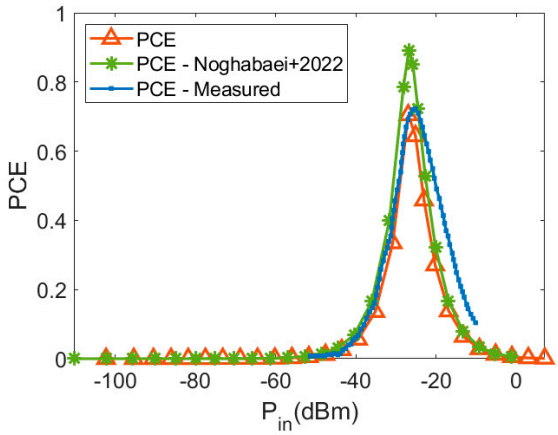


Figure 18. Measurement of PCE and predicted PCE by the proposed model and the model of [16].

7. Discussion

For a single stage, the deviation is relatively large when the input voltage is near 150 mV. This is due to the fact that our model is based on BSIM4, which is only valid in particular regions of operation, and several approximate models were connected mathematically to provide a continuous model. The transistors were working at the junction of the depletion region and weak inversion region when the input voltage was near 150 mV. Therefore, the regional approach leads to inaccuracy between regions.

In addition, the *V*th compensation technique is effective in limiting the "dead zone", but it has no significant impact on the final output voltage. Evaluating the effects of the *V*th compensation technique and finding the optimum ($V_{C,N}$, $V_{C,P}$) pair to maximize the output voltage at a given input power level in any specific process are our future plans and will be proposed in our next paper.

Finally, the model is specific to the topology in Figure 1. CCDD topology is a large class of commonly utilized rectifiers, and a great number of new rectifiers are based on CCDD topology. It is very easy to model and analyze them on the basis of our model. Certainly, the model cannot be adapted to other topologies, such as Dickson.

8. Conclusions

In this paper, we successfully modeled a CMOS CCDD rectifier in the subthreshold region for an Ultra-Low-Power ambient RF energy harvester. The effect of the compensation voltages was also considered in this model. This model was validated with the simulation results with CCDD rectifiers (with or without compensation voltages). Each rectifier was tested over four different loading conditions with an external resistive under different ambient RF levels. The results derived from our model had excellent consistency with simulation results. Some measurement results reported in previous papers were also used to verify our model. This model can be applied to implement a non-iterative algorithm to make an optimum choice of parameters to achieve the optimized gain.

Author Contributions: Conceptualization, P.L.; validation, H.W. and R.L.; formal analysis, L.Z. and J.W. All authors have read and agreed to the published version of the manuscript.

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Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author.

Conflicts of Interest: Author Runze Li was employed by the Tianjin Keepsens Information Technology Co. The remaining authors declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

References

1. Zhang, X.; Grajal, J.; Lopez-Vallejo, M.; Mcvay, E.; Palacios, T. Opportunities and Challenges of Ambient Radio-Frequency Energy Harvesting. *Joule* **2020**, *4*, 1142–1152. [CrossRef]
2. Portilla, L.; Loganathan, K.; Faber, H.; Eid, A.; Hester, J.G.D.; Tentzeris, M.M.; Fattori, M.; Cantatore, E.; Jiang, C.; Nathan, A.; et al. Wirelessly powered large-area electronics for the Internet of Things. *Nat. Electron.* **2023**, *6*, 10–17. [CrossRef]
3. Gu, X.; Hemour, S.; Wu, K. Far-Field Wireless Power Harvesting: Nonlinear Modeling, Rectenna Design, and Emerging Applications. *Proc. IEEE* **2022**, *110*, 56–73. [CrossRef]
4. Gu, X.; Grauwin, L.; Dousset, D.; Hemour, S.; Wu, K. Dynamic Ambient RF Energy Density Measurements of Montreal for Battery-Free IoT Sensor Network Planning. *IEEE Internet Things J.* **2021**, *8*, 13209–13221. [CrossRef]
5. Ibrahim, H.H.; Singh, M.J.; Al-Bawri, S.S.; Ibrahim, S.K.; Islam, M.T.; Alzamil, A.; Islam, M.S. Radio Frequency Energy Harvesting Technologies: A Comprehensive Review on Designing, Methodologies, and Potential Applications. *Sensors* **2022**, *22*, 4144. [CrossRef]
6. Sharma, P.; Singh, A.K. A Survey on RF energy harvesting techniques for lifetime enhancement of wireless sensor networks. *Sustain. Comput. Inform. Syst.* **2023**, *37*, 100836. [CrossRef]
7. Clerckx, B.; Zhang, R.; Schober, R.; Ng, D.W.K.; Kim, D.I.; Poor, H.V. Fundamentals of Wireless Information and Power Transfer: From RF Energy Harvester Models to Signal and System Designs. *IEEE J. Sel. Areas Commun.* **2019**, *37*, 4–33. [CrossRef]
8. Ramalingam, L.; Mariappan, S.; Parameswaran, P.; Rajendran, J.; Nitesh, R.S.; Kumar, N.; Nathan, A.; Yarman, B.S. The Advancement of Radio Frequency Energy Harvesters (RFEHs) as a Revolutionary Approach for Solving Energy Crisis in Wireless Communication Devices: A Review. *IEEE Access* **2021**, *9*, 106107–106139. [CrossRef]
9. Mohan, A.; Mondal, S.; Dan, S.S.; Paily, R.P. Design Considerations for Efficient Realization of Rectifiers in Microscale Wireless Power Transfer Systems: A Review. *IEEE Sens. J.* **2023**, *23*, 20691–20704. [CrossRef]
10. Yong, J.K.; Lian, X.L.; Ramiah, H.; Churchill, K.K.P.; Chong, G.; Lai, N.S.; Chen, Y.; Mark, P.; Martins, R.P. A Fully Integrated CMOS Tri-Band Ambient RF Energy Harvesting System for IoT Devices. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2023**, *70*, 4705–4718. [CrossRef]
11. Liang, Z.; Yuan, Y. A Compact Dual-Band Four-Port Ambient RF Energy Harvester with High-Sensitivity, High-Efficiency, and Wide Power Range. *IEEE Trans. Microw. Theory Tech.* **2022**, *70*, 641–649. [CrossRef]
12. Chun, A.C.C.; Ramiah, H.; Mekhilef, S. Wide Power Dynamic Range CMOS RF-DC Rectifier for RF Energy Harvesting System: A Review. *IEEE Access* **2022**, *10*, 23948–23963. [CrossRef]
13. Choo, A.; Lee, Y.C.; Ramiah, H.; Chen, Y.; Mak, P.; Martins, R.P. A High-PCE Range-Extension CMOS Rectifier Employing Advanced Topology Amalgamation Technique for Ambient RF Energy Harvesting. *IEEE Trans. Circuits Syst. II Express Briefs* **2023**, *70*, 3747–3751. [CrossRef]
14. Mohamed, M.M.; Fahmy, G.A.; Abdel-Rahman, A.B.; Allam, A.; Barakat, A.; Abo-zahhad, M.; Jia, H.; Pokharel, R. High-Efficiency CMOS RF-to-DC Rectifier Based on Dynamic Threshold Reduction Technique for Wireless Charging Applications. *IEEE Access* **2018**, *6*, 46826–46832. [CrossRef]
15. Almansouri, A.S.; Kosel, J.; Salama, K.N. A Dual-Mode Nested Rectifier for Ambient Wireless Powering in CMOS Technology. *IEEE Trans. Microw. Theory Tech.* **2020**, *68*, 1754–1762. [CrossRef]
16. Noghabaei, S.M.; Radin, R.L.; Savaria, Y.; Sawan, M. A High-Sensitivity Wide Input-Power-Range Ultra-Low-Power RF Energy Harvester for IoT Applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2022**, *69*, 440–451. [CrossRef]
17. Lian, W.X.; Ramiah, H.; Chong, G.; Churchill, K.K.P.; Lai, N.S.; Mak, P.; Martins, R.P. A −20-dBm Sensitivity RF Energy-Harvesting Rectifier Front End Using a Transformer IMN. *IEEE Trans. Very Large Scale Integr. (VLSI) Syst.* **2022**, *30*, 1808–1812. [CrossRef]
18. Karami, M.A.; Moez, K. A Highly-Efficient RF Energy Harvester Using Passively-Produced Adaptive Threshold Voltage Compensation. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2021**, *68*, 4603–4615. [CrossRef]
19. Moghaddam, A.K.; Chuah, J.H.; Ramiah, H.; Ahmadian, J.; Mak, P.; Martins, R.P. A 73.9%-Efficiency CMOS Rectifier Using a Lower DC Feeding (LDCF) Self-Body-Biasing Technique for Far-Field RF Energy-Harvesting Systems. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 992–1002. [CrossRef]
20. Li, Y.; Li, Q.; Liu, X.; Wang, X.; Liu, Y. A high efficiency CMOS RF rectifier for RF energy harvesting with dynamic self-body-biasing technique. *IEICE Electron. Express* **2019**, *16*, 20190462. [CrossRef]
21. Al-absi, M.A.; Alkhalifa, I.M.; Mohammed, A.A.; Al-Khulaifi, A.A. A CMOS Rectifier Employing Body Biasing Scheme for RF Energy Harvesting. *IEEE Access* **2021**, *9*, 105606–105611. [CrossRef]
22. Sadagopan, K.R.; Kang, J.; Ramadass, Y.; Natarajan, A. A cm-Scale 2.4-GHz Wireless Energy Harvester with NanoWatt Boost Converter and Antenna-Rectifier Resonance for WiFi Powering of Sensor Nodes. *IEEE J. Solid-State Circuits* **2018**, *53*, 3396–3406. [CrossRef]
23. Theilmann, P.T.; Presti, C.D.; Kelly, D.J.; Asbeck, P.M. A μW Complementary Bridge Rectifier with Near Zero Turn-on Voltage in SOS CMOS for Wireless Power Supplies. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2012**, *59*, 2111–2124. [CrossRef]
24. Izad, M.; Jiang, N.; Filanovsky, I.M.; Moez, K. A Non-Iterative Method for Design of Radio Frequency Energy Harvesters. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2024**, *71*, 133–146. [CrossRef]
25. Saffari, P.; Basaligheh, A.; Moez, K. An RF-to-DC Rectifier with High Efficiency over Wide Input Power Range for RF Energy Harvesting Applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2019**, *66*, 4862–4875. [CrossRef]

26. Gharehbaghi, K.; Kocer, F.; Kulah, H. Optimization of Power Conversion Efficiency in Threshold Self-Compensated UHF Rectifiers with Charge Conservation Principle. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 2380–2387. [CrossRef]
27. Chong, G.; Ramiah, H.; Yin, G.; Rajendran, J.; Wong, W.R.; Mak, P.; Martins, R.P. CMOS Cross-Coupled Differential-Drive Rectifier in Subthreshold Operation for Ambient RF Energy Harvesting—Model and Analysis. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 1942–1946. [CrossRef]
28. Kotani, K.; Sasaki, A.; Ito, T. High-Efficiency Differential-Drive CMOS Rectifier for UHF RFIDs. *IEEE J. Solid-State Circuits* **2009**, *44*, 3011–3018. [CrossRef]
29. Xu, P.C.; Flandre, D.; Bol, D. Analysis, Modeling, and Design of a 2.45-GHz RF Energy Harvester for SWIPT IoT Smart Sensors. *IEEE J. Solid-State Circuits* **2019**, *54*, 2017–2029. [CrossRef]
30. Cardoso, A.J.; Carli, L.G.D.; Galup-Montoro, C.; Schneider, M.C. Analysis of the Rectifier Circuit Valid Down to Its Low-Voltage Limit. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2012**, *59*, 106–112. [CrossRef]
31. Liang, Z.; Yuan, J. Modelling and optimisation of high-efficiency differential-drive complementary metal-oxide-semiconductor rectifier for ultra-high-frequency radio-frequency energy harvesters. *IET Power Electron.* **2019**, *12*, 588–597. [CrossRef]
32. Kotsubo, R.; Tanzawa, T. Modeling of Cross-Coupled AC–DC Charge Pump Operating in Subthreshold Region. *Electronics* **2023**, *12*, 5031. [CrossRef]
33. Haeri, A.A.R.; Karkani, M.G.; Sharifkhani, M.; Kamarei, M.; Fotowat-Ahmady, A. Analysis and Design of Power Harvesting Circuits for Ultra-Low Power Applications. *IEEE Trans. Circuits Syst. I Regul. Pap.* **2017**, *64*, 471–479. [CrossRef]
34. Schneider, M.C. *Mosfet Modeling for Circuit Analysis and Design*; World Scientific: Singapore, 2007; pp. 367–386.
35. Department of Electrical Engineering and Computer Science University of California: BSIM4 4.8.2 MOSFET Model User's Manual. 2020. Available online: http://bsim.berkeley.edu/models/bsim4/ (accessed on 18 March 2024).

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