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Increase in Power Efficiency When Discharging Series Capacitors with a Step-Down Circuit Compared to Discharging Parallel Capacitors with a Step-Up Circuit

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Abstract: A discharging circuit with high energy efficiency is designed for supercapacitors. In this design, the capacitors are connected in parallel during charging and connected in series during discharging. With this method, the voltage of the capacitors in series becomes two times larger during discharging; thus, the step-down circuit can be used to produce the desired output voltage. The efficiency of the step-down circuit is four times larger than that of the step-up circuit in simulations. The experimental results agree well with the theoretical values. These results show that a step-down circuit is superior to a step-up circuit for extracting electrical energy from supercapacitors.

Keywords: extracting energy from supercapacitors; step-down circuit; step-up circuit; series–parallel conversion

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1. Introduction

Recently, the storage of renewable energy has become an important issue [1–15]. To store this energy, supercapacitors are important due to their large power density, which is 10 times larger than that of lithium-ion batteries [1,3,9]. Moreover, their operating temperature has a wider range [3]. The lifetime of supercapacitors is 1,000,000 cycles [4], while that of lithium-ion batteries is about 5000 cycles [5,6], and their energy density is currently about 17 Wh/kg [2], which is 20% that of iron phosphate lithium-ion batteries at 100 Wh/kg [7]. However, this energy density is not a serious problem when they are used in a sufficiently wide space. These advantageous characteristics make supercapacitors very suitable for storing energy from renewable resources. However, there is a problem in that the energy-stored capacitor voltage decreases when a supercapacitor is discharged. Therefore, a step-up circuit is usually used to maintain the output voltage. However, the discharging method with a step-up circuit is not the only one that uses two supercapacitors. Another method uses capacitors that are connected in parallel during charging and in series during discharging. With this series–parallel conversion method [16,17], the capacitor voltage becomes two times larger during discharging; thus a step-down circuit can be used to produce the desired output voltage. In this paper, we investigate which method, the step-up or step-down method, is better from the viewpoint of power efficiency.

2. Theoretical Analysis

Figure 1 shows a step-down circuit, which has two switching transistors (S_1 and S_2), an inductor, and a load resistor R_L [18,19]. The power supply voltage is V_{DD}. The S_1 and S_2 transistors are turned on alternately. The inductor has inductance L and resistance R_{ind}. The switching transistor is set to be ideal like a mechanical switch, and the on-resistance in the transistor is R_{on}. The ratio between the time when S_1 is ON and a period is defined as the duty ratio d. Then, the output voltage V_{out} is equal to dV_{DD}. The inductor current i is almost constant in the steady state.

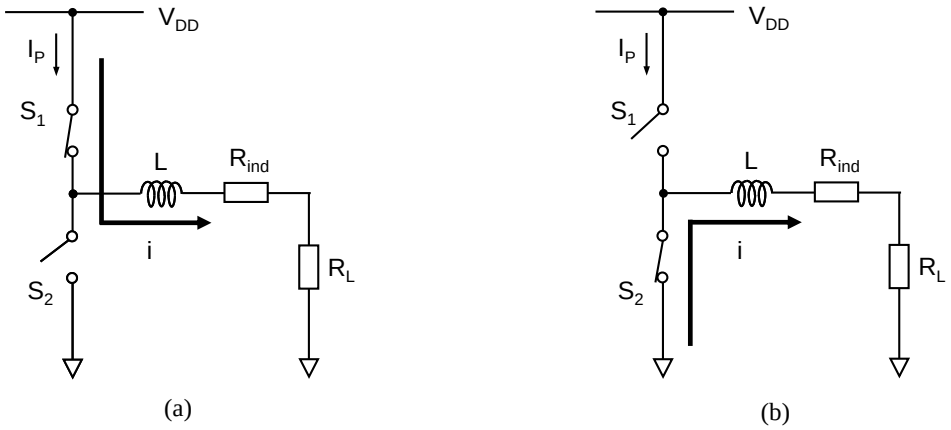

Figure 1. Step-down circuit: (**a**) S_1 is closed; (**b**) S_2 is closed.

Figure 2 shows a step-up circuit, which has two switching transistors (S_1 and S_2), an inductor, a capacitor, and a load resistor. The inductor has inductance L and resistance R_{ind}. Similar to the step-down circuit, the ratio between the time when S_1 is ON and a period is defined as d. In this circuit, the output voltage is equal to V_{DD}/d. When S_1 or S_2 is turned on, the inductor current i flows as shown in Figure 2a or Figure 2b, respectively. The current i is also almost constant in the steady state. Here, the current through the load resistor i_{RL} is investigated. The current through the capacitor in Figure 2a is defined as i_{C1}. The direction of the current flowing from the top to the bottom of the capacitor is defined as positive. From the current law, we have $i = i_{C1} + i_{RL}$. Next, we consider the current law in Figure 2b. The current through the capacitor in Figure 2b is defined as i_{C2}. The positive direction is the same as from top to bottom. Then, we have $i_{C2} + i_{RL} = 0$ in Figure 2b. Using the law of charge conservation at the capacitor, we have:

$$di_{C1} + (1-d)i_{C2} = 0. \tag{1}$$

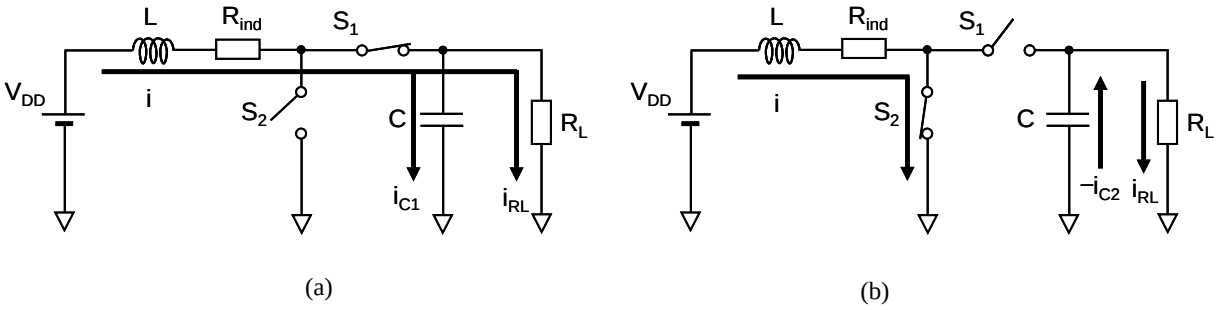

Figure 2. Step-up circuit: (**a**) S_1 is closed; (**b**) S_2 is closed.

The value of di_{C1} is equal to the charge amount from the power supply to the capacitor when S_1 is ON, and $(1-d)i_{C2}$ is equal to the charge amount from the capacitor to the load resistor when S_2 is ON. Therefore, using (1), we have:

$$i_{RL} = -i_{C2} = \frac{d}{1-d} \cdot i_{C1}. \tag{2}$$

Then, we have:

$$i = i_{C1} + i_{RL} = i_{C1} + \frac{d}{1-d} \cdot i_{C1} = \frac{1}{1-d} \cdot i_{C1} = \frac{i_{RL}}{d}. \tag{3}$$

Therefore, we have the following relationship in the circuit shown in Figure 2:

$$i_{RL} = di. \tag{4}$$

This relationship was confirmed in SPICE simulations, as shown in Figure 3. In the simulation, i was a constant 5 A and d was 0.8. Then, i_{RL} was equal to 4 A. When S_1 was ON ($1 \leqq t \leqq 9$ µs), i_{C1} was 1 A. During this time, $i = i_{C1} + i_{RL}$ was satisfied. When S_2 was ON ($9 \leqq t \leqq 11$ µs), i_{C2} was -4 A.

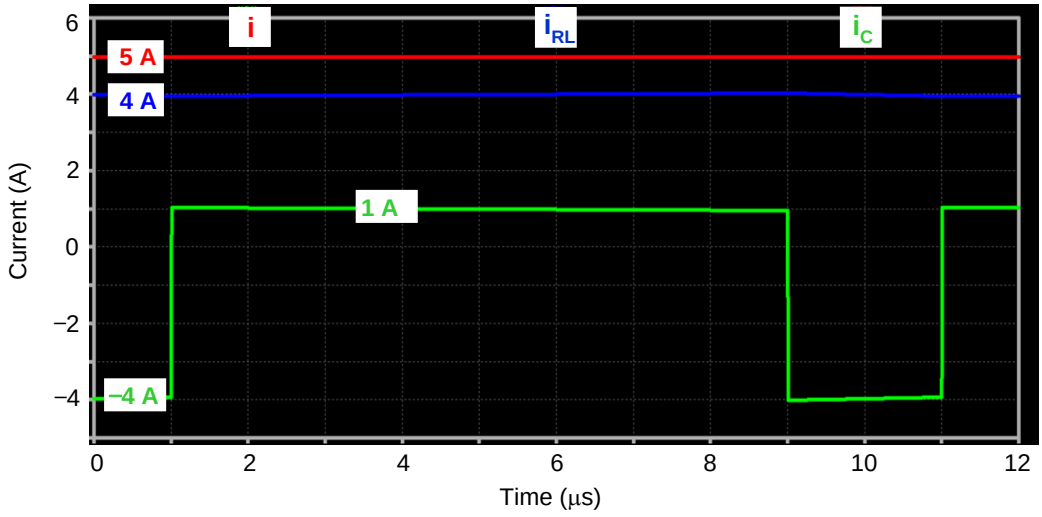

Figure 3. Current waveforms of inductor current (red line), load resistor current (blue line), and capacitor current (green line).

The relationship $i_{C2} + i_{RL} = 0$ was also satisfied during this time. From the simulation, the described equation could be confirmed.

Next, the energy efficiency of the step-down circuit η_{dn} was considered. The current trough load resistor is a constant i. Then, the output power P_{out} is $R_L i^2$. The input power P_{in} is the sum of the power consumption of $R_{on}i^2$, $R_{ind}i^2$, and $R_L i^2$. Then, η_{dn} is derived as P_{out}/P_{in} and written as:

$$\eta_{dn} = \frac{R_L}{R_{on} + R_{ind} + R_L}. \tag{5}$$

The energy efficiency of the step-up circuit η_{up} can be calculated in the same way. This time, the current trough load resistor is written as di from (4). Then, η_{up} is derived as:

$$\eta_{up} = \frac{R_L d^2}{R_{on} + R_{ind} + R_L d^2}. \tag{6}$$

Next, we investigated the energy efficiency in a SPICE simulation. During the step-down simulation, the power supply voltage was set to 5 V and the output voltage was 3 V. During the step-up simulation, the power supply voltage was set to 2.5 V and increased to 3 V. L was set as 1 H. R_{ind} was set as 1 or 0.01 Ω. R_L was set as 10 Ω. R_{on} was changed, with values of 0.01, 0.05, 0.1, and 0.5 Ω. On the other hand, the value of the off-resistance in the transistor was 10 MΩ. The power efficiency was calculated as P_{out}/P_{in} in SPICE. The simulation and analytical results of η_{dn} and η_{up} from (5) and (6) are shown in Tables 1 and 2, respectively. They were perfectly consistent with each other. For a clear understanding of the dependence of R_{on}, the simulation results are shown in Figure 4. The graph shows that the step-down circuit exhibits better efficiency than the step-up circuit.

Table 1. Comparison of the step-down circuit efficiency between theory and SPICE simulation.

R_{on} (Ω)	R_{ind} = 1 (Ω)		R_{ind} = 0.01 (Ω)	
	SPICE	**Theory**	**SPICE**	**Theory**
0.01	0.9082	0.9083	0.9979	0.9980
0.05	0.9049	0.9050	0.9939	0.9940
0.1	0.9008	0.9009	0.9890	0.9891
0.5	0.8695	0.8696	0.9514	0.9514

Table 2. Comparison of the step-up circuit efficiency between theory and SPICE simulation.

R_{on} (Ω)	R_{ind} = 1 (Ω)		R_{ind} = 0.01 (Ω)	
	SPICE	**Theory**	**SPICE**	**Theory**
0.01	0.8236	0.8237	0.9970	0.9971
0.05	0.8143	0.8145	0.9911	0.9913
0.1	0.8035	0.8037	0.9838	0.9839
0.5	0.6862	0.6864	0.9187	0.9189

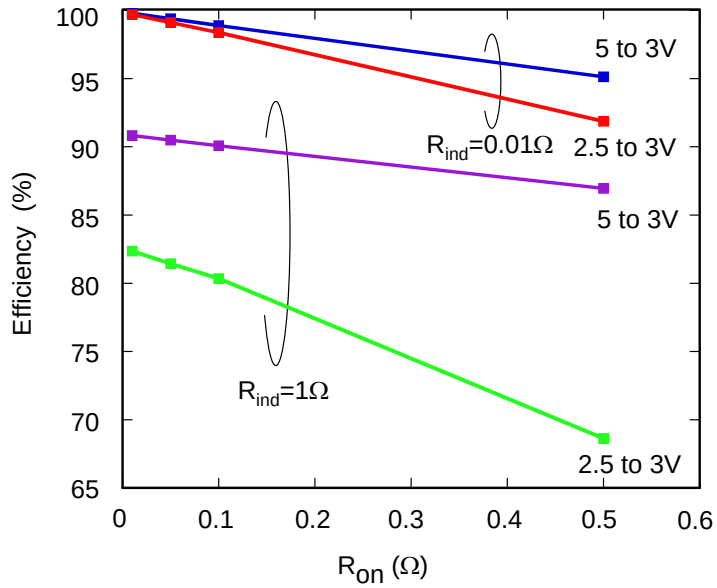

Figure 4. Power efficiencies of the step-down and step-up circuits as a function of R_{on}.

The efficiencies increased when the resistance values (R_{ind} and R_{on}) decreased. When both R_{ind} and R_{on} were 0.01 Ω, the efficiency reached almost 100%.

Next, the dependence of R_L was investigated. The values of R_{ind} and R_{on} were set to 0.01 and 0.05 Ω, respectively. Figure 5a shows the efficiency of the step-down circuit as a function of R_L when the power supply voltage of 5 V was reduced to an output voltage of 4 V. The simulation and theoretical results are shown as solid and dashed lines, respectively, and they were extremely consistent with one another. Figure 5b shows the efficiency of the step-up circuit when the power supply voltage of 2.5 V was increased to the same output voltage of 4 V. The simulation and theoretical values are shown as solid and dashed lines, respectively. They agreed well with one another. When R_L =0.8 Ω, the efficiencies of the step-down and step-up circuits were 93 and 72%, respectively. These efficiencies meant that the energy loss decreased to 1/4. This result shows that the step-down circuit is superior to the step-up circuit for producing the same output voltage of 4 V.

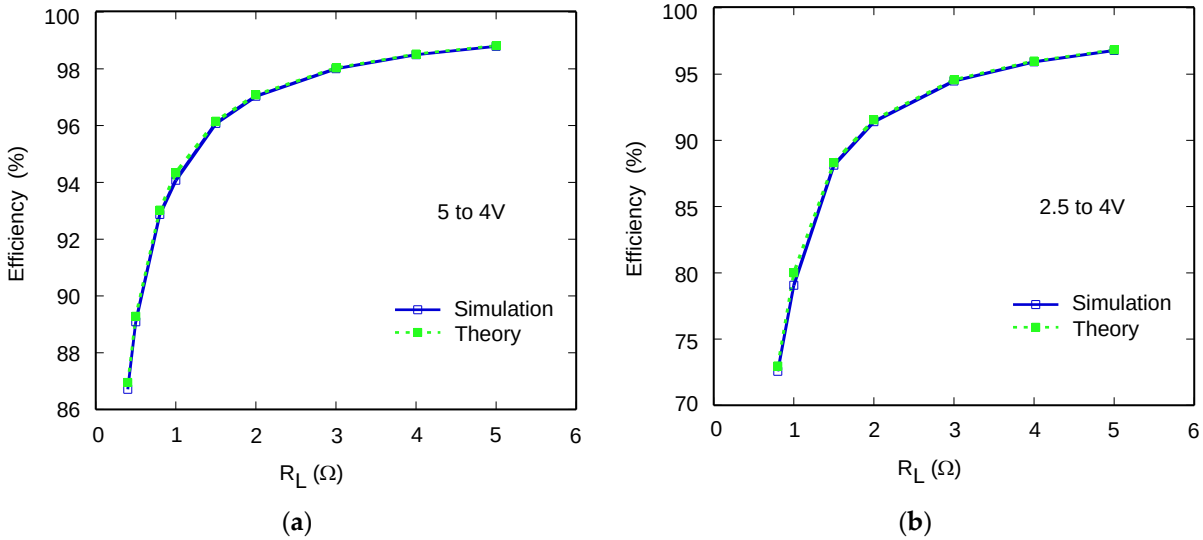

Figure 5. Power efficiency as a function of R_L: (**a**) the step-down circuit; (**b**) the step-up circuit.

Figure 6 shows the simulation results of the efficiencies of the step-down and step-up circuits as a function of R_L with two output voltages of 3 and 4 V. Regarding the step-down circuit, the power supply voltage was set to 5 V. The efficiencies from 5 to 3 V and from 5 to 4 V were consistent with one another. This is well understood using (5). Equation (5) does not include d, which means that η_{dn} is not dependent on d. In other words, η_{dn} is not dependent on the output voltage. Therefore, whether the output voltage was 3 or 4 V, η_{dn} had the same value when R_L was the same.

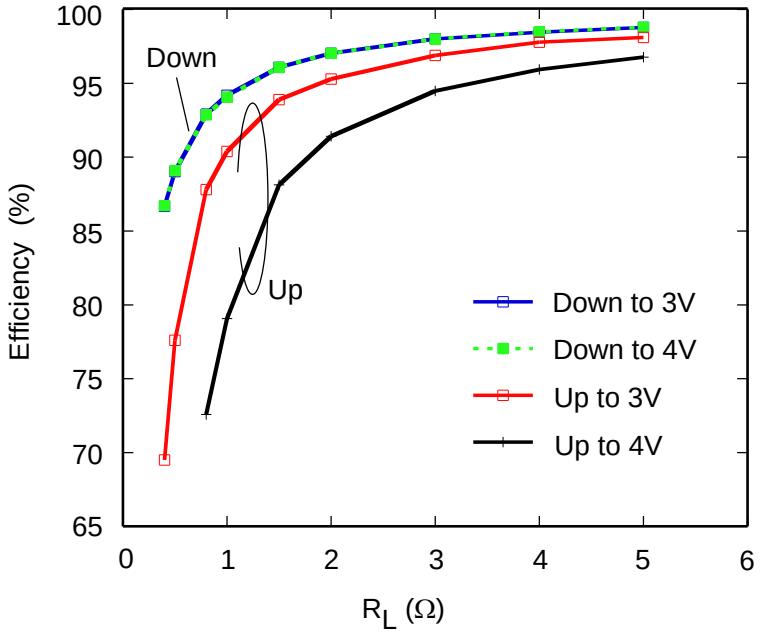

Figure 6. Comparison of power efficiencies between the step-down and step-up circuits as a function of R_L.

Regarding the step-up circuit, the power supply voltage was set to 2.5 V. The simulated efficiency from 2.5 to 4 V was much lower than that from 2.5 to 3 V. This was due to the fact that (6) includes d, which means that η_{up} is dependent on d. When the output voltage increases, d is decreased via the relationship $V_{out} = V_{DD}/d$. Therefore, it is understood from (6) that the theoretical efficiency becomes smaller when the output voltage increases.

3. Experimental Results

Next, the experimental efficiency was measured with a breadboard. Regarding the step-down circuit, a pMOS transistor (2SJ438) and a diode (2GWJ42) were used for S_1 and S_2. As an inductor, a toroidal coil of 100 µH was used. The values of R_L were 12, 20, and 50 Ω. The power supply voltage was 18 V and decreased to an output voltage of 12 V.

Regarding the step-up circuit, the same diode and an nMOS transistor (2SK2231) were used for S_1 and S_2. The same toroidal coil was used as the inductor. As the capacitor, an aluminum electrolytic capacitor was used, where C was 100 µF. The power supply voltage was 8 V and was increased to the same output voltage of 12 V.

To turn the MOS transistor on, a pulse width modulation (PWM) signal was used, which was produced from a microprocessor (PIC16F627A). Using the PIC, the value of d of the pulse could be changed digitally. Figure 7 shows the experimental step-up circuit with a breadboard. In the circuit, the diode and the nMOS transistor were used.

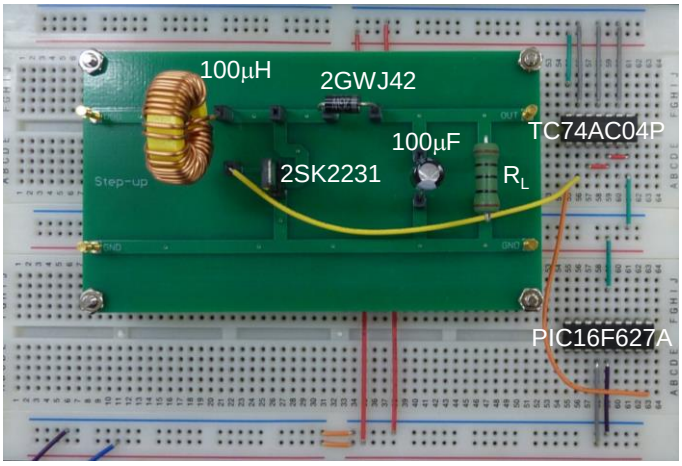

Figure 7. Breadboard of the experimental step-up circuit.

The experimental results are shown as blue lines in Figure 8. When R_L decreased or, in other words, the power consumption increased, the efficiency decreased rapidly. The efficiency of the step-down circuit was larger than that of the step-up circuit when R_L was the same or, in other words, the output power was the same. This was the same characteristic as already discussed in Figure 6. This result showed that discharging from series capacitors with a step-down circuit is superior to discharging from parallel capacitors with a step-up circuit.

Next, we considered the theoretical efficiency using the experimental physical parameters. In (5), R_{on} was assumed to be constant. However, in the step-down experiment, the average resistance of the pMOS and the diode $\overline{R}_{dn}$ had to be considered. The ratio when the pMOS or the diode was turned on was d or $1 - d$, respectively. Therefore, $\overline{R}_{dn}$ was calculated as:

$$\overline{R}_{dn} = dR_{pMOS} + (1 - d)R_D, \tag{7}$$

where dR_{pMOS} and R_D are the on-resistance in the pMOS transistor and the diode resistance, respectively. When R_L was 12, 20, and 50 Ω, i_{RL} was 1.0, 0.6, and 0.24 A, respectively, due to an output voltage of 12 V. These values were calculated from $V_{out} = R_L i_{RL}$. The experimental i_{RL} was well consistent with these values. The values of R_{pMOS} and R_D were calculated with i_{RL} from the equipment datasheets of 2SJ438 and 2GWJ42. Next, we considered the value of d. When the output voltage was 12 V, d could be estimated from the experiment. The values of d at R_L = 12, 20, and 50 Ω were calculated as 0.80, 0.72, and 0.67, respectively. When R_L was comparatively large, such as 50 Ω, it was confirmed that the output voltage of 12 V was consistent with 0.67 × 18 V or, in other words, dV_{DD}. Using d, $\overline{R}_{dn}$ was calculated as 0.172, 0.297, and 0.827 Ω at R_L = 12, 20, and 50 Ω, respectively.

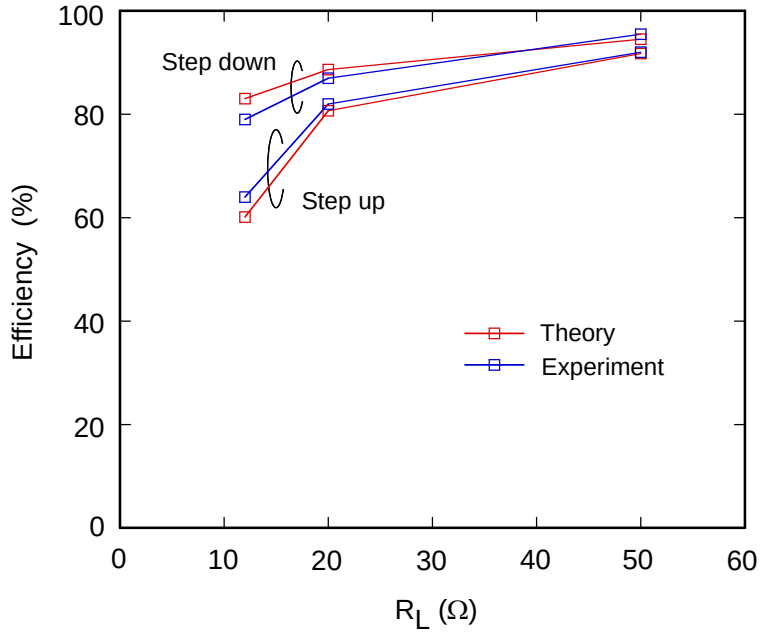

Figure 8. The experimental power efficiencies of the step-down and step-up circuits.

Similarly, in the step-up experiment, the average resistance of the nMOS and the diode $\overline{R}_{up}$ had to be considered. The ratio when the nMOS or the diode was turned on was $1 - d$ or d, respectively. Therefore, $\overline{R}_{up}$ was calculated as:

$$\overline{R}_{up} = (1 - d)R_{nMOS} + dR_D, \tag{8}$$

where R_{nMOS} is the on-resistance in the nMOS transistor. When the output voltage was 12 V, d was also derived from the experiment. The values of d at R_L = 12, 20, and 50 Ω were calculated as 0.40, 0.54, and 0.66, respectively. When R_L was comparatively large, such as 50 Ω, it was confirmed that the output voltage of 12 V was consistent with 8 V/0.67 or, in other words, V_{DD}/d. Using the measured power supply current, which was equal to i, R_{nMOS} and R_D were calculated from the equipment datasheet of 2SK2231 and 2GWJ42. Using these resistance values and d, $\overline{R}_{up}$ was calculated as 0.172, 0.297, and 0.827 Ω at R_L = 12, 20, and 50 Ω, respectively. Inserting $\overline{R}_{dn}$ and $\overline{R}_{up}$ into (5) and (6) instead of R_{on}, the theoretical efficiency could be calculated and is shown as the red lines in Figure 8. These values were almost consistent with the experimental values.

4. Conclusions

In this paper, it is clarified using a theoretical method, circuit simulations, and experiments that discharging series capacitors with a step-down circuit is better than discharging parallel capacitors with a step-up circuit from the aspect of power efficiency.

This circuit can be applied in various situations. For example, an IoT (Internet of Things) society is being realized through innovative sensing technologies. A battery-less energy storage system using supercapacitors is useful for an IoT system. This is because supercapacitors have long service lives with a large number of charge and discharge cycles, and they are maintenance-free. The proposed circuit, which can efficiently charge energy into a supercapacitor and discharge energy from the supercapacitor, will be widely used in the future.

Other applications of supercapacitors are electric cars. They are already being used in electric vehicle hybrid systems and will be widely used in the future, not only for passenger cars and buses, but also for cranes, bulldozers, and excavators.

Capacitors are also useful in overhead wireless trains. Rapid charging systems with raised pantographs at stops will be widespread in the future.

A further important application is the storage of renewable energy, such as wind energy and solar power. Supercapacitors based on carbon elements have an advantage in that they are easier to recycle than battery cells. This means that the mass production of supercapacitors will not encounter major problems related to disposal. In a supercapacitor energy storage system, the highly efficient charge–discharge system based on series–parallel capacitor conversion proposed in this study would be extremely useful.

A future problem is the circuit design of series–parallel capacitor conversion. Whether transistors or mechanical relays should be used as switching devices should be considered in terms of cost, service life, and safety. The number of capacitors for series–parallel conversion was assumed to be two in this study, but it could also be four or more. The number of capacitors or capacitor modules is an issue that should be studied in the future from the perspectives of energy efficiency and circuit design.

By studying these issues, the proposed series–parallel capacitor conversion system is expected to make a significant contribution to solving problems in a wide range of energy fields, from the IoT to power sources for cars and trains and renewable energy storage.

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