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A Novel Non-Isolated Bidirectional DC-DC Converter with Improved Current Ripples for Low-Voltage On-Board Charging

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Abstract: This paper presents a novel single-phase non-isolated bidirectional buck converter topology. The proposed converter uses a basic switching cell structure with a coupled inductor and an interleaving switching scheme. This article addresses a crucial challenge in bidirectional DC-DC conversion by prioritizing reducing output current ripples and minimizing filter inductor size. The employed method includes using MOSFETs with fast recovery diodes to mitigate reverse recovery and body diode losses. Furthermore, the optimization of the switching frequency of the output inductor to be twice the actual switching frequency contributes to reducing the component size of the converter. The coupled inductor also helps to reduce stress on components by distributing currents among its legs. The experimental result demonstrates the proposed converter has a very low ripple current as compared to the conventional converter. The low current ripples and smaller filter inductor size enabled by high-frequency operation have improved the efficiency and size of the converter. A common ground between input and output terminals ensures robust performance without common mode current concerns. Overall, the proposed converter represents a significant improvement in DC-DC converters, promising enhanced efficiency, reliability, and compactness in bidirectional DC-DC conversion systems. In order to verify the performance of the proposed converter, a 460 W buck converter prototype was built and tested.

Keywords: buck converter; coupled inductor; current ripples; bidirectional converter

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Citation: Khan, J.M.; Khan, A.A.; Jamil, M. A Novel Non-Isolated Bidirectional DC-DC Converter with Improved Current Ripples for Low-Voltage On-Board Charging. *Energies* **2024**, *17*, 3570. https://doi.org/10.3390/en17143570

Academic Editor: Miguel Castilla

Received: 13 June 2024
Revised: 10 July 2024
Accepted: 15 July 2024
Published: 20 July 2024

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1. Introduction

The rise in fossil fuel usage has led to significantly increased greenhouse gas emissions, which are the primary cause of global warming. Therefore, sourcing the world's energy needs from clean and renewable energy sources is inevitable. These renewable sources are environmentally sustainable and align with the 2030 Sustainable Development Goals (SDGs) [1].

Renewable energy sources such as photovoltaics, wind power generation, and fuel cells provide a stable voltage to a DC bus through DC-DC converters [2]. These DC-DC converters are further used to charge batteries. DC-DC converters can be categorized into unidirectional and bidirectional. Unidirectional converters allow the flow of current only in one direction, while bidirectional converters allow current flow in both directions, enabling the use of a single converter for both energy transfer and storage applications [3].

Bidirectional DC-DC converters (BDCs) play a pivotal role across various applications such as aerospace power systems, energy storage systems (ESS) in DC micro-grids [4], and electric vehicles (EVs). As already discussed in the existing literature [4,5], BDCs store generated energy in batteries, and in time of need, these converters enable energy transfer from batteries to load. The bidirectional operation of these converters is essential, allowing them to transfer energy in both directions while ensuring voltage stability and efficiency. Moreover, bidirectional converters are integral to electric drive systems, particularly in electric transportation [6], where they fulfill the dual function of stepping up voltage

during power delivery from the source to the motor and stepping down voltage during regenerative braking.

Bidirectional DC-DC converters (BDCs) can be further classified into isolated and non-isolated converters. Isolated converters have electrical isolation for safety, but they can be bulky and costly due to the use of transformers, and they also suffer from high leakage inductance [7]. Non-isolated converters lack galvanic isolation but offer higher efficiency, compact size, and lower cost, making them preferable in many applications [8]. The conventional non-isolated buck/boost bidirectional DC-DC converters are famous for their simple structure and affordability. However, circuit parasitic parameters and the requirement for an extreme duty ratio limit its maximum achievable voltage gain. Additionally, the converter experiences high-voltage stress [7]. These converters also encounter a common issue of high ripple current on the low-voltage (LV) side. This causes the performance of BDC applications involving ESS as the large ripple current negatively impacts battery performance and lifespan [9].

Several conversion techniques are used in BDCs, including multilevel techniques [8,10], cascaded techniques [11,12], voltage multiplier [13], switched-inductor, switched-capacitor [14,15], and coupled-inductor [2,12,16,17].

The multilevel technique improves the voltage conversion ratio and reduces voltage stresses on power switches. However, this method increases the number of switches and the control complexity. Cascaded structures reduce the high-voltage stresses on power switches but result in a lower power density and increased converter cost. Similarly, a switch inductor can lead to low switch stress and high gain, but the difference between the low-voltage side (LVS) and high-voltage side (HVS) can lead to EMI problems [14]. The couple-inductor topologies can increase the gain, but the leakage inductance issue can produce high-voltage spikes on switches and may require additional snubber circuitry [16].

One common issue in the above-mentioned BDCs is the presence of a significant ripple current on the LVS. This ripple current is a problem for battery energy storage systems (BESSs), which are sensitive to such fluctuations. Excessive ripple currents can shorten the lifespan of the BESS [18,19]. To minimize current ripples in converters, several techniques can be used as discussed below:

- One approach is to increase the inductance of the inductors. This reduces the current ripple, but it can slow down the dynamic response, cost, and size of the converter due to the larger inductor size [20].
- Using a large capacitor can solve the ripple issues, but it increases the size and cost of the converter.
- Increasing the switching frequency can help reduce ripple current and allow for smaller inductors. However, the switching frequency increase is constrained by gate drive circuit limitations, switching losses, and electromagnetic compliance requirements.
- Implementing DCM in converters can lower inductor size. However, the higher inductor current in DCM mode increases switch stress, leading to increased power loss.
- The inductor ripple can be reduced by employing the interleaving technique [21]. Although effective, this method increases the number of switches and inductors, thereby complicating control and increasing the converter cost.
- Utilizing cascaded converters with phase shifts can also decrease inductor ripples [19]. However, this approach may raise the complexity and cost due to an increase in the component count. The converter must also operate within a fixed duty cycle.

Each technique for reducing the ripple current in bidirectional DC-DC converters involves trade-offs in performance, complexity, and cost. The choice depends on specific design requirements and constraints. Recent advancements in interleaving DC-DC converters have made them an excellent choice for increased power density and higher efficiency; for example, the authors of [22] discussed the design and modeling of a DC-DC converter using an interleaving technique, and by exploiting the quasi-saturated inductor, the authors reduced the size of the inductor. Similarly, in [23], a more robust nonlinear control technique was devised for an interleaved converter against parameter variations.

While previous studies have examined various non-isolated bidirectional converters, few have focused on using a coupled inductor in a non-isolated DC-DC converter, as shown in our design (Figure 1). This concept, however, has been applied in DC-AC converters [24,25], as well as in AC-AC applications [26]. This observation highlights the versatility and widespread applicability of the mentioned coupled inductor with cell structure topology across various domains within power electronics.

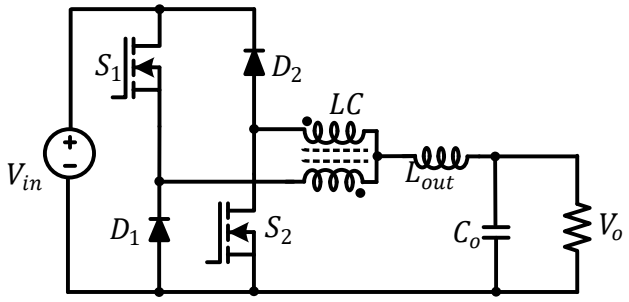


Figure 1. Proposed DC-DC buck converter.

This study addresses the challenge of optimizing voltage reduction while maintaining efficiency and compactness in bidirectional buck converters. We propose a novel design for onboard charging and battery energy storage systems (BESSs), employing coupled inductors and an interleaved PWM scheme for improved efficiency, reduced size, and simplified control. The proposed non-isolated BDC has the following main characteristics:

- Low-output ripple current;
- The inductor operates at twice the switching frequency;
- Reduced inductor size;
- Low-voltage stresses on power switches;
- Common ground between LVS and HVS;
- No additional RC snubber circuit is required;
- No shoot-through or dead time issue;
- Less component count and reduced overall size.

The subsequent sections of this paper delve into the proposed buck converter topology, proposed switching (Section 2), modes of operation (Section 3), ripple current analysis and component selection (Section 4), stress and power loss analysis (Section 5), experimental results (Section 6), and discussion and conclusion in the last section.

2. Proposed Buck Converter Topology and Switching Scheme

2.1. Proposed Topology

The proposed circuit of a non-isolated bidirectional buck DC-DC converter is shown in Figure 1. This converter employs two active switches (S_1, S_2) and two independent diodes (D_1, D_2), a coupled inductor (CL) which is specifically chosen with a coupling factor of $k = 1$, an output filter inductor (L_{out}) and capacitor (C_o). The input source voltage is denoted by V_{in}, and V_o represents the output voltage. The switches operate at a switching frequency of 50 kHz. This circuit configuration offers several benefits. This converter demonstrates reduced output filter inductor (L_{out}) requirements as it experiences double switching frequency and low-voltage stress. Additionally, by utilizing a fundamental switching cell structure, the proposed circuit eliminates the shoot-through and dead-time concerns. Moreover, the circuit features a shared ground, making it well-suited for applications in renewable energies.

2.2. Proposed Switching Scheme

The proposed modulating signals designed for driving the switches are shown in Figure 2. The suggested converter employs an interleaved PWM switching scheme depicted in Figure 2. The switching signals are generated by comparing a DC reference voltage with

two 50 kHz triangular waves (V_{tri1}, V_{tri2}), which are out of phase by 180 degrees. The output signal for triangular wave (V_{tri1}) is fed to a NOT gate to operate Switch S_1. This configuration encompasses both dead time and overlap time operation modes. The duty cycle, as denoted by D, signifies the duration during which S_1 is in the "ON" state within a single switching period (Ts).

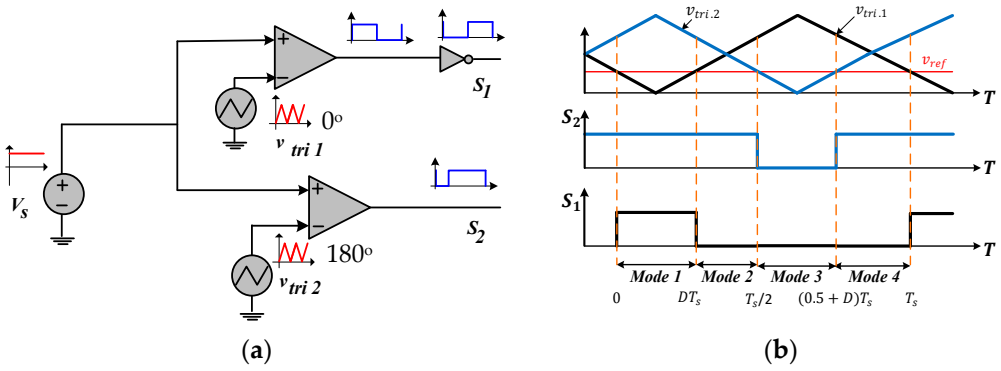


Figure 2. Proposed PWM scheme. (**a**) Switching signal generation; (**b**) switching waveform.

3. Modes of Operation

The suggested converter operates in four different modes as shown in Figure 3. The green bold path in the Figure 3 indicate the current path, the dotted line indicate the common mode current (I_{cm}), the brown doted path indicate the output capacitor current. The system comprises two current components: the output inductor current (I_{out}); the common mode current (I_{cm}), often referred to as circulating current as shown in Figure 4. In this topology, it is assumed that the coupled inductors are identical, and the coupling coefficient, K, is deliberately set to 1, signifying tight coupling. The operation modes are discussed below for a duty ratio greater and less than zero ($D < 0$, $D > 0$). The key simulation waveforms are shown in Figure 5a,b for each duty ration ($D < 0$, $D > 0$). The green color triangular wave (V_{tr1}) and the dotted colored triangular signal (V_{tr2}), which are 180 degree out of phase are compared with a reference voltage indicated by the red line (V_{ref}). The corresponding switching signal (S_1) is generated when the reference voltage is greater than (V_{tr1}), similarlry, switching signal (S_2) is generated when the reference voltage (V_{ref}) is less than (V_{tr2}).

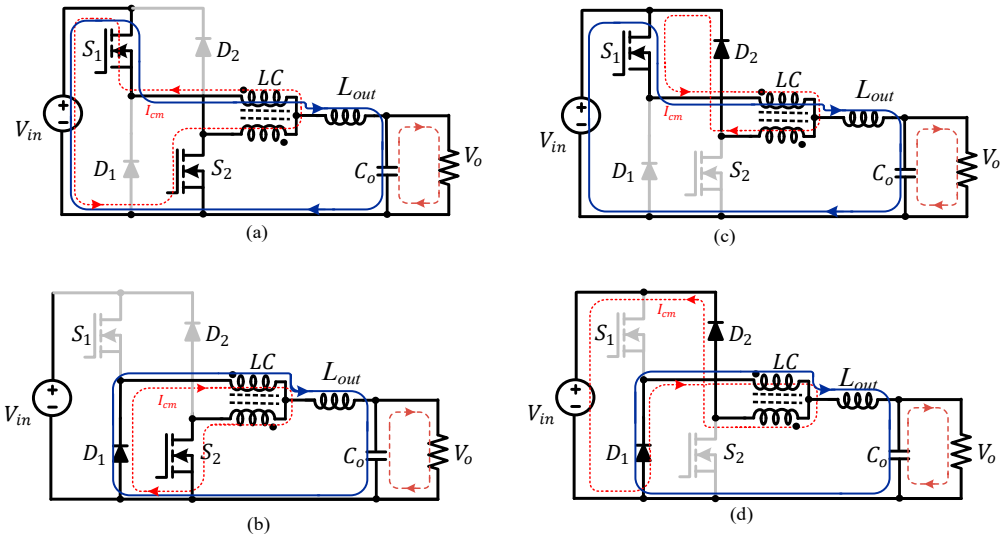


Figure 3. Proposed converter operation modes. (**a**) Mode 1 for $D < 0.5$ and $D > 0.5$. (**b**) Mode 2, Mode 4 for $D < 0.5$. (**c**) Mode 2, Mode 4 for $D > 0.5$. (**d**) Mode 3 for $D < 0.5$ and for $D > 0.5$.

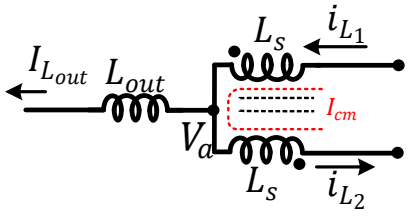


Figure 4. Couple inductor and common mode current.

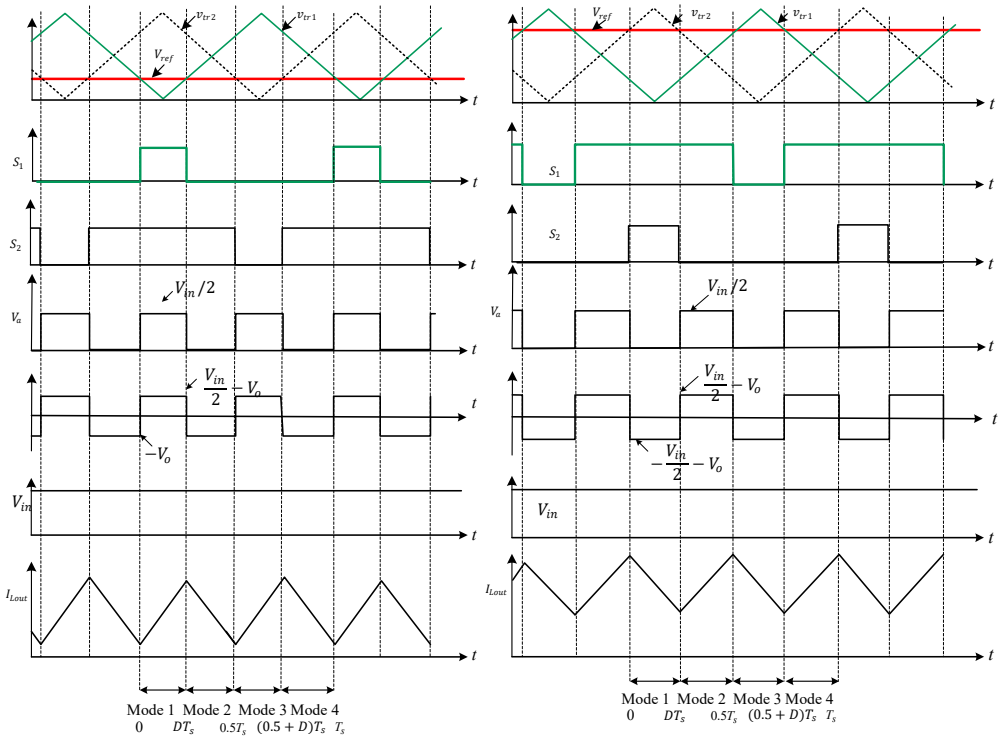


Figure 5. Key simulation waveforms: (**a**) $D < 0.5$; (**b**) $D > 0.5$.

3.1. Operation Mode for D < 0

Mode 1: Mode 1 is shown in Figure 3a. During this mode, switches S_1 and S_2 are both turned ON, and the diodes D_1, and D_2 are reverse-biased. The output inductor (L_{out}) is charged in this mode, and the filter capacitor C_o supplies the output voltage. The voltage and current equations are as follows:

For tight coupling, $k = 1$ and $V_{C_o} = V_o$, and we obtain

$$V_{L_{out}} = \frac{V_{in}}{2} - V_o \tag{1}$$

$$L_{out}\frac{dI_{L_{out}}}{dt} = \frac{V_{in}}{2} - V_o \tag{2}$$

Similarly, the voltage across the coupled inductor is given by

$$V_{L_{out}} = L\frac{dI_{in}}{dt} \tag{3}$$

where L is the inductance of L_1 and L_2.

Mode 2: During this interval, the switch S_1 is turned OFF, and S_2 is ON; the diode D_1 is conducting the circulating current due to freewheeling action, and D_2 remains OFF. Mode 2 is shown in Figure 3b. The voltage and current equations are as follows:

$$V_{L_{out}} = -V_o \tag{4}$$

$$L_{out}\frac{dI_{L_{out}}}{dt} = -V_o \tag{5}$$

Mode 3: During this interval, S_1 and S_2 are turned off, and diodes D_1 and D_2 are conducting as shown in Figure 3d. The voltage and current equation are as follows

$$V_{L_{out}} = \frac{V_{in}}{2} - V_o \tag{6}$$

$$L_{out}\frac{dI_{L_{out}}}{dt} = \frac{V_{in}}{2} - V_o \tag{7}$$

Mode 4: Mode IV is shown in Figure 3b. It is same as Mode II.

3.2. Operation Modes for D > 0

Mode 1: As shown in Figure 3a, Mode I is the same for both $D < 0$ and $D > 0$.

Mode 2: During this interval, the switch S_1 is turned ON and S_2 is OFF, the diode D_2 is conducting the circulating current due to freewheeling action, and D_1 remains OFF. From Figure 3c the equations for voltage and current are the same as Equations (6) and (7)

Mode 3: During this mode, S_1 and S_2 are turned off and diodes D_1 and D_2 are conducting as shown in Figure 3d. Mode III is same for both $D > 0$ and $D < 0$.

Mode 4: Mode IV is the same as Mode II, as indicated in Figure 3c.

The output voltage gain of the proposed buck converter can be obtained by applying the Volt-Sec balance condition on L_{out}, which leads to the following equation:

$$V_o = DV_{in} \tag{8}$$

Equation (8) is the ideal gain equation of the proposed converter. This equation is similar to a conventional buck converter

The non-ideal model of the proposed converter is shown in the Figure 6. To derive the non-ideal gain equation, different non-idealities such as equivalent series resistance (ESR) of inductor r_{la}, ESR of capacitor r_c, switch on-resistance r_{sw}, diode forward resistance r_D, Coupled inductor equivalent series resistance r_{La}, and diode forward voltage drop V_F are considered. The values of these parasitic resistances are very small in comparison to load resistance R.

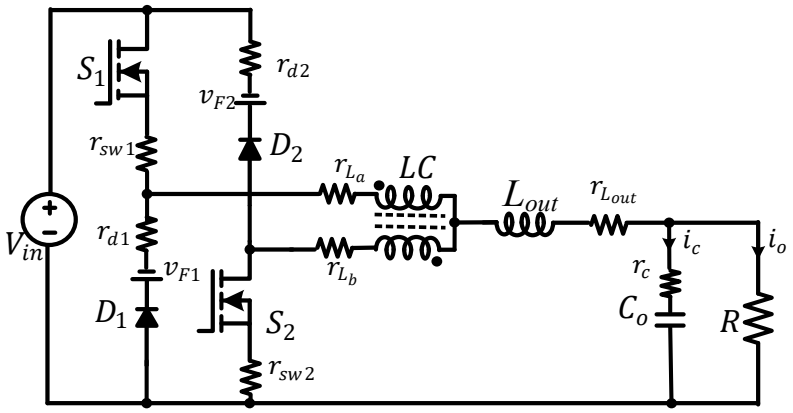


Figure 6. Non-ideal model of the proposed converter.

Since, a negligible current is passing through inductor of the coupled inductor L_b, the ESR of this branch is therefore not considered. The non-ideal gain equation is given by Equation (9)

$$V_{out} = \frac{V_{in}D}{2D\left(1 + \frac{(r_{sw} + r_{la} + r_{Lout})}{R}\right) + 2(0.5 - D)(1 + \frac{r_{L_{out}}}{R})} \tag{9}$$

4. Ripple Current Analysis and Component Selection

In this section, the current ripple magnitudes of the input and coupled inductors are discussed.

4.1. Inductor Design

From Equations (7) and (8), the input inductor equation can be derived as

$$L_{out}\frac{dI_{L_{out}}}{dt} = \frac{(V_{in} - 2V_{out})}{2} \tag{10}$$

From Equation (6)

$$\begin{cases} L_{out} \geq \frac{(V_{in} - 2V_{in}D)DT_s}{2\Delta I} \\ L_{out} \geq \frac{V_{in}\left(D - 2D^2\right)}{2\Delta I f_{sw}} \end{cases} \tag{11}$$

$\Delta I = x\%I_{out}$, with $x\%$ denoting the maximum permissible current ripple (10–20%) for the inductors and $T_s = \frac{1}{f_s}$ is the switching period of the converter

$$L_{out} \geq \frac{V_{in} \cdot D(1 - 2D)}{x\%I_{L_{out}}f_s} \tag{12}$$

Assuming that the ripple inductor current ripple ΔI_{Lout} is equal to the output ripple current ΔI_{out}, since the capacitor draws a negligible current. The output inductance equation L_{out} can be derived using (10) as

$$L_{out} \geq \frac{V_{in}D(1 - 2D)}{x\%I_{out}f_s} \tag{13}$$

The inductor equation can be written in terms of the input voltage by assuming that the converter is lossless; i.e., $P_{out} = P_{in}$. Equation (11) becomes

$$L_{out} \geq \frac{{V_{in}}^2D^2(1 - 2D)}{x\%P_{out}f_s} \tag{14}$$

4.2. Output Inductor Ripple

The current ripple $\Delta I_{L_{out}}$ through the filter inductor L_{out} can be calculated from (11)

$$\Delta I_{L_{out}} = \frac{V_{in}D(1 - 2D)}{L_{out}f_s} \tag{15}$$

From Equation (13), maximum ripples in the inductor current occur at D = 0.25 and $T_s = \frac{1}{f_s}$ is the switching period of the converter.

4.3. Comparison of Current Ripples

The ripple current for the conventional converter can be derived as

$$\Delta I_{conv} = \frac{(V_{in} - V_o)DT_s}{L_{conv}} \tag{16}$$

Using (15) and (16), the ratio of conventional versus proposed induction ripple current ($\Delta I_{conv}/\Delta I_{L_{prop}}$) can be written as

$$\frac{\Delta I_{conv}}{\Delta I_{L_{out}}} = \left| \frac{(1-D)}{(1-2D)} \right| \tag{17}$$

Figure 7 illustrates the current ripple ratio with variations in the duty ratio (D) from 0 to 0.5. As depicted, the ripple current for the conventional buck converter (ΔL_{conv}) is notably larger compared to that of the proposed converter ($L_{in_{conv}}$). For example, when D = 0.47, (ΔI_{conv}) is nearly 10 times greater than the current ripples of the proposed converter ($\Delta I_{L_{out}}$). The graph clearly illustrates that the proposed converter offers a very low ripple current, making it suitable for charging energy storage elements without affecting their health.

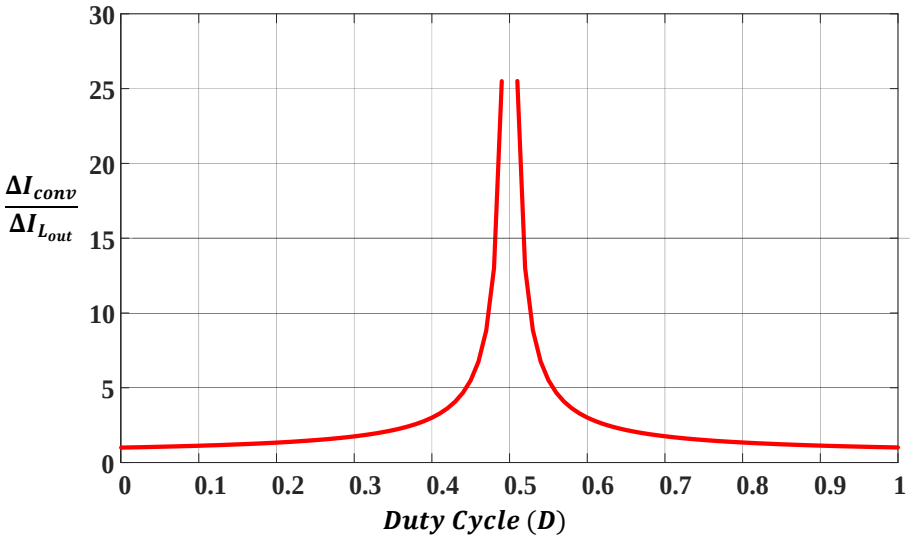


Figure 7. Output current ripple comparison of the proposed and conventional buck converter.

4.4. Couple Inductor Design

The coupled inductance using common mode current from Equation (3) can be written as

$$\begin{cases} \frac{dI_{cm}}{dt} = \frac{V_{in}}{4L_s} \\ dI_{cm} = \frac{dtV_{in}}{4L_s} \end{cases} \tag{18}$$

$$L_s = \frac{V_{in} \times DT_s}{4dI_{cm}} \tag{19}$$

where L_s is self-inductance of the coupled inductor.

$$L_s = L_K + L_m \tag{20}$$

The leakage inductance is considered very small ($L_K \approx 0$), and Equation (20) becomes

$$L_s = L_m \tag{21}$$

Equation (19) can be written as

$$L_m = \frac{V_{in} \times DT_s}{4dI_{cm}} \tag{22}$$

4.5. Output Inductor Comparison

Using Equations (15) and (16), the normalized ratio of the conventional versus proposed output inductance ($\frac{L_{conv}}{L_{prop}}$) can be derived as below.

$$\frac{L_{conv}}{L_{prop}} = \frac{(1-D)}{(1-2D)} \tag{23}$$

Figure 8 illustrates the necessary inductance value for the conventional DC-DC converter for the same current ripple value as observed in the proposed converter, with variations in duty ratio (D) from 0 to 0.5. As depicted, the output inductance for the conventional DC-DC converters ($L_{out.conv}$) is notably larger than that of the proposed converter ($L_{out.prop}$). For example, when D = 0.47, $L_{out.conv}$ is nearly 13.5 times the size of the proposed output inductor.

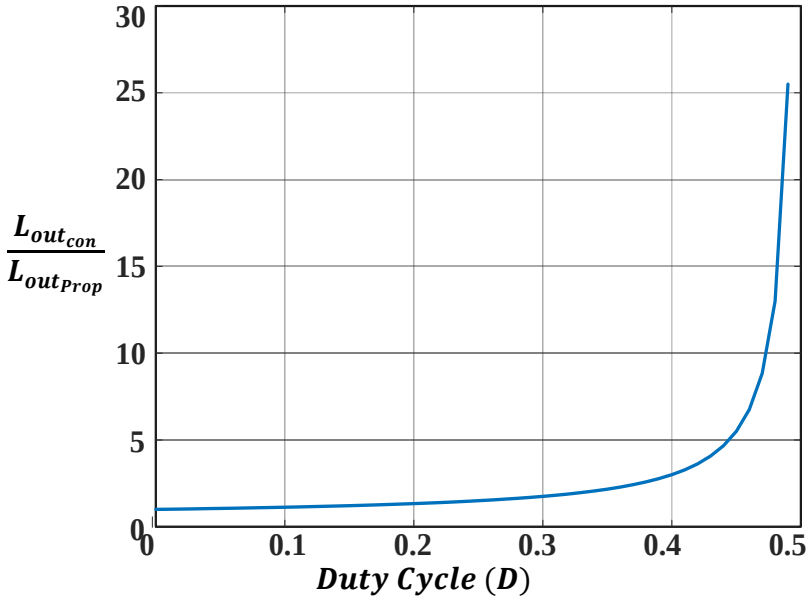


Figure 8. Output inductance comparison of the conventional versus the proposed converter.

5. Stress and Power Loss Analysis

5.1. Voltage and Current Stress

Voltage stress (V_{DS_n}) across switches of the proposed converter is given below

$$V_{DS_n} = V_{in} \tag{24}$$

(24) Shows that the voltage stress across the switches is equal to the input voltage. Similarly, the current stress is the sum of output current ($I_{L\,out}$) and the output inductor ripples.

$$I_{stress} = I_{Lout} + \Delta I_{L_{out}} \tag{25}$$

5.2. Power Loss Analysis

The major contributors to the power dissipation the proposed converter are the conduction losses of the parasitic components and switching losses of the MOSFET. The parasitic components, r_{DS_n}, r_{D_n}, V_{F_n}, r_{L_n}, and r_c are the switch ON-state resistance, the diode's forward resistance, the diode forward drop voltage, the inductor's ESR, and the capacitor's ESR respectively.

The conduction loss of the switches ($P_{con_{sn}}$) can be derived as

$$P_{con_{sn}} = {I_{Sn_{rms}}}^2 \times r_{DS} \tag{26}$$

The switching loss of the switches S_1 and S_2 ($P_{sw_{sn}}$) is given by

$$P_{sw_n} = f_s \times C_{eq} \times \frac{{V_{DS_n}}^2}{2} \tag{27}$$

where f_s is switching frequency, C_{eq} is the constant equivalent capacitance of the switch, and V_{DS_n} is the voltage stress across the switches. From Equation (24), $V_{DS_n} = V_{in}$, (27) can be written as

$$P_{sw_n} = f_s \times C_{eq} \times \frac{{V_{in}}^2}{2} \tag{28}$$

where $I_{Sn_{rms}}$ is the switch rms current, and f_s is the switching frequency. The conduction loss of the diodes ($P_{con_{Dn}}$) is due to r_{D_n} and V_{F_n}. The estimated conduction loss is

$$P_{con_{Dn}} = I_{Dn_{avg}} \times V_{F_n} + {I_{Dn_{rms}}}^2 \times r_{D_n} \tag{29}$$

The conduction losses of the inductors are estimated as

$$P_{con_{Ln}} = {I_{Ln_{rms}}}^2 \times r_{L_n} \tag{30}$$

The conduction losses of the capacitor is given by

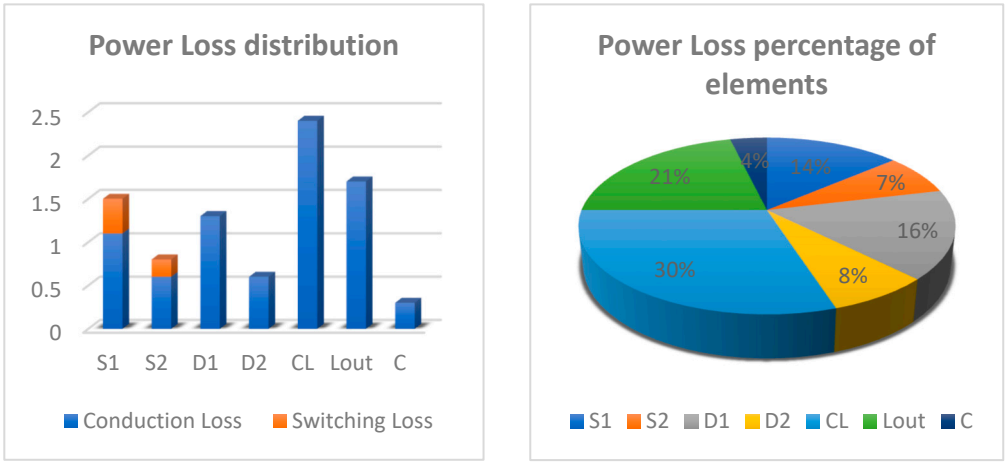
$$P_{con_{Cn}} = {I_{Cn_{rms}}}^2 \times r_{L_n} \tag{31}$$

The inductors also experience core losses in their operation. The core loss inductors are given by

$$\begin{cases} P_{fe(L_{out})} = lm \times Ac \times K \times fe \times {B_{max}}^{\beta} \\ P_{fe(CL)} = lm \times Ac \times Kfe \times {B_{max}}^{\beta} \\ P_{fe(total)} = P_{fe(L_{out})} + P_{fe(CL)} \end{cases} \tag{32}$$

where lm, Ac, Kfe, B_{max}, and β represent the magnetic path length, the core's cross-sectional area, the core loss coefficient, maximum flux density, and the core loss exponent, respectively.

In the experimental works, at an output power of 460 W, the component's power loss breakdown is included to provide a clear analysis of the proposed converter, as shown in Figure 9a. Additionally, Figure 9b illustrates the percentage power loss distribution among the switch, diodes, inductors, and capacitors.



(**a**) (**b**)

Figure 9. Power loss analysis. (**a**) Conduction and switching loss of elements. (**b**) Component-wise percentage loss.

6. Experimental Results and Discussion

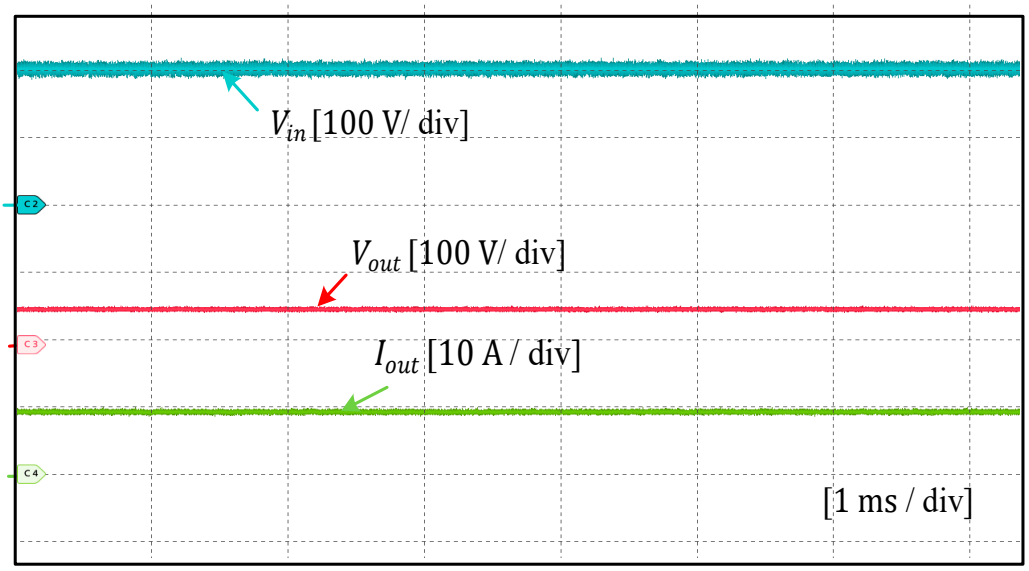
The experimental setup was designed based on the previous analysis. The proposed converter prototype was tested on a 460 W hardware prototype to verify its operations. Table 1 shows the electrical component specifications needed to build the prototype.

Table 1. Component specifications.

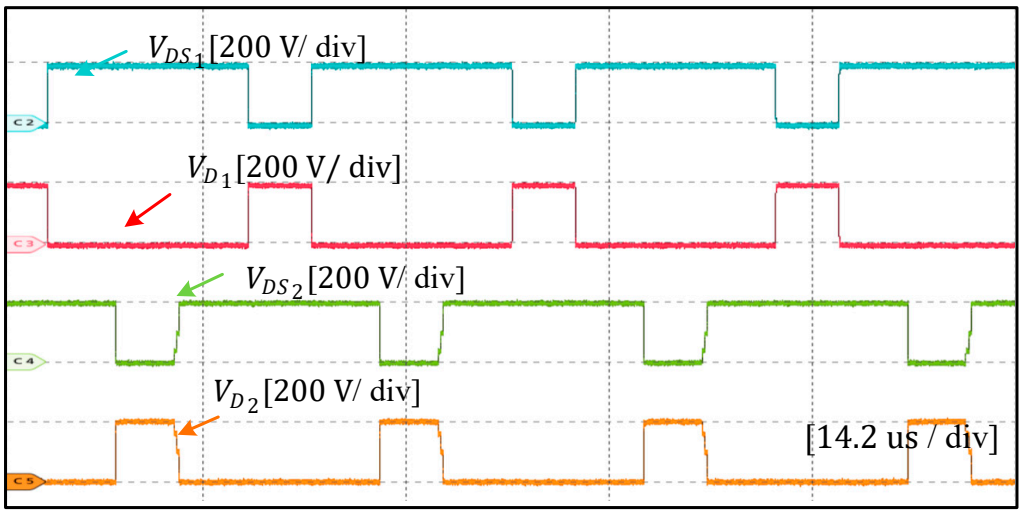
Components	Values
Input voltage (V_{in})	200 V
Output voltage (V_{out})	48 V
Rated output power	460 W
MOSFET (S_1, S_2)	NTHL065N65S3HF (ONSEMI, St.John's, NL, Canada)
Switching frequency	50 Khz
Diodes (D_1, D_2)	BYC30JT-600PSQ
Controller	TMS320F28335
Inductors (L_{out})	0.1 mH
Output Capacitor (C_O)	100 µF

The experimental results were performed with a duty ratio less than 0.5. Figures 10 and 11 illustrate the experimental results obtained with resistive load. Figure 10a show the input voltage (V_{in}), output voltage (V_{out}) and output current (I_{out}) Figure 10b shows the voltage stress across the switches (V_{DS_1}, V_{DS_2}) and diodes (V_{D_1}, V_{D_2}). These results indicate that the voltage stress is equal to the input voltage of the proposed buck converter. Figure 10c shows current stress across the switches and diodes. Figure 11a provides the experimental results of the voltage stress across the switches (V_{DS_1}, V_{DS_2}) and the current through the output inductor ($I_{L_{out}}$). Figure 11b provide an expanded view of Figure 11a; it illustrates that the output inductor ($I_{L_{out}}$) frequency is twice the switching frequency, thus resulting in a lower ripple current. Similarly, Figure 11c simulation results of the output inductor current ($I_{L_{out}}$) along with coupled inductor currents (I_{L_1}, I_{L_2}). Figure 11d provide expanded view of Figure 11c. Furthermore, Figure 12a illustrates the inductor current of the proposed ($I_{L_{Prop}}$) and conventional ($I_{L_{Conv}}$) converter. From Figure 12b, the zoomed-in simulation results, it is evident that the current flowing through the inductor of the proposed converter for the same output voltage is very small compared to that of the conventional converter. Figure 13 shows the experimental result of the inductor's voltages of the proposed and conventional converter ($V_{L_{prop}}$, $V_{L_{Conv}}$). These results clearly show that the voltage across the proposed converter's inductor is minimal compared to the conventional converter. Figure 14 shows the response to the change in the input voltage; when the input voltage is

increased from 200 V to 300 V, the corresponding output voltage and current remain stable. Figure 15 shows the experimental setup of the proposed converter.

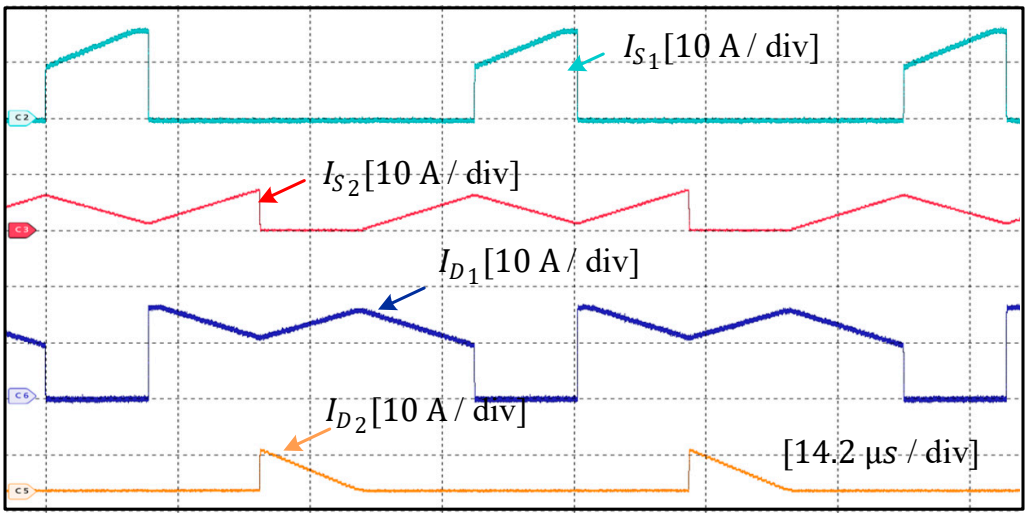


(**a**)



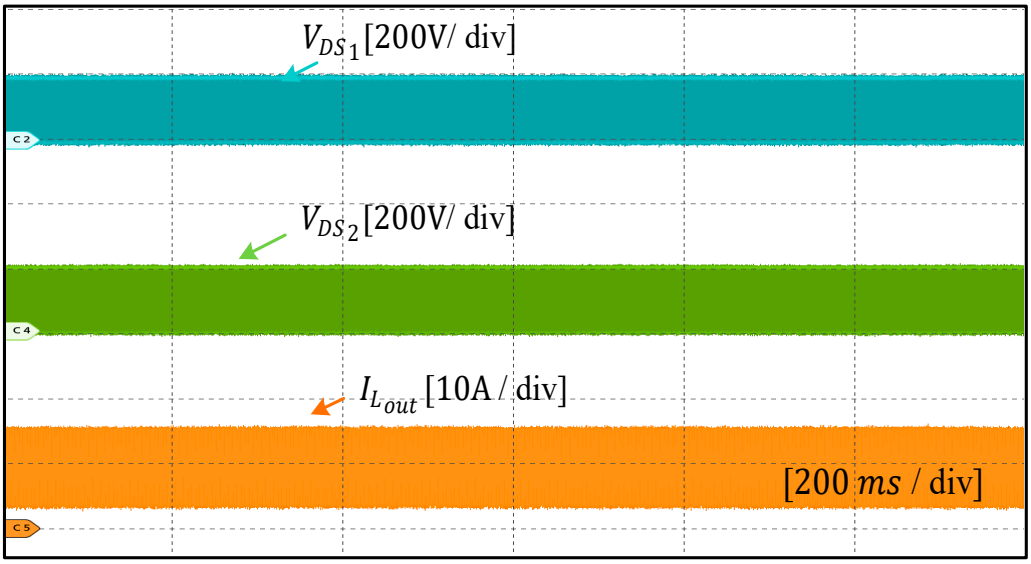
(**b**)

Figure 10. *Cont.*



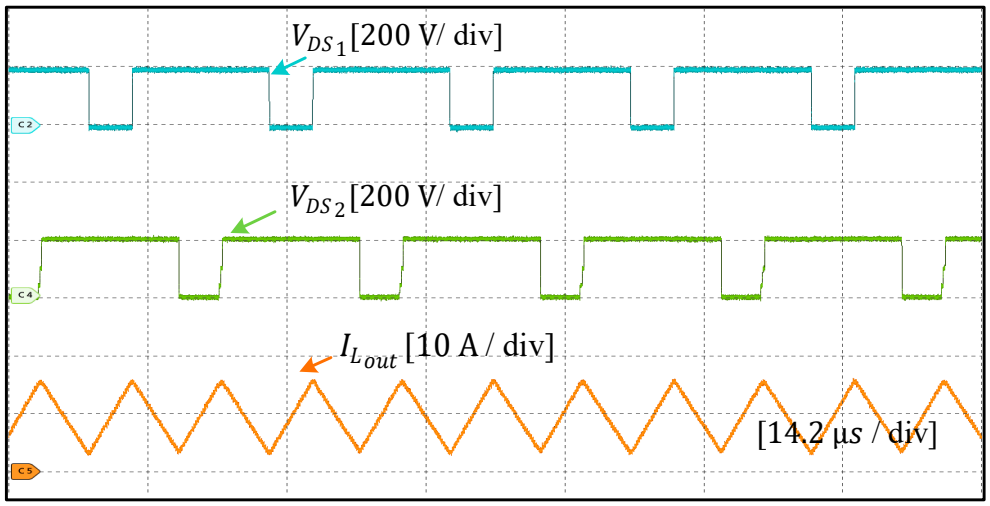
(**c**)

Figure 10. Experimental results: (**a**) Input voltage (V_{in}), output voltage (V_{out}), output current (I_{out}) (**b**) Drain source voltages of switches (V_{DS_1}, V_{DS_2}) and voltage stress across diodes (D_1, D_2). (**c**) Current stress across switches and diodes.

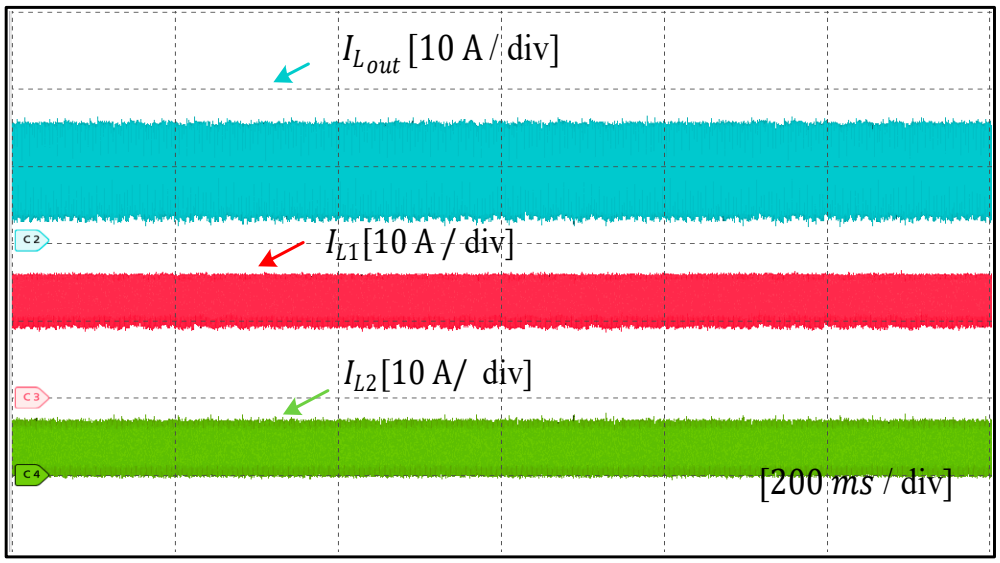


(**a**)

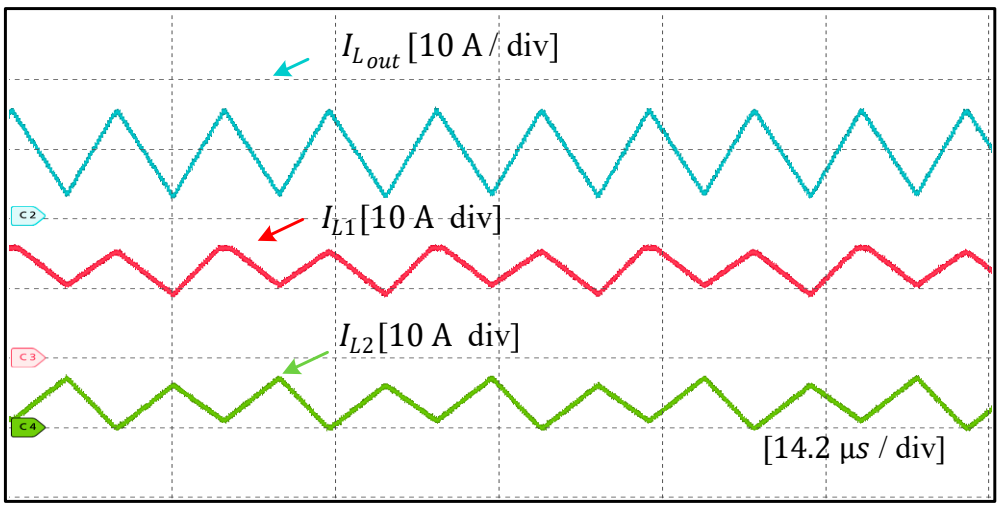
Figure 11. *Cont.*



(**b**)

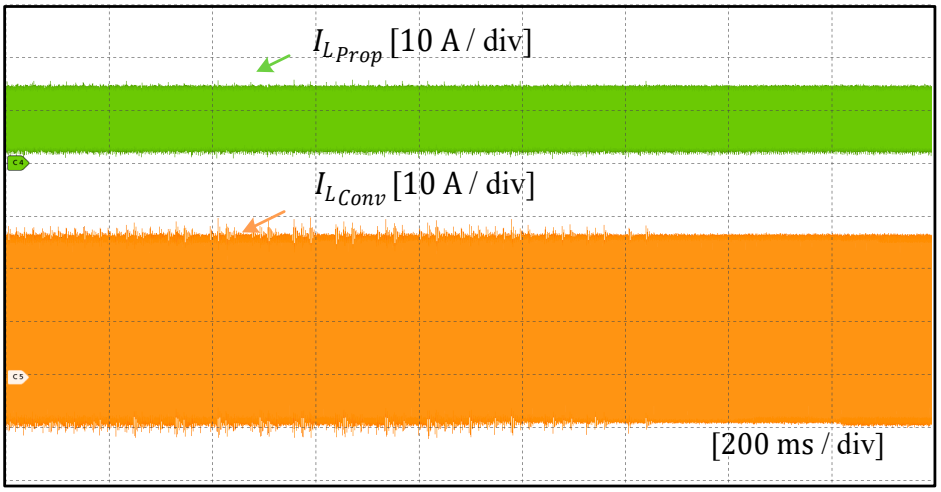


(**c**)

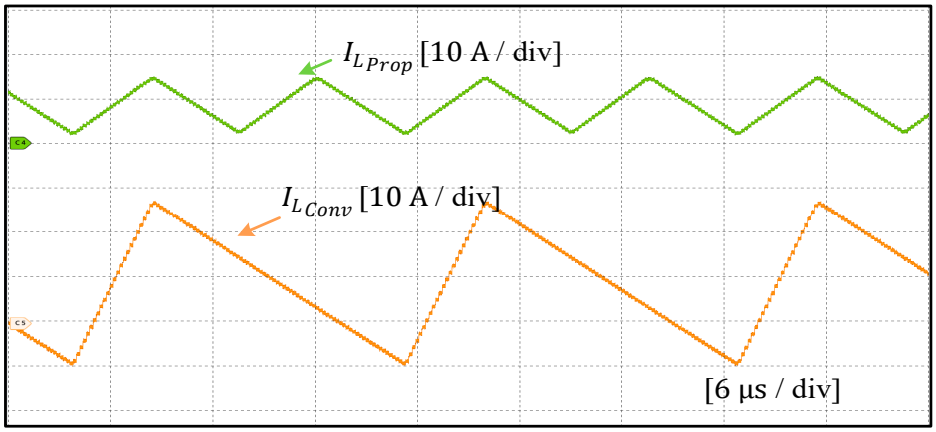


(**d**)

Figure 11. Experimental results. (**a**) Expanded results of the voltages stress (V_{DS_1}, V_{DS_2}) and ($I_{L_{out}}$). (**b**) Zoomed-in simulation results of (**a**). (**c**) Expanded simulation results of $I_{L_{out}}$ and (I_{L_1}, I_{L_2}). (**d**) Zoomed-in simulation results of (**c**).

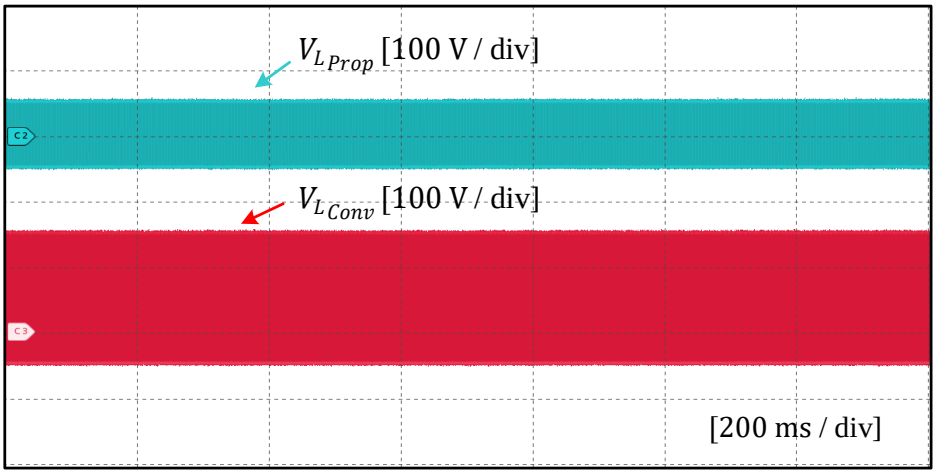


(**a**)



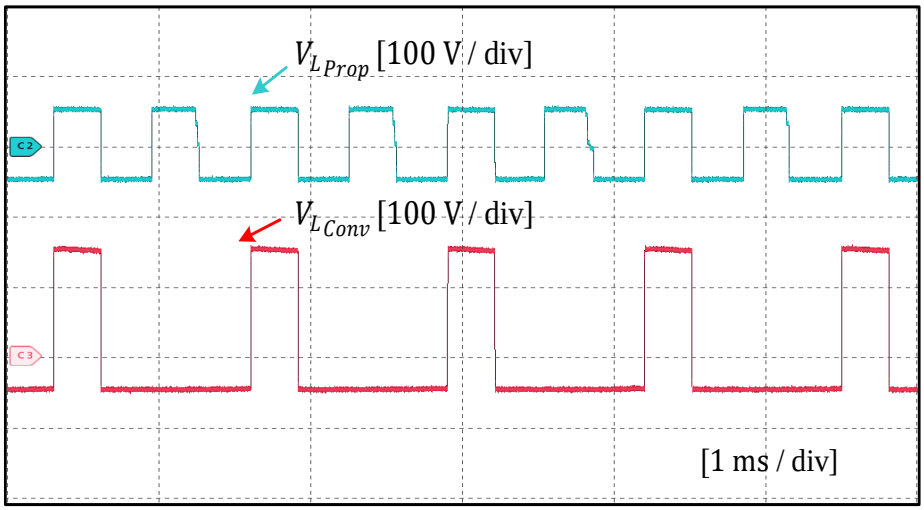
(**b**)

Figure 12. Experiment results. (**a**) Inductor current of the proposed $\left(I_{L_{Prop}}\right)$ and conventional $\left(I_{L_{Conv}}\right)$ converter. (**b**) Zoomed-in results of (**a**).



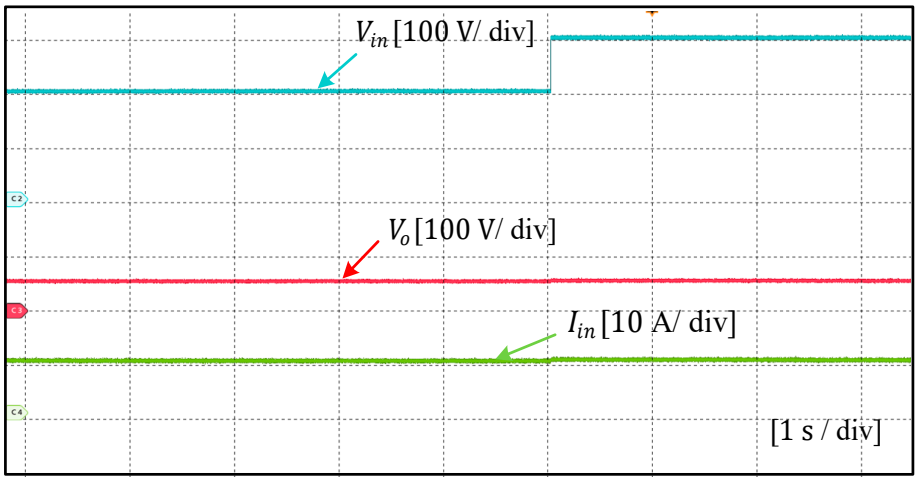
(**a**)

Figure 13. *Cont.*

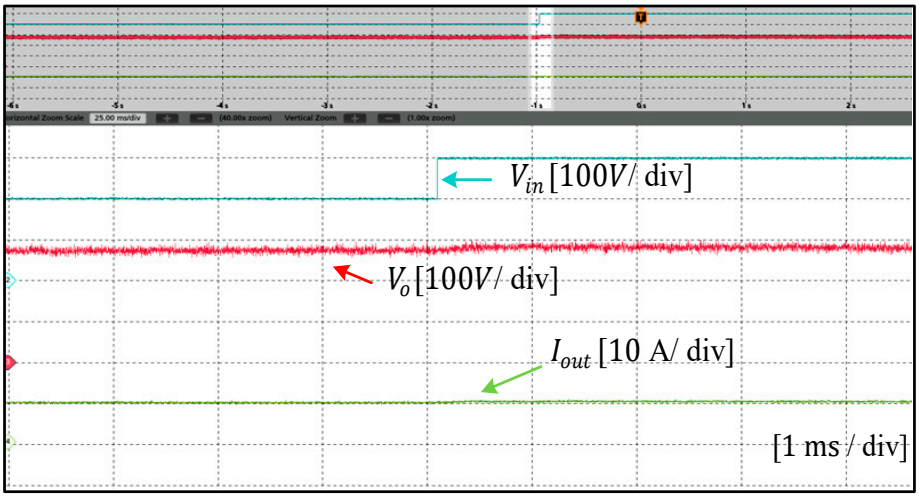


(**b**)

Figure 13. Experimental results. (**a**) Expanded results of inductor voltage of the proposed and conventional converter ($V_{L_{Conv}}$, $V_{L_{Conv}}$). (**b**) Zoomed-in results of (**a**).



(**a**)



(**b**)

Figure 14. Experimental results. (**a**) Expanded results of variations in input voltage vs. output voltage and current. (**b**) Zoomed-in results of (**a**).

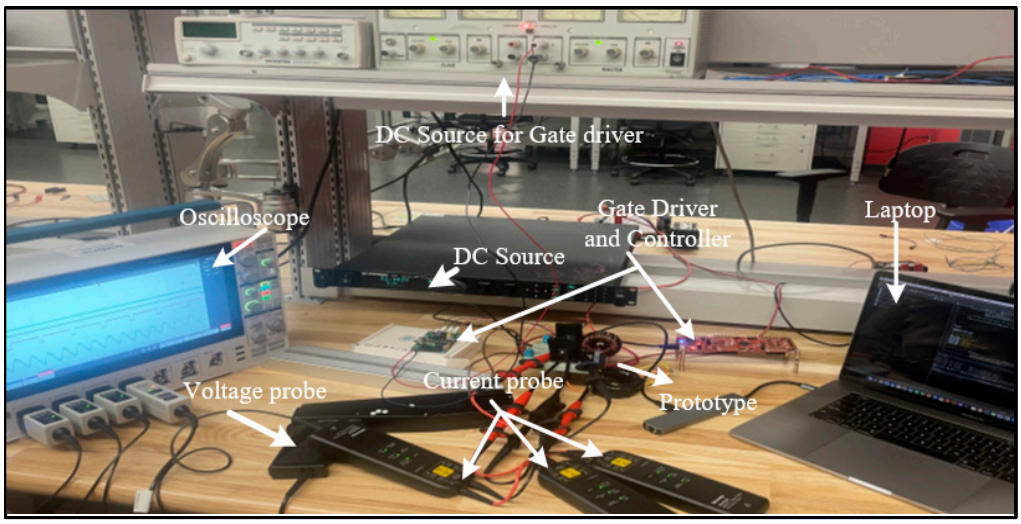


Figure 15. Experimental setup.

7. Conclusions

This article introduces a non-isolated bidirectional DC-DC converter (BDC) designed for battery energy storage systems (BESSs). It thoroughly discusses the converter's operating principles, specifications, and circuit parameter design. The proposed BDC is highlighted for its ability to handle low output currents, minimize component voltage stresses, and maintain a common ground across input and output ports, making it a suitable interface for battery storage applications. Additionally, using a small filter inductor reduces the output current ripple, effectively safeguarding the BESS and extending its operational lifespan. The experimental results illustrating the performance and ripple comparison further validate the effectiveness of this converter for BESS applications.

Author Contributions: Conceptualization, J.M.K. and A.A.K.; Investigation, A.A.K.; Methodology J.M.K.; Funding Acquisition, A.A.K.; Supervision, A.A.K.; Writing—Review and Editing J.M.K., A.A.K. and M.J. All authors have read and agreed to the published version of the manuscript.

Funding: This research was supported by Natural Sciences and Engineering Research Council of Canada (NSERC), Discovery Grant.

Data Availability Statement: The original contributions presented in the study are included in the article, further inquiries can be directed to the corresponding author/s.

Conflicts of Interest: The authors declare that there are no conflicts of interest regarding the publication of this paper.

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