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A Reconfigurable Phase-Shifted Full-Bridge DC–DC Converter with Wide Range Output Voltage

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Abstract: This paper analyzes, designs and implements a reconfigurable phase-shifted full-bridge (PSFB) converter. It adopts the topology of the traditional PSFB converter and incorporates clamping circuits to solve some fundamental problems of conventional topology. In addition, auxiliary switches are employed for output reconfiguration, which allows expanding the output voltage range without compromising the system efficiency. Single pole double throw (SPDT) mechanical switches are used to realize series and parallel connections. In this paper, the characterization of the PSFB converter with clamping circuit and its design considerations are discussed. A 10 kW prototype with a power density of 0.485 W/cm^3, 900 V input voltage and 400/800 V nominal output voltage was manufactured. The experimental results validated the analysis and confirmed the high conversion efficiency for a wide load range; an efficiency of 96.69% was obtained for the full load condition.

Keywords: phase-shifted full-bridge converter; reconfiguration; wide voltage range

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1. Introduction

The phase-shifted full-bridge (PSFB) converter is very attractive for medium- and high-power applications due to its high efficiency and power density [1,2]. It is widely used in many modern industrial fields, such as renewable energy conversion [3,4] and electric vehicle (EV) charging [5]. The phase-shift pulse-width modulation technique provides zero voltage switching (ZVS) in the primary-side switches by introducing a phase-shift angle between the half-bridge legs [6,7]. The traditional PSFB converter features simple structure, natural soft-swiching, isolation capability and simple control. However, it has some well-known drawbacks that need to be resolved, such as narrow ZVS range, circulating current, duty-cycle loss, secondary parasitic oscillation and large output filter [8].

Several modified PSFB converters have been proposed to overcome the aforementioned problems [9–24]. In [9,10], the range of ZVS operation is extended by utilizing the stored energy in passive auxiliary circuits. However, these increase conduction loss and the circulating current cannot be eliminated. In [11,12], passive auxiliary circuits with adaptive ZVS energy reduce conduction loss, but the circulating current still exists. In [13,14], active auxiliary circuits with zero-voltage zero-current switching (ZVZCS) operation are adopted to eliminate the circulating current. In [15,16], the active switches are employed in secondary side and the circulating current is suppressed by adjusting the phase-shifted angle between primary and secondary switches. However, these active auxiliary circuits increase the complexity of the converter due to additional driver circuits. The hybrid-type converters proposed in [17,18] are another solution to remove the circulating current and expand the ZVS range. But many auxiliary components are required, and the improvements of cost and power density are limited. In order to mitigate the voltage oscillation across the rectifier diodes, a resistor–capacitor–diode (RCD) clamp circuit is generally

used [19]. However, it causes considerable losses and reduces the efficiency of the converter. In [20], two clamping diodes on the primary side are employed to clamp the voltage across the secondary side rectifier diodes. But the added diodes cannot eliminate the circulating current. In [21], a capacitor–diode–diode (CDD) clamp circuit is used on the secondary side to reduce the voltage stress on these rectifier diodes. However, a large output capacitor is necessary to cover the large ripple current, which consequently reduces power density. In [22,23], a CDD clamp circuit with center tap of the transformer on the secondary side is employed. This simple clamp mechanism, which is detailed in [24], can solve several drawbacks of the traditional PSFB converter. However, simplified mathematical analysis and conservative design constraints are some shortcomings to be resolved.

PSFB converters are widely used in EV charging applications. Currently, most manufacturers adopt the 400 V battery voltage architecture, but new EV models with 800 V battery voltage architecture are being introduced into the market. Therefore, power electronic converters that operate with extremely wide battery voltage ranges are necessary. In [25,26], the idea of reconfigurable PSFB converters is proposed, where a wide range input and output voltage is realized by controlling several auxiliary switches to enable the series and parallel reconfigurations on the primary and secondary side. In [27], a reconfigurable PSFB converter prototype with RCD snubbers is developed, in which three mechanical switches are employed to realize the series or parallel connection on the secondary side of the converter. Therefore, this paper designs and implements a reconfigurable PSFB converter with CDD clamp circuits, where series and parallel reconfigurations on the secondary side are enabled by two single pole double throw (SPDT) mechanical switches. Furthermore, an extended analysis of the CDD clamp mechanism is elaborated on.

The proposed reconfigurable PSFB converter has reduced complexity compared to state-of-the-art solutions and is primarily designed to provide a wide range output voltage. The paper is organized as follows: Section 2 presents a comprehensive description of the proposed reconfigurable PSFB converter system. Section 3 describes the prototype and discusses the experimental results. Finally, Section 4 presents the study conclusions.

2. Materials and Methods

2.1. Circuit Description

The circuit diagram of the proposed reconfigurable PSFB converter is shown in Figure 1. Two transformers are used, which have a primary winding and a secondary winding with a center tap connected to a CDD clamp circuit. An equivalent series inductance L_{lk} that represents an external series inductance added to the leakage inductance of the transformer is present in the primary sides. In addition, a blocking capacitor C_b is added in the primary sides to eliminate DC current in transformers. The primary sides are connected in parallel and fed by an FB inverter. Each of the secondary sides is connected to an FB rectifier, a CDD clamp circuit and an LC output filter. Two auxiliary switches, S_s and S_p, connect the two secondary sides and enable series and parallel reconfigurations according to their switching states. When S_s is kept ON and S_p is maintained at OFF, the two secondary sides are connected in series. Conversely, when S_p is kept ON and S_s is maintained at OFF, the two secondary sides are connected in parallel.

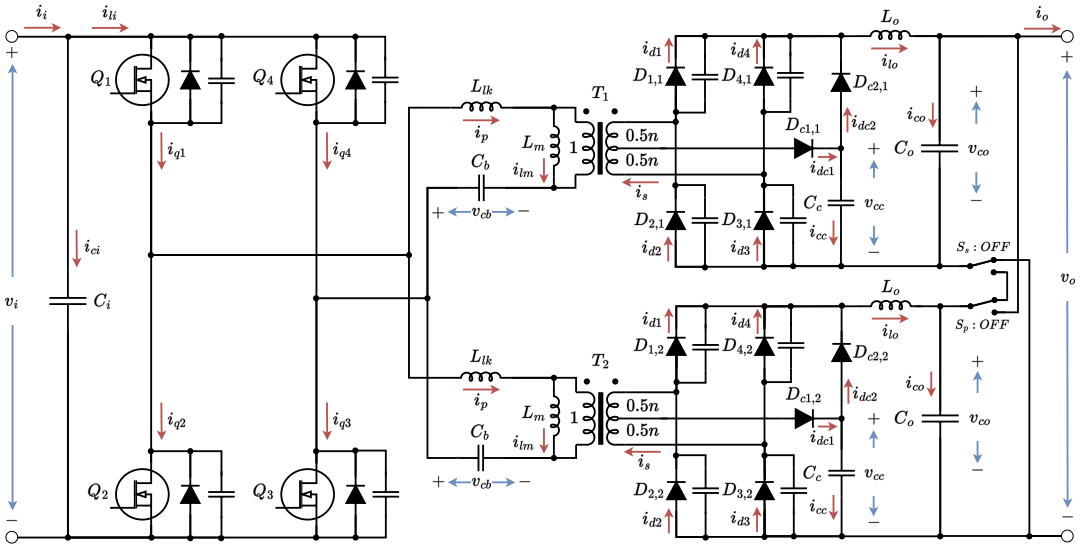


Figure 1. Circuit diagram of the proposed reconfigurable PSFB converter adapted from [28].

2.2. Operation Analysis

The proposed reconfigurable PSFB converter can be seen as equivalent to a traditional PSFB converter with a CDD clamp circuit, being either the series or parallel connection configuration. The equivalent circuit of the proposed reconfigurable PSFB converter is shown in Figure 2. Table 1 lists the equivalent circuit parameters.

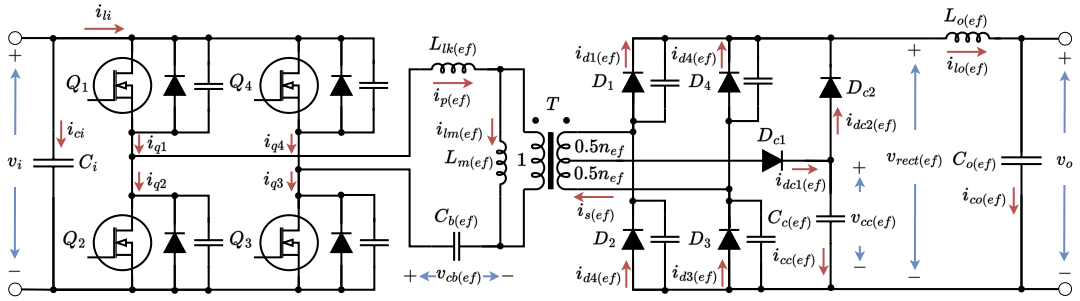


Figure 2. Equivalent circuit of the proposed reconfigurable PSFB converter.

Table 1. Equivalent circuit parameters.

	S_s, S_p	$L_{lk(ef)}$		$L_{m(ef)}$		$C_{b(ef)}$		$i_{p(ef)}$		$i_{lm(ef)}$	
	-	$0.5L_{lk}$		$0.5L_m$		$2C_b$		$2i_p$		$2i_{lm}$	
	S_s, S_p	n_{ef}	$C_{c(ef)}$	$L_{o(ef)}$	$C_{o(ef)}$	$i_{s(ef)}$	$i_{d(ef)}$	$i_{dc(ef)}$	$i_{cc(ef)}$	$v_{cc(ef)}$	$i_{lo(ef)}$
series	1, 0	$2n$	$0.5C_c$	$2L_o$	$0.5C_o$	i_s	i_d	i_{dc}	i_{cc}	$2v_{cc}$	i_{lo}
parallel	0, 1	n	$2C_c$	$0.5L_o$	$2C_o$	$2i_s$	$2i_d$	$2i_{dc}$	$2i_{cc}$	v_{cc}	$2i_{lo}$

The control method is pulse-width modulation with phase-shift. Figure 3 shows the key waveforms of the equivalent circuit in Figure 2. Each switching period T_s is divided into two half-cycles, where each half-cycle is subdivided into ten operation modes. Since the operation modes are symmetrical, only one half-cycle is analyzed. The equivalent operation circuits are shown in Figure 4. In order to analyze the operation modes, the following assumptions are made to simplify analysis: (1) The clamping capacitance $C_{c(ef)}$ is sufficiently large to be treated as a constant voltage source. (2) The output filter inductance $L_{o(ef)}$ is sufficiently large to be treated as a constant current source. (3) The blocking capacitance $C_{b(ef)}$ is sufficiently large to be treated as a negligible constant voltage source. (4) The transformer is ideal, except for its leakage inductance $L_{lk(ef)}$ and magnetizing

inductance $L_{m(ef)}$. (5) MOSFETs Q_1–Q_4 are identical and ideal, except for their output parasitic capacitances C_{oss} and body diodes. (6) The rectifier diodes D_1–D_4 are identical and ideal, except for their junction capacitances. (7) The clamping diodes D_{c1}–D_{c2} are identical and ideal. (8) An external inductor L_{ext} is included into the leakage inductor L_{lk}. In addition, the following notations are described: v_q and i_q are the MOSFET voltage and current, $v_{llk(ef)}$ and $i_{p(ef)}$ are the leakage inductor voltage and current, $v_{lm(ef)}$ and $i_{lm(ef)}$ are the transformer magnetizing voltage and current, $i_{d(ef)}$ is the rectifier diode current, $i_{dc(ef)}$ is the clamping diode current, $v_{cc(ef)}$ and $i_{cc(ef)}$ are the clamping capacitor voltage and current, $v_{rect(ef)}$ is the rectifier output voltage, $v_{cb(ef)}$ is the blocking capacitor voltage, and $v_{lo(ef)}$ and $i_{lo(ef)}$ are the output filter inductor voltage and current, d_e is the effective duty cycle and d is the duty cycle.

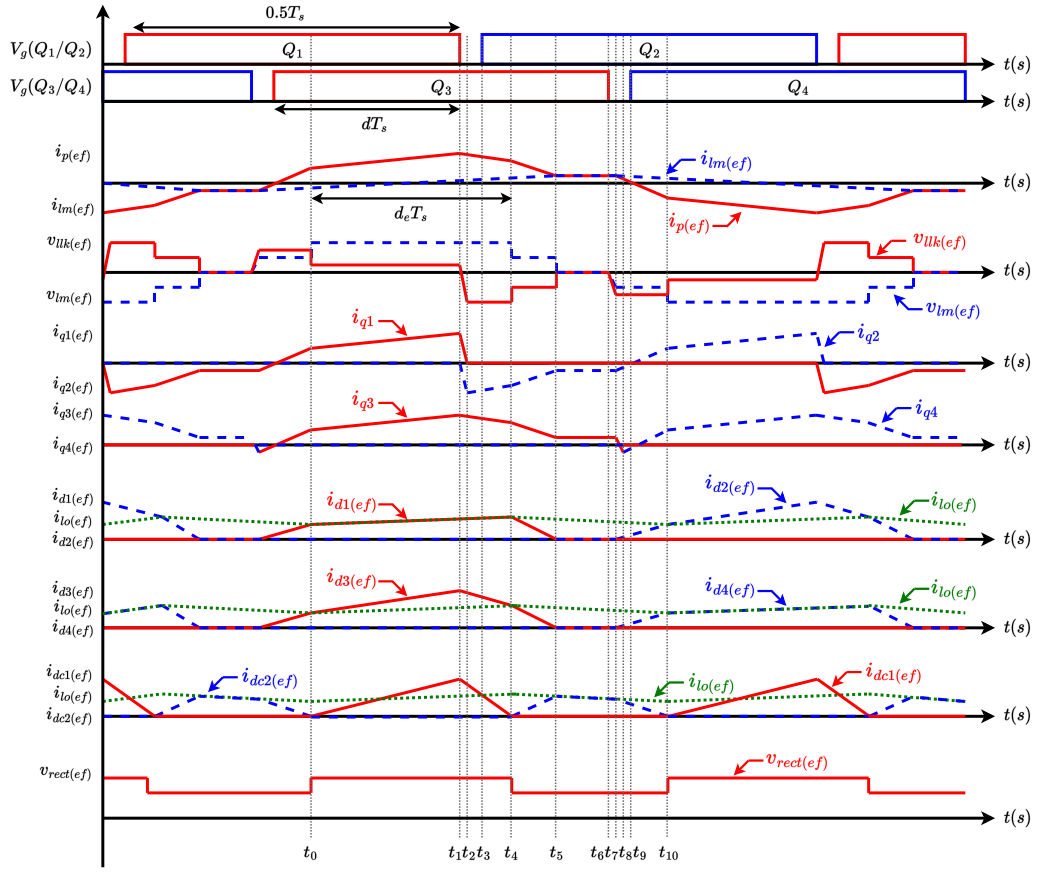


Figure 3. Key waveforms of the equivalent circuit in Figure 2.

Mode 1 ($t_0 - t_1$): This mode starts when D_{c2} is turned off and D_{c1} is turned on. During this interval, the energy is transferred from the input to the output. In addition, $v_{rect(ef)}$ is clamped to $2V_{cc(ef)}$, $v_{llk(ef)}$ is $(n_{ef}V_i - 2V_{cc(ef)})/n_{ef}$, $v_{lm(ef)}$ is $2V_{cc(ef)}/n_{ef}$ and $v_{lo(ef)}$ is $2V_{cc(ef)} - V_o$. Thus, $i_{p(ef)}$, $i_{lm(ef)}$ and $i_{cc(ef)}$ are given as follows:

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_0) + \frac{n_{ef}V_i - 2V_{cc(ef)}}{n_{ef}L_{lk(ef)}}(t - t_0), \tag{1}$$

$$i_{lm(ef)}(t) = i_{lm(ef)}(t = t_0) + \frac{2V_{cc(ef)}}{n_{ef}L_{m(ef)}}(t - t_0), \tag{2}$$

$$i_{cc(ef)}(t) = \frac{i_{p(ef)}(t) - i_{lm(ef)}(t) - n_{ef}I_{lo(ef)}}{0.5n_{ef}}. \tag{3}$$

Mode 2 ($t_1 - t_2$): This mode begins when Q_1 is turned off. During this interval, the parasitic capacitances of Q_1 and Q_2 are charged and discharged by $i_{p(ef)}$. As a result, v_{q1} and v_{q2} are expressed as follows:

$$v_{q1}(t) + v_{q2}(t) = V_i, \tag{4}$$

$$\frac{dv_{q1}(t)}{dt} - \frac{dv_{q2}(t)}{dt} = \frac{i_{p(ef)}(t = t_1)}{C_{oss}}. \tag{5}$$

Mode 3 ($t_2 - t_3$): This mode starts when the body diode of Q_2 is turned on. Here, the freewheel period is started. In addition, the energy is transferred from the primary side to the secondary side. Furthermore, $v_{llk(ef)}$ is $-2V_{cc(ef)}/n_{ef}$. Thus, $i_{p(ef)}$ is given as follows:

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_2) - \frac{2V_{cc(ef)}}{n_{ef}L_{lk(ef)}}(t - t_2). \tag{6}$$

Mode 4 ($t_3 - t_4$): This mode begins when Q_2 is turned on with ZVS. During this interval, Q_2 begins to operate in the third quadrant [29].

Mode 5 ($t_4 - t_5$): This mode starts when D_{c2} is turned on and D_{c1} is turned off. During this interval, $v_{rect(ef)}$ is clamped to $V_{cc(ef)}$, $v_{llk(ef)}$ is $-V_{cc(ef)}/n_{ef}$, $v_{lm(ef)}$ is $V_{cc(ef)}/n_{ef}$ and $v_{lo(ef)}$ is $V_{cc(ef)} - V_o$. As a result, $i_{p(ef)}$, $i_{lm(ef)}$ and $i_{cc(ef)}$ are expressed as follows:

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_4) - \frac{V_{cc(ef)}}{n_{ef}L_{lk(ef)}}(t - t_4), \tag{7}$$

$$i_{lm(ef)}(t) = i_{lm(ef)}(t = t_4) + \frac{V_{cc(ef)}}{n_{ef}L_{m(ef)}}(t - t_4), \tag{8}$$

$$i_{cc(ef)}(t) = -\frac{n_{ef}I_{lo(ef)} + i_{lm(ef)}(t) - i_{p(ef)}(t)}{n_{ef}}. \tag{9}$$

Mode 6 ($t_5 - t_6$): This mode begins when $i_{p(ef)}$ reaches $i_{lm(ef)}$. During this interval, the turn-off process of the rectifier diodes is initiated, where $v_{rect(ef)}$ is clamped to $V_{cc(ef)}$. Here, the stored energy in C_c is transferred to the output. In addition, $v_{llk(ef)}$ and $v_{lm(ef)}$ are 0. Thus, $i_{p(ef)}$, $i_{lm(ef)}$ and $i_{cc(ef)}$ are given as follows:

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_5) = i_{lm(ef)}(t = t_5), \tag{10}$$

$$i_{lm(ef)}(t) = i_{lm(ef)}(t = t_5) = i_{p(ef)}(t = t_5), \tag{11}$$

$$i_{cc(ef)}(t) = -I_{lo(ef)}. \tag{12}$$

Mode 7 ($t_6 - t_7$): This mode starts when Q_3 is turned off. During this interval, the parasitic capacitances of Q_3, Q_4 and D_1–D_4 are charged and discharged. Here, L_m participates in the charge and discharge resonance process. Thus, v_{q3} and v_{q4} are expressed as follows:

$$v_{q3}(t) + v_{q4}(t) = V_i, \tag{13}$$

$$\frac{dv_{q3}(t)}{dt} - \frac{dv_{q4}(t)}{dt} = \frac{i_{p(ef)}(t = t_6)}{C_{oss}}. \tag{14}$$

Mode 8 ($t_7 - t_8$): This mode begins when D_2 and D_4 are turned on. During this interval, the output parasitic capacitances of Q_3 and Q_4 are charged and discharged by $i_{p(ef)}$. In addition, $v_{lm(ef)}$ is $-V_{cc(ef)}/n_{ef}$. As a result, v_{q3}, v_{q4}, $i_{p(ef)}$, $i_{lm(ef)}$ and $i_{cc(ef)}$ are given as follows:

$$v_{q3}(t) = \frac{V_{cc(ef)}}{n_{ef}} + z_o i_{p(ef)}(t = t_7) \sin \omega_o (t - t_7), \tag{15}$$

$$v_{q4}(t) = V_i - v_{q3}(t), \tag{16}$$

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_7)\cos\omega_o(t - t_7), \tag{17}$$

$$i_{lm(ef)}(t) = i_{lm(ef)}(t = t_7) - \frac{V_{cc(ef)}}{n_{ef}L_{m(ef)}}(t - t_7), \tag{18}$$

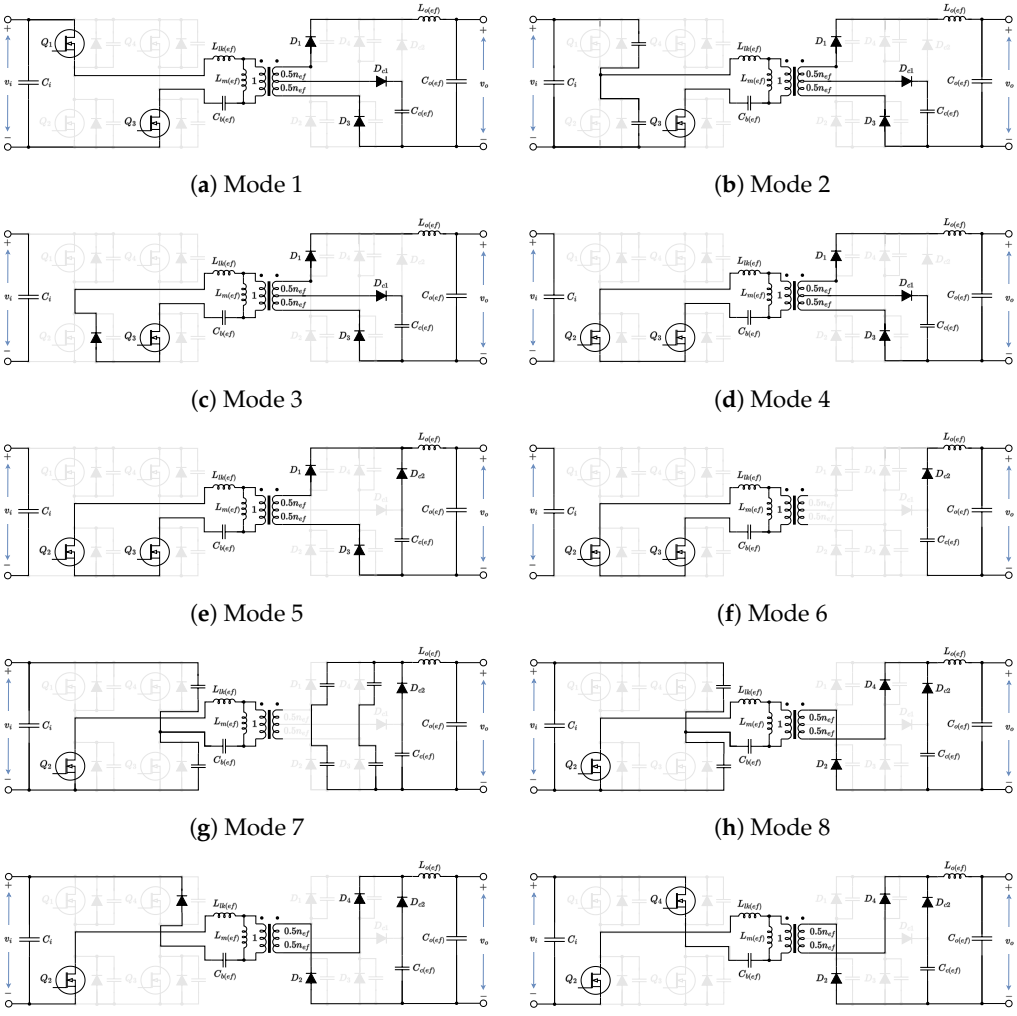
$$i_{cc(ef)}(t) = -\frac{n_{ef}I_{lo(ef)} - i_{lm(ef)}(t) + i_{p(ef)}(t)}{n_{ef}}, \tag{19}$$

where $z_o = \sqrt{0.5L_{lk(ef)}/C_{oss}}$ and $\omega_o = 1/\sqrt{2L_{lk(ef)}C_{oss}}$.

Mode 9 ($t_8 - t_9$): This mode starts when the body diode of Q_4 is turned on. Here, the freewheel period is ended. In addition, a portion of the stored energy is returned to the input. Furthermore, $v_{llk(ef)}$ is $-(n_{ef}V_i - V_{cc(ef)})/n_{ef}$. Thus, $i_{p(ef)}$ is given as follows:

$$i_{p(ef)}(t) = i_{p(ef)}(t = t_8) - \frac{n_{ef}V_i - V_{cc(ef)}}{n_{ef}L_{lk(ef)}}(t - t_8). \tag{20}$$

Mode 10 ($t_9 - t_{10}$): This mode begins when Q_4 is turned on with ZVS. During this interval, Q_4 begins to operate in the third quadrant. In addition, the energy is transferred from the input to the output.



(**a**) Mode 1 (**b**) Mode 2

(**c**) Mode 3 (**d**) Mode 4

(**e**) Mode 5 (**f**) Mode 6

(**g**) Mode 7 (**h**) Mode 8

(**i**) Mode 9 (**j**) Mode 10

Figure 4. Operation modes of the equivalent circuit in Figure 2.

2.3. Steady-State Analysis

In order to simplify the mathematical analysis, the time intervals of the modes that describe the switching processes of the primary-side switches are neglected.

Since $i_{cc(ef)}(t = t_4)$ is 0, then from (7) to (11) the time interval $t_4 - t_5$ can be obtained as follows:

$$t_{4\to5} = t_5 - t_4 = \frac{I_{lon(ef)}}{V_{cn(ef)}} T_s. \tag{21}$$

where $I_{lon(ef)} = n_{ef} L_{lk(ef)} f_s I_{lo(ef)} V_i^{-1}$ is the normalized output filter inductor current, $V_{cn(ef)} = L_n V_{cc(ef)} n_{ef}^{-1} V_i^{-1}$ is the normalized clamping capacitor voltage, and $L_n = 1 + L_{lk(ef)} L_{m(ef)}^{-1}$ is the inductance factor.

From (1) to (3), (18) to (20), and since $i_{cc(ef)}(t = t_0)$ is 0, the time interval $t_8 - t_{10}$ can be expressed as follows:

$$t_{8\to10} = t_{10} - t_8 = \frac{I_{lon(ef)}}{1 - V_{cn(ef)}} T_s. \tag{22}$$

As $t_4 - t_0 = D_e T_s$, from (1) to (3) and (6) to (9), the time intervals $t_0 - t_1$ and $t_1 - t_4$ can be obtained as follows:

$$t_{0\to1} = t_1 - t_0 = 2 D_e V_{cn(ef)} T_s, \tag{23}$$

$$t_{1\to4} = t_4 - t_1 = D_e (1 - 2 V_{cn(ef)}) T_s. \tag{24}$$

From (21) to (24), the time interval $t_5 - t_8$ can be expressed as follows:

$$t_{5\to8} = t_8 - t_5 = \left(0.5 - D_e - \frac{I_{lon(ef)}}{V_{cn(ef)} (1 - V_{cn(ef)})} \right) T_s. \tag{25}$$

From (3), (9), (12) and (19), and by using the capacitor charge balance principle, the clamping capacitor voltage can be obtained as follows:

$$0 = \alpha_3 V_{cn(ef)}^3 - \alpha_2 V_{cn(ef)}^2 + \alpha_1 V_{cn(ef)} - \alpha_0. \tag{26}$$

where $\alpha_3 = 2\sigma_1^2 + \sigma_2$, $\alpha_2 = 5\sigma_1^2 - 3\sigma_1 + 2\sigma_2$, $\alpha_1 = 2\sigma_1^2 + 2(\sigma_1 - 1)^2 + \sigma_2$, $\alpha_0 = (\sigma_1 - 1)^2 + \sigma_1$, $\sigma_1 = D I_{lon(ef)}^{-1}$, and $\sigma_2 = I_{lon(ef)}^{-1}$. The unique real solution of Equation (26) is obtained considering that $V_{cn(ef)} < D < 0.5$. Thus, the clamping capacitor voltage is obtained by solving (26) and calculated as $V_{cc(ef)} = n_{ef} V_{cn(ef)} V_i L_n^{-1}$.

Then, by using the inductor volt-second balance principle, the voltage gain, defined as $M_{ef} = V_o n_{ef}^{-1} V_i^{-1}$, is obtained as follows:

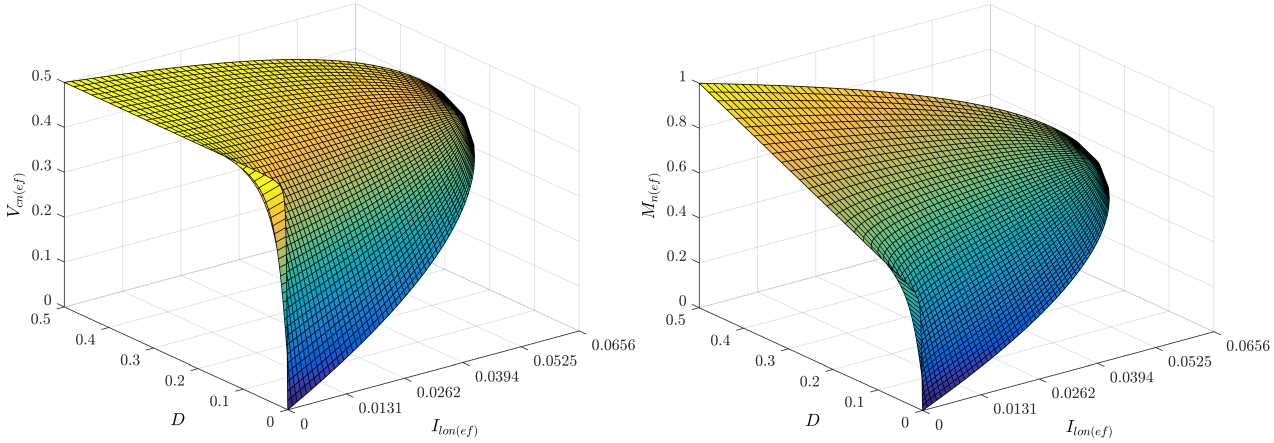
$$M_{n(ef)} = V_{cn(ef)} (2 D_e + 1). \tag{27}$$

where $M_{n(ef)} = L_n M_{ef}$ is the normalized voltage gain. Thus, the voltage gain is calculated as $M_{ef} = L_n^{-1} M_{n(ef)}$.

Finally, as $D T_s = t_{0\to1} + t_{8\to10}$, the effective duty cycle can be expressed as follows:

$$D_e = \frac{0.5}{V_{cn(ef)}} \left(D - \frac{I_{lon(ef)}}{1 - V_{cn(ef)}} \right). \tag{28}$$

The relationship surfaces of $V_{cn(ef)}$ and $M_{n(ef)}$ according to D and $I_{lon(ef)}$ are illustrated in Figure 5. An increase in $I_{lon(ef)}$ reduces the available operating range of $V_{cn(ef)}$ and $M_{n(ef)}$ to their limiting value of 0.0656. Conversely, a decrease in $I_{lon(ef)}$ increases the available operating range. However, smaller values and narrower variations of D are required to guarantee a wide operating range of the converter.



(**a**) Normalized clamping capacitor voltage (**b**) Normalized voltage gain

Figure 5. Relationship surfaces according to D and $I_{lon(ef)}$ adapted from [28].

2.4. Electrical Stress

In Figure 3, the maximum magnetizing current $i_{lm(ef),max}$, the maximum clamping capacitor current $i_{cc(ef),max}$, and the maximum primary current $i_{p(ef),max}$ are given by

$$i_{lm(ef),max} = n_{ef} I_{lo(ef)} \zeta_d;\ \zeta_d = \frac{V_i D}{2 f_s L_{m(ef)} L_n n_{ef} I_{lo(ef)}}, \tag{29}$$

$$i_{cc(ef),max} = \varepsilon I_{lo(ef)};\ \varepsilon = \frac{4 D_e V_{cn(ef)} (1 - 2V_{cn(ef)})}{I_{lon(ef)}}, \tag{30}$$

$$i_{p(ef),max} = n_{ef} I_{lo(ef)} \zeta_b;\ \zeta_b = \left(1 + \frac{(1 - L_n)(1 - 2V_{cn(ef)})}{2L_n(1 - V_{cn(ef)})} + \frac{(1 + L_n - 4V_{cn(ef)})}{L_n I_{lon(ef)} D_e^{-1} V_{cn(ef)}^{-1}} \right). \tag{31}$$

Then, the primary current $i_{p(ef)}$ at $t = t_0$ and $t = t_4$ can be expressed as follows:

$$i_{p(ef)}(t = t_0) = n_{ef} I_{lo(ef)} \zeta_a;\ \zeta_a = \left(\zeta_b - \frac{2 D_e V_{cn(ef)} (L_n - 2V_{cn(ef)})}{L_n I_{lon(ef)}} \right), \tag{32}$$

$$i_{p(ef)}(t = t_4) = n_{ef} I_{lo(ef)} \zeta_c;\ \zeta_c = \left(\zeta_b - \frac{2 D_e V_{cn(ef)} (1 - 2V_{cn(ef)})}{L_n I_{lon(ef)}} \right), \tag{33}$$

Furthermore, the current stresses on the components can be calculated. Table 2 summarizes the current stresses in the components of the equivalent circuit in Figure 2. In Table 2, $I_{q(ef),1th}$ and $I_{q(ef),3th}$ are the MOSFET currents on the first and third quadrant, $I_{q(ef),lag}$ and $I_{q(ef),lead}$ are the MOSFET currents on the leading and lagging legs, $I_{d(ef),up}$ and $I_{d(ef),dw}$ are the rectifier diode currents on the lower and upper diodes of the FB rectifier.

Table 2. Current stresses in the components of the equivalent circuit in Figure 2.

	Variable	Value
Q	$I_{q(ef),1th,lag,rms}$	$n_{ef} I_{lo(ef)} \sqrt{\frac{1}{3T_s} \left(\frac{\zeta_b^3 - \zeta_a^3}{\zeta_b - \zeta_a} t_{0\to1} + \frac{\zeta_a^3 + \zeta_d^3}{\zeta_a + \zeta_d} t_{8\to10} \right)}$
	$I_{q(ef),1th,lead,rms}$	$n_{ef} I_{lo(ef)} \sqrt{\frac{1}{3T_s} \left(\frac{\zeta_b^3 - \zeta_a^3}{\zeta_b - \zeta_a} t_{0\to1} + \frac{\zeta_b^3 - \zeta_c^3}{\zeta_b - \zeta_c} t_{1\to4} + \frac{\zeta_c^3 - \zeta_d^3}{\zeta_c - \zeta_d} t_{4\to5} + 3\zeta_d^2 t_{5\to8} + \frac{\zeta_a^3 + \zeta_d^3}{\zeta_a + \zeta_d} t_{8\to10} \right)}$
	$I_{q(ef),3th,lag,rms}$	$n_{ef} I_{lo(ef)} \sqrt{\frac{1}{3T_s} \left(\frac{\zeta_b^3 - \zeta_c^3}{\zeta_b - \zeta_c} t_{1\to4} + \frac{\zeta_c^3 - \zeta_d^3}{\zeta_c - \zeta_d} t_{4\to5} + 3\zeta_d^2 t_{5\to8} \right)}$
	$I_{q(ef),3th,lead,rms}$	0

Table 2. *Cont.*

	Variable	Value
D	$I_{d(ef),up,avg}$	$I_{lo(ef)}\frac{1}{2T_s}(2D_eT_s + t_{4\to5} + t_{8\to10})$
	$I_{d(ef),up,rms}$	$I_{lo(ef)}\sqrt{\frac{1}{T_s}(D_eT_s + \frac{t_{4\to5}}{3} + \frac{t_{8\to10}}{3})}$
	$I_{d(ef),dw,avg}$	$0.5I_{lo(ef)}$
	$I_{d(ef),dw,rms}$	$I_{lo(ef)}\sqrt{\frac{1}{T_s}(0.5T_s + \frac{\varepsilon^2D_eT_s}{3} + \frac{t_{4\to5}}{3} + t_{5\to8} + \frac{t_{8\to10}}{3})}$
D_c	$I_{dc1(ef),avg}$	$\varepsilon I_{lo(ef)}D_e$
	$I_{dc1(ef),rms}$	$\varepsilon I_{lo(ef)}\sqrt{\frac{2D_e}{3}}$
	$I_{dc2(ef),avg}$	$\varepsilon I_{lo(ef)}D_e$
	$I_{dc2(ef),rms}$	$I_{lo(ef)}\sqrt{\frac{2}{T_s}(\frac{t_{4\to5}}{3} + t_{5\to8} + \frac{t_{8\to10}}{3})}$
C_c	$I_{cc(ef),rms}$	$I_{lo(ef)}\sqrt{\frac{2}{T_s}(\frac{\varepsilon^2D_eT_s}{3} + \frac{t_{4\to5}}{3} + t_{5\to8} + \frac{t_{8\to10}}{3})}$
C_b	$I_{cb(ef),rms}$	$n_{ef}I_{lo(ef)}\sqrt{\frac{2}{3T_s}(\frac{\zeta_b^3-\zeta_a^3}{\zeta_b-\zeta_a}t_{0\to1} + \frac{\zeta_b^3-\zeta_c^3}{\zeta_b-\zeta_c}t_{1\to4} + \frac{\zeta_c^3-\zeta_d^3}{\zeta_c-\zeta_d}t_{4\to5} + 3\zeta_d^2t_{5\to8} + \frac{\zeta_a^3+\zeta_d^3}{\zeta_a+\zeta_d}t_{8\to10})}$
T	$I_{p(ef),rms}$	$n_{ef}I_{lo(ef)}\sqrt{\frac{2}{3T_s}(\frac{\zeta_b^3-\zeta_a^3}{\zeta_b-\zeta_a}t_{0\to1} + \frac{\zeta_b^3-\zeta_c^3}{\zeta_b-\zeta_c}t_{1\to4} + \frac{\zeta_c^3-\zeta_d^3}{\zeta_c-\zeta_d}t_{4\to5} + 3\zeta_d^2t_{5\to8} + \frac{\zeta_a^3+\zeta_d^3}{\zeta_a+\zeta_d}t_{8\to10})}$
	$I_{s(ef),rms}$	$I_{lo(ef)}\sqrt{\frac{1}{T_s}(0.5T_s + (\frac{\varepsilon^2}{3}+1)D_eT_s + \frac{2t_{4\to5}}{3} + t_{5\to8} + \frac{2t_{8\to10}}{3})}$

2.5. Parameter Design

2.5.1. Leakage Inductance

The necessary and sufficient condition to guarantee the sequence of operating modes is $t_{5\to8} > 0$. From this, the design condition of the leakage inductance is derived as follows:

$$0 = x_{ilo}^3 + \gamma_2 x_{ilo}^2 + \gamma_1 x_{ilo} + \gamma_0, \tag{34}$$

$$L_{lk(ef)} \le \frac{V_i I_{lon(ef),sol}}{n_{ef} f_s I_{lo(ef)}}. \tag{35}$$

where $\gamma_2 = 4y_m^2 - 3.5y_m$, $\gamma_1 = 0.875y_m^4 - 0.625y_m^3 - 1.25y_m^2 + y_m$, $\gamma_0 = 0.25y_m^2(y_m-1)^3$, $I_{lon(ef),sol} = \min\{x_{ilo,min}, x_{ilo,max}\}$, $x_{ilo,min}$ and $x_{ilo,min}$ are the real solutions in (34) for $M_{n(ef),min}$ and $M_{n(ef),max}$, and $M_{n(ef),min}$ and $M_{n(ef),max}$ are the minimum and maximum normalized voltage gains to be designed.

2.5.2. Magnetizing Inductance

From (15) to (17), the condition to achieve ZVS on the lagging leg is given by:

$$\frac{1}{2}L_{lk(ef)}i_{lm(ef),max}^2 \ge C_{oss}\left(V_i - \frac{V_{cc(ef)}}{n_{ef}}\right)^2. \tag{36}$$

Then, the design condition of the magnetizing inductance is obtained as follows:

$$L_{m(ef)} \le \frac{z_o L_n D}{2f_s(L_n - V_{cn(ef)})}. \tag{37}$$

2.5.3. Output Filter Inductance

In Figure 2, The output filter inductor current ripple can be expressed as follows:

$$\Delta i_{lo(ef)} = \frac{(2V_{cc(ef)} - V_o)D_e}{L_{o(ef)}f_s}. \tag{38}$$

Given a maximum value of current ripple in the output filter inductor $\Delta i_{lo(ef),max}$ to be designed, the design condition of the output filter inductance is derived as follows:

$$L_{o(ef)} \geq \frac{(2V_{cc(ef)} - V_o)D_e}{\Delta i_{lo,max} f_s}. \tag{39}$$

2.5.4. Clamping Capacitance

In Figure 2, The clamping capacitor voltage ripple can be obtained as follows:

$$\Delta v_{cc(ef)} = \frac{i_{cc(ef),max} D_e}{2 f_s C_{c(ef)}}. \tag{40}$$

In order to avoid clipping in current waveforms due to clamping capacitor voltage ripple saturation, the condition $V_{cc(ef)} + 0.5\Delta v_{cc(ef)} < 0.5 n_{ef} V_i$ must be fulfilled. From this, the design condition of the clamping capacitance can be expressed as follows:

$$C_{c(ef)} \geq \frac{i_{cc(ef),max} D_e}{2 f_s (n_{ef} V_i - 2V_{cc(ef)})}. \tag{41}$$

2.5.5. Input Filter Capacitance

In Figure 2, the input filter capacitor voltage ripple can be approximated as follows:

$$\Delta v_{ci} \approx \frac{i_{p(ef),max} D(1-D)^2}{2 f_s C_i}. \tag{42}$$

Given a maximum value of voltage ripple in the input filter capacitor $\Delta v_{ci,max}$ to be designed, the design condition of the input filter capacitance is derived as follows:

$$C_i \geq \frac{i_{p(ef),max} D(1-D)^2}{2 f_s \Delta v_{ci,max}}. \tag{43}$$

2.5.6. Output Filter Capacitance

In Figure 2, the output filter capacitor voltage ripple can be expressed as follows:

$$\Delta v_{co(ef)} = \frac{\Delta i_{lo(ef)}}{8 f_s C_{o(ef)}}. \tag{44}$$

For a maximum value of voltage ripple in the output filter capacitor $\Delta v_{co(ef),max}$ to be designed, the design condition of the output filter capacitance is obtained as follows:

$$C_{o(ef)} \geq \frac{\Delta i_{lo(ef)}}{8 f_s \Delta v_{co(ef),max}}. \tag{45}$$

2.5.7. Blocking Capacitance

In Figure 2, the blocking capacitor voltage ripple can be obtained as follows:

$$\Delta v_{cb(ef)} = \frac{n_{ef} I_{lo(ef)} \Gamma_{cb}}{2 f_s C_{b(ef)}}. \tag{46}$$

where $\Gamma_{cb} = ((\zeta_a + \zeta_b)t_{0\to1} + (\zeta_b + \zeta_c)t_{1\to4} + (\zeta_c + \zeta_d)t_{4\to5} + 2\zeta_d t_{5\to8} + (\zeta_a - \zeta_d)t_{8\to10}) f_s$. For a maximum value of voltage ripple in the blocking capacitor $\Delta v_{cb(ef),max}$ to be designed, the design condition of the blocking capacitance is derived as follows:

$$C_{b(ef)} \geq \frac{n_{ef} I_{lo(ef)} \Gamma_{cb}}{2\Delta v_{cb(ef),max} f_s}. \tag{47}$$

2.5.8. Dead Time

From (4) to (5) and (15) to (17), The dead time conditions required to ensure ZVS in both the lagging and leading legs are determined as follows:

$$\Delta t_{dt,lead} \geq \frac{2C_{oss} V_i}{i_{p(ef),max}}, \tag{48}$$

$$\Delta t_{dt,lag} \geq \frac{2C_{oss} V_{cc(ef)}}{n_{ef} i_{lm(ef),max}} + \frac{1}{\omega_o} \arcsin\left(\frac{n_{ef} V_i - V_{cc(ef)}}{n_{ef} z_o i_{lm(ef),max}}\right). \tag{49}$$

2.6. Transient-State Analysis

The dynamic model is obtained from the average model. From the principle of charge balance and volt-second balance, the large signal average model is given by:

$$\left\langle \frac{d i_{lo(ef)}(t)}{dt} \right\rangle_{T_s} = \frac{(2v_{cc(ef)}(t) - v_{co(ef)}(t)) d_e(t) - (v_{co(ef)}(t) - v_{cc(ef)}(t)) d'_e(t)}{0.5 L_{o(ef)}}, \tag{50}$$

$$\left\langle \frac{d v_{cc(ef)}(t)}{dt} \right\rangle_{T_s} = \frac{i_{lo(ef)}(t)(\varepsilon(t) d_e(t) T_s - (d'_e(t) T_s + t_{5\to 8}(t)))}{C_{c(ef)} T_s}. \tag{51}$$

where $d'_e(t) = 0.5 - d_e(t)$. From (50) and (51), the variables are defined as $x_i(t) = X_i + \tilde{x}_i$, where X_i is the average value and $\tilde{x}_i$ is the small signal disturbance. Then, the small signal average model can be expressed as follows:

$$L_{o(ef)} \frac{d\tilde{i}_{lo(ef)}(t)}{dt} = \gamma_{vcc} \tilde{v}_{cc(ef)} + \gamma_{de} \tilde{d}_e - \tilde{v}_{co(ef)}, \tag{52}$$

$$C_{c(ef)} \frac{d\tilde{v}_{cc(ef)}(t)}{dt} = \lambda_{ilo} \tilde{i}_{lo(ef)} + \lambda_{vcc} \tilde{v}_{cc(ef)} + \lambda_{de} \tilde{d}_e + \lambda_{vi} \tilde{v}_i. \tag{53}$$

where $\lambda_{vi} = I_{lo(ef)} V_i^{-1} \{I_{lon(ef)} (1 - V_{cn(ef)})^{-2} - 8V_{cn(ef)}^2 D_e^2 I_{lon(ef)}^{-1}\}$, $\gamma_{de} = 2V_{cc(ef)}$, $\lambda_{ilo} = 2D_e - 1 + 2I_{lon(ef)} V_{cn(ef)}^{-1} (1 - V_{cn(ef)})^{-1}$, $\lambda_{de} = I_{lo(ef)} \{16(0.5 - V_{cn(ef)}) V_{cn(ef)} D_e I_{lon(ef)}^{-1} + 2\}$, $\lambda_{vcc} = I_{lo(ef)} V_{cn(ef)} V_{cc(ef)}^{-1} \{8(0.5 - 2V_{cn(ef)}) D_e^2 I_{lon(ef)}^{-1} - I_{lon(ef)} (1 - 2V_{cn(ef)}) V_{cn(ef)}^{-2} (1 - V_{cn(ef)})^{-2}\}$, $\gamma_{vcc} = 1 + 2D_e$, and $\lambda_{vi} = I_{lo(ef)} V_i^{-1} \{I_{lon(ef)} (1 - V_{cn(ef)})^{-2} - 8V_{cn(ef)}^2 D_e^2 I_{lon(ef)}^{-1}\}$.

Since $DT_s = t_{0\to 1} + t_{8\to 10}$, the small signal average model of the control variable is obtained as follows:

$$\tilde{d} = \delta_{ilo} \tilde{i}_{lo(ef)} + \delta_{vcc} \tilde{v}_{cc(ef)} + \delta_{de} \tilde{d}_e - \delta_{vi} \tilde{v}_i \tag{54}$$

where $\delta_{vcc} = V_{cn(ef)} V_{cc(ef)}^{-1} \{2D_e + I_{lon(ef)} (1 - V_{cn(ef)})^{-2}\}$, $\delta_{ilo} = I_{lon(ef)} I_{lo(ef)}^{-1} (1 - V_{cn(ef)})^{-1}$, $\delta_{de} = 2V_{cn(ef)}$, and $\delta_{vi} = V_i^{-1} (2D_e V_{cn(ef)} + I_{lon(ef)} (1 - V_{cn(ef)})^{-2})$.

From (52) to (54), the small signal average model in the Laplace domain is expressed as follows:

$$\Psi_{ilo} \tilde{i}_{lo(ef)}(s) = \Psi_d \tilde{d}(s) + \Psi_{vi} \tilde{v}_i(s) - \Psi_{vco} \tilde{v}_{co(ef)}(s). \tag{55}$$

where $\Psi_{ilo} = (L_{o(ef)} C_{c(ef)} \delta_{de}) s^2 + \{L_{o(ef)} (\lambda_{de} \delta_{vcc} - \lambda_{vcc} \delta_{de}) + C_{c(ef)} (\gamma_{de} \delta_{ilo})\} s + \lambda_{de} \gamma_{vcc} \delta_{ilo} + \lambda_{ilo} \gamma_{de} \delta_{vcc} - \lambda_{vcc} \gamma_{de} \delta_{ilo} - \lambda_{ilo} \gamma_{vcc} \delta_{de}$, $\Psi_{vco} = (C_c \delta_{de}) s + \lambda_{de} \delta_{vcc} - \lambda_{vcc} \delta_{de}$, $\Psi_d = (C_{c(ef)} \gamma_{de}) s + \lambda_{de} \gamma_{vcc} - \lambda_{vcc} \gamma_{de}$, and $\Psi_{vi} = (C_{c(ef)} \gamma_{de} \delta_{vi}) s + \lambda_{de} \gamma_{vcc} \delta_{vi} + \lambda_{vi} \gamma_{de} \delta_{vcc} - \lambda_{vcc} \gamma_{de} \delta_{vi} - \lambda_{vi} \gamma_{vcc} \delta_{de}$.

Considering an output impedance disturbance $\tilde{z}_o(s) = \tilde{v}_o/\tilde{i}_o$, the small signal average model is restructured as follows:

$$\tilde{i}_{lo(ef)}(s) = G_{ilod}\tilde{d}(s) + G_{ilovi}\tilde{v}_i(s). \tag{56}$$

where $G_{ilod} = \Psi_d\Psi_{zo}(\Psi_{ilo}\Psi_{zo} + \Psi_{vco})^{-1}$, $G_{ilovi} = \Psi_{vi}\Psi_{zo}(\Psi_{ilo}\Psi_{zo} + \Psi_{vco})^{-1}$, and $\Psi_{zo} = (C_{o(ef)})s + \tilde{z}_o^{-1}(s)$. Figure 6 shows the control block diagram used for the converter.

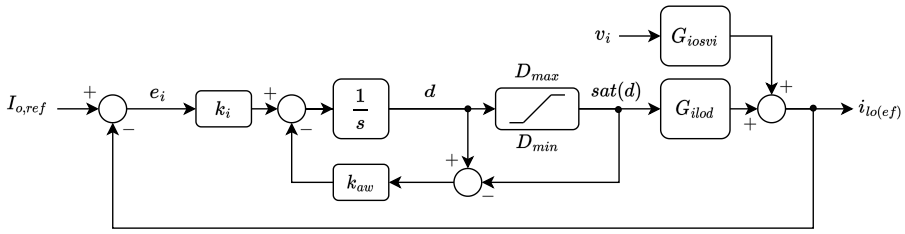


Figure 6. Control block diagram.

3. Results

A 10 kW reconfigurable PSFB converter prototype was designed and built according to Table 3. Figure 7 shows the photograph of the top and bottom views of the prototype, whose outer dimensions are 320 mm × 460 mm × 140 mm. Table 4 illustrates the main components employed in the prototype. The design of the prototype is based on efficiency, volume and cost for commercial purposes. Thus, SiC MOSFETs were used on the primary side switches in order to take advantage of their reduced switching and conduction losses. Low-voltage hyperfast diodes were used on the secondary side switches to reduce losses and costs. Sendust toroidal cores were used to reduce the size of the output filter inductors. Finally, N87 EE cores were used to reduce losses at high frequencies of the transformers and external inductors. In addition, for measuring the performance of the proposed reconfigurable PSFB converter, KEYSIGHT RP7952A is used as an input power supply, TEKTRONIX PA4000 as an input and output power analyzer, and TEKTRONIX MS046 to capture the experimental waveforms.

Table 3. Parameters of the reconfigurable PSFB converter prototype.

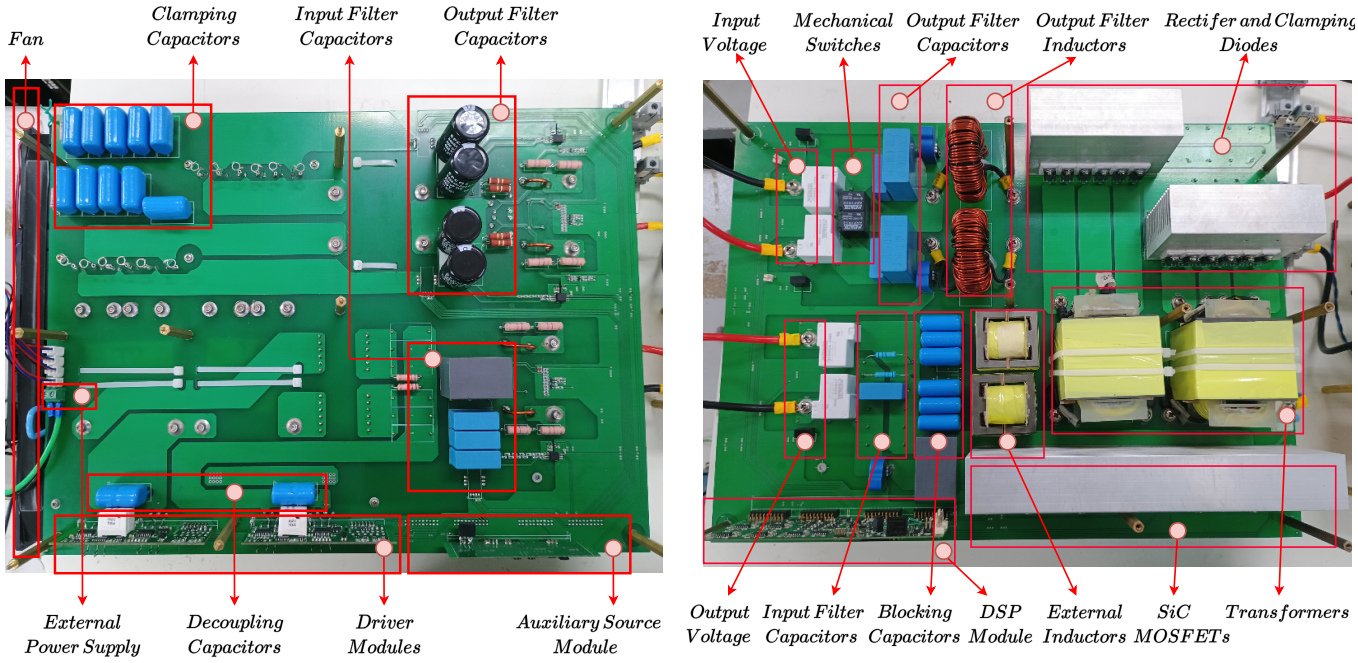
Parameter	Symbol	Value
Input voltage	V_i	900 V
Rated output voltage	V_o	400 V/800 V
Rated output current	I_o	25 A/12.5 A
Rated output power	P_o	10 kW
Switching frequency	f_s	100 kHz
Maximum output current ripple	$\Delta i_{lo,max}$	4.5 A
Maximum input voltage ripple	$\Delta v_{ci,max}$	9 V
Maximum output voltage ripple	$\Delta v_{co,max}$	5 V
Maximum blocking voltage ripple	$\Delta v_{cb,max}$	9 V
Transformer turns ratio	n	0.6
Leakage Inductance	L_{lk}	27.4 µH
Magnetizing Inductance	L_m	640 µH

Table 4. Main devices using in the prototype

Component	Symbol	Description
MOSFET	Q_1–Q_4	NTHL080N120SC1 (1200 V, 22 A, 110 mΩ , C_{oss} = 80 pF)
Rectifier Diode	D_1–D_4	VS-ETX3007-M3 (650 V, 30 A, V_f = 1.6 V, t_{rr} = 35 ns)
Clamping Diode	D_{c1}	VS-15ETH03-M3 (300 V, 15 A, V_f = 0.85 V, t_{rr} = 32 ns)
	D_{c2}	VS-30ETH06-M3 (600 V, 30 A, V_f = 1.34 V, t_{rr} = 23 ns)

Table 4. *Cont.*

Component	Symbol	Description
Transformer	T	Core: 2 × MMT140EE6527 L_m = 641 µH/665.3 µH , L_{lkg} = 8.4 µH/8.83 µH $N_p : N_{s1} : N_{s2} = 20 : 6 : 6$
External Inductor	L_{ext}	Core: 1 × MMT140EE4220 L = 18.37 µH/18.6 µH
Output Filter Inductor	L_o	Core: 1 × MMTS60T5715 L = 237.8 µH/342.51 µH
Input Filter Capacitor	C_i	MP F863H KEMET (10 µF, 1200 V) + MP B32774 TDK (4 × 1.5 µF, 1200 V)+ B43840-A9477 Epcos (2/3 × 470 µF, 400 V)
Blocking Capacitor	C_b	MP B32614 TDK (3 × 1 µF, 630 V)
Clamping Capacitor	C_c	MP B32614 TDK (5 × 2.2 µF, 630 V)
Output Filter Capacitor	C_o	MP B32776 TDK (12 µF, 1000 V)+ MP B32774 TDK (1.5 µF, 1200 V)+ B43845-A5227 Epcos (1/2 × 220 µF, 450 V)



(**a**) Top view (**b**) Bottom view

Figure 7. Prototype of the proposed reconfigurable PSFB converter.

Figure 8 shows the test scheme of the prototype. High-voltage pre-charge circuit-based IGBTs were developed and used to manage the inrush current. EMI filter circuits were developed and used to suppress conducted EMI noise. An auxiliary source module-based DC–DC switching regulator IC was developed and employed to provide various voltage levels required by different components. Driver module-based Si8285 ICs were developed and used for driving SiC MOSFETs with safety features. Finally, a DSP module-based TMS320F280037C DSP core was developed and employed for signal conditioning, communication and implementation of digital control algorithms.

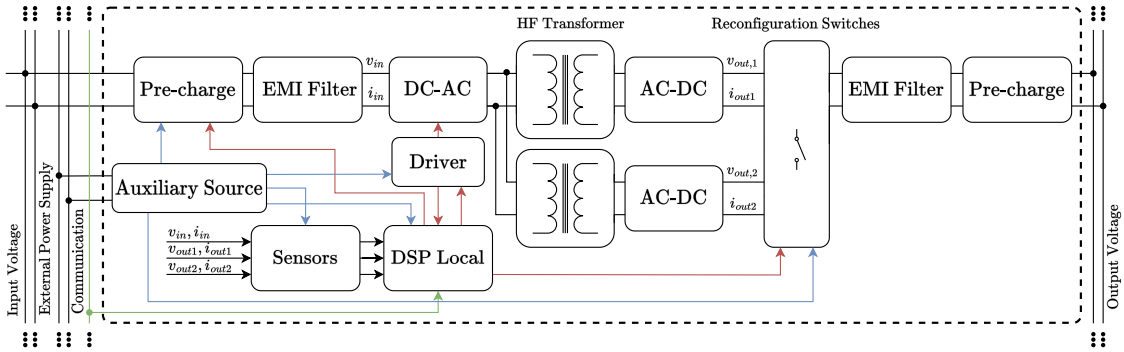
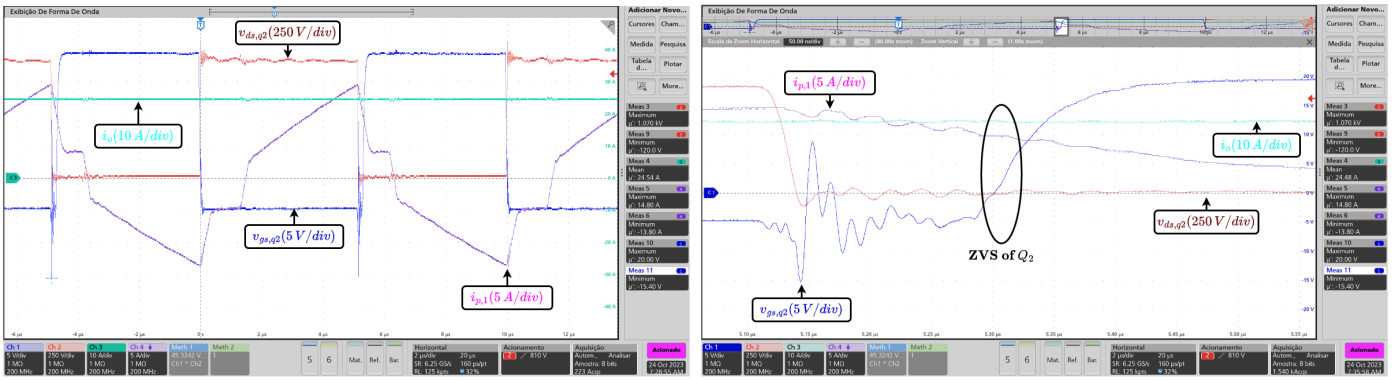


Figure 8. Reconfigurable PSFB converter prototype test scheme.

A set of resistive loads of 16 Ω and 64 Ω were used for experimental tests with parallel and series connection, respectively, in order to reach the nominal values of the prototype. In addition, a gate resistor of 10 Ω is built-in, and a dead time of 238 ns is configured in the Driver modules. In addition, an integral controller with $k_i = 6$ and $k_{aw} = 10$ is designed to control the output current i_o. The integral controller has a gain margin of $GM = 56.7$ dB at 14 kHz and a phase margin of $PM = 114°$ at 20 Hz under full load condition. Instead, a gain margin of $GM = 27.9$ dB at 4 kHz and a phase margin of $PM = 124°$ at 80 Hz under half load condition is obtained.

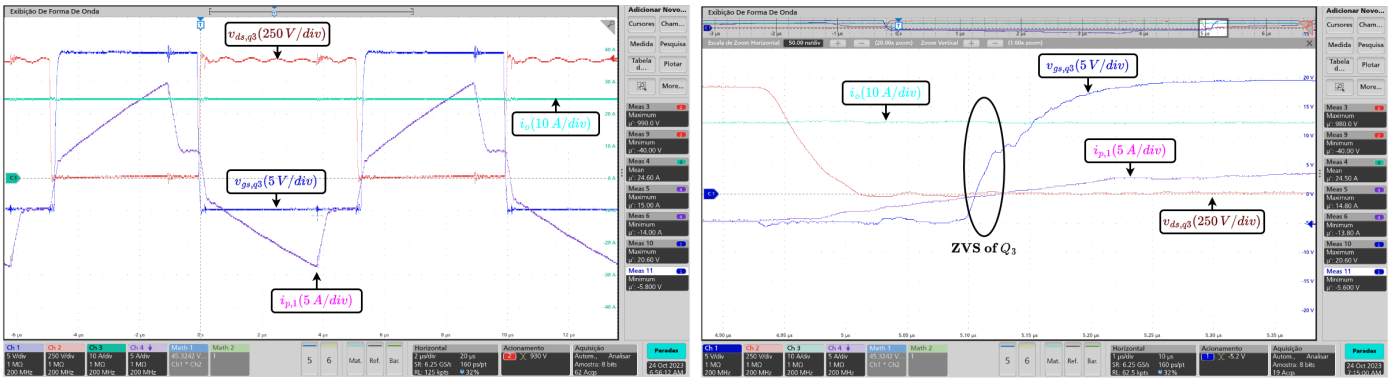
The experimental tests are performed at different power and voltage levels. Figures 9 and 10 show experimental waveforms in the leading and lagging legs under full load condition ($i_o = 25$ A) for the parallel connection case. As shown in Figures 9a and 10a, the proposed reconfigurable PSFB converter regulates well the output current with $D = 0.3859$. Moreover, as can be seen in Figures 9b and 10b, the ZVS turn-on operation is achieved. Under half load condition ($i_o = 15$ A), the experimental waveforms in the lagging leg are shown in Figure 11. Figure 11a shows that the output current is regulated with $D = 0.1625$. Furthermore, Figure 11b shows that the lagging leg fails to achieve the ZVS operation; however, the low voltage switching (LVS) operation is performed.



(**a**) (**b**)

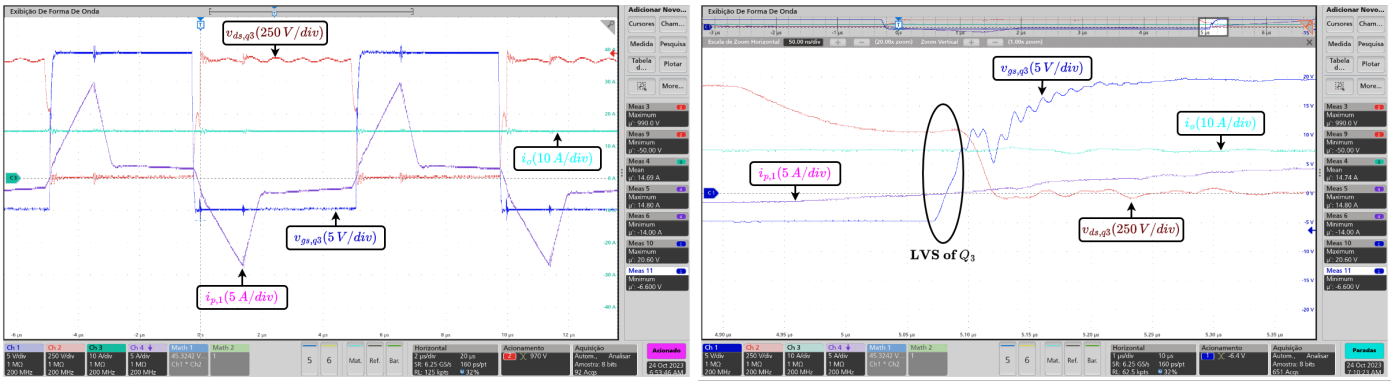
Figure 9. Parallel connection case: experimental waveforms in the leading leg under full load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q2}$ and gate-source voltage $v_{gs,q2}$ of switch Q_2, primary current $i_{p,1}$, and output current i_o. (**b**) ZVS waveforms.

Figures 12 and 13 show the waveforms in the leading and lagging legs under full load condition ($i_o = 12.5$ A) for the series connection case. In Figures 12 and 13, it is shown that the output current is controlled with $D = 0.3549$, and the ZVS turn-on operation is achieved. From Figure 14, it is shown that, under half load condition ($i_o = 7.5$ A), the output current is controlled with $D = 0.1549$ and the lagging leg achieves the LVS operation.



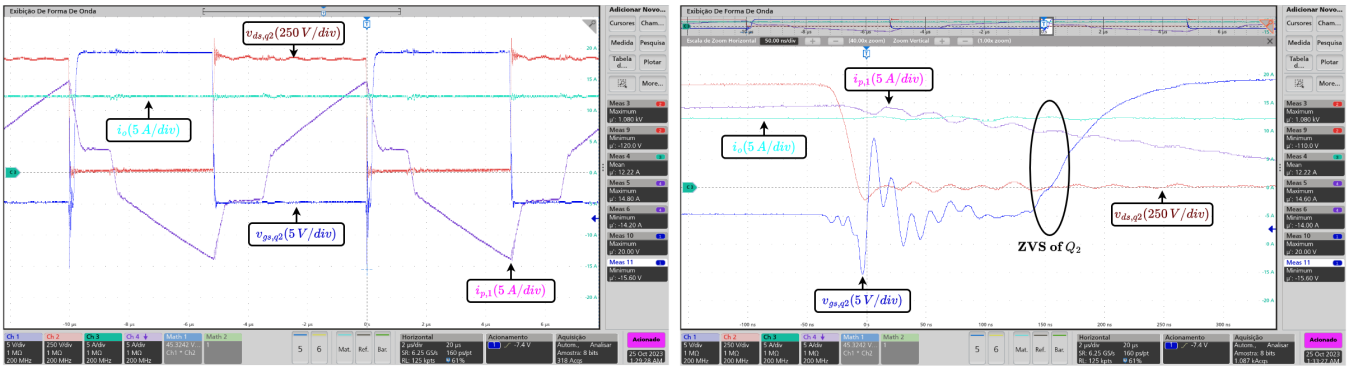
(**a**) (**b**)

Figure 10. Parallel connection case: Experimental waveforms in the lagging leg under full load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q3}$ and gate-source voltage $v_{gs,q3}$ of switch Q_3, primary current $i_{p,1}$, and output current i_o. (**b**) ZVS waveforms.



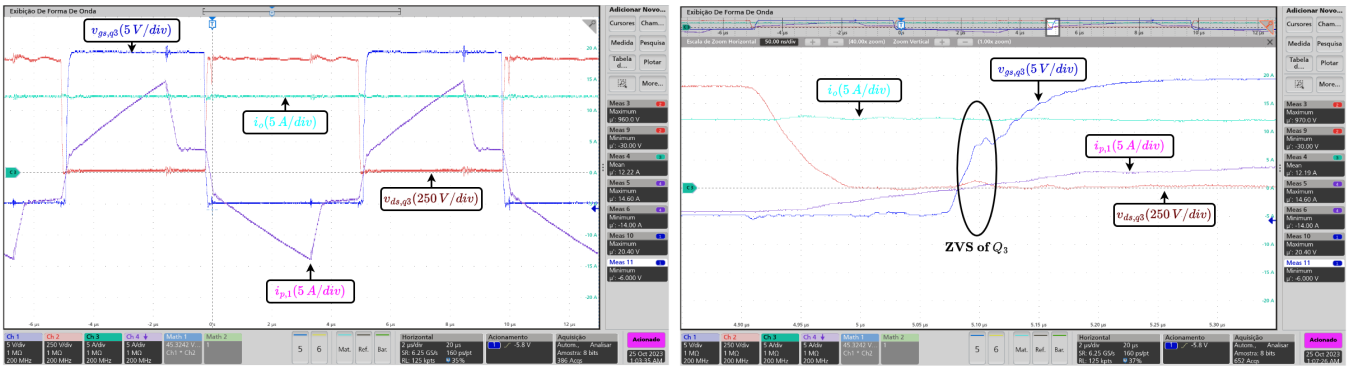
(**a**) (**b**)

Figure 11. Parallel connection case: Experimental waveforms in the lagging leg under half load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q3}$ and gate-source voltage $v_{gs,q3}$ of switch Q_3, primary current $i_{p,1}$, and output current i_o. (**b**) LVS waveforms.



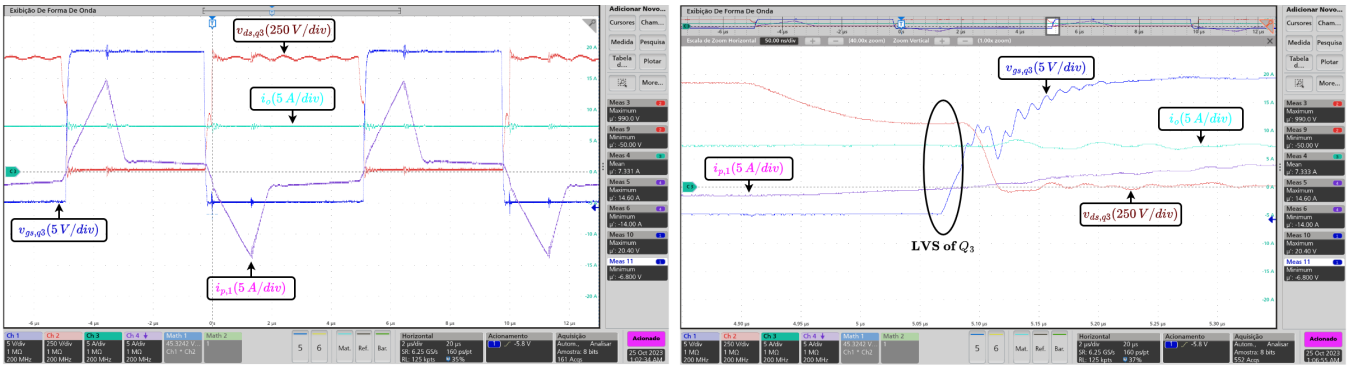
(**a**) (**b**)

Figure 12. Series connection case: Experimental waveforms in the leading leg under full load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q2}$ and gate-source voltage $v_{gs,q2}$ of switch Q_2, primary current $i_{p,1}$, and output current i_o. (**b**) ZVS waveforms.



(**a**) (**b**)

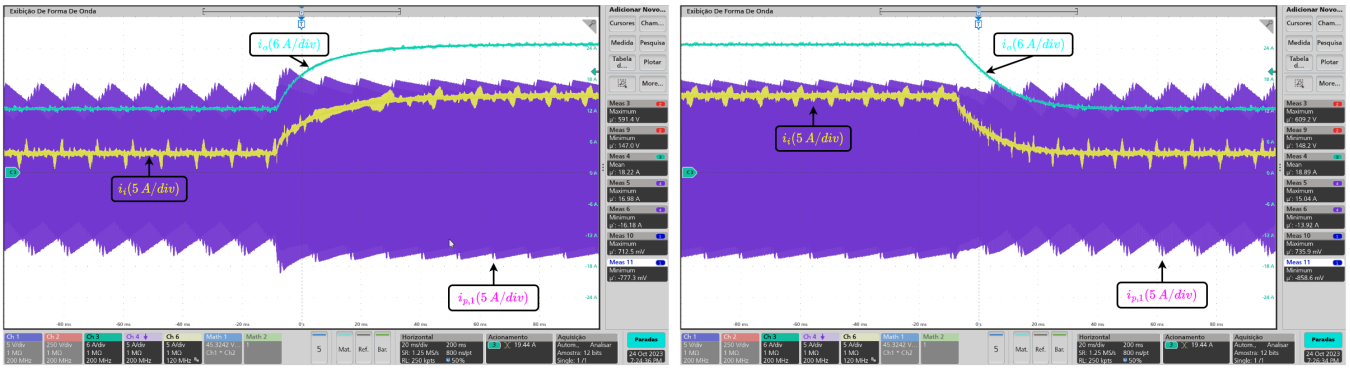
Figure 13. Series connection case: Experimental waveforms in the lagging leg under full load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q3}$ and gate-source voltage $v_{gs,q3}$ of switch Q_3, primary current $i_{p,1}$, and output current i_o. (**b**) ZVS waveforms.



(**a**) (**b**)

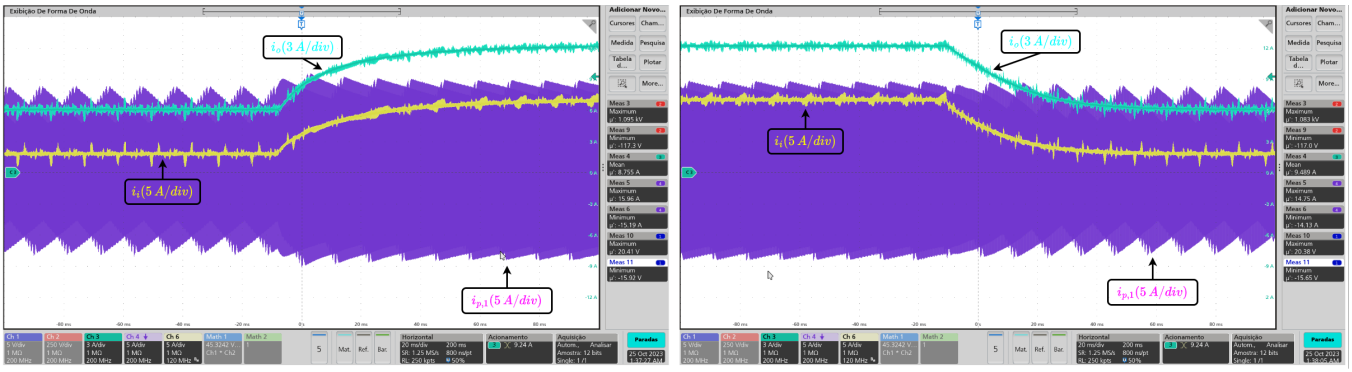
Figure 14. Series connection case: Experimental waveforms in the lagging leg under half load condition. (**a**) Waveforms of the drain-source voltage $v_{ds,q3}$ and gate-source voltage $v_{gs,q3}$ of switch Q_3, primary current $i_{p,1}$, and output current i_o. (**b**) LVS waveforms.

The experimental waveforms depicted in Figures 15 and 16 illustrate the output current transients between the full load and half load conditions, and vice versa, for cases of series and parallel connection. As shown in Figures 15 and 16, the control strategy enables the rapid adjustment of the output current.



(**a**) (**b**)

Figure 15. Parallel connection case: Experimental waveforms for a load transient. (**a**) Output current from 12.5 A to 25 A. (**b**) Output current from 25 A to 12.5 A.



(**a**) (**b**)

Figure 16. Series connection case: Experimental waveforms for a load transient. (**a**) Output current from 6.25 A to 12.5 A. (**b**) Output current from 12.5 A to 6.25 A.

Tables 5 and 6 show the voltage measurements on the output filter capacitors v_{co} and the current measurements on the output filter inductors i_{lo} of the prototype for the series and parallel configuration. As shown in Tables 5 and 6, the designed prototype presents minimal current and voltage imbalance errors, which are caused by uncertainties in the parameters of the elements that constitute the primary and secondary sides. The error e is calculated as the relationship between the difference and the mean of the measurements.

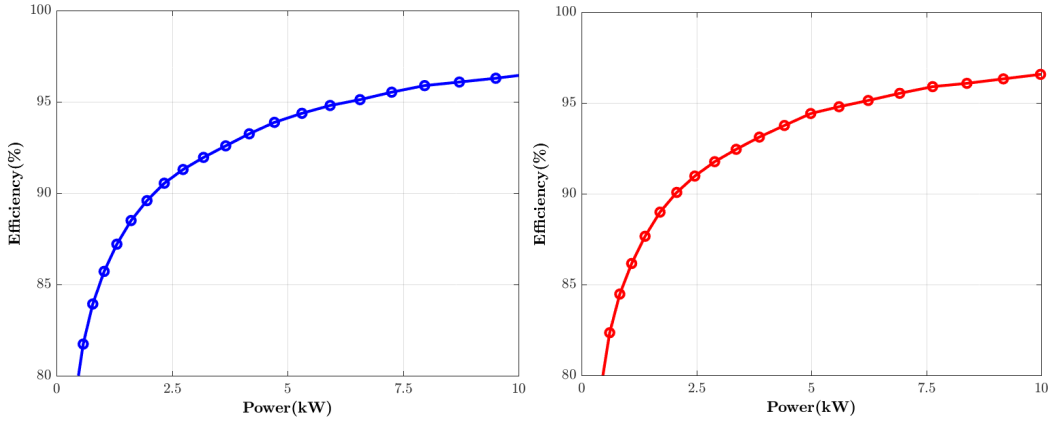
Table 5. Voltage and current measurements of the prototype for the series configuration.

$i_{o,ref}$	$i_{lo,1}$	$i_{lo,2}$	e_{ilo}	$v_{co,1}$	$v_{co,2}$	v_o	e_{vco}
1.5 A	1.552 A	1.484 A	4.48%	44.066 V	40.984 V	85.050 V	7.25%
3 A	2.999 A	2.961 A	1.27%	85.817 V	81.617 V	167.434 V	5.01%
4.5 A	4.542 A	4.466 A	1.68%	128.305 V	123.881 V	252.186 V	3.51%
6 A	6.037 A	5.932 A	1.75%	171.706 V	166.629 V	338.335 V	3.01%
7.5 A	7.532 A	7.481 A	0.67%	213.501 V	210.126 V	423.627 V	1.59%
9 A	9.077 A	8.979 A	1.08%	256.547 V	254.688 V	511.235 V	0.72%
10.5 A	10.583 A	10.476 A	1.01%	298.008 V	297.991 V	595.999 V	0.01%
12.5 A	12.576A	12.498 A	0.62%	357.791 V	356.973 V	714.764 V	0.23%

Table 6. Voltage and current measurements of the prototype for the parallel configuration.

$i_{o,ref}$	$i_{lo,1}$	$i_{lo,2}$	i_o	e_{ilo}	$v_{co,1}$	$v_{co,2}$	e_{vco}
3 A	1.567 A	1.449 A	3.016 A	7.82%	45.241 V	44.744 V	1.11%
6 A	3.073 A	2.917 A	5.99 A	5.21%	88.545 V	88.026 V	0.58%
9 A	4.671 A	4.335 A	9.01 A	7.46%	133.171 V	133.411 V	0.18%
12 A	6.212 A	5.765 A	11.977 A	7.46%	177.872 V	178.241 V	0.21%
15 A	7.721 A	7.224 A	14.945 A	6.65%	222.922 V	223.813 V	0.39%
18 A	9.304 A	8.703 A	18.007 A	6.67%	268.946 V	269.741 V	0.29%
21 A	10.836 A	10.138 A	20.974 A	6.65%	312.028 V	314.963 V	0.93%
25 A	13.077 A	11.926 A	25.003 A	9.21%	374.269 V	375.429 V	0.31%

Figure 17 shows the measured efficiency of the prototype for the series and parallel configuration. The measurement did not consider the external power supply or external circuits used in the test scheme. As shown in Figure 17, the prototype has a high efficiency in a wide load range, achieving 96.69% under full load conditions.



(**a**) Series configuration (**b**) Parallel configuration

Figure 17. Measured efficiency of the prototype.

4. Conclusions

In this paper, a reconfigurable PSFB converter has been proposed and analyzed. Its topology is based on two traditional PSFB converters with CDD clamping circuits connected at their outputs by switches. SPDT mechanical switches enabled series and parallel reconfigurations on the secondary side. In addition, an exhaustive analysis of the clamping mechanism was carried out, in which the main electrical parameters, electrical stresses, design conditions, and a small signal dynamic model were derived. Compared to state-of-the-art solutions, the proposed reconfigurable PSFB converter allows the design of a compact structure and reduced costs, making it attractive for commercial applications. A commercial prototype of 10 kW was developed in the laboratory, achieving a power density of 0.485 W/cm^3. The series and parallel configuration made it possible to change the nominal output voltage between 400 V and 800 V, enabling the operation of the converter over an output voltage wide range. The experimental results showed that the reconfigurable PSFB converter can achieve high efficiency under various load conditions, reaching 96.69% efficiency at full load.

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