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An Improved Near-State Pulse-Width Modulation with Low Switching Loss for a Permanent Magnet Synchronous Machine Drive System

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Abstract: Common-mode voltage (CMV) leads to the shaft voltage and shaft current by coupling the capacitor network in the permanent magnet synchronous machine (PMSM), which affects the reliability of the whole motor drive system. Based on the low-CMV modulation strategy for the PMSM drive system, this paper proposed an improved near-state pulse-width modulation (NSPWM) on switching loss. First, the generation mechanism for the switching signals of NSPWM was analyzed, and it was observed that there exists one phase of switches in an inactive state for every sector. Then, to reduce the switching loss of the NSPWM, this paper proposed an improved NSPWM modulation strategy based on power factor angle to adjust switching action, which ensures the switching tubes that have the biggest conduction current have no switching action. In addition, the switching loss analytic formula of the NSPWM was derived to prove the correctness of the proposed method for optimizing switching loss. Finally, the proposed modulation strategy was carried out in the simulation and experimental platform. Under the premise of good steady and dynamic performance, the results show that the proposed modulation strategy has less switching loss.

Keywords: inverter; modulation strategy; switching losses; common-mode voltage

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1. Introduction

Compared to current source inverters (CSIs) and other multilevel inverters, three-phase two-level voltage source inverters (VSIs) have the advantage of a simple structure and bidirectional energy conversion [1,2], so VSIs have been widely used in permanent magnet synchronous machine (PMSM) drive systems [3], and many modulation methods for VSIs have been proposed, such as SPWM, SVPWM, DPWM and dual-vector modulation [4,5]. However, there are some problems that endanger the safe and stable operation of this system. For example, the common-mode voltage (CMV) generated at the neutral point leads to the shaft voltage and shaft current by coupling the capacitor network in the motor [6], which affects the reliability of the whole PMSM drive system [7].

To reduce the CMV of the PMSM drive system fed by VSI, Reference [8] introduces CMV into the cost function and proposes a model predictive control scheme that takes into account CMV. An optimized zero-sequence voltage injection method is proposed [9], and the CMV amplitude can decrease to 50%. In [10], a kind of harmonic elimination pulse-width modulation with a common-mode voltage reduction ability is presented. However, the CMV reduction method proposed in [11] is suitable for multi-level inverters.

For two-level VSIs, a switching tube is introduced to the DC bus, which makes the AC part of the three-phase converter float in the zero state. Through improvements in structure and control strategy, the CMV remains unchanged in the zero state [12]. Reference [13] proposes a three-phase AC-side voltage-doubling topology with an intrinsic buck–boost

unit, which suppresses the average CMV to zero by modulating the output phase voltage around its negative bus. However, the above two methods add the hardware circuit in the three-phase two-level VSI, which not only increases costs but also reduces efficiency and reliability. Therefore, reducing CMV through modulation is the most effective means.

Since the amplitude of CMV in zero state is Udc/2, which is 3 times of that in active state, reducing the common-mode voltage of the zero vector or eliminating the zero vector is the most effective modulation method [14]. References [15,16] control the dead time switching tube by current sector determination and switch function direct control, so the CMV amplitude is suppressed by changing the current freewheeling path. Although this method can reserve the zero state, the dead time at the commutation time will cause a zero current clamping effect. Active zero-state PWM (AZSPWM) adopts two opposite AVVs to replace the ZVV, so the high-frequency CMV can be effectively reduced. However, the ripple of the current is too great [17]. In comparison, near-state PWM (NSPWM) adopts three adjacent active vectors to synthesize the reference vector; it can reduce the high- and low-frequency CMV simultaneously, and the steady state under NSPWM is better than that under AZSPWM [18]. It should be noted that no matter where the reference vector is located, there are two vector synthesis methods, and there exists one phase of switches in an inactive state.

Based on the characteristic analysis of NSPWM, to reduce the switching loss, this paper proposed an improved NSPWM modulation strategy based on power factor to adjust the switching action. To ensure the switching tube that has the biggest conduction current has no switching action, the NSPWM with the least switching loss is proposed. In the simulation and experiment part, the effectiveness of the proposed method on steady-state, dynamic-state performance and switching loss optimization is shown.

This paper is organized as follows: Section 2 describes the topology and whole control system. Then, an improved NSPWM scheme is proposed in Section 3. Consequently, the effectiveness and superiority of the proposed scheme are validated by the simulation and experiment results in Sections 4 and 5. Finally, the conclusion is drawn in Section 6.

2. Topology and Field-Oriented Control

2.1. Topology of PMSM Control System

According to [18], the NSPWM has a limited linearity region, which means it can only modulate the voltage in that the modulation index M is greater than 0.61. However, when PMSM operates at low speed, the NSPWM generates high CMV and does not modulate the reference voltage correctly. Therefore, to reduce the DC voltage, the buck converter is introduced in the DC side of the PMSM drive system.

Figure 1 shows the topology of the PMSM control system fed by a three-phase voltage source inverter with a buck converter, where u_{in} represents the DC source voltage; u_{dc} represents the DC-link voltage; C_{dc}, S_0, D_0 and L_{dc} constitute the buck converter; S_1, S_2, S_3, S_4, S_5 and S_6 represent the switching tube of the three-phase VSI bridge.

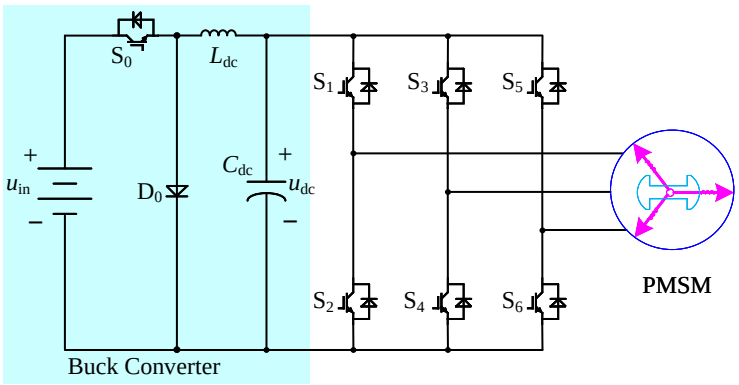


Figure 1. Topology of PMSM fed by three-phase VSI with DC-DC boost converter.

2.2. Mathmatical Model of PMSM

According to [19], in the synchronous rotating frame ($d-q$ frame), the voltage state equations of the PMSM are shown as follows:

$$u_d = R_s i_d + \frac{d\psi_d}{dt} - \omega\psi_q \tag{1}$$

$$u_q = R_s i_q + \frac{d\psi_d}{dt} - \omega\psi_d \tag{2}$$

where u_d and u_q represent the stator voltage in the $d-q$ frame, i_d and i_q represent the stator current in the $d-q$ frame, R_s is the stator resistance, ω is the synchronous angle frequency and ψ_d and ψ_q are the flux linkage in the $d-q$ axis.

The equations of electromagnetic flux linkage are shown as [20]

$$\psi_d = L_d i_d + \psi_f \tag{3}$$

$$\psi_d = L_q i_q \tag{4}$$

where L_d and L_q are the stator inductance in the $d-q$ frame and ψ_f is the flux linkage of PMSM.

The electromagnetic torque equation is shown as

$$T_e = \frac{3}{2} n_p [\psi_f i_q + (L_d - L_q) i_d i_q] \tag{5}$$

where T_e represents the electromagnetic torque and n_p is the pole pairs.

2.3. Field-Oriented Control

Field-oriented control (FOC) is adopted in this paper; the whole diagram is shown in Figure 2. FOC mainly includes speed closed-loop and current closed-loop control. The given rotational speed is compared with the actual rotational speed, the deviation is passed through the speed PI controller and the i_d and i_q are compared with the actual value to obtain the deviation to the current PI controller. And the output of the current controller u_d and u_q are transformed into the $\alpha-\beta$ coordinate system. Through the modulation module output switching signals to the inverter, the inverter outputs three-phase voltage to directly drive the PMSM.

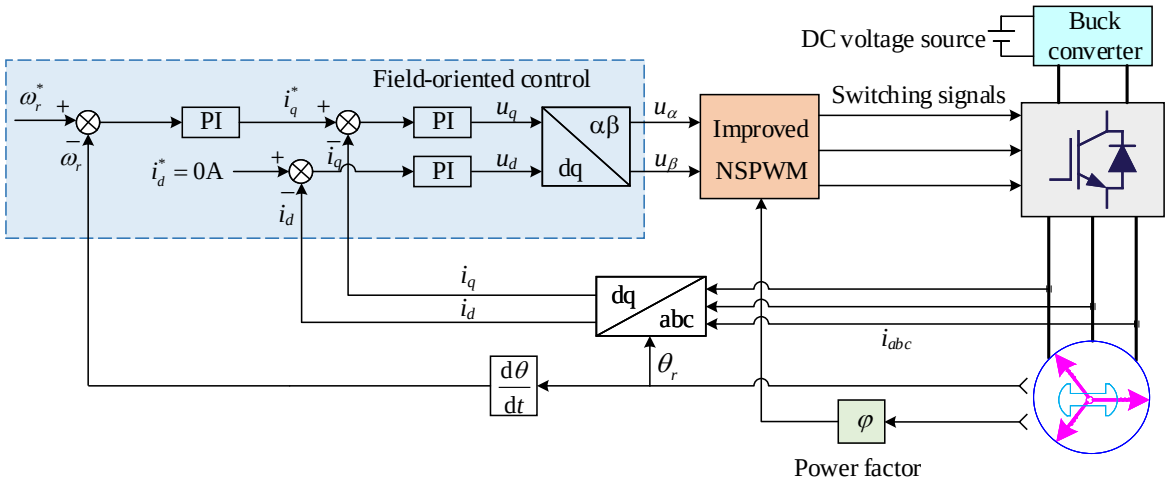


Figure 2. Block diagram of the proposed improved NSPWM based on FOC.

2.4. Conventional NSPWM

NSPWM adapts three neighbor voltage vectors to match the reference voltage. The three voltage vectors are the voltage vectors that are closest to the reference voltage vector and its two neighbors (Figure 3b). The utilized voltage vectors are changed every 60° throughout the space. As shown in Figure 3a, the voltage vector space is divided into six sectors. Defined with indices i, voltage vectors V_{i-1}, V_i, V_{i+1} are utilized for region A_i.

Utilizing the three near-state voltage vectors, the volt–seconds balance equation and the PWM period constraint for NSPWM are given for region A_i in the equations below.

$$V_{i-1}t_{i-1} + V_i t_i + V_{i+1}t_{i+1} = V_{ref}T_s \tag{6}$$

$$t_{i-1} + t_t + t_{i+1} = T_s \tag{7}$$

where T_s is the PWM period.

Normalizing the voltage vector, the vector duty cycles can be found as $d_k = \frac{t_k}{T_s}$, where k is $i-1$, i, $i+1$. Utilizing the above equations, the duty cycles of the voltage vectors can be calculated for region A_i as follows:

$$d_{t-1} = 1 - \frac{2\sqrt{3}}{\pi} M_i sin(\theta - \frac{(i-2)\pi}{3}) \tag{8}$$

$$d_{t-1} = -1 + \frac{3}{\pi} M_i cos(\theta - \frac{(i-2)\pi}{3}) + \frac{3\sqrt{3}}{\pi} M_i sin(\theta - \frac{(i-2)\pi}{3}) \tag{9}$$

$$d_{t-1} = 1 - \frac{3}{\pi} M_i cos(\theta - \frac{(i-2)\pi}{3}) - \frac{\sqrt{3}}{\pi} M_i sin(\theta - \frac{(i-2)\pi}{3}) \tag{10}$$

In the above equations, θ is the angle of the reference voltage vector with the α axis and M_i is the modulation index which indicates the voltage utilization level $M_i = \frac{V_m}{\frac{2V_{dc}}{\pi}}$. Equations (8)–(10) yield a valid solution only in the colored region shown in Figure 3c, and in the white remaining regions, there is no solution.

The sequence of NSPWM is shown in Table 1 for region definitions of Figure 3a.

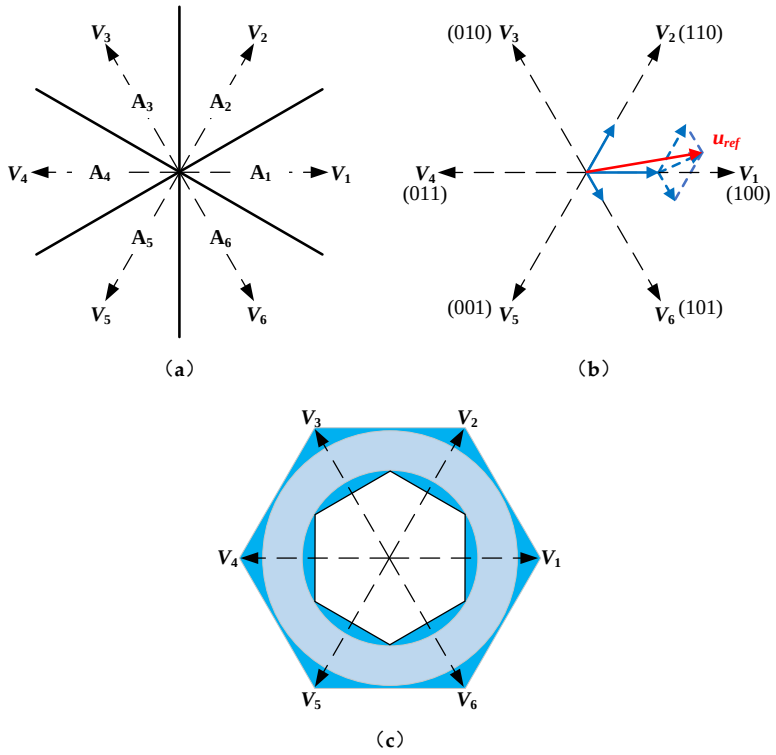


Figure 3. (**a**). Region division (**b**). Vector synthesis strategy (**c**). Linearity region.

Table 1. Basic synthesized vector sequence for NSPWM in all sectors.

	A_1	A_2	A_3	A_4	A_5	A_6
1st Vector	V_2	V_3	V_4	V_5	V_6	V_1
2nd Vector	V_1	V_2	V_3	V_4	V_5	V_6
3rd Vector	V_6	V_1	V_2	V_3	V_4	V_5
4th Vector	V_1	V_2	V_3	V_4	V_5	V_6
5th Vector	V_2	V_3	V_4	V_5	V_6	V_1

3. Optimized NSPWM Strategy

3.1. Conventional NSPWM Redundancy Analysis

NSPWM adopts three near-basic voltage vectors to synthesize the reference voltage vector; it has one phase switch that remains clamped for every PWM period. For example, in A_1, the voltage vectors u_6, u_1 and u_2 are adopted, and phase A remains clamped open. Figure 4 shows the three-phase switching signals for all six sectors.

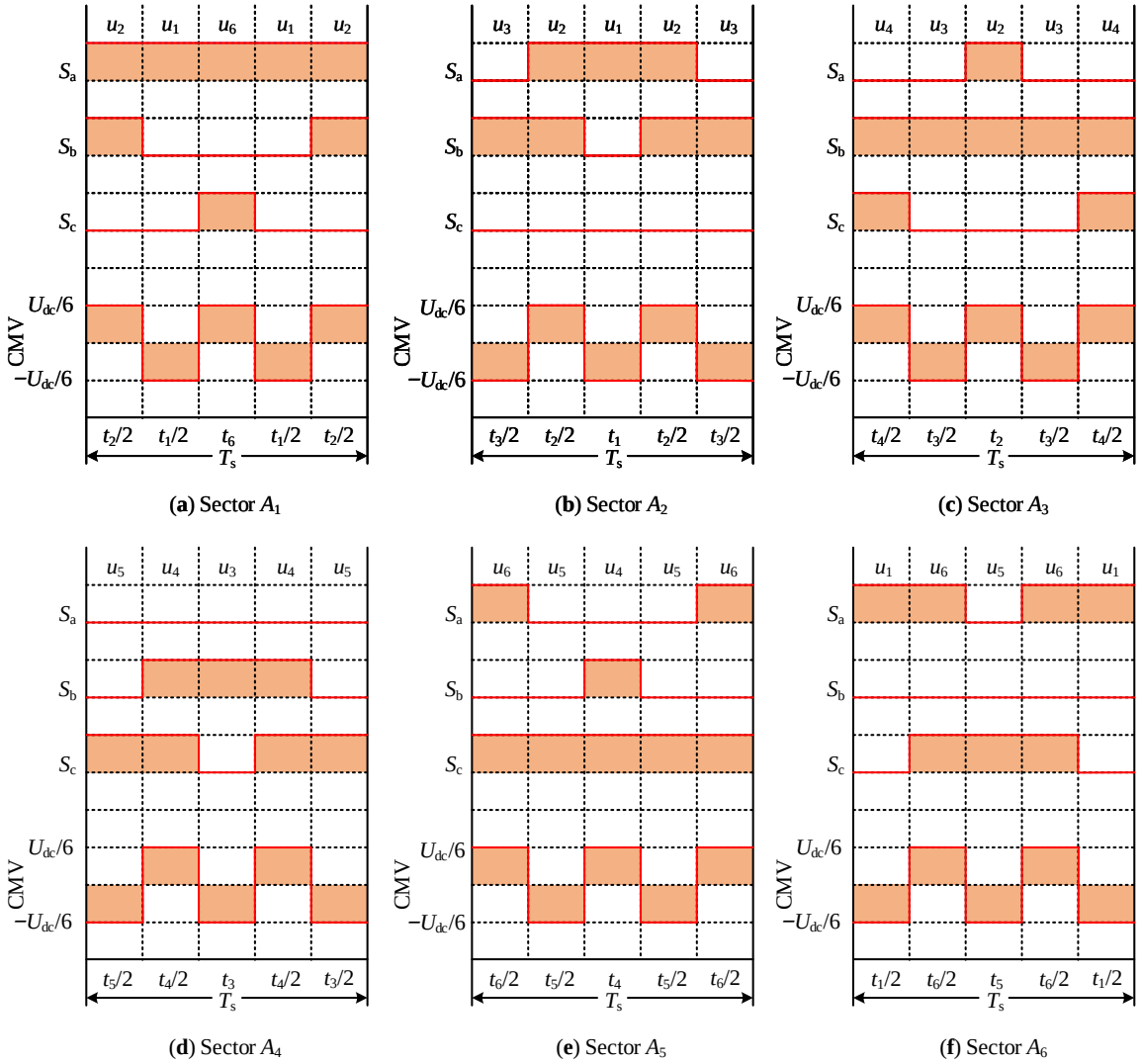


Figure 4. Switching signals for all six sectors.

A conventional NSPWM can reduce switching loss by voltage clamping. However, the conventional NSPWM synthesis strategy does not optimize the switching loss. To analyze the switching loss, Figure 5 shows the three-phase reference voltage vector and

three-phase current vector in the synchronous station frame (α-β) through the Clarke transform in Equation (11).

$$i = \frac{2}{3}(i_a + i_b e^{j\frac{2\pi}{3}} + i_c e^{j\frac{2\pi}{3}}) \tag{11}$$

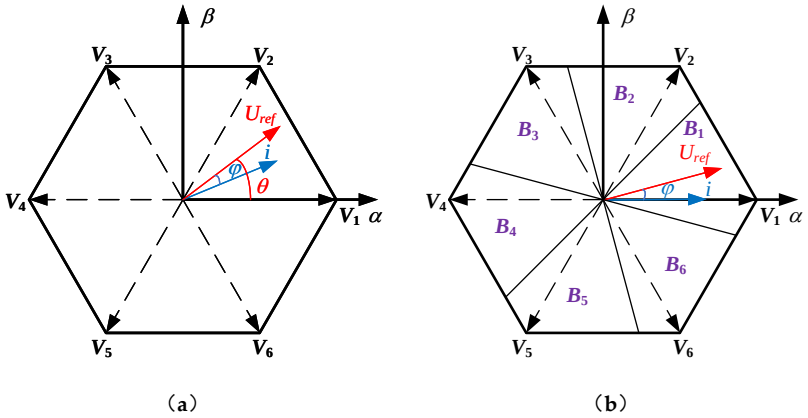


Figure 5. Reference voltage vector and current vector (**a**). $\varphi \neq \theta$ (**b**). $\varphi = \theta$.

In Equation (11), i represents the actual current vector, and i_a, i_a and i_a represent the current magnitude in phases a, b and c.

For PMSM, the current vector i lags reference voltage vector U_{ref} by power factor angle (φ), and the angle between U_{ref} with α axis is θ. The U_{ref} location determines the basic synthesized vector group, but it still can be improved. For example, Figure 6 shows the two methods to synthesize the U_{ref} when U_{ref} is located near the sector boundary, but the current vector i could be used to optimize the switching loss. In Figure 5b, when $\varphi = \theta$, the phase A current is maximum. Therefore, to reduce the switching loss, phase A needs clamping, and the best-synthesized group is V_6, V_1, V_2. Actually, when U_{ref} is located in B_1, the phase A current magnitude is the biggest phase current, so the best-synthesized vector group for U_{ref} located in B_1 is V_6, V_1, V_2. In conclusion, when the inverter works in a non-unit power factor, the conventional NSPWM cannot best optimize the switching loss.

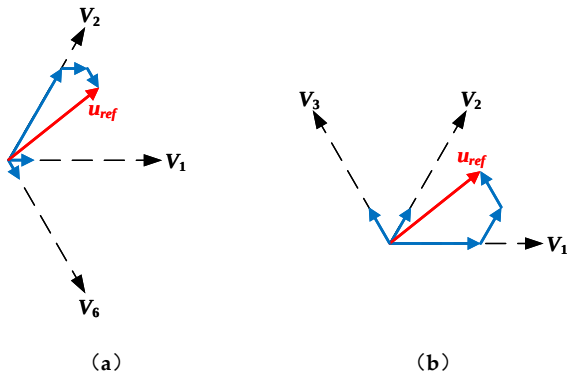


Figure 6. Synthesized strategies comparison (**a**). Strategy 1 (**b**). Strategy 2.

3.2. Improved NSPWM on Switching Loss

When an inverter switches, it will cause large switching loss, reduce the working efficiency and cause large heat dissipation. To reduce the switching loss of NSPWM, the improved NSPWM method is proposed. Compared with NSPWM, the proposed method adopts different sector division methods, which introduce angle variable α to dynamically adjust the sector division, as shown in Figure 7a. The synthesized voltage vector sequences for all sectors are shown in Table 2, which are the same as those for the conventional NSPWM.

Table 2. Basic synthesized vector sequence for the improved NSPWM in all sectors.

	B_1	B_2	B_3	B_4	B_5	B_6
1st Vector	V_2	V_3	V_4	V_5	V_6	V_1
2nd Vector	V_1	V_2	V_3	V_4	V_5	V_6
3rd Vector	V_6	V_1	V_2	V_3	V_4	V_5
4th Vector	V_1	V_2	V_3	V_4	V_5	V_6
5th Vector	V_2	V_3	V_4	V_5	V_6	V_1

3.3. Linearity Region

Compared with the conventional NSPWM, the proposed improved NSPWM just optimizes the synthesized vector group; the basic vector synthesis strategy is the same as NSPWM. Therefore, the improved method still has the limited linearity region problem. From the synthesized principle, the linearity region is related to variable α. For example, in Figure 7b, the basic vector group u_6, u_1, u_2 can only synthesize the reference voltage vector in the black-lined region, and the linearity region is the light blue region, which is expressed as

$$\frac{\pi}{6\cos(|\alpha| + 30^\circ)} \leq M_i \leq 0.907 \tag{12}$$

Therefore, only when $\alpha \in [-24.74^\circ, 24.74^\circ]$, the improved NSPWM has per-fundamental linearity region. The larger the $|\alpha|$, the smaller the linearity region. So, choosing α not only relates to switching loss but also relates to the linearity region.

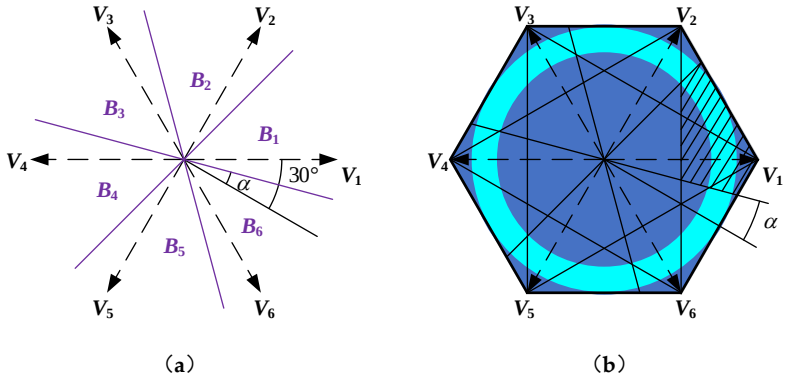


Figure 7. Space vector sectors and modulation regions. (**a**). Space vector sectors. (**b**). Modulation region.

3.4. Switching Loss Analysis

In this paper, to evaluate the switching loss of the proposed method and the conventional NSPWM, the current ripple is neglected, and thus, the phase current i_p can be assumed as

$$i_p = I\cos(\theta - \varphi) \tag{13}$$

In the equation above, I represents the amplitude of the fundamental current component, φ is the power factor angle and θ represents the electrical angle of the reference voltage.

From [21], the phase average switching loss in one unit for a one-carrier cycle is defined as

$$P_{sw_p} = \frac{f_{sw}u_{dc}(E_{on} + E_{off})}{2\pi I_{rate}U_{rate}}\left[\int_a^b |i_p(\theta)|d\theta\right] \tag{14}$$

In the equation above, E_{on} and E_{off} represent the switch-on energy loss and switch-off energy loss under f_{sw} working frequency, I_{rate} and U_{rate} represent the rated current and rated voltage for the switch and $\int_a^b$ represent the interval that the switch does not clamp.

For phase a, it has voltage clamping in sectors A_1 and A_4, so for the improved NPSWM, the switching loss for phase A in a one-carrier cycle is expressed as

$$P_{sw_a} = \frac{f_{sw} u_{dc}(E_{on} + E_{off})}{2\pi I_{rate} U_{rate}} [\int_{\frac{\pi}{6}}^{\frac{5\pi}{6}} |i_a(\theta)| d\theta + \int_{\frac{7\pi}{6}}^{\frac{11\pi}{6}} |i_a(\theta)| d\theta] \tag{15}$$

By simplifying the equation above, the switching loss for improved NSPWM can be obtained as follows:

$$P_{sw_a} = \frac{I f_{sw} u_{dc}(E_{on} + E_{off})}{\pi I_{rate} U_{rate}} \tag{16}$$

It can be seen that the switching loss is proportional to the switching frequency, the DC-link voltage and the phase current. The same conclusion can be obtained in reference [22]. For comparison, in the conventional NPSWM, the switching loss in a one-carrier cycle is expressed as

$$P'_{sw_a} = \frac{f_{sw} u_{dc}(E_{on} + E_{off})}{2\pi I_{rate} U_{rate}} [\int_{\frac{\pi}{6}+\varphi}^{\frac{5\pi}{6}+\varphi} |i_a(\theta)| d\theta + \int_{\frac{7\pi}{6}+\varphi}^{\frac{11\pi}{6}+\varphi} |i_a(\theta)| d\theta] \tag{17}$$

By simplifying the equation above, the switching loss for the conventional NSPWM can be obtained as follows:

$$P'_{sw_a} = \frac{I f_{sw} u_{dc}(E_{on} + E_{off})}{\pi I_{rate} U_{rate}} [2 - \cos(\varphi)] \tag{18}$$

It is obvious that the conventional NSPWM switching loss is larger than the improved NSPWM ($P_{sw_a} < P'_{sw_a}$). The correctness of the proposed method on optimizing the division of the sector by introducing variable α has been theoretically proved. For phases b and c, the switching loss expression is similar.

4. Simulation Results

The simulation models with thermal analysis of the proposed method and the conventional NSPWM are established in the Matlab Simulink(R2023b)/PLECS (4.8.4.) environment. PLECS is a particular tool working in Simulink to analyze the thermal environment of some equipment. The Simulink and PLECS models are both used in this model; the Simulink model mainly works on the signal processing and NSPWM control signal generation, while the PLCES model works mainly on the thermal analysis of the three-phase inverter. The steady state, dynamic performance and switching loss are verified by the simulation results; the PMSM parameters are shown in Table 3.

Table 3. Parameters of PMSM.

Parameters	Description	Value
R_s (Ω)	Stator resistance	1.443
L_d (mH)	d-axis inductance	5.541
L_q (mH)	q-axis inductance	5.541
ψ_f (Web)	Flux linkage	0.2852
i_N (A)	Rated current	4.5
n_N (r/min)	Rated speed	1000
T_N (N·m)	Rated torque	10
n_p	Pole pairs	4
J ($kg \cdot m^2$)	Rotational inertia	0.00194
u_{dc} (v)	DC-bus voltage	270
f_s (Hz)	Carrier frequency	10,000
P_N (kW)	Rated power	1.0
U_N (V)	Rated voltage	110

4.1. Steady-State Experiment

PMSM operates at a rated speed and rated load, and u_{ref} is located in the at linearity region. $\alpha = 30°$ was set for the proposed method; the speed, torque and phase A current waveforms are shown in Figure 8a,b for the conventional NSPWM and the proposed NSPWM, respectively. Because the proposed method just optimizes the division of sectors and does not change the vector synthesis strategy, the results show that both methods operate at good steady-state performance with 6.05% and 5.61% current THD and 0.2283 N·m and 0.2290 N·m torque ripple, respectively. The results prove that the proposed method has the same steady-state performance as the conventional NSPWM.

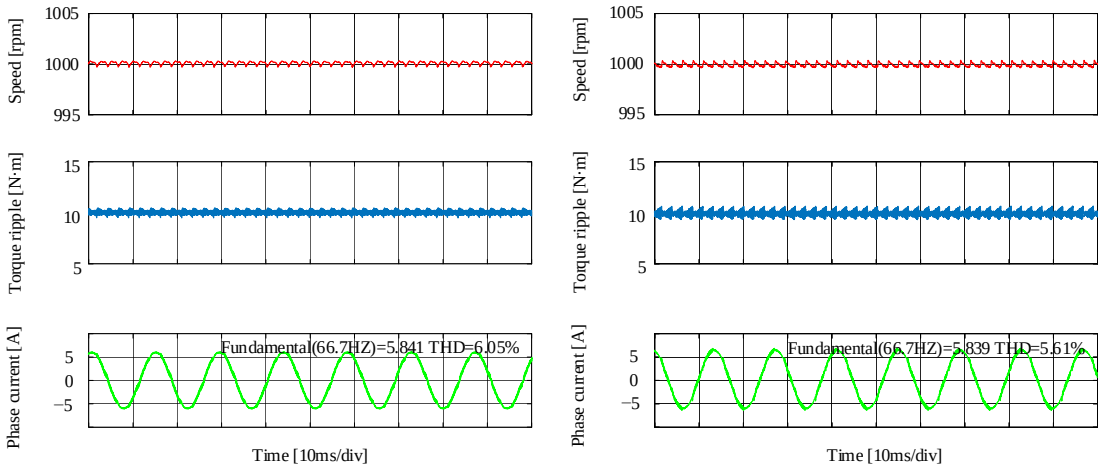


Figure 8. Steady-state performance for PMSM operating at rated speed and rated load. (**a**). Conventional NSPWM. (**b**). Improved NSPWM.

4.2. Dynamic-State Experiment

To verify the dynamic-state performance of the proposed method, $\alpha = 30°$ was set, and PMSM was given a speed control step from static to rated speed without load. The comparison waveforms of speed, load and phase A current are shown in Figure 9a,b for the conventional NSPWM and the proposed method, respectively. The response time of the conventional NSPWM is 5.03 ms, and for the proposed method, it is 4.98 ms. The results show that the proposed method has the same dynamic performance as the conventional NSPWM.

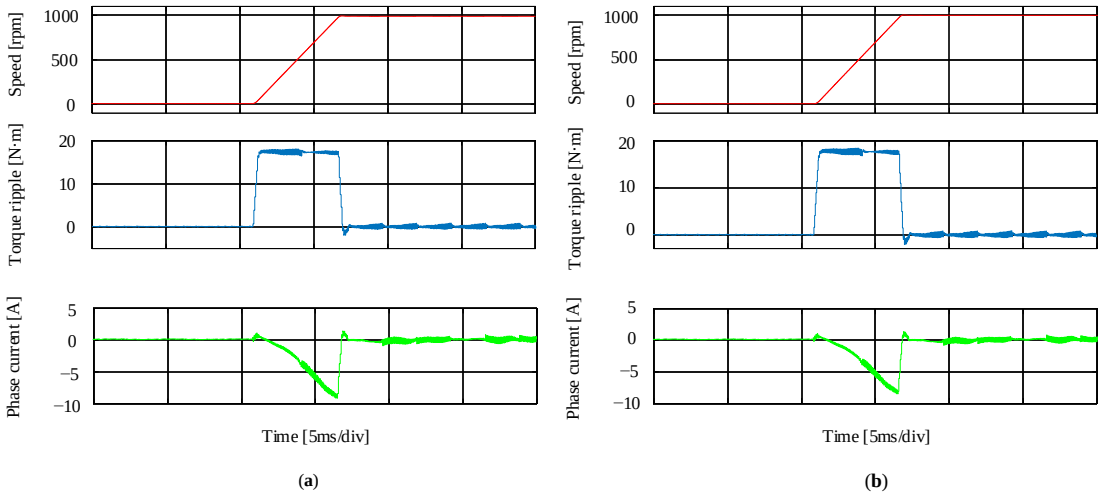


Figure 9. Dynamic performance for PMSM operating from static to rated speed without load. (**a**). Conventional NSPWM. (**b**). Improved NSPWM.

4.3. Switching Loss Analysis

To analyze the switching loss of the IGBT, a thermal model was established in the PLECS environment and a thermal library was established based on the IGBT datasheet in Figure 10. Figure 11a,b show the three-phase inverter conductivity, switching loss and the phase current waveforms for the conventional NSPWM and the proposed method in a one-carrier cycle, respectively. The electrical angle waveforms of PMSM are shown at the top of Figure 11. The switching loss waveform comparison of the inverter show that the proposed method has less energy loss compared with the conventional NSPWM. This further proves that the proposed method optimizes the switching loss by optimizing the division of sectors.

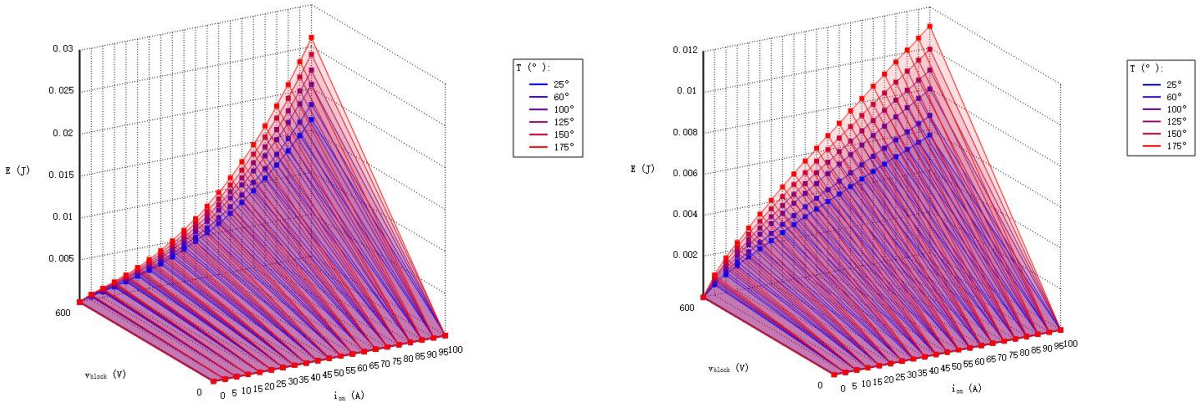


Figure 10. Thermal library. (**a**). Turn-on energy loss. (**b**). Turn-off energy loss.

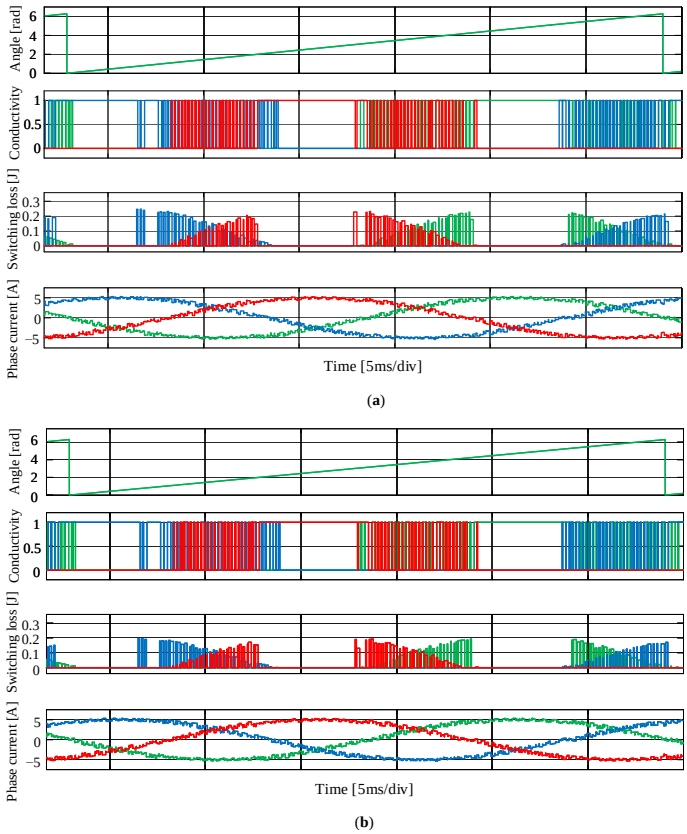


Figure 11. *Cont.*

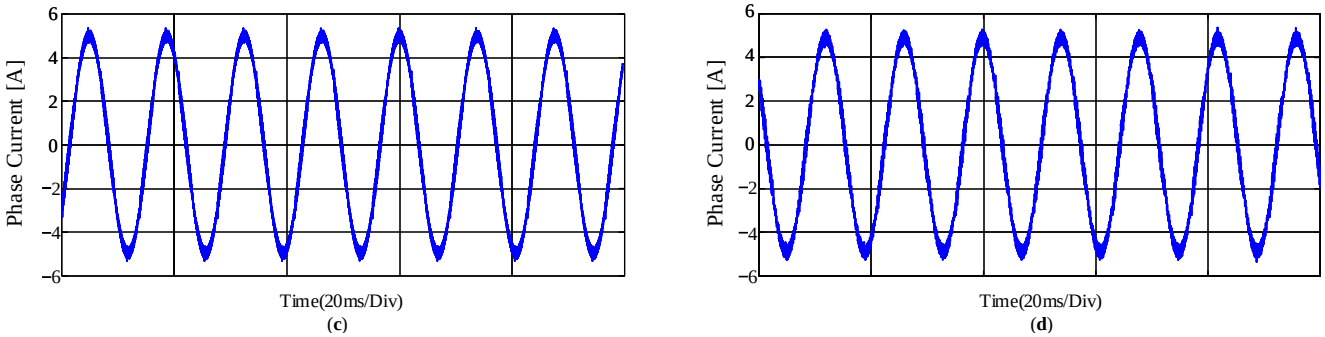


Figure 11. Switching loss comparison analysis over one carrier cycle. (**a**). Conventional NSPWM. (**b**). Improved NSPWM. (**c**). Phase current for conventional NSPWM. (**d**). Phase current for improved NSPWM.

5. Experiment Results

To show the correctness of the proposed method, the experimental platform was set up in Figure 12 according to Table 4. The parameters of the PMSM are presented in Table 3, and a magnetic powder brake with a rated torque of 10 N·m is used as the load of PMSM. The torque and speed are converted into analog signals with a refresh rate of 5 kHz through the DAC module.

Table 4. Parameters of experimental platform.

Description	Value (Type)
IGBT module	FS400R07AE3
Film capacitor	400 μF/600 V
DC-link voltage	270V
DC source	PR300-4
Current sensors	ACS724-10AB
DSP	TMS320F28335
Carrier and sampling frequency	10 kHZ

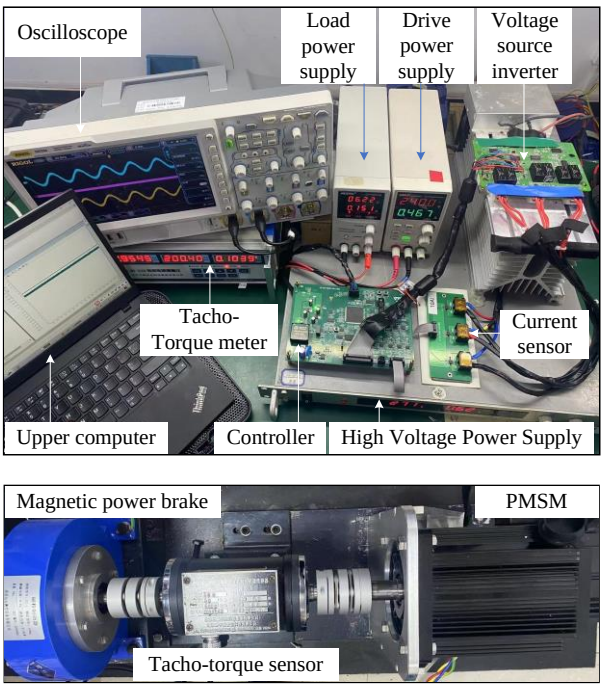


Figure 12. Experimental platform of PMSM control system.

5.1. Steady-State Performance

Experimental verification used the same operating conditions as the simulation. For the operational condition, 1000 rpm with a load of 10 N·m, u_{ref} was located in the linear region of NSPWM. The steady experimental waveforms are shown in Figure 13a,b, and the current THD analysis results are shown in Figure 14a,b for the conventional NSPWM and the proposed method, respectively. The results show that the proposed method has the same steady-state performance as the conventional NSPWM method, operating with good current ripple.

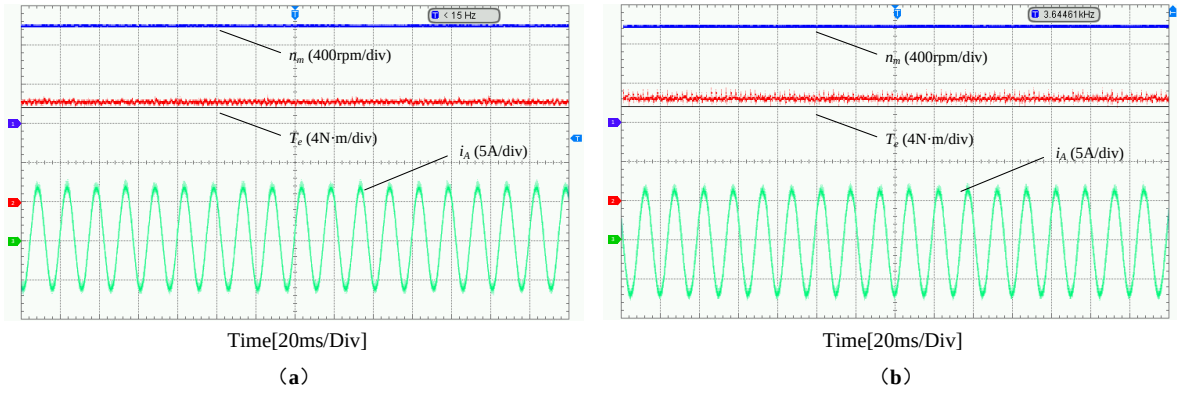


Figure 13. Steady-state waveform experiment results. (**a**). Conventional NSPWM. (**b**). Proposed method.

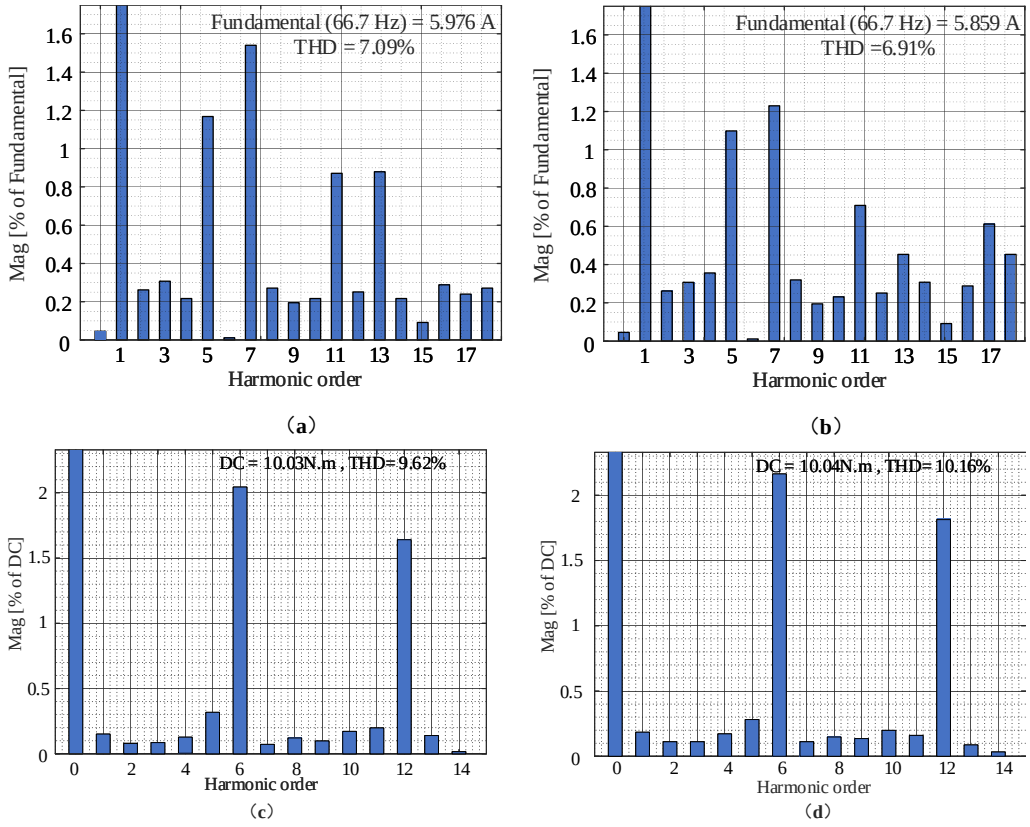


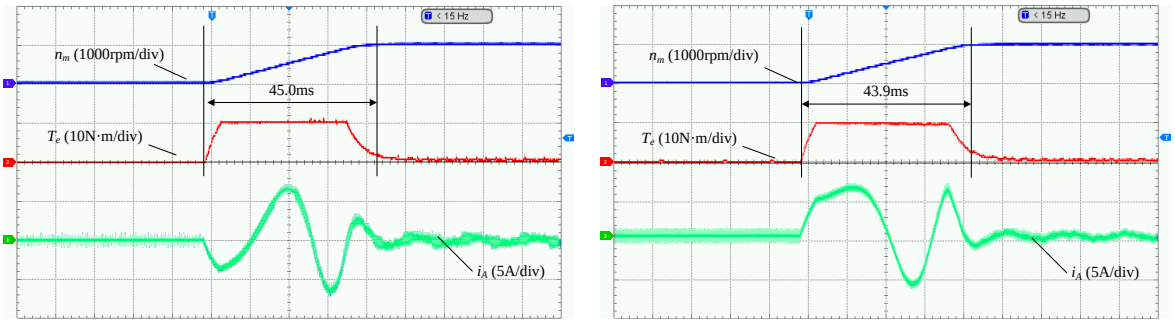
Figure 14. Steady-state experiment current and load torque THD analysis. (**a**). Current THD for conventional NSPWM. (**b**). Current THD for proposed method. (**c**). Load torque THD for conventional NSPWM (**d**). Load torque THD for proposed method.

The main harmonic components of the phase current are 5th, 7th, 11th and 13th orders, which are reflected in the 6th and 12th components in the torque. Meanwhile, the current

THD of the proposed method is slightly smaller than that of the conventional NSPWM, so the electromagnetic torque THD of the proposed method is 9.62%, which is less than that of the conventional NSPWM.

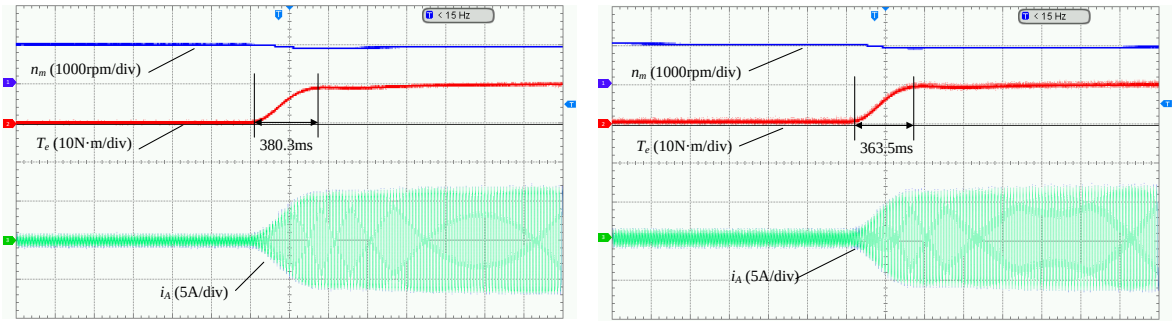
5.2. Dynamic-State Performance

To verify the dynamic performance of the proposed method, the speed step and load step experiments were set up, from static to rated speed without load (Figure 15a,b) and load increasing from no load to rated load at rated speed (Figure 16a,b). The results show that the proposed improved NSPWM has a similar response time to the conventional NSPWM, which proves that the proposed improved NSPWM has a similar dynamic performance to the conventional NSPWM.



(**a**) (**b**)

Figure 15. Dynamic speed step experiment results. (**a**). Conventional NSPWM. (**b**). Proposed method.



(**a**) (**b**)

Figure 16. Dynamic load step experiment results. (**a**). Conventional NSPWM. (**b**). Proposed method.

5.3. Switching Loss Analysis

The switching loss of the inverter in various operation conditions is collected, as well as for PMSMs operating at rated speeds with different load torques (Figure 17) and for PMSMs operating at rated load torques with different speeds (Figure 18). According to Equations (16) and (18), the switching loss is linearly proportional to the current peak value, so the mathematical switching loss results, the current peak value and the measured switching loss are all shown in these figures. Obviously, the switching loss of the proposed improved NSPWM is less than the conventional NSPWM under all operational conditions. The results show that, with the increase in load torque, the current magnitude increases, so the switching loss is also nearly linearly proportional to the increase. But the speed does not affect the current magnitude, so the switching loss remains nearly the same. Meanwhile, the theortical results from Equations (16) and (18) have little error with the experimental switching loss results, which prove the correctness of the derived switching loss analytic formula (Equations (16) and (18)) for the improved NSPWM and conventional NSPWM.

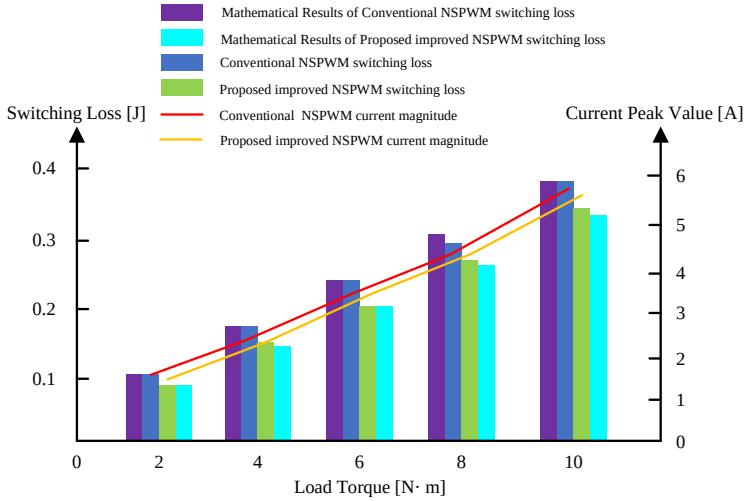


Figure 17. Switching loss at different speeds.

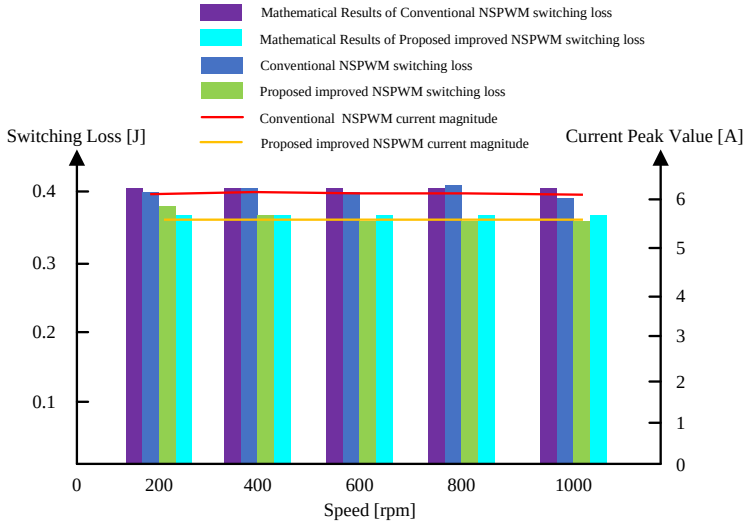


Figure 18. Switching loss at different load torques.

5.4. Common-Mode Voltage Analysis

To verify the common-mode voltage reduction performance of the proposed method, the steady-state CMV results are collected for the proposed method and SVPWM for comparison in Figure 19a,b. Because of the benefits of the voltage vector synthesizing strategy, the common-mode voltage waveform results show that the proposed improved NSPWM reduces the common-mode voltage peak value by three times compared with SVPWM.

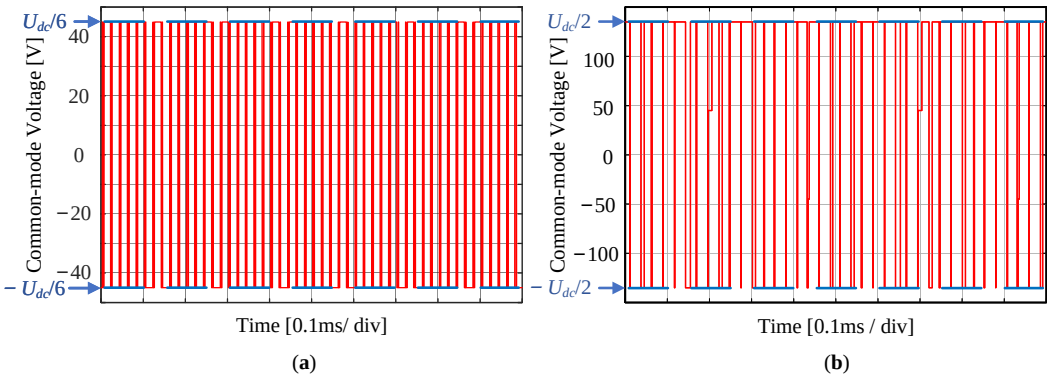


Figure 19. Common-mode voltage. (**a**). The proposed method. (**b**). Conventional SVPWM.

6. Conclusions

To optimize the switching loss of the common-mode voltage suppressing scheme, this paper has proposed an improved near-state pulse-width modulation scheme. The proposed NSPWM optimizes the sector division, introducing a power factor angle to dynamically adjust the sector division and ensure the longest voltage clamping for the largest current. The feasibility and correctness are verified by the simulation and experimental results. The main conclusions can be summarized as follows:

1. The proposed method ensures the switching tube that has the biggest conduction current has no switching action. So, the least switching loss can be obtained.
2. According to the derived switching loss analytic formula, the proposed method has the least switching loss, and it does not relate to the power factor angle.
3. The proposed method has the same steady-state performance and dynamic-state performance as the conventional NSPWM because it only introduces a power factor that does not change the vector synthesized strategy.

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Conflicts of Interest: The authors declare no conflicts of interest.

References

1. Miao, Y.; Liao, W.; Huang, S.; Liu, P.; Wu, X.; Song, P.; Li, G. DC-Link Current Minimization Scheme for IM Drive System Fed by Bidirectional DC Chopper-Based CSI. *IEEE Trans. Transp. Electrif.* **2023**, *9*, 2839–2850. [CrossRef]
2. Roy, T.; Tesfay, M.W.; Nayak, B.; Panigrahi, C.K. A 7-Level Switched Capacitor Multilevel Inverter With Reduced Switches and Voltage Stresses. *IEEE Trans. Circuits Syst. II Express Briefs* **2021**, *68*, 3587–3591. [CrossRef]
3. Dong, Z.; Liu, C. Three-Dimension Space Vector Modulation for Three-Phase Series-End Winding Voltage-Source Inverters. *IEEE Trans. Ind. Electron.* **2024**, *71*, 82–92. [CrossRef]
4. Ayano, H.; Nakagaki, T.; Iguchi, Y.; Matsui, Y.; Itoh, J.-i. Theoretical Study of Rampwise DPWM Technique to Reduce Motor Acoustic Noise. *IEEE Trans. Power Electron.* **2023**, *38*, 8102–8114. [CrossRef]
5. Zhang, X.; Hou, B. Double Vectors Model Predictive Torque Control Without Weighting Factor Based on Voltage Tracking Error. *IEEE Trans. Power Electron.* **2018**, *33*, 2368–2380. [CrossRef]
6. Dabour, S.; Abdel-Wahab, S.M.; Rashad, E.M. Common-Mode Voltage Reduction Algorithm with Minimum Switching Losses for Three-Phase Inverters. In Proceedings of the 21st International Middle East Power Systems Conference (MEPCON), Cairo, Egypt, 17–19 December 2019; Volume 9, pp. 1210–1215.
7. Kan, S.; Ruan, X.; Huang, X.; Dang, H. Second Harmonic Current Reduction for Flying Capacitor Clamped Boost Three-Level Converter in Photovoltaic Grid-Connected Inverter. *IEEE Trans. Power Electron.* **2021**, *36*, 1669–1679. [CrossRef]
8. Xu, Z.; Wang, Z.; Wang, X. A predictive current control method for a T-type three-level dual three-phase pmsm with zero common-mode voltage. *Proc. CSEE* **2020**, *40*, 4301.
9. Xing, X.; Li, X.; Qin, C.; Chen, J.; Zhang, C. An Optimized Zero-Sequence Voltage Injection Method for Eliminating Circulating Current and Reducing Common Mode Voltage of Parallel-Connected Three-Level Converters. *IEEE Trans. Ind. Electron.* **2020**, *67*, 6583–6596. [CrossRef]
10. Wu, M.; Xue, C.; Li, Y.W.; Yang, K. A Generalized Selective Harmonic Elimination PWM Formulation With Common-Mode Voltage Reduction Ability for Multilevel Converters. *IEEE Trans. Power Electron.* **2021**, *36*, 10753–10765. [CrossRef]
11. Li, W.; Wang, Y.; Hu, J.; Yang, H.; Li, C.; He, X. Common-mode current suppression of transformer-less nested five-level converter with zero common-mode vectors. *IEEE Trans. Power Electron.* **2019**, *34*, 4249. [CrossRef]
12. Xiang, Y.; Pei, X.; Wang, M.; Shi, P.; Kang, Y. An Improved H8 Topology for Common-Mode Voltage Reduction. *IEEE Trans. Power Electron.* **2019**, *34*, 5352–5361. [CrossRef]
13. Li, P.; Adam, G. P.; Hu, Y.; Holliday, D.; Williams, B. W. Three-Phase AC-Side Voltage-Doubling High Power Density Voltage Source Converter With Intrinsic Buck–Boost Cell and Common-Mode Voltage Suppression. *IEEE Trans. Power Electron.* **2015**, *30*, 5284–5298. [CrossRef]

14. Guo, L.; Jin, N.; Gan, C.; Xu, L.; Wang, Q. An Improved Model Predictive Control Strategy to Reduce Common-Mode Voltage for Two-Level Voltage Source Inverters Considering Dead-Time Effects. *IEEE Trans. Ind. Electron.* **2019**, *66*, 3561–3572. [CrossRef]
15. Lai, Y.-S.; Shyu, F.-S. Optimal common-mode Voltage reduction PWM technique for inverter control with consideration of the dead-time effects-part I: Basic development. *IEEE Trans. Ind. Appl.* **2004**, *40*, 1605–1612. [CrossRef]
16. Guo, Y.; Zhang, J.; Wang, S.; Jin, P. Common-mode voltage suppression strategy of PMSM system using model predictive control. *Electr. Mach. Control* **2024**, *28*, 56–65.
17. Hava, A.M.; Ün, E. Performance Analysis of Reduced Common-Mode Voltage PWM Methods and Comparison With Standard PWM Methods for Three-Phase Voltage-Source Inverters. *IEEE Trans. Power Electron.* **2009**, *24*, 241–252. [CrossRef]
18. Qing, P.; Xiong, J.; Ma, F. A Model Predictive Control Scheme with Minimum Common-Mode Voltage for PMSM Drive System Fed by VSI. *Machines* **2024**, *12*, 292. [CrossRef]
19. Dong, H.; Zhang, Y. A Low-Complexity Double Vector Model Predictive Current Control for Permanent Magnet Synchronous Motors. *Energies* **2024**, *17*, 147. [CrossRef]
20. Yang, R.; Li, L.; Wang, M.; Zhang, C. Force Ripple Compensation and Robust Predictive Current Control of PMLSM Using Augmented Generalized Proportional–Integral Observer. *IEEE J. Emerg. Sel. Top. Power Electron.* **2021**, *9*, 302–315. [CrossRef]
21. Ayachit, A.; Kazimierczuk, M. K. Averaged Small-Signal Model of PWM DC-DC Converters in CCM Including Switching Power Loss. *IEEE Trans. Circuits Syst. II Express Briefs* **2019**, *66*, 262–266. [CrossRef]
22. Ma, Z.; Pei, Y.; Wang, L.; Yang, Q.; Qi, Z.; Zeng, G. An Accurate Analytical Model of SiC MOSFETs for Switching Speed and Switching Loss Calculation in High-Voltage Pulsed Power Supplies. *IEEE Trans. Power Electron.* **2023**, *38*, 3281–3297. [CrossRef]

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