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Novel Integrated Zeta Inverter for Standalone Applications

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Abstract: In recent years, distributed generation systems based on renewable energy sources have gained increasing prominence. Thus, the DC/AC converters based on power electronics devices have become increasingly important. In this context, this article presents an integrated Zeta inverter for low-power conditions, which operates in continuous conduction mode (CCM), achieving efficiency greater than 95%. The proposed topology is composed of four power switches, two operating at high frequency and two operating at low frequency, i.e., at the output frequency. Compared with the topologies in the literature, these configurations make it a competitive solution from the point of view of efficiency, number of elements, and, consequently, implementation cost. The proposed converter operates as a sinusoidal voltage source for local loads and is supplied by a DC source, such as batteries or a photovoltaic array. A multi-resonant voltage controller was used to guarantee the sinusoidal voltage provided to the non-linear load while dealing with the complex dynamics of the Zeta converter in the CCM. Experimental results from a 324 W prototype show the converter's implementation feasibility and the high efficiency of the DC/AC conversion.

Keywords: DC/AC conversion; integrated inverter; power electronics; Zeta inverter

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1. Introduction

With the electrical energy demand increase and the growing concern about the decarbonization of the power system, distributed generation (DG) based on renewable energy sources (RES) is gaining more and more prominence, to the detriment of energy sources based on fossil fuels [1].

In this context, devices based on power electronics are a key point for this energy transition, given that the DG energy must be conditioned to be used in conjunction with the grid or to supply energy to local loads [2]. Therefore, when choosing a converter topology that integrates DG, the load is directly linked to its efficiency and cost, which are directly related to the quantity, arrangement, and quality of switches and passive elements in the converter.

When dealing with photovoltaic (PV) systems, the DC/AC converters used can be single-stage [3,4], in which the PV array is connected directly to the inverter's DC-link, or double-stage [5–7], in which there is a DC/DC stage voltage adjustment between the PV array and the inverter's DC-link. Although single-stage topologies are more efficient, as they have one less conversion stage, the PV array output voltage must be equal to the inverter DC-link voltage, which implies many PV panels in series and partial shading problems [8], in addition to the impossibility of using them at low powers. On the other hand, in addition to reduced efficiency, double-stage topologies tend to be more expensive due to the increase in the number of active and passive components [9–11]. In this context, low-power integrated converters have been gaining prominence for various DC/AC conversion applications, as they simultaneously increase the input voltage and synthesize sinusoidal voltages/currents at the output. Thus, integrated converters make it possible to improve conversion efficiency and minimize converter volume and costs [12,13].

Integrated converters based on the Zeta converter have been proposed in the literature. In [10], an isolated converter operating in the continuous conduction mode (CCM) was proposed. This converter uses five power switches, two inductors, and a high-frequency transformer. According to the authors, the converter efficiency around the nominal power was approximately 93%. Also operating in CCM, in [11], an isolated bridgeless Zeta inverter was proposed. The topology comprises five power switches, a high-frequency transformer, and an LCL output filter. Considering the dynamic response of the proposed converter, which is influenced by a right half-plane zero, the output is controlled using a repetitive controller. In [14], a non-isolated integrated inverter based on Zeta topology is proposed, which operates without an electrolytic input capacitor. Despite the absence of an electrolytic capacitor and the ability to reject common mode current, the inverter topology utilizes six power switches, three diodes, and two inductors, besides needing a specific modulation strategy.

This paper aims to contribute to the scenario of renewable energy by proposing a novel low-power integrated inverter based on the Zeta converter, named single-phase integrated Zeta inverter (SP-IZI). The converter is composed of four switches, two of which operate at high frequency, while the other two operate at low frequency, more specifically at the frequency of the output voltage. In this paper, the converter is presented to operate as a sinusoidal voltage source in standalone mode, which is helpful in supplying local loads from a DC voltage source, such as a PV array or a battery.

This converter is the evolution of Zeta-based integrated inverters. In [15], the converter operates as a current source, injecting energy into the grid and into the discontinuous conduction mode (DCM). However, this integrated inverter employs series diodes connected to the input inductors, leading the system to present high voltages on the power switches, limiting the overall system operation. In [16], the converter was modified to solve this problem. However, the converter also operates in the DCM and is grid-tied as a current source.

The Zeta-based integrated inverter was also presented in [17], operating as a standalone sinusoidal voltage source for autonomous GD/battery systems. However, the operation in the DCM can be represented by less complex and challenging mathematical models from the point of view of the output voltage controller. However, using the converter in the CCM for the same power level reduces the RMS value of the currents in the power switches and diodes, which indicates a more efficient operation once the elevated RMS currents are related to conduction losses. Nonetheless, this article proposes the SP-IZI converter operating in the CCM, making it more efficient than previous proposals [15–17] and able to operate as a sinusoidal voltage source for local loads. At the same time, the proposed controller overcomes the difficulties in controlling the output voltage without the need to measure the output inductor current.

The SP-IZI topology proposed in this paper also presents some advantages when compared to [10,11,14], such as: (i) fewer switching devices and gate drivers; (ii) reduced costs by using fewer switching/gate-driver devices; and (iii) the use of a high-frequency transformer is not necessary for the system operation. Therefore, as the proposed SP-IZI employs unidirectional power switches, the inverter works with characteristics similar to those of the traditional Zeta converter.

Given the phase margin characteristics of the Zeta converter transfer function, the sinusoidal output voltage was controlled using a proportional–integrative multi-resonant controller. Thus, obtaining output voltage with low total harmonic distortion (THD) was possible even when operating with a non-linear load. The complete analysis, performance, efficiency, and development of the proposed SP-IZI are evaluated and validated via the experimental results.

This paper is organized as follows: Section 2 describes the SP-IZI topology and its operation in CCM, while Section 3 presents the switching logic and the mathematical modeling of the converter and the voltage controller. Section 4 presents and discusses the experimental results, and Section 5 presents the conclusions.

2. Description of the Integrated Zeta Inverter

The proposed SP-IZI operates in a symmetrical converter structure, as shown in Figure 1. This integrated inverter is deployed by integrating two modified Zeta converters. Each structure operates for the respective positive and negative half-wave cycles, defined by the actuation of the complementary low-frequency switches S_2 and S_4. The proposed topology can generate an AC-regulated voltage in its output.

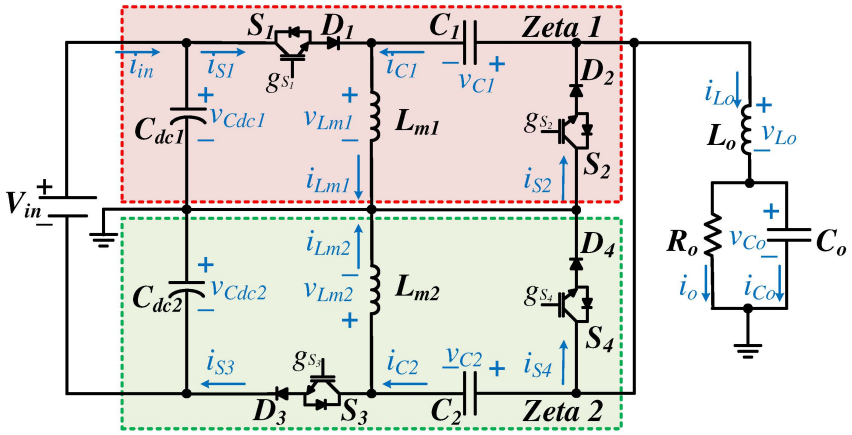


Figure 1. Power circuit of the proposed SP-IZI topology.

2.1. Positive Half-Wave Cycle

In the positive half-wave cycle, the low-frequency S_2 is turned on, and the Zeta converter related to the positive half-wave cycle (Zeta 1) is operational with its high-frequency S_1 switch. In this case, the switches S_3 and S_4 are switched off. However, considering the D_2 diode in series with S_2, the SP-IZI operating in the CCM presents two stages of operation for each high-frequency switching period, as shown in Figure 2. Considering the operation at the high switching frequency, the operation stages of the SP-IZI are similar to those of the traditional Zeta converter.

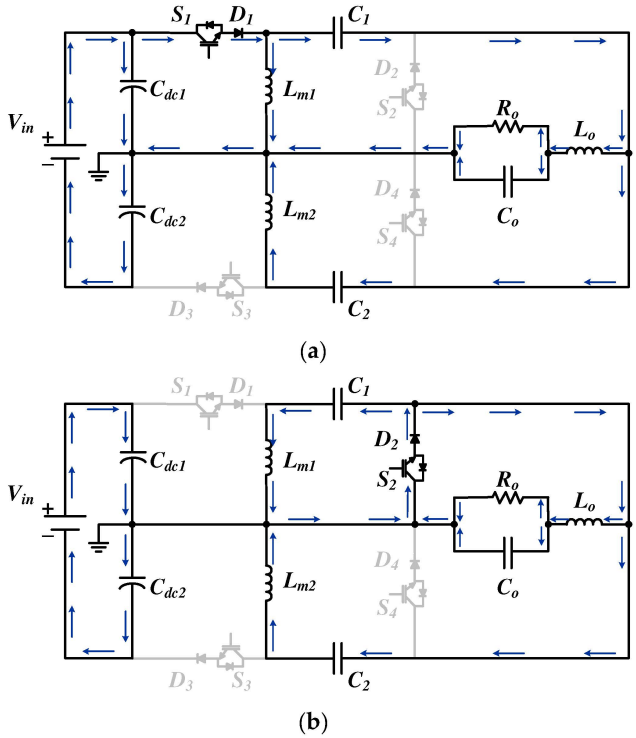


Figure 2. Operation intervals of the SP-IZI in the positive half-wave cycle: (**a**) D_pT_s; (**b**) D'_pT_s.

The first operation stage (D_pT_s) starts when the switch S_1 is turned on, when the energy flows through the diode D_1 and, in consequence, magnetizes the inductor L_{m1}. However, the diode D_2 is inverse-polarized, and its current is equal to zero. The voltage across the inductor L_{m1} is equal to the voltage in the capacitor C_{dc1}, i.e., ideally half of the input voltage V_{in}, defining the first equation. Already, the inductor L_o is magnetized by the sum of the voltages across the capacitors C_{dc1}, C_1 and C_o, i.e., $v_{Lo} = v_{C_{dc1}} + v_{C1} - v_{Co}$. The inductor L_{m2} is magnetized by the voltage across capacitors C_{dc1}, C_1 and C_2, i.e., $V_{Lm2} = v_{C_{dc1}} + v_{C1} - v_{C2}$. The equivalent electrical circuit of this operation interval is presented in Figure 2a.

The second interval (D'_pT_s) starts when the switch S_1 is turned off, blocking the diode D_1. In this interval, the inductor L_{m1} is demagnetized, transferring its accumulated energy to the capacitor C_1 through the switch S_2 and the diode D_2. Thus, the voltage on the inductor L_{m1} is the same as that of the capacitor C_1, while the voltage across the inductor L_o is the same as the voltage in the output capacitor C_o, and the voltage across inductor L_{m2} equals the capacitor C_2 voltage. This interval can be seen in Figure 2b.

2.2. Negative Half-Wave Cycle

In the negative half-wave cycle, the low-frequency S_4 is turned on, and the Zeta converter related to the negative half-wave cycle (Zeta 2) is operational with its high-frequency switch S_3. In this case, the switches S_1 and S_2 are switched off. In the same way as for the positive half-wave cycle, the diode D_4 in series with S_4 operates in a complementary way to the power switch S_3, and the SP-IZI operating in the CCM presents two stages of operation, as shown in Figure 3.

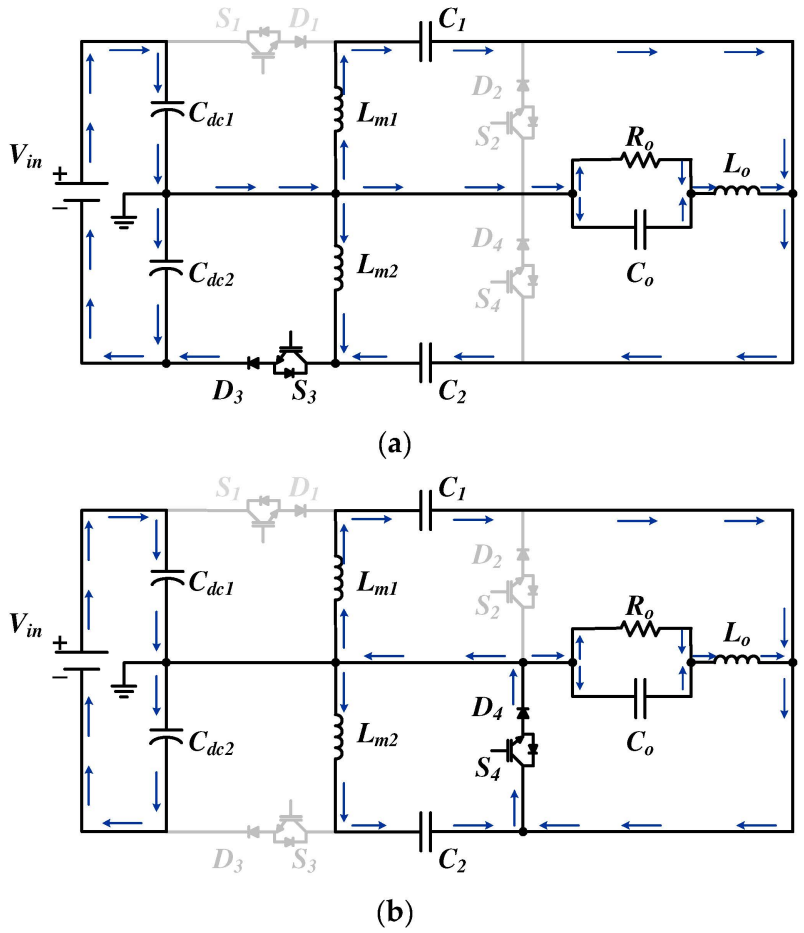


Figure 3. Operation intervals of the SP-IZI in the negative half-wave cycle: (**a**) D_nT_s; (**b**) D'_nT_s.

The first operation interval (D_nT_s) of the negative half-wave cycle starts when the switch S_3 is commuted on; here, the diode D_3 is forward-biased and, in consequence, magnetizes the inductor L_{m2}. During this interval, the diode D_4 is reverse-biased. The voltage across the inductor L_{m2} is equal to the voltage across the capacitor C_{dc2}, ideally half of the input voltage. Already, the inductor L_o is magnetized by the sum of the voltages across the capacitors C_{Cdc2}, C_2 and C_o, i.e., $v_{Lo} = -v_{C_{dc2}} + v_{C2} - v_{Co}$. The inductor L_{m1} is magnetized by the sum of the voltages across the capacitors C_{Cdc2}, C_1 and C_2, resulting in $v_{L_{m1}} = -v_{C1} + v_{C2} - v_{C_{dc2}}$. The equivalent electrical circuit of this operation interval is presented in Figure 3a.

The second interval (D'_nT_s) starts when the switch S_3 is turned off, blocking the diode D_3 and turning on the diode D_4. In this interval, the inductor L_{m2} is demagnetized, transferring its accumulated energy to the capacitor C_2 through the switch S_4 and the diode D_4. Thus, the voltage on the inductor L_{m2} is the same as that of the capacitor C_2, while the voltage across the inductor L_o is the same as the voltage in the output capacitor C_o. This interval can be seen in Figure 3b.

3. Output Voltage Control of SP-IZI

The SP-IZI operates with two high-frequency and two low-frequency power switches. Thus, Figure 4 presents a block diagram of the proposed converter's switching logic. As can be seen, the decision criterion for defining the switches and, consequently, the converter in operation is the sign of output voltage reference signal. This sinusoidal signal is self-generated and has 60 Hz. When it operates in its positive half-cycle, the Zeta 1 converter switches (see Figure 1) are in operation. When the output voltage reference is negative, the Zeta 2 converter switches operate. In this way, the low-frequency switches operate at the output voltage frequency. On the other hand, high-frequency switches are driven by a PWM modulator, with modulating signal d generated by the controller. Finally, this control signal d is rectified before being compared with the sawtooth-shaped carrier.

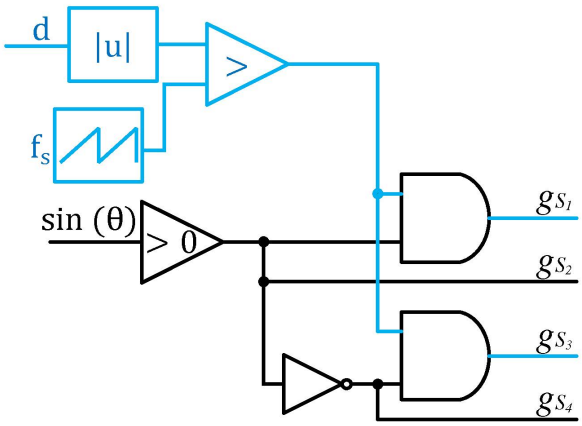


Figure 4. Block diagram of the modulation technique applied in the SP-IZI inverter.

In this paper, the SP-IZI is controlled to operate as an AC single-phase voltage source, delivering an AC-regulated voltage to the load. The mathematical model that represents the output voltage v_{Co} from the duty-cycle d was achieved from the SP-IZI equivalent circuit, which can be obtained considering that both Zeta-modified converters operate symmetrically. The high-frequency equivalent circuit of the SP-IZI converter is shown in Figure 5. It is important to highlight that the low-frequency switches are disregarded. This circuit considers the equivalent inductance $L_m = (L_{m1}L_{m2})/(L_{m1} + L_{m2})$ and capacitance $C_a = (C_1 + C_2)$.

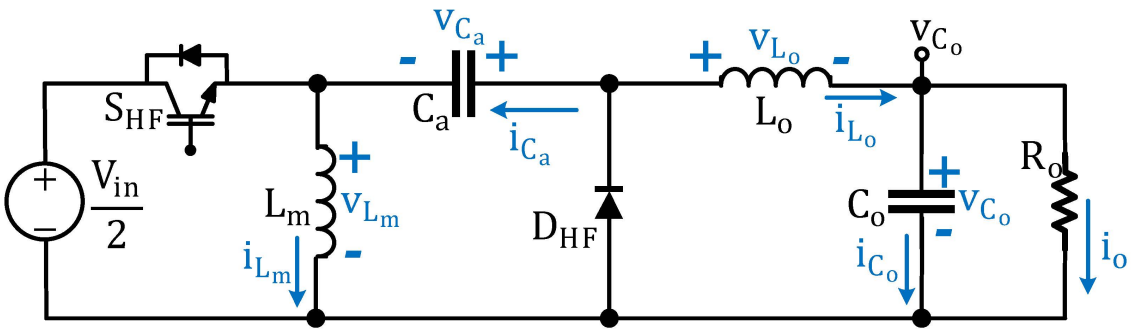


Figure 5. Equivalent high-frequency circuit of the SP-IZI converter operating as a voltage source.

From this circuit, it is possible to obtain the differential equations representing the circuits formed in the two operation stages. All the elements were considered as ideal. When the high-frequency switch is turned on, the equations for the derivatives of states are presented below:

$$\underbrace{\begin{bmatrix} \dot{i}_{L_m} \\ \dot{i}_{L_o} \\ \dot{v}_{C_a} \\ \dot{v}_{C_o} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 0 \\ 0 & 0 & \frac{1}{L_o} & -\frac{1}{L_o} \\ 0 & -\frac{1}{C_a} & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & -\frac{1}{R_o C_o} \end{bmatrix}}_{A_D} \underbrace{\begin{bmatrix} i_{L_m} \\ i_{L_o} \\ v_{C_a} \\ v_{C_o} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} \frac{1}{L_m} \\ \frac{1}{L_o} \\ 0 \\ 0 \end{bmatrix}}_{B_D} \underbrace{\begin{bmatrix} \frac{V_{in}}{2} \end{bmatrix}}_{u} \tag{1}$$

On the other hand, when the high-frequency switch is turned off, the diode is forward-biased. Thus, the equations for the derivatives of states are shown below.

$$\underbrace{\begin{bmatrix} \dot{i}_{L_m} \\ \dot{i}_{L_o} \\ \dot{v}_{C_a} \\ \dot{v}_{C_o} \end{bmatrix}}_{\dot{x}} = \underbrace{\begin{bmatrix} 0 & 0 & -\frac{1}{L_m} & 0 \\ 0 & 0 & 0 & -\frac{1}{L_o} \\ \frac{1}{C_a} & 0 & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & -\frac{1}{R_o C_o} \end{bmatrix}}_{A_{D'}} \underbrace{\begin{bmatrix} i_{L_m} \\ i_{L_o} \\ v_{C_a} \\ v_{C_o} \end{bmatrix}}_{x} + \underbrace{\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}}_{B_{D'}} \underbrace{\begin{bmatrix} \frac{V_{in}}{2} \end{bmatrix}}_{u} \tag{2}$$

The small-signal modeling technique [18] was applied to obtain the small-signal model of the converter. The variables in capital letters are the values calculated in the nominal operation point of the converter. In this analysis, D' is the complementary value of the nominal duty-cycle D, calculated as $D' = 1 - D$.

$$\underbrace{\begin{bmatrix} \dot{\hat{i}}_{L_m} \\ \dot{\hat{i}}_{L_o} \\ \dot{\hat{v}}_{C_a} \\ \dot{\hat{v}}_{C_o} \end{bmatrix}}_{\dot{\hat{x}}} = \underbrace{\begin{bmatrix} 0 & 0 & -\frac{D'}{L_m} & 0 \\ 0 & 0 & -\frac{D}{L_o} & -\frac{1}{L_o} \\ \frac{D'}{C_a} & -\frac{D}{C_a} & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & -\frac{1}{R_o C_o} \end{bmatrix}}_{\hat{A}} \underbrace{\begin{bmatrix} \hat{i}_{L_m} \\ \hat{i}_{L_o} \\ \hat{v}_{C_a} \\ \hat{v}_{C_o} \end{bmatrix}}_{\hat{x}} + \underbrace{\begin{bmatrix} \frac{V_g + V_{Ca}}{L_m} & \frac{D}{L_m} \\ \frac{V_g + V_{Ca}}{L_o} & \frac{D}{L_o} \\ 0 & 0 \\ 0 & 0 \end{bmatrix}}_{\hat{B}} \underbrace{\begin{bmatrix} \hat{d} \\ \hat{v}_g \end{bmatrix}}_{\hat{u}} \tag{3}$$

$$\hat{y} = \underbrace{\begin{bmatrix} 0 & 0 & 0 & 1 \end{bmatrix}}_{\hat{C}} \underbrace{\begin{bmatrix} \hat{i}_{L_m} \\ \hat{i}_{L_o} \\ \hat{v}_{C_a} \\ \hat{v}_{C_o} \end{bmatrix}}_{\hat{x}}$$

From the state-space model (3), it is possible to obtain the small signal transfer function of the output voltage $\hat{v}_{Co}$ from the duty-cycle $\hat{d}$ by applying it in (4) [19]:

$$G_{vd}(s) = \frac{\hat{v}_{C_o}(s)}{\hat{d}(s)} = \hat{C}(sI - \hat{A})^{-1}\hat{B} \tag{4}$$

where s is the Laplace variable and I is an identity matrix with the dimension of $\hat{A}$.

Thus, in terms of the converter parameters, the transfer function $G_{vd}(s)$ is presented below.

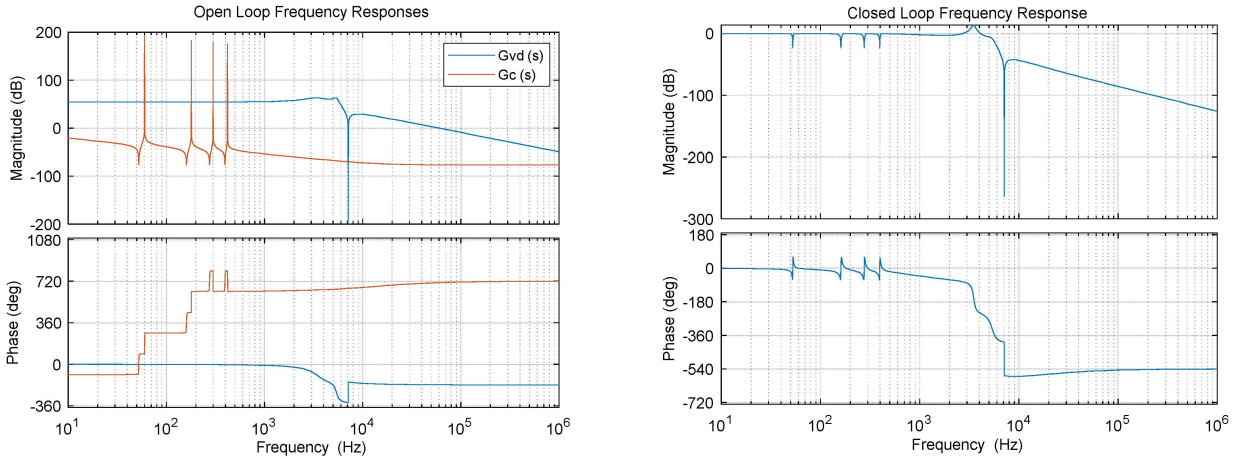
$$G_{vd}(s) = \frac{\hat{v}_{C_o}(s)}{\hat{d}(s)} = R_o\left(V_{Ca} + \frac{V_{in}}{2}\right)\frac{C_a L_m s^2 + D'^2 + DD'}{C_a C_o L_m L_o s^4 + C_a L_m L_o s^3 + \left(C_o L_o R_o D'^2 + C_a L_m R_o + C_o L_m R_o D^2\right)s^2 + \left(L_o D'^2 + L_m D^2\right)s + D'^2 R_o} \tag{5}$$

Considering the converter parameters presented in Table 1, the transfer function's open loop frequency response is presented in Figure 6a. As can be seen, there is a range at low frequencies in which the system can be controlled with a proportional–integral (PI) controller since the open-loop phase of the system is between 0° and 180° [20]. Therefore, a PI voltage controller was used to ensure adequate settling time during transients and the rejections of harmonic components over a wide range of frequencies. On the other hand, the PI controller cannot provide a null steady-state error for sinusoidal references, or even the complete rejection of harmonic disturbances caused by non-linear load currents. Thus, a first-, third-, fifth-, or seventh-order multi-resonant (MR) controller was added in parallel to the PI controller, yielding a PI-MR controller [21]. The controller transfer function $G_c(s)$ is presented below.

$$G_c(s) = G_{PI}(s) + G_{MR}(s) = K_P + \frac{K_I}{s} + \sum_{n=1}^{7}\frac{K_n s}{s^2 + (2\pi n f)^2} \tag{6}$$

Table 1. SP-IZI specifications.

Parameter	Value
Nominal Output RMS Voltage	$V_o = 127$ V
Output Voltage Frequency	$f = 60$ Hz
Switching Frequency	$f_s = 50$ kHz
Sampling Frequency A/D Converter	$f_a = 60$ kHz
Input DC-Link Capacitance	$C_{dc1} = C_{dc2} = 4500$ µF
Nominal Input DC-Link Voltage	$v_{in} = 170$ V
Input Inductive Filter	$L_{m1} = L_{m2} = 200$ µH
Output Inductive Filter	$L_o = 1.5$ mH
Coupling Capacitances	$C_1 = C_2 = 1$ µF
Output Capacitance	$C_o = 1.5$ µF
Equivalent Capacitor Nominal Voltage	$V_{Ca} = V_o\sqrt{2}$ V
Nominal Duty-Cycle	$D = 0.5991$
Nominal Power	$P = 324$ W
Output Voltage Control System 0 dB Crossover Frequency	$f_0 = 500$ Hz
Output Voltage Control System Phase Margin	$\gamma = 89.99°$
Output Voltage Control System Proportional Gain	$K_P = 1.4522.10^{-4}$
Output Voltage Control System Integral Gain	$K_I = 5.7906$
DC-Link Unbalance Controller Proportional Gain	$K_{P_{unb}} = 1$
Gains of the Resonant Controllers	$K_1 = K_3 = K_5 = K_7 = \frac{5}{3}$



(**a**) (**b**)

Figure 6. Frequency responses of the control system: (**a**) Open-loop frequency responses of $G_{vd}(s)$ and $G_c(s)$ transfer function; (**b**) frequency response of the control system in the closed loop.

The PI controller was designed with specifications of a 0 dB crossover frequency f_0 and a phase margin of γ. The gains were obtained with the methodology presented in [20]. The design specifications and gains of the controllers are presented in Table 1. Figure 6a presents the controller's open-loop frequency response. In the 0 dB crossover frequency (f_0), the controller's gain compensates for the gain of the open loop system. At the same time, at resonant frequencies, the controllers guarantee gains tending to infinity. Thus, as shown in the closed-loop frequency response presented in Figure 6b, the system is stable and presents gains and phases equal to zero at the resonance frequencies. At the same time, there is a wide passband with the gain close to 0 dB and a small phase delay, indicating that the PI controller acts at frequencies with no tuned resonant controllers.

The block diagram of the control system is presented in Figure 7. As can be seen, the output reference voltage signal is obtained with a self-generated sinusoidal wave with the desired output frequency. Furthermore, the SP-IZI presents a split-capacitor structure in its DC-link. Thus, it is necessary to implement a voltage unbalance controller to prevent the DC-link capacitor voltages from diverging [22]. We implemented a proportional controller with unitary gain $K_{P_{unb}}$.

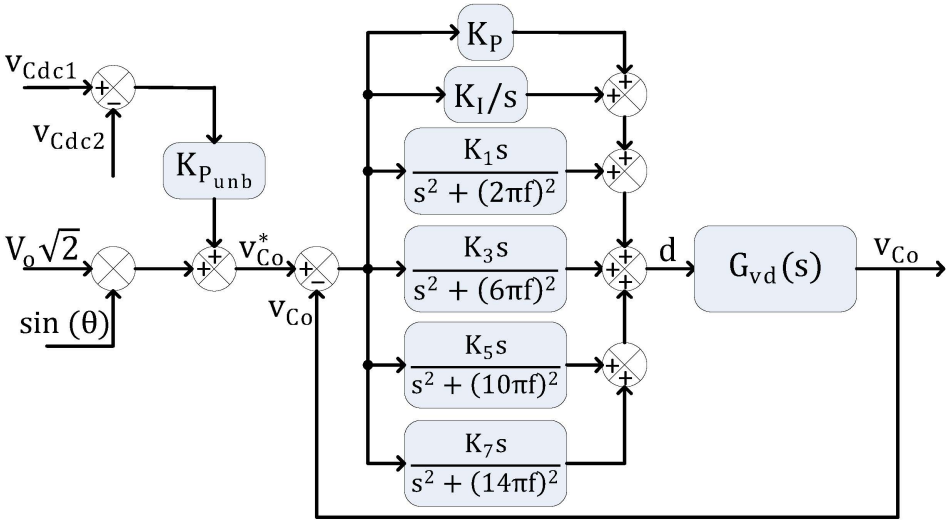


Figure 7. Block diagram of the output voltage control system.

4. Experimental Results

A 324 W prototype was developed to experimentally evaluate the proposed SP-IZI, as shown in Figure 8a. The power switches were placed under the printed circuit board and could not be visualized. The experimental setup was deployed using discrete CoolMOS switches IPW65R037C6 (Infineon, Neubiberg, Germany) and SiC Schottky diodes FFSP2065B-F085 (OnSemi, Poenix, AZ, USA). It is important to highlight that it is a modular prototype, helpful in evaluating some other topologies. Thus, the conditioning signal system has more components than the SP-IZI control system. The block diagram of the control system implemented in discrete time is presented in Figure 8b. The voltage and current quantities were measured using LEM transducers, and the signals were conditioned by specific conditioning boards. All the controllers and algorithms were embedded into the digital signal controller TMS320F28335 (Texas Instruments, Dallas, TX, USA), and the output voltage controller was discretized using the Tustin method. The power quality indexes and system efficiency were measured by Fluke 43B and Yokogawa WT3000, respectively, while the waveforms were collected with a digital oscilloscope 190 series II (Fluke, Everett, WA, USA). The main SP-IZI parameters employed for building the experimental tests are presented in Table 1.

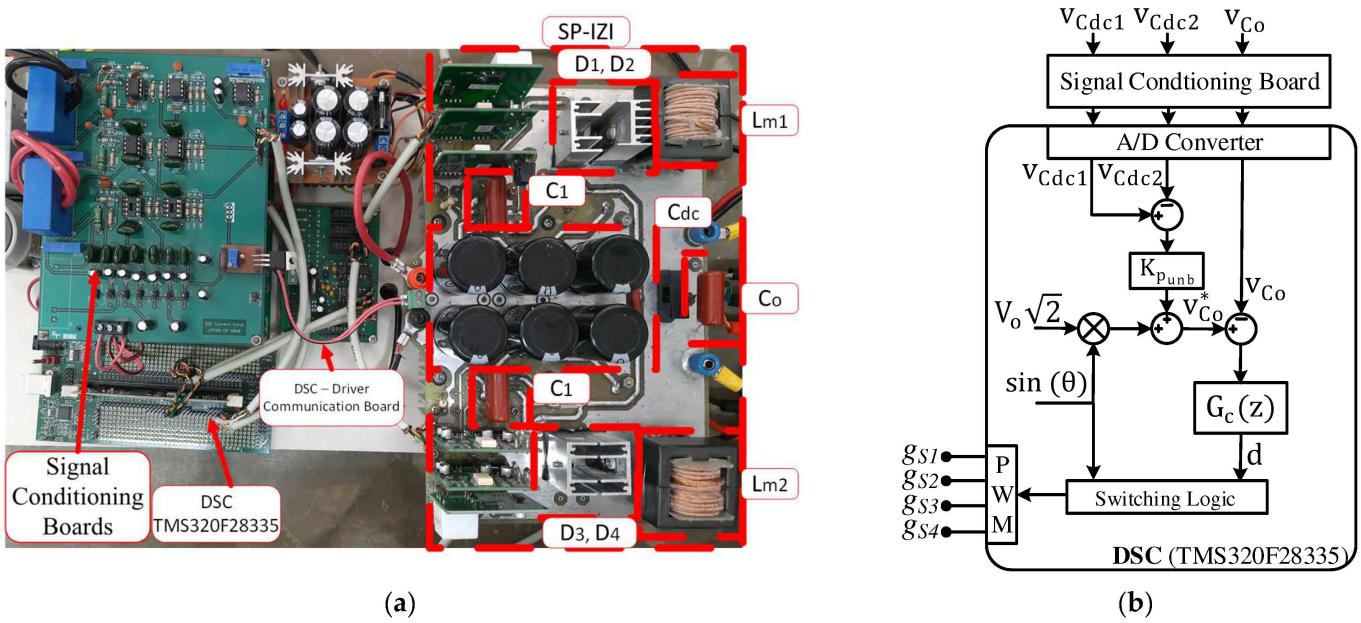


Figure 8. SP-IZI experimental setup: (**a**) experimental setup; (**b**) control embedded into the DSC.

The topology was evaluated experimentally under several static conditions, considering resistive loads. This paper shows the waveforms of the tests with the resistive loads of 162 W and 324 W, as well as a test with a resistive load of 162 W in parallel with a single-phase rectifier followed by an RC Load (200 Ω and 100 µF), forming a non-linear load.

Figure 9 presents the experimental results obtained for the resistive loads mentioned above, in which the voltage and current supplied to the load are shown in conjunction with the currents of the inductors L_{m1} and L_{m2}. As demonstrated in Figure 9, the SP-IZI delivers a sinusoidal voltage to the loads in both conditions. The frequency spectra of the voltages supplied to the loads are shown in Figure 10. As can be seen, the output voltages are regulated and present low THD. At the same time, it is important to highlight that the main harmonic components that compose the voltage are at frequencies with no resonant controllers.

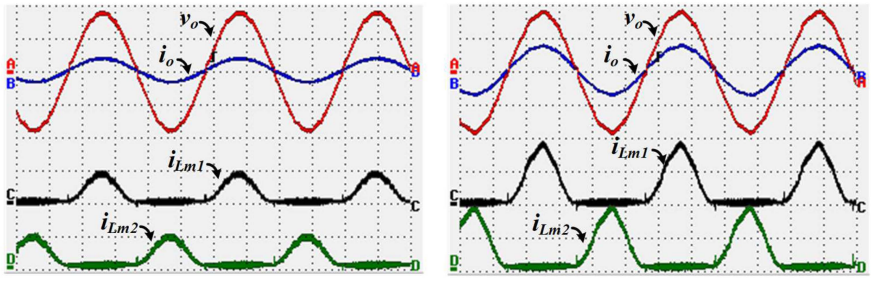


Figure 9. Experimental waveforms for 100 V/div, 5 A/div, 4 ms/div: (**a**) 162 W resistive load; (**b**) 324 W resistive load.

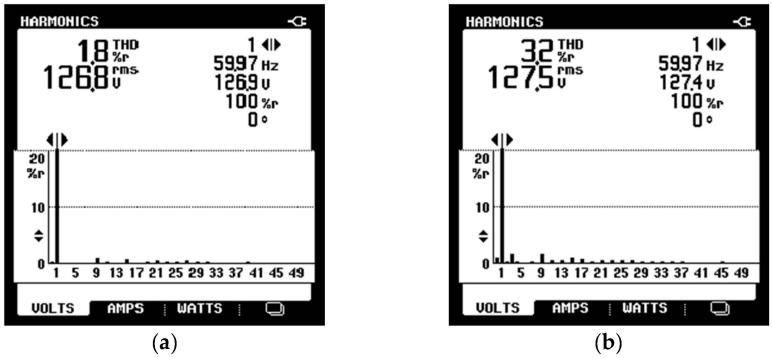


Figure 10. Frequency spectrum of the output voltage: (**a**) 162 W resistive load; (**b**) 324 W resistive load.

Figure 11a shows the waveforms of the output voltage and current considering the non-linear load. At the same time, the frequency spectra of these variables are shown in Figure 11b. As can be seen, the current drained by the load has a THD = 50.7%. On the other hand, the output voltage controlled by the SP-IZI reached THD = 4.2%, meeting the main power quality standards [23,24].

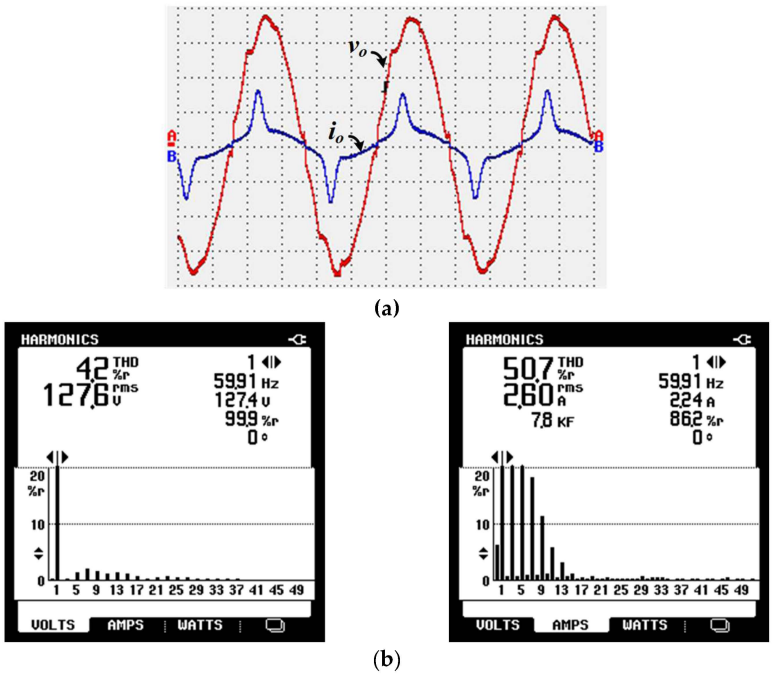


Figure 11. Experimental results for the non-linear load (50 V/div, 5 A/div, 4 ms/div): (**a**) waveforms of output voltage and current; (**b**) THD of the output voltage and current.

The efficiency of the SP-IZI operating in the CCM and as a sinusoidal voltage source was evaluated experimentally by varying the resistive load. Figure 12 shows a graph of the efficiency measured from the resistive load power. As can be observed, the efficiency is near 95% in a wide range of operation points. Thus, the SP-IZI is a suitable inverter for replacing the conventional cascade association of the DC/DC step-up converter with the voltage source inverter.

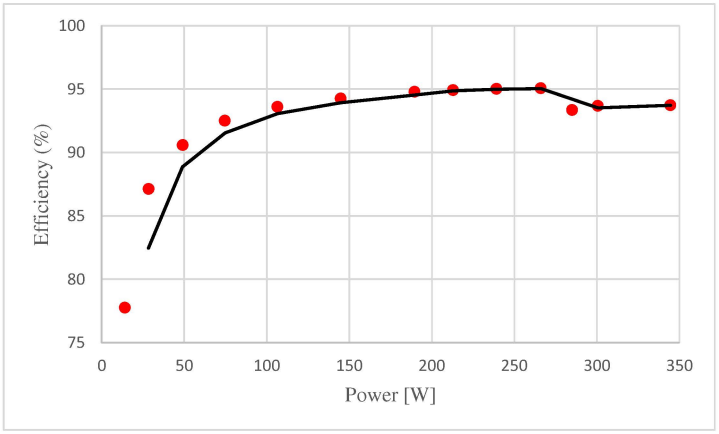


Figure 12. SP-IZI experimental efficiency.

Figure 13 shows the losses in each element of the converter and their percentage value concerning the whole, with the integrated inverter operating at nominal power. The values were obtained by measuring the currents and voltages of the elements in computational simulations and applying them to the specifications determined in the datasheets of the power switches and diodes.

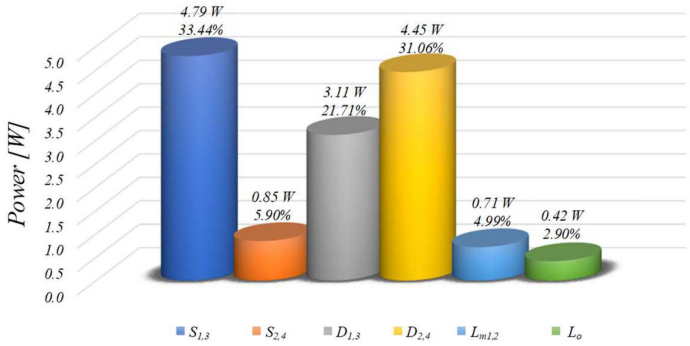


Figure 13. Distribution of losses in each SP-IZI device, operating at nominal power.

As can be seen, around 33% of the losses are associated with the high-frequency switches S_1 and S_3, where 3.18 W is related to conduction losses and 1.61 W is related to the commutation losses. In the diodes D_2 and D_4, which are complementary to high-frequency switches, the losses represent 31%, divided into 2.35 W for conduction losses and 2.10 W for switching losses. In addition, the diodes placed in series with the high-frequency switches (D_1 and D_3) are responsible for 21% of the overall losses. On the other hand, it is possible to verify that the losses associated with the low-frequency switches represent less than 6% of the losses, mainly related to conduction losses. Finally, all inductors' core and windings losses correspond to less than 8% of the overall losses.

Table 2 summarizes a comparative analysis between the SP-IZI and the main similar inverters available in the literature, considering the number of devices in each topology and its efficiency, focusing on topologies that operate with low voltages in their inputs. As can be seen, the topologies [7,14,25,26] that obtain an efficiency greater than or equal to 96% have more power switches than the proposed topology. On the other hand, the

topology [27] has the same number of switches and fewer inductors and diodes. However, its efficiency is limited to 94%.

Table 2. Comparative analysis involving SP-IZI and others.

Integrated Inverter	Number of Switches	Number of Diodes	Number of Inductors	Efficiency	THD of the Output Variable at Nominal Power
Single-Phase Integrated Zeta Inverter (SP-IZI)	4	4	3	95.06%	Voltage source 3.2%
Five-level common ground type (5L-CGT) [7]	8	0	1	96.54%	Not shown; voltage source output with high-frequency components
Buck-Boost Integrated Step-Up Inverter [27]	4	2	2	94%	Voltage source ∼ 2%
Transformerless Integrated DC–DC Converter [25]	9	1	2	96.13%	Active parallel power filter $i_s = 4.1\%$
Cuk module-integrated inverter (MII) [26]	6	1	2	96.5%	Grid-tied current source; simulation results, $i_s \sim 2.15\%$
A Novel Single-Stage Common-Ground Zeta-Based Inverter [14]	6	3	2	96.5%	Grid-tied current source, $i_s = 3.4\% - 3.9\%$

From an implementation cost perspective, the inverters use distinct quantities of active and passive components, which generate different costs. In this way, a direct cost comparison may be unrepresentative. However, some similarities are found when analyzing the models of switches and diodes used in the converter presented in Table 2.

This paper and the topologies proposed in [7,25–27] employ switches around 600–650 V and a maximum collector current between 40 and 53.5 A. The topology proposed in [25] uses a high-speed IGBT with a fast and soft recovery antiparallel diode presenting 650 V of breakdown and a maximum collector current of 53.5 A. This IGBT is enough for the mentioned works, and was considered in the cost comparison of these topologies. In [26], distinct switches were considered, with 150 V as the maximum voltage and 50 A as the maximum current. The other one presents 650 V and 11 A maximum voltage and current, respectively, totaled for the six switches in this topology. Finally, [14] uses switches of 1200 V and 40 A maximum.

Those used in SP-IZI and [27] are similar as regards their diodes. However, [27] uses diodes that tolerate 650 V and 30 A, while the diodes in this paper present the maximum as 650 V and 20 A. Thus, the diode used in [27] is adopted for the cost comparison. Additionally, Table 3 also includes costs related to capacitors and inductors. The costs involving capacitors are estimated based on the capacitance and application, i.e., whether it is a coupling capacitor or used in the DC-link.

Table 3. Comparative estimated cost per unit involving SP-IZI and others.

Integrated Inverter	Switches	Diodes	Inductors	Capacitors	Total
Single-Phase Integrated Zeta Inverter (SP-IZI)	0.19 pu	0.46 pu	0.33 pu	0.01 pu	1.00 pu
Five-level common ground type (5L-CGT) [7]	0.38 pu	0.00 pu	0.42 pu	0.17 pu	0.97 pu
Buck-Boost Integrated Step-Up Inverter [27]	0.19 pu	0.23 pu	0.62 pu	0.03 pu	1.07 pu
Transformerless Integrated DC–DC Converter [25]	0.43 pu	0.13 pu	0.82 pu	0.03 pu	1.41 pu
Cuk module-integrated inverter (MII) [26]	0.31 pu	0.04 pu	0.80 pu	0.02 pu	1.17 pu
A Novel Single-Stage Common-Ground Zeta-Based Inverter [14]	0.55 pu	0.17 pu	1.06 pu	0.13 pu	1.91 pu

On the other hand, the costs for the inductors consider the inductance. Generally, an inductor with elevated inductance needs a bulkier core and windings, increasing costs. Table 3 summarizes the main costs and exhibits the values per unit (pu).

Concerning the topology proposed in [7], which obtains slightly higher efficiency and slightly lower cost than the proposed SP-IZI, it is necessary to consider that such a topology uses twice as many power switches as the topology proposed in this paper. Thus, the number of components required to drive all the power switches, as well as the largest capacity required from the microcontroller to activate it, also need to be bigger. At the same time, the output voltage of this converter is composed of many high-frequency components. Thus, considering Tables 2 and 3, it can be concluded that the SP-IZI integrated converter is an option that has good efficiency ratio for the number of active and passive components.

Finally, the experimental dynamic result is presented in Figure 14, with a 70 W power load step (140 W to 210 W). As can be seen, the output voltage presents as transient when the load is connected. However, there is no discernible long-term transient. Figure 14 also shows the voltages v_{dc1} and v_{dc2} of the DC-link capacitors. As can be seen, as a characteristic of a split-capacitor DC-link inverter, the voltages v_{dc1} and v_{dc2} oscillate at the output frequency [28]. It is also possible to verify that the voltages are balanced, indicating the operation of the voltage-unbalance controller with zero error in a steady state.

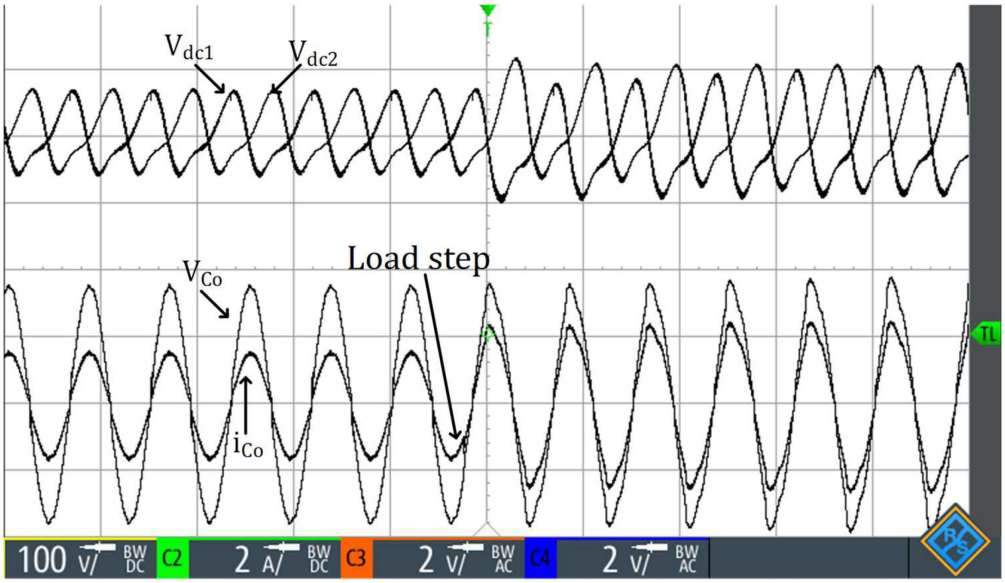


Figure 14. Experimental dynamic results in a 140 W to 210 W power load step (v_{C_o}: 100 V/div. i_o: 2 A/div. v_{dc_1}, v_{dc_2}: 2 V/div, 4 ms/div).

5. Conclusions

This paper has proposed a new integrated inverter (SP-IZI) for grid-isolated applications, combining two modified Zeta converters to replace the traditional two-stage converter system, in which a step-up DC-DC converter was associated with a voltage source inverter.

The proposed integrated inverter has been detailed by presenting and analyzing its topological states. Although it has four power switches, two operate at the output voltage frequency, which facilitates analysis and switching logic, in addition to reducing switching losses. Then, the converter was mathematically modeled from its equivalent model, and a proportional–integrative plus a multi-resonant controller was designed and used to control the output voltage without the need to measure the output inductor current.

Static and dynamic experimental results have been presented to evaluate the feasibility of the proposed SP-IZI. The inverter provided sinusoidal voltage with a low THD for linear and non-linear loads. At the same time, data were presented on the converter's efficiency at various load powers. The converter achieved close to 95% efficiency with a wide range of powers. A comparative study on the implementation cost of the converter proposed in this article and the main topologies proposed in the literature is also presented, from which

it has been possible to conclude that the proposed converter obtains good ratios between implementation cost, efficiency, and number of components. Finally, the dynamic results demonstrate that the employed controller was effective, since it was stable and achieved an adequate establishment time in response to load variations.

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Conflicts of Interest: The authors declare no conflicts of interest.

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