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Investigation of SiC MOSFET Body Diode Reverse Recovery and Snappy Recovery Conditions

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Abstract: This paper investigates the behavior of SiC MOSFETs body diode reverse recovery as a function of different operating conditions. The knowledge of their effects is crucial to properly designing and driving power converters based on SiC devices, in order to optimize the MOSFETs commutations aiming at improving efficiency. Indeed, reverse recovery is a part of the switching transient, but it has a significant role due to its impact on recovery energy and charge. The set of different operating conditions has been properly chosen to prevent or force the snappy recovery of the device under testing. The experimental results and specific software simulations have revealed phenomena unknown in the literature. More specifically, the analysis of the reverse recovery charge, Q_{rr}, revealed two unexpected phenomena at high temperatures: it decreased with increasing gate voltage; the higher the device threshold, the higher the Q_{rr}. TCAD-Silvaco (ATLAS v. 5.29.0.C) simulations have shown that this is due to a displacement current flowing in the drift region due to the output capacitance voltage variation during commutation. From the analysis of the snappy recovery, it has emerged that there is a minimum forward current slope, below which the reverse recovery cannot be snappy, even for a high current level. Once this current slope is reached, Q_{rr} varies with the forward current only.

Keywords: body diode; MOSFET switching; power electronics; power electronics devices; reverse recovery; SiC MOSFETs

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1. Introduction

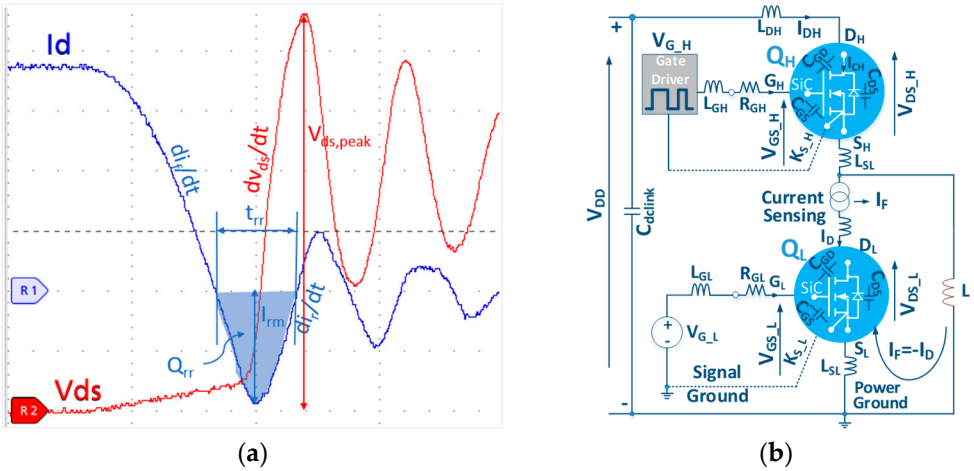
The body diode reverse recovery phenomenon is an important research topic [1–14], since its study is fundamental to improving the prediction of the performance of power converters adopting SiC MOSFETs. Indeed, the reverse recovery impacts the device switching speed and, as a consequence, the device operating voltage level due to the potential generation of over-voltages. Reverse recovery depends on a combination of factors related to the operating conditions such as DC-link voltage, load current, transient speed, and temperature, as well as on the MOSFET structure, which can be planar or trench. These operating conditions and the structure influence the occurring reverse recovery, which can be soft, hard or snappy [15]. Many studies compare the performance of Si and SiC MOSFETs [16–29]. Other studies have shown the response of the latter at varying operating conditions, such as gate-source voltage, temperature, drain current, current slope and so on [30–42]. However, the effects of the working conditions during snappy recovery have hardly been investigated and experimentally verified so far [43–46]. A double pulse test (DPT) with inductive load has been executed at different operating conditions to compare reverse recovery on different SiC MOSFET technologies: planar and trench [47,48]. The results show that the ringing and peak reverse current is highest in the planar SiC MOSFET,

and the difference increases with increasing temperature. In both technologies, the reverse recovery shows a small dependency on the forward current and the blocking voltage. At high current, the body diode recovery performance of the planar SiC MOSFET is better than the trench one, since it presents a lower forward voltage (V_f).

In this paper, the analysis is focused on investigating the impacts of operating conditions variation on reverse recovery, and then on analyzing the limit conditions between the hard and snappy recovery of third-generation planar SiC MOSFET 750 V 11 mΩ devices made by STMicroelectronics in the HIP247-4L package. The paper contributes to increasing the knowledge about reverse recovery in SiC MOSFETs. More specifically, the measurements and TCAD simulations have revealed two unexpected phenomena at high temperatures. First, the reverse recovery charge, Q_{rr}, decreases as the gate voltage increases. Moreover, the higher the threshold of the SiC MOSFET, the higher the Q_{rr}. TCAD simulations have shown that the phenomenon is due to a displacement current flowing in the drift region due to the output capacitance voltage variation during commutation. An additional contribution is made by the deep analysis of the snappy recovery phenomenon, which has highlighted a set of conditions that the designer must consider in order to set or prevent its occurrence. Moreover, the experimental analysis has shown that below a given forward current slope, the snappy recovery phenomenon does not occur regardless of the current level. In particular, Q_{rr} depends only on the forward current when the aforesaid current slope is forced. The paper is organized as follows. A brief description of the theoretical concepts regarding soft, hard and snappy recovery and the correlated issues are reported in Section 1. Section 2 recalls the basic concepts of reverse recovery for completeness, while Section 3 describes the experimental setup and reports some experimental results and TCAD simulations. Further results are reported in Section 4, which highlight the conditions for snappy recovery occurrence. Finally, the main conclusions are summarized in the last section.

2. Reverse Recovery Theoretical Concepts

Reverse recovery occurs when the MOSFET body diode is switched off because of a positive voltage across device drain-source terminals (V_{ds}). Before the switching-off, the charges in the drift region must be removed by a current that flows from the drain to the source, named the reverse recovery current [49]. Figure 1a shows an example of the body diode current and voltage during the switching-off and the quantities of interest that impact the reverse recovery analysis. The waveforms are obtained considering a classical half-bridge converter, as shown in Figure 1b.



(**a**) (**b**)

Figure 1. Reverse recovery waveforms: (**a**) electrical signal and factors of interest, (**b**) equivalent electrical scheme of half-bridge configuration.

The body diode of the low side (LS) device begins the reverse recovery when the complementary one (high side device—HS) is turning on. Since the reverse recovery of the LS device is investigated, a negative constant voltage V_{G_L} is applied to its gate through a gate resistance R_{GL} to keep it off. On the contrary, the HS device is driven by a double pulse signal applied to its gate through a gate resistance R_{GH}. In order to measure the reverse recovery current, a current sensor is placed in series with the device under test (DUT). The electrical scheme also reports all the parasitic inductances and capacitances of the devices responsible for overvoltages and oscillations, and consequently impacting device switching speed.

Of particular interest are the reverse current slope di_r/dt and the forward current slope di_f/dt, whose ratio (called snappiness factor, S) determines the kind of reverse recovery:

$$S = \frac{|di_r/dt|}{|di_f/dt|} \quad (1)$$

If S < 1, then the recovery is soft, else the recovery is hard, and when S is very high (S >> 1), the recovery is snappy (SR) [44]. Figure 2 reports the waveforms occurring in the three cases. The recovery is soft when the reverse current recovers to zero slowly and without oscillations impacting on the smooth rising of the drain-source voltage of the device working as a freewheeling diode. The recovery is hard when the current recovers to zero quickly, involving oscillations due to the resonant circuit formed by the stray circuit inductance and diode depletion layer capacitance. In this case, the diode reverse recovery can lead to serious voltage spikes. The recovery is snappy when these voltage spikes present an increment in the slope before reaching the peak. This increment is due to a faster charge removal. An experimental example of these three kinds of reverse recovery is reported in Figure 2.

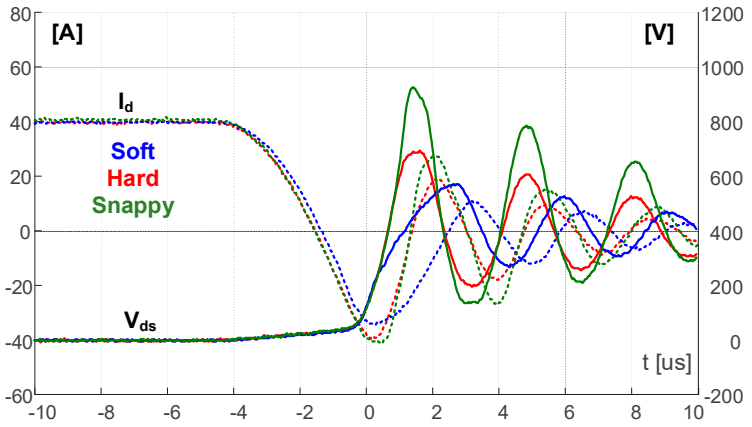


Figure 2. Soft, hard and snappy recovery waveform examples.

How the current recovers to zero must always be investigated during device characterization, considering different parameters such as the forward current, the gate-source voltage, the temperature, and the forward and reverse slopes. This investigation is important in order to prevent oscillation and high voltage spikes that may lead to overpassing the breakdown voltage (BV) of the device.

Snappy recovery mainly occurs in SiC MOSFETs with high breakdown voltage ($\geq$1700 V), which are designed to work at very high dc-link voltage, and consequently, very high drain-source voltage slopes could arise [44].

Three main factors mainly affect the SR. A factor is the junction capacitance, which depends on the MOSFET's geometrical and process parameters. Another factor is the parasitic inductances of the power loop layout and the package of the converter. Finally, the switching speed also affects the SR. During the reverse recovery phase, the SR occurs if the free charges leave the junction before the current extinction. As a result, the current

immediately "snaps" to 0. In this case, the interaction among the sudden change of current slope together with the layout's parasitic elements and the diode's depletion layer capacitance could lead to sustained voltage oscillations across the SiC MOSFET drain-source terminals [30,46].

3. Experimental Analysis and TCAD Simulation of Reverse Recovery

Figure 3 shows the characterization board used to analyze the reverse recovery, where the driving section and the power section are highlighted.

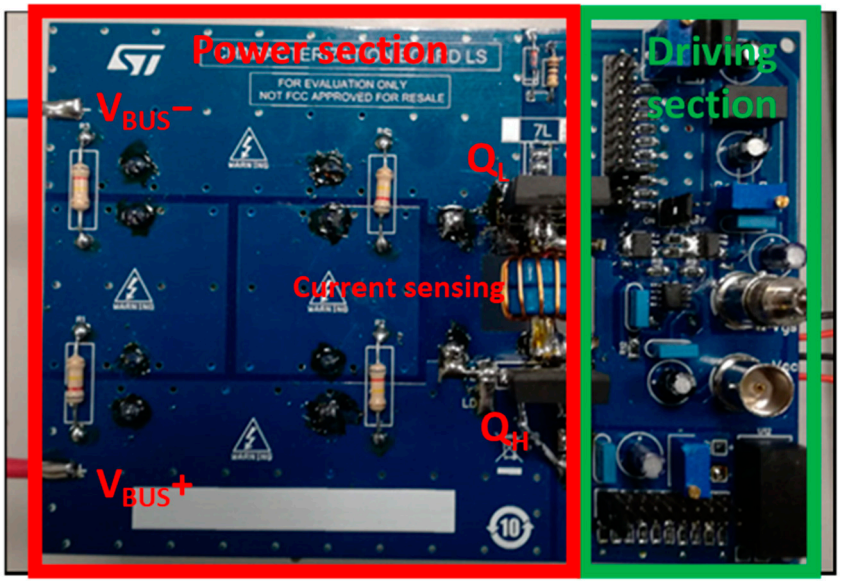


Figure 3. Reverse recovery characterization board.

As reported in the electric scheme in Figure 2, the high-side device is used as a driver, and at its gate is applied a double pulse signal. The low side device is the DUT, and it is kept off by a negative voltage V_{G_L}. Figure 4 shows the trends of double pulse test signals V_{gs} and V_{ds} of the high-side MOSFET, the V_{ds} of the low-side MOSFET and the load current. The front at which reverse recovery occurs is highlighted by the shaded orange area (t_2). During the first pulse (t_0–t_1), the inductor L is charged. During the dead time between the two pulses (t_1–t_2), the inductor forces a current to flow through the body diode of the low-side MOSFET, and, in the rising edge of the second pulse (t_2), a positive V_{DS_L} is applied to the body diode, so its current decreases to zero and then flows in the opposite direction in order to carry out the charges stored in the drift region (reverse recovery current). The device used for this analysis is a Gen 3 750 V SiC MOSFET 11 mΩ. Three samples have been selected considering the distribution of static parameters among a sample of 200 devices. The devices under tests belong to three different values of threshold voltage, according to the statistical distribution reported in Figure 5. Considering that 50% of devices have V_{th} between 2.15 V and 2.25 V, this group has been considered to select the device ("Typ") with typical V_{th}. The device ("Min") with minimum V_{th} has been selected from the group 1.75 V–1.85 V, while the device ("Max") with maximum V_{th} has been selected from the group 2.45 V–2.55 V. These three values of V_{th} have been chosen in order to investigate how parasitic turn-on (PTO) and snappy recovery (SR) are influenced by the threshold voltage of the device.

The aim of the experimental tests is the evaluation of the reverse recovery response by looking at the trend of the following recovery parameters (Figure 1a):

- Q_{rr} reverse recovery charge;
- t_{rr} reverse recovery time;
- I_{rm} negative peak current;
- E_{rec} reverse recovery losses.

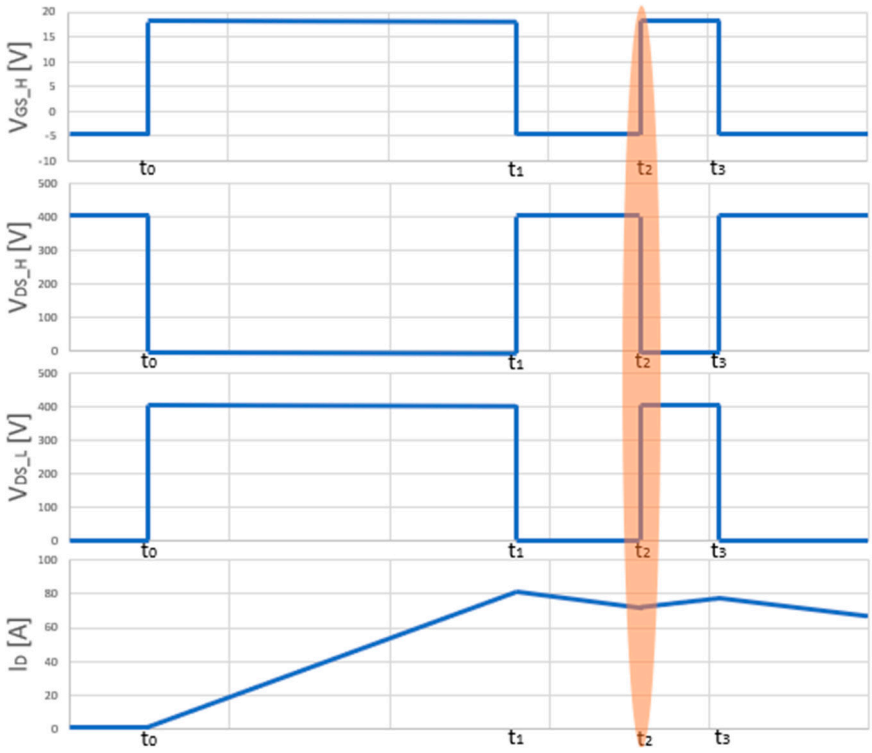


Figure 4. Double pulse test.

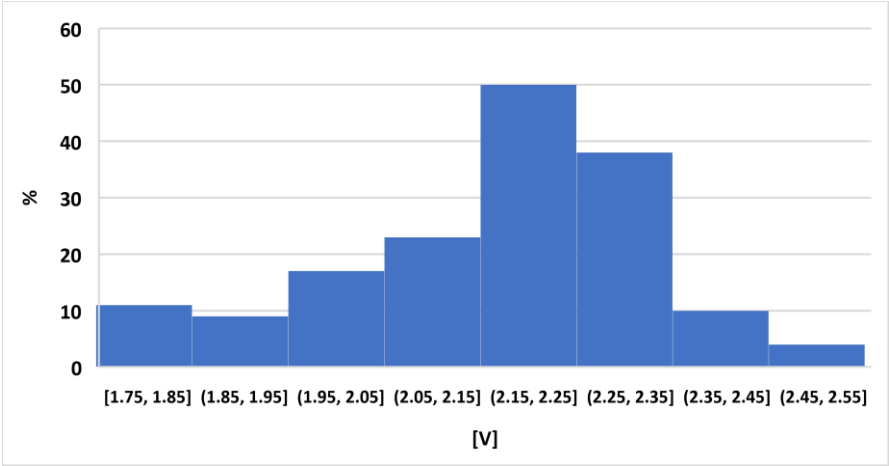


Figure 5. Threshold voltage statistical distribution at 5 mA, 25 °C.

For each of the three devices, a set of measurements has been executed by varying three external operating settings:

- Temperature, T_c, (25 °C and 175 °C);
- Load current, I_d, (40 A, 75 A and 120 A);
- Gate voltage, V_{G_L}, (−8 V, −5 V, −3 V and 0 V).

Since Q_{rr} is the area of the current waveform during t_{rr} and it is also impacted by I_{rm}, it is possible to summarize the reverse recovery performance by looking principally at Q_{rr}. According to this, Figure 6 shows the reverse recovery charge as a function of V_{G_L} at two different temperatures (25 °C and 175 °C) for the three devices, Min, Typ and Max, while keeping the current constant at 40 A. The DC bus voltage is set to 400 V and the current slope is regulated to around 2.5 A/ns. These tests verify that at 25 °C (Figure 6a), Q_{rr} increases with the increment of V_{G_L}. This behavior is expected at V_{G_L} equal to zero, where PTO (parasitic turn-on) more easily occurs with a high injection of charges (coming

from the channel) in the drift region, with a consequent increment of Q_{rr}. For the case at V_{G_L} equal to −8 V, PTO action can be excluded, and Q_{rr} is basically related to minority carrier charges that at 25 °C have low average life time. On the contrary, at V_{G_L} = 0 V, the operative conditions of the test (forward current and di/dt) lead to the injection of charges that are, in part, due to the PTO, which appears as though Q_{rr} would be larger. The Q_{rr} data for an intermediate value of V_{G_L}, such as −3 V, experimentally show a different value of Q_{rr} than the one at −8 V due to the non-ideal body-drain junction and drop voltage across parasitic inductors. Moreover, there is a different charge distribution due to the modulation of the depletion region next to the gate due to the different (negative) gate voltage. This means that in this intermediate case, due to the MOSFET structure, the combination of a limited injection of charges from the channel and the different charge distribution is responsible for an apparent Q_{rr} increment. This behavior is confirmed by the waveforms shown in Figure 7 that highlight increased values of t_{rr} and I_{rm} for higher V_{G_L} levels. It is translated also in the form of a higher rising slope of the V_{DS_L} as the V_{G_L} is lower, since it is strictly correlated with the reverse recovery current slope.

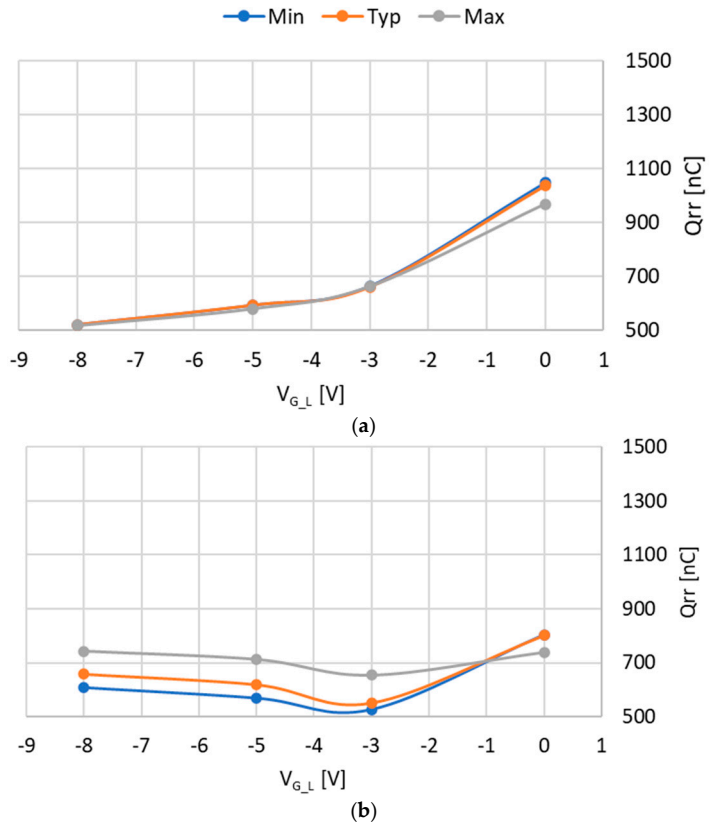


Figure 6. Q_{rr} vs. V_{G_L} for the three devices, Min, Typ and Max, at 40 A, (**a**) 25 °C, (**b**) 175 °C.

At 175 °C, Figure 6b, the average lifetime of minority carriers is longer, and consequently, this modifies the Q_{rr} values and action of PTO according to V_{G_L} values. Therefore, considering the working conditions adopted to evaluate the results reported in Figure 6a,b, the response of Q_{rr} will be different because it depends on the temperature and V_{G_L} value. Q_{rr} shows a decrement from V_{G_L} = −8 V to −3 V and then an increment from −3 V to 0 V. The most oscillatory recovery of the current waveforms at high temperatures reported in Figure 8 is amplified for lower values of V_{G_L} (−8 V), causing a higher I_{rm} compared to V_{G_L} = −3 V and V_{G_L} = 0 V. On the contrary, at V_{G_L} = 0 V, the PTO causes a longer recovery time t_{rr} that determines a higher Q_{rr} compared to V_{G_L} = −8 V.

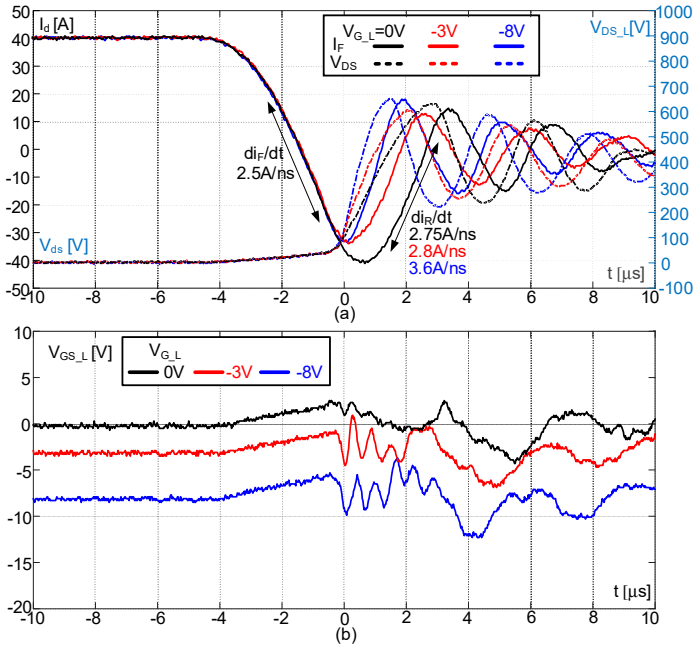


Figure 7. (**a**) I_d, V_{ds} and (**b**) V_{GS_L} of device "Typ" at 40 A, 25 °C, and different values of V_{G_L}.

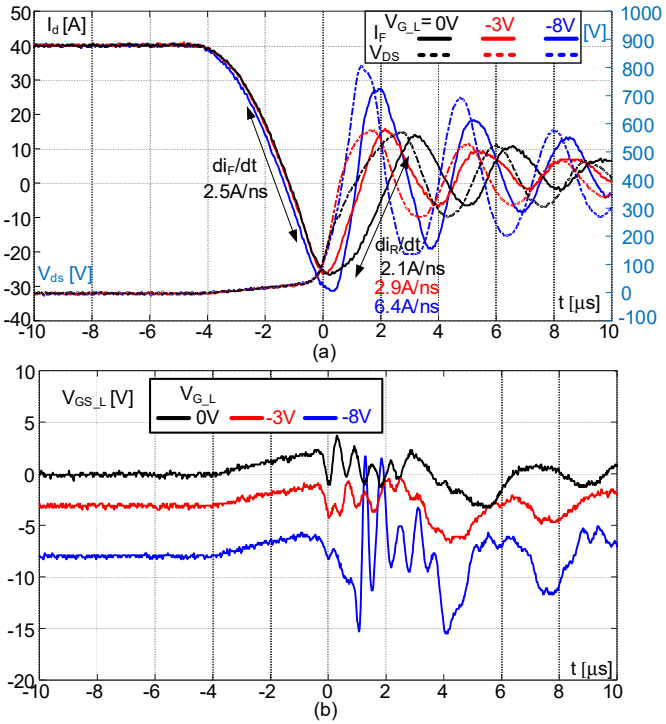


Figure 8. (**a**) I_d, V_{ds} and (**b**) V_{GS_L} of Typ at 40 A of forward current, 175 °C (junction temperature) and different values of V_{G_L}.

Comparing Figure 6a,b, the most significant result is related to Q_{rr} values at V_{G_L} = 0, where Q_{rr} is higher at 25 °C than 175 °C, despite V_{GS_L} overvoltages being higher at 175 °C than 25 °C. This means that at high temperature, Q_{rr} trends cannot be justified only by PTO. The Q_{rr} reduction at 175 °C and V_{G_L} = 0 is reasonable, since I_{rm} here is also lower than the case at 25 °C (−40 A at 25 °C and −25 A at 175 °C).

The reverse recovery response, inferred from the Q_{rr} trendline at 25 °C, 40 A, in Figure 6a, is also confirmed at high currents, as verified by the results illustrated in Figure 9a,b, respectively, at 75 A and 120 A for the same devices under test: "Min", "Typ"

and "Max". The Q_{rr} in these two cases varies from ≅500 nC (V_{G_L} = −8 V) to ≅800 nC (V_{G_L} = 0 V) against the variation observed at 40 A, where it reaches a value of ≅1000 nC (V_{G_L} = 0 V).

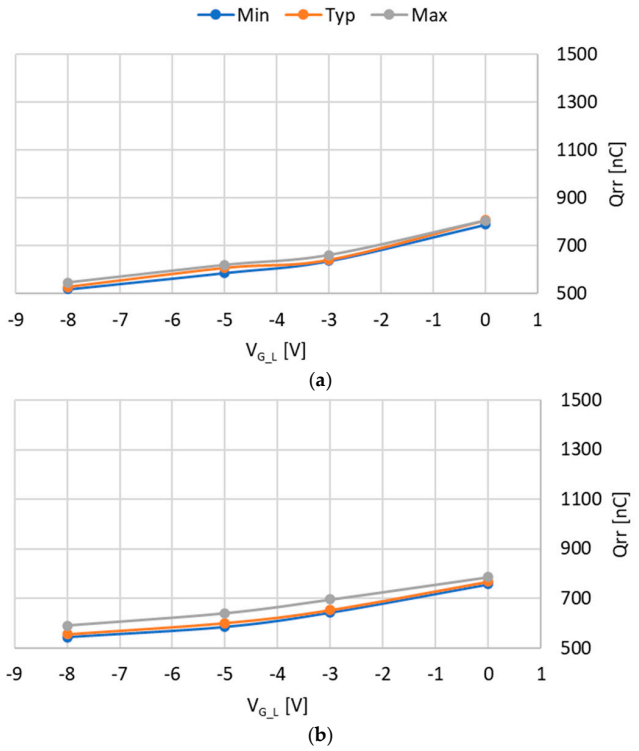


Figure 9. Q_{rr} vs. V_{G_L} for the three devices Min, Typ and Max at 25 °C, (**a**) 75 A, (**b**) 120 A.

In this structure, with a high current, the drift region is more quickly emptied than in the low-current case. Indeed, by comparing the waveforms of Figures 7a and 10a, the higher the forward current, the higher the reverse recovery current slope (di_r/dt).

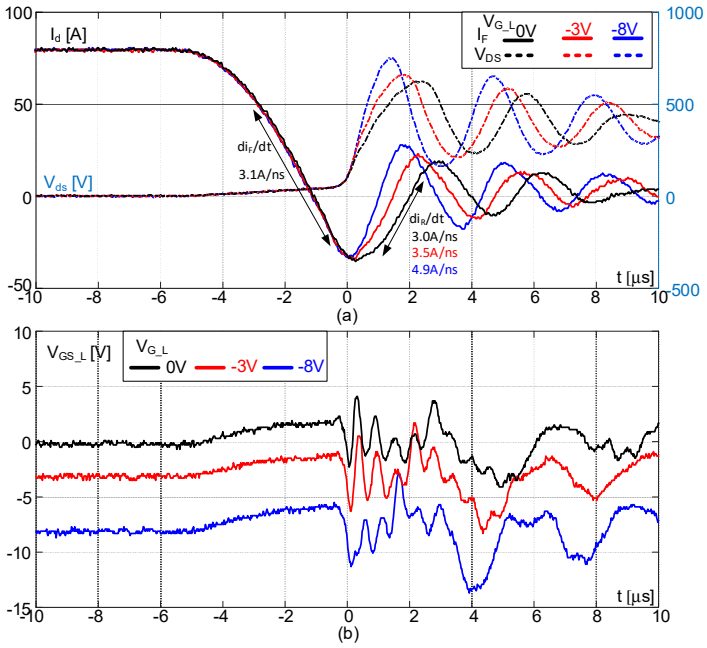


Figure 10. (**a**) I_d, V_{ds} and (**b**) V_{GS_L} of device "Typ" at 75 A of forward current, 25 °C and different values of V_{G_L}.

Figure 11 shows an opposite trend of Q_{rr} vs. V_{G_L} for the three devices Min, Typ and Max, compared to Figure 9, evaluated only by changing the temperature to 175 °C. In fact, at this temperature, Q_{rr} decreases with the increment of V_{G_L}. It is an unexpected behavior, and in order to understand it, some simulations based on TCAD-Silvaco have been executed. The results related to some working conditions are not reported because they have not been executed to avoid a drain-source voltage overshoot exceeding the breakdown voltage.

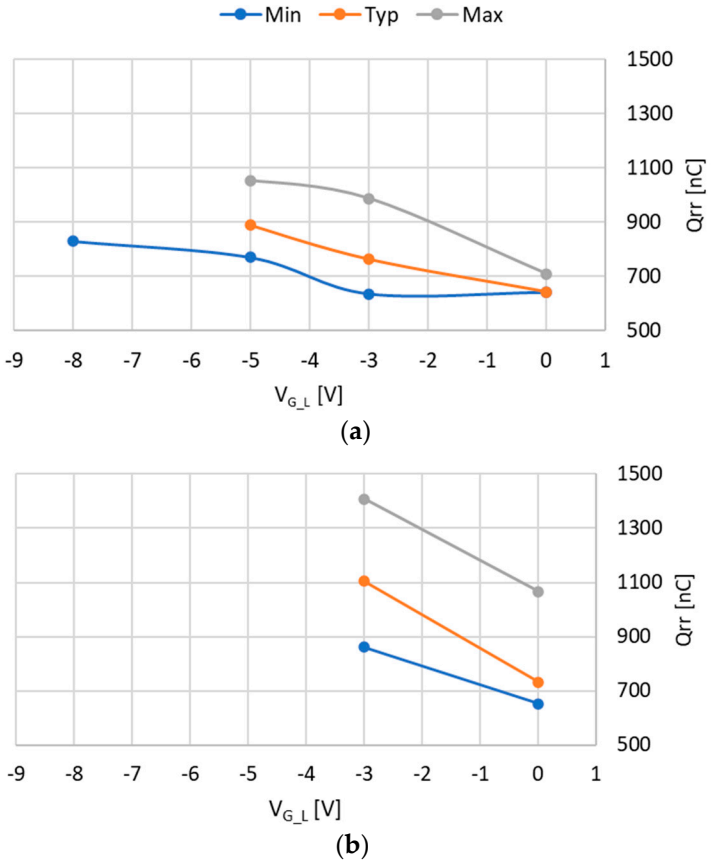
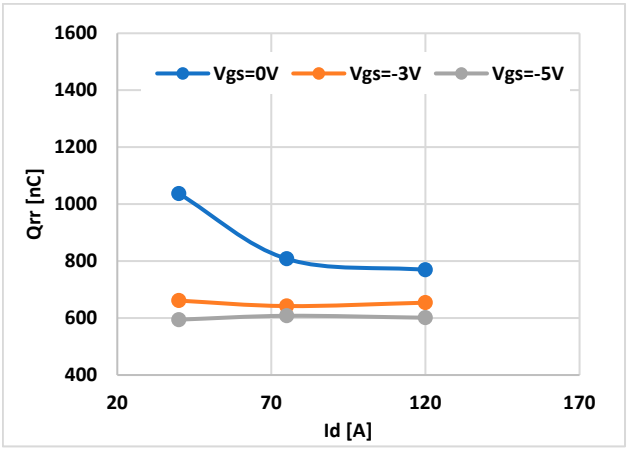


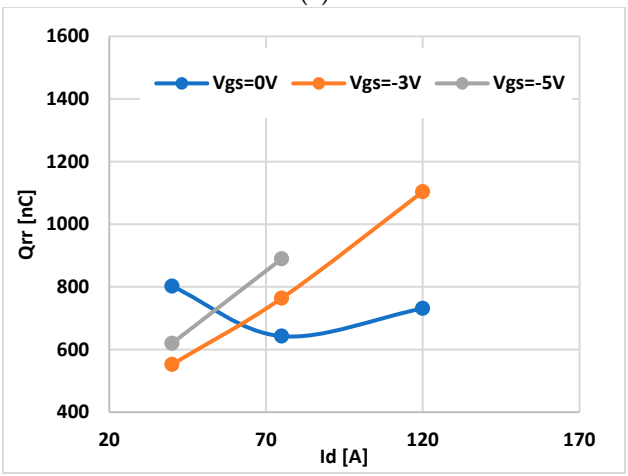
Figure 11. Q_{rr} vs. V_{G_L} at 175 °C for three devices Min, Typ and Max for different values of forward current. (**a**) 75 A (**b**) 120 A.

Figure 12 reports Q_{rr} as a function of the forward current at different V_{G_L} and temperature values for device "Typ". The temperature influences the average lifetime of minority carriers and, consequently, drastically changes the Q_{rr} trendline, providing very different response depending on the operative conditions.

To support and better understand the mechanism of reverse recovery of the device under test, the half-bridge configuration has been developed in TCAD-Silvaco software, and the electrical parameters of the devices used to set the model are included in Table 1. The physics model used in the simulation was the Schottky–Read–Hall (SRH), for recombination, bandgap narrowing, incomplete ionization of the dopant, the ATLCVT mobility model and anisotropic impact ionization (IMPACT ANISO). The material specification of 4H-SiC and dielectric properties are reported in the ATLAS SILVACO manual (Silvaco International (2015) ATLAS User's Manual Device Simulation Software Silvaco International, Santa Clara), and some of those used in this model are reported in Table 1.



(**a**)



(**b**)

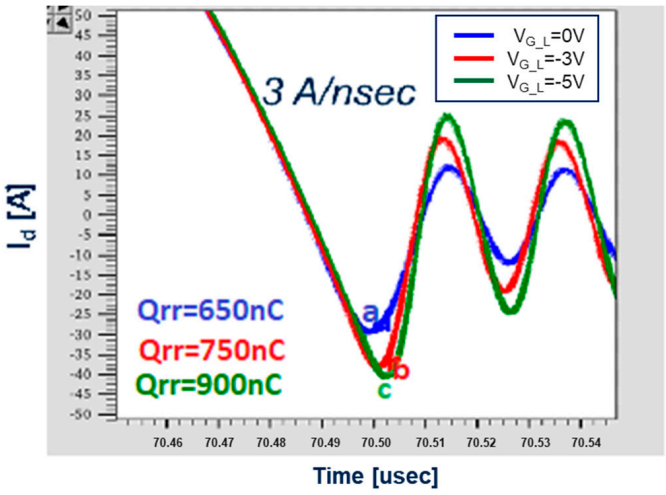
Figure 12. Q_{rr} vs. forward current for "Typ" device for different values of V_{G_L} at (**a**) 25 °C, (**b**) 175 °C.

Table 1. Material specifications for 4H-SiC, ATLAS SILVACO manual.

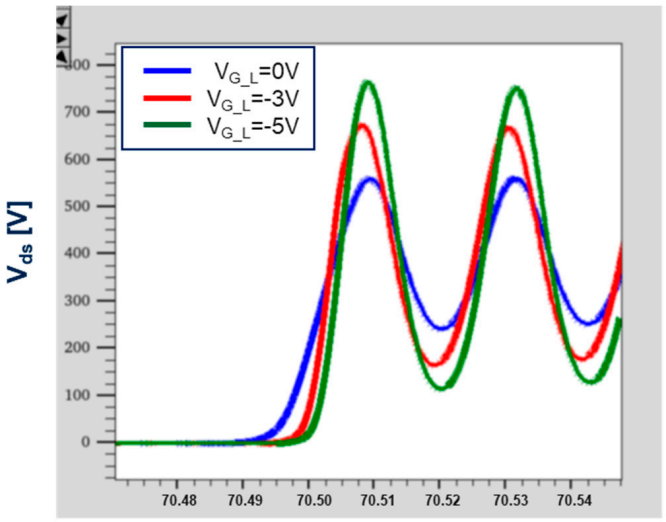
Quantity	Value
Relative permittivity	9.76
Bandgap Eg (@300 K)	3.26 eV
Affinity	3.7
Alpha coeff. for temperature dependence of bandgap	$3.3{\cdot}10^{2}$ eV/K
Beta coeff. for temperature dependence of bandgap	10^{5} K
Conduction band density (@300 K)	$1.7{\cdot}10^{19}$ cm^{-3}
Valence band density (@300 K)	$2.5{\cdot}10^{-19}$ cm^{-3}
Richardson constant for electrons	146 $A/cm^{2}/K^{2}$
Richardson constant for holes	30 $A/cm^{2}/K^{2}$
Electron/Holes Auger coefficient	$3{\cdot}10^{-29}$ cm^{6}/s

Figure 13a reports the magnification of the simulated body diode current (at 75 A) and Figure 13b reports the simulated V_{ds} voltage for V_{G_L} = 0 V, −3 V and −5 V at T_j = 175 °C. Figure 14 shows the gate-source voltage of the device operating as a freewheeling diode. The TCAD simulations confirm that Q_{rr} decreases from 900 nC to 650 nC; hence, the higher the V_{G_L} (shown in Figure 11), the lower Q_{rr}. This happens despite the V_{G_L} peak voltage, measured in correspondence with the maximum negative peak of the current I_{rm} (points a, b and c in Figure 13a), overpassing the threshold voltage for a period sufficient to cause a PTO in the worst case (i.e., V_{G_L} = 0 V). In addition, the color maps of the current density (Figure 15) (related to the maximum negative peak of I_{rm} shown in Figure 13a) also confirm that there is a higher current density in the drift region when V_{G_L} = −3 V and V_{G_L} = −5 V

than when V_{G_L} = 0 V. This counterintuitive behavior of the current density in Figure 15b,c is due to a displacement current, which flows in the drift region due to the variation of the parasitic output capacitance voltage during the commutation of the high-side device. This current causes an increment of charges in the drift region and, consequently, a higher Q_{rr} with respect to the case at V_{G_L} = 0 V. It is also worth noting that the device with a higher threshold voltage (Max) presents the highest $Q_{rr,}$ as evident from Figure 11.



(**a**)



(**b**)

Figure 13. Body diode (**a**) current and (**b**) voltage for V_{G_L} = 0 V, V_{G_L} = −3 and V_{G_L} = −5 V simulated with TCAD (at 75 A).

To sum up, the experimental results and TCAD simulations demonstrate that there is not a unique response of the intrinsic body diode during reverse recovery. Considering the operating conditions related to V_{DD} and di_f/dt, it is possible to separate the behavior at the low current, with V_{G_L} changing from −8 V to 0 V (where Q_{rr} increases at low temperatures (25 °C) and high temperatures (175 °C)), from the behavior at high current. In this last case, at a low temperature, Q_{rr} increases when V_{G_L} moves from −8 V to 0 V, while, at a high temperature, it decreases despite the possible effect related to the triggering of PTO, especially at V_{G_L} = 0. However, the worsening of the operative conditions, in terms of forward current level and temperature, does not impart reverse recovery with

a strong oscillatory behavior; instead, it is possible to see V_{DS} voltage waveforms with limited oscillations.

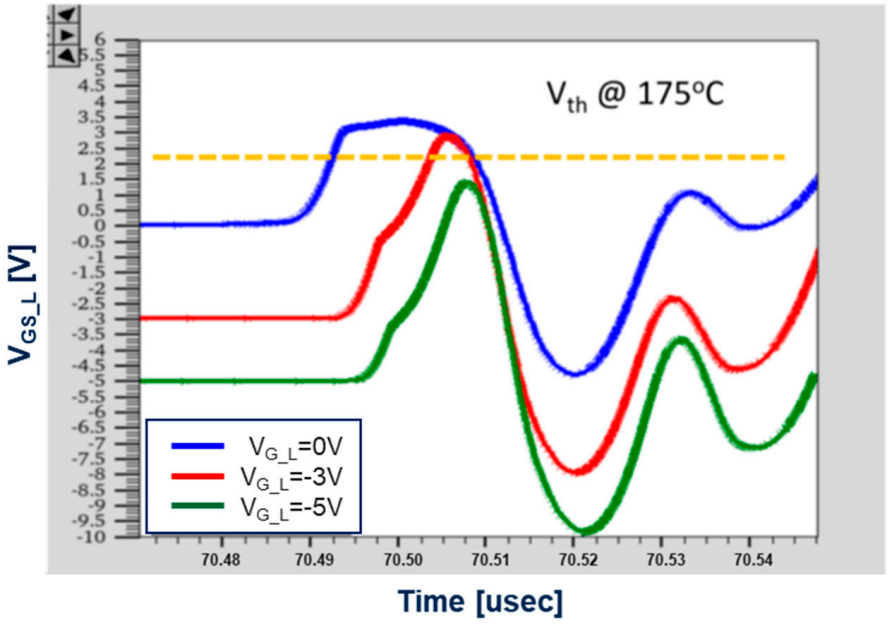


Figure 14. Instantaneous gate-source voltage of DUT during turning on of the complementary device.

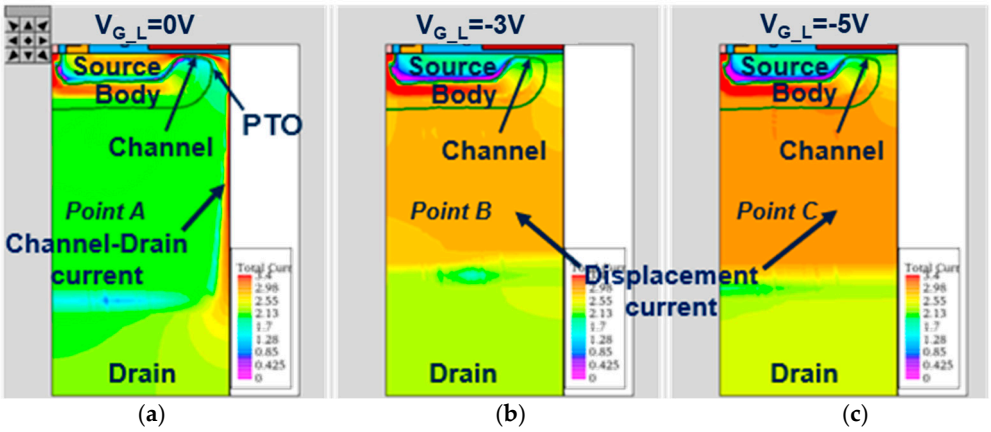


Figure 15. Current density color map [A/cm^2] in logarithmic scale during commutation for (**a**) V_{G_L} = 0, (**b**) V_{G_L} = −3 V and (**c**) V_{G_L} = −5 V relative to the minimum current value of Figure 13a, indicated with "a", "b", "c".

4. Analysis of Snappy Recovery Limits

In this section, we investigate the reverse recovery response when the extremization of the operative conditions is responsible for the generation of significant drain-source overvoltage. This behavior is usually called "snappy recovery" [44].

It is desirable to have fast recovery, and this can be achieved with a high current and voltage slope. However, in this case, the reverse recovery will belong to the "hard" type, as indicated in the JEDEC standard [15]. Unlike soft recovery, where voltage and current profiles do not present significant overvoltage and/or overcurrent, in this case, oscillatory behavior during the recovery is expected. The hard recovery can become snappy for specific values of forward current, slope, temperature or V_{G_L}. Hence, it is useful to change these operating conditions to identify when this phenomenon is triggered. A representation of this occurrence has been illustrated in Figure 16.

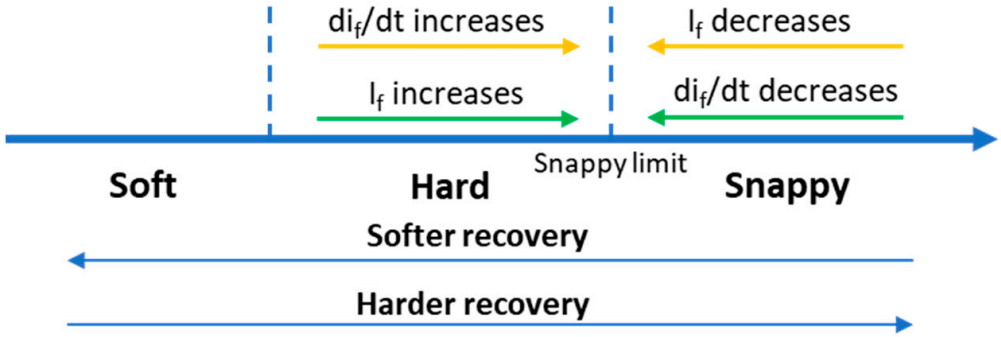


Figure 16. Identification of "snappy limit condition".

To find the conditions leading to snappy recovery (snappy limit defined in Figure 16), dedicated measurements have been executed for the DUT, at different values of:

- Temperature (175 °C and 200 °C);
- Gate-source voltage (−5 V and −8 V).

The procedure is reported in the flow chart of Figure 17. Starting from a condition of T_j, I_f and V_{G_L} where the recovery is surely snappy (point 1), the forward current is decreased (point 2) until the snappy recovery is maintained. Once a current value that precludes snappy recovery is found, this value represents the limit current, set as I_{limit} (point 3), which determines a limit condition between hard and snappy recovery. It is worth noticing that di_f/dt is lower than at the beginning. Starting from this value of current, I_{limit} (where the recovery is hard), the forward current is reduced until a softer recovery is reached (point 4), hence the di_f/dt is a little reduced. Therefore, the di_f/dt that is set by the active device is increased (point 5) by changing its gate resistance, to come back again to the limit between the hard and snappy recovery. The di_f/dt at which this occurs is the $(di_f/dt)_{limit}$ (point 6). The snappy recovery boundary is asymptotically reached by considering forward current reduction and increasing of di_f/dt. This procedure is iterated until I_f reaches low values (set to about 20 A for this device), at which an even higher di_f/dt cannot trigger snappy recovery. Once the iteration is concluded, the forward current is set to the I_{limit} value (point 7) found in point 3, and the process is repeated by increasing the value of I_f (point 8), moving to a harder recovery. Hence, the di_f/dt is decreased (point 9) to reach again the limit between hard and snappy recovery (point 10). This process is iterated as long as the gap between the $(di_f/dt)_{limit}$ at the n iteration is almost equal to the $(di_f/dt)_{limit}$ at the $n-1$ iteration. However, the process is interrupted if a high current is reached (set to about 70 A for this device) to avoid stressing the device.

The research process of determining the snappy recovery limit condition and the relation between I_{limit} and di_f/dt can be repeated by varying the temperature and the gate-source voltage of the device used as a freewheeling diode. The experimental results derived to study this behavior have been collected for the three devices (Min, Typ, Max) under test, considering the most stressful temperatures 175 °C and 200 °C and $V_{G_L} = -8$ V and −5 V, since these operating conditions can easily trigger snappy recovery.

According to the aforementioned procedure, we establish the current values I_d where the devices operate in snappy recovery, and these are reported in Table 2. From these values, we take I_{limit} as the starting point of the research process of snappy recovery limit conditions. The experimental application of the algorithm shown in Figure 17 has allowed us to identify the di_f/dt that determines the snappy limit conditions (associated with a specific I_{limit} current value), which can be correlated to reverse recovery charge Q_{rr}.

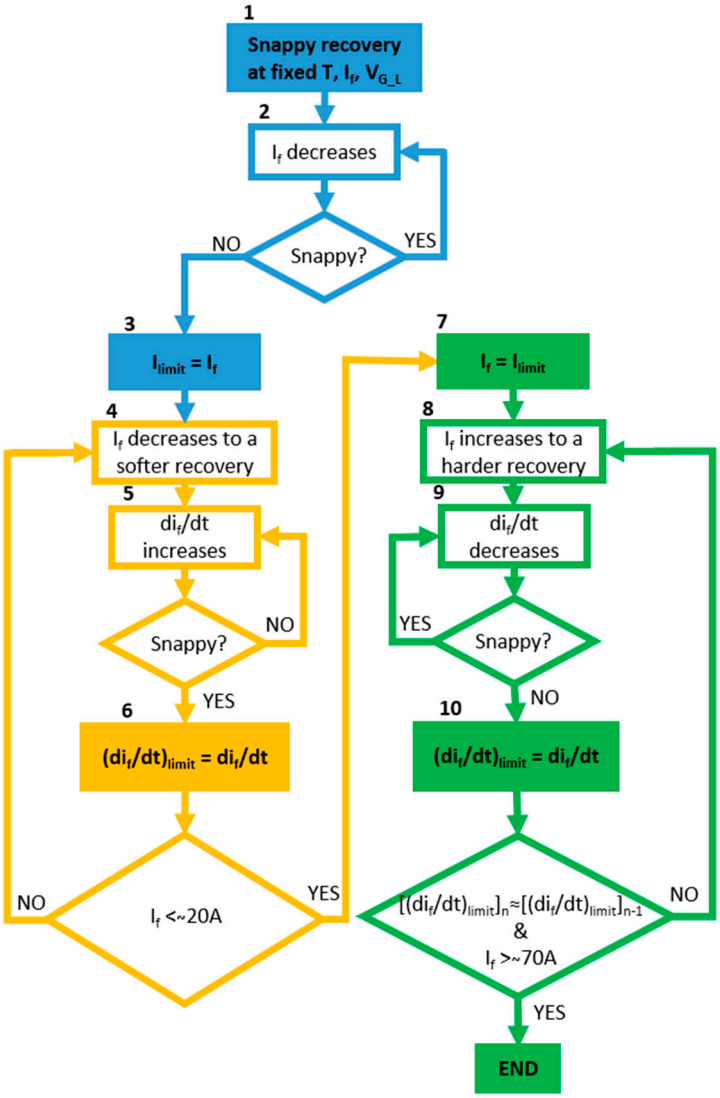


Figure 17. Snappy limit flow chart.

Table 2. Limit current between hard and snappy recovery at different conditions of V_{th}, V_{G_L}, T_j and I_d.

Device	T_j [°C]	V_{G_L} [V]	I_d [A]	I_{limit} [A]
Min	175	−8	75	36
	200		40	26
	175	−5	75	58
Typ	175	−8	40	30
	200		40	25
	175	−5	75	51
Max	175	−8	40	15
	200		40	15
	175	−5	75	70

Figure 18 shows the I_d and V_{ds} waveforms of the Min at T_j = 175 °C, and V_{G_L}= −8 V at the starting current I_d = 75 A, where the device operates in snappy recovery, as well as the limit current I_{limit} = 36 A where the recovery is no longer snappy. Figure 19 shows a

set of curves of Q_{rr} trend vs. di_f/dt for different combinations of V_{G_L} and T_j values for the three devices (a) Min, (b) Typ and (c) Max. According to the flow chart of Figure 17, the increasing di_f/dt and consequently decreasing I_f are correlated with the applications of the procedure described in points 3-4-5-6, while the snappy limit conditions where di_f/dt decreases and I_f increases correspond to the application of points 7-8-9-10 of the aforementioned flow chart. It is important to note that each point of the curves of Q_{rr} with respect to di_f/dt is obtained at a different value of forward current, since they are points that define the limit condition for snappy recovery. In particular, the higher the di_f/dt, the lower the I_f. The procedure described in the flow chart is applied in Figure 19 when $V_{G_L} = -8$ V/$T_c = 175$ °C and $V_{G_L} = -8$ V/$T_c = 200$ °C. When $V_{G_L} = -5$ V/$T_c = 175$ °C, it is not possible to reach the snappy condition at a low value of current because it requires a too-high di_f/dt.

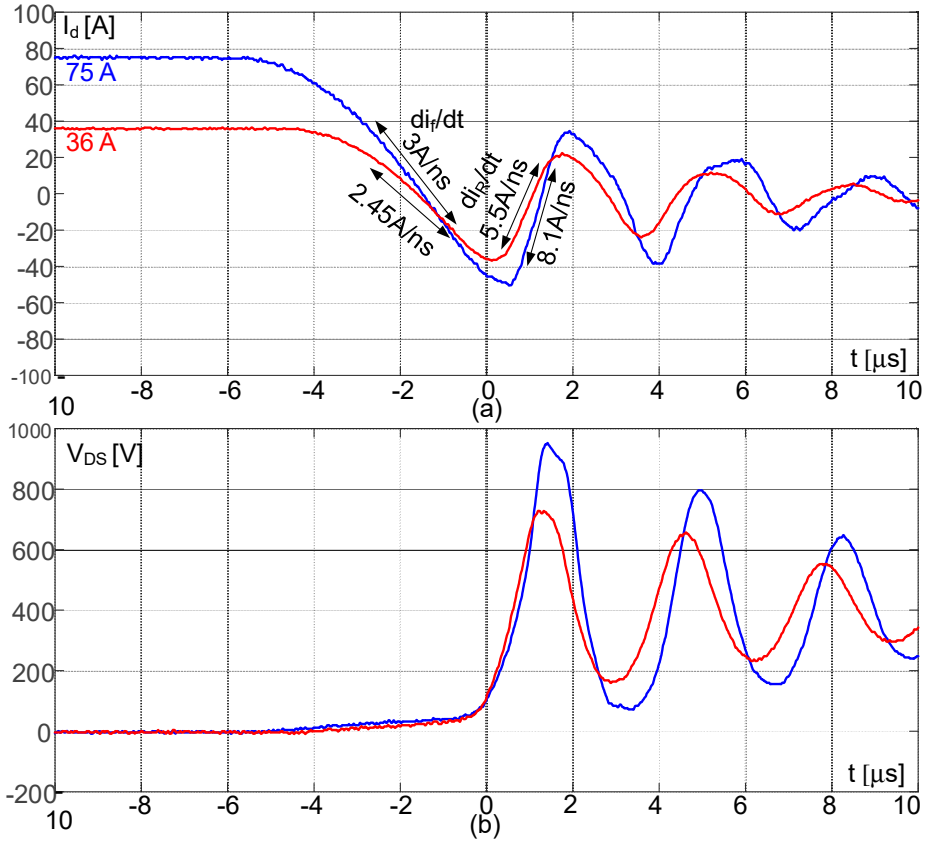


Figure 18. (**a**) I_f and (**b**) V_{ds} of device "Min" at $V_{G_L} = -8$ V, $T_c = 175$ °C and two current values: one causing snappy behavior (75 A) and one at the snappy limit condition (36 A).

Figure 20 highlights the current and the V_{ds} voltage of the typical device at $V_{G_L} = -8$ V, $T_j = 200$ °C and two different conditions of forward current (43 A and 70 A), as already shown in Figure 19b. Both cases are snappy limit cases and, although they have different values of current, they have almost the same di_f/dt. This analysis has highlighted the presence of a $(di_f/dt)_{min}$ below which the recovery is not snappy, even for a high current level. Moreover, once $(di_f/dt)_{min}$ is reached, Q_{rr} depends only on I_f. It must be noted that this behavior is true in the case of $V_{G_L} = -8$ V and T_c equal to 175 °C and 200 °C. In the case of $V_{G_L} = -5$ V and $T_c = 175$ °C, the trend is quite different, since very high current and di_f/dt are needed, so the condition of a $(di_f/dt)_{min}$ is not reached. This limit is lower when the temperature (Figure 19) and the V_{th} (Figure 21) of the device are higher.

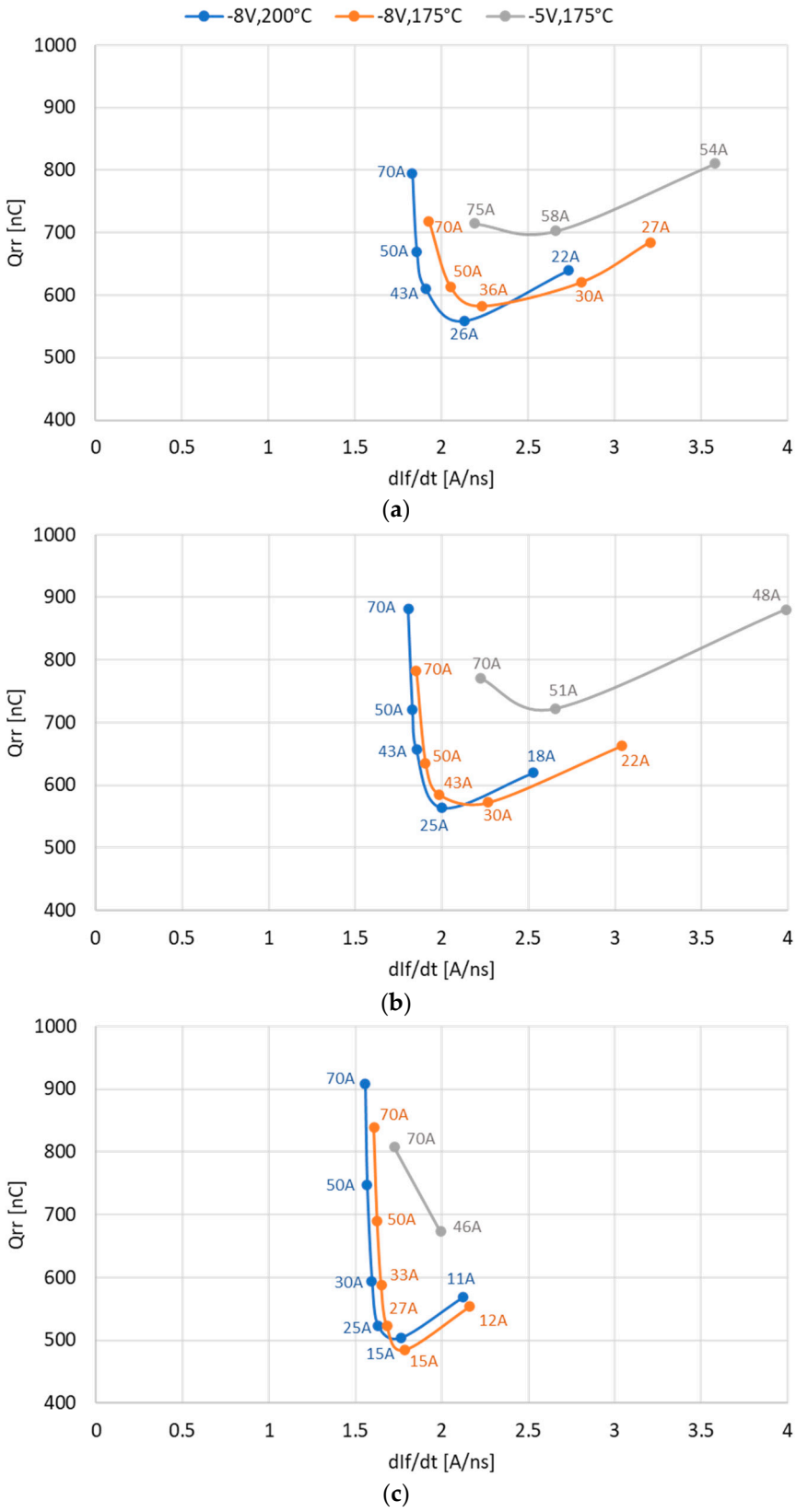


Figure 19. Q_{rr} evaluation at the snappy recovery limit condition as a function of di_f/dt and I_f for three devices: (**a**) "Min", (**b**) "Typ" and (**c**) "Max".

This analysis allows us to understand the condition of a fast recovery at the operative condition boundary, and of the avoidance of the snappy recovery working region. Accord-

ing to the selected devices and their static parameters (in particular, the threshold voltage), snappy recovery can be triggered at a lower di_f/dt and current when the V_{th} is higher. This aspect must be taken into account, especially in case of devices connected in parallel, as is usually the case in power modules.

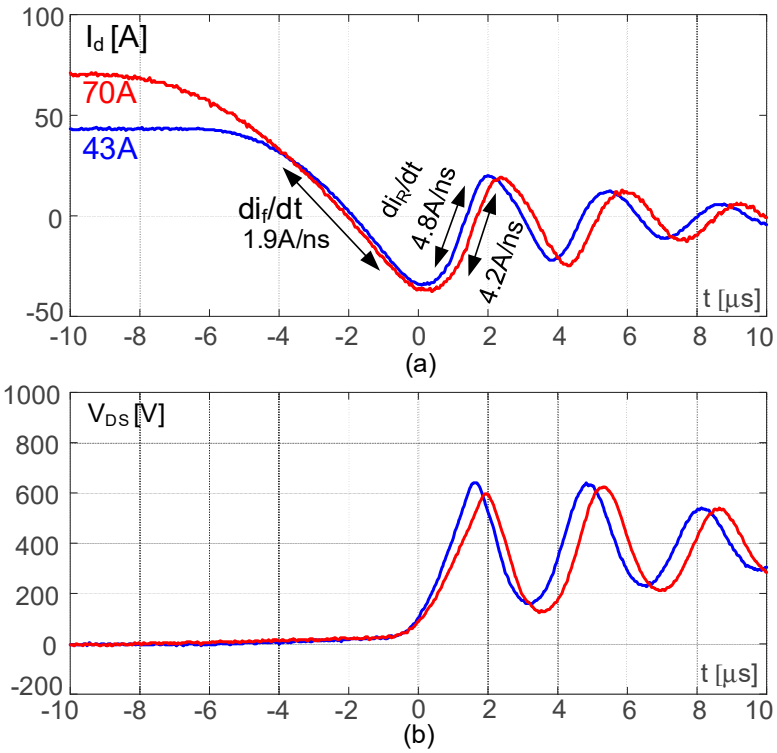


Figure 20. (**a**) Forward current and (**b**) V_{ds} voltage of device "Typ" at T_j = 200 °C, V_{G_L} = −8 V and forward current of 43 A and 70 A.

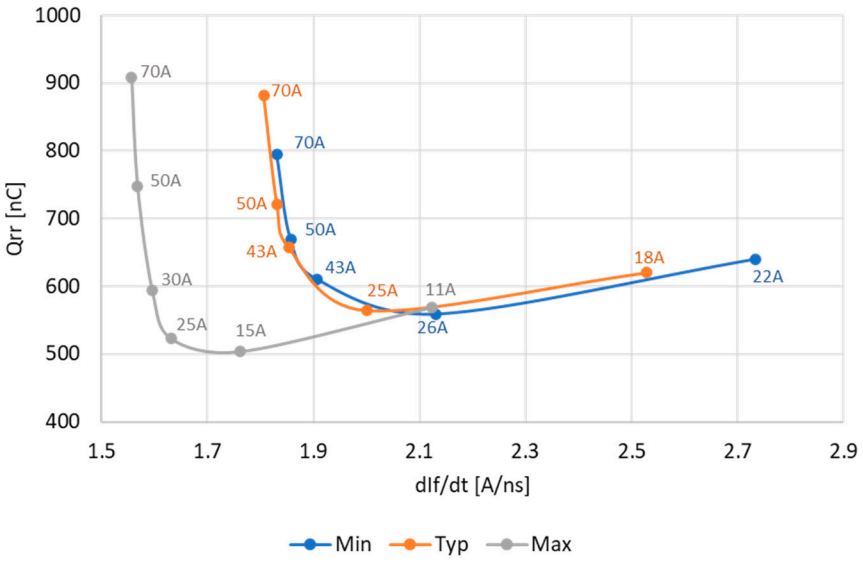


Figure 21. Q_{rr} vs. di_f/dt of three devices Min, Typ and Max at V_{G_L} = −8 V and T_j = 200 °C.

In the analysis reported in Figures 19 and 21, Q_{rr} varies as a function of the forward current and di_f/dt. There is a "valley" in the Q_{rr} curves because Q_{rr} decreases as the current decreases, while it increases as di_f/dt increases, and the snappy condition occurs at high di_f/dt and low current. More specifically, at low current, a further current reduction

requires a very large increment in di_f/dt to obtain snappy conditions, thus the effect of the latter is prevalent, showing an increment in Q_{rr}, and consequently there is a "valley" in the curve. For example, in Figure 19a, at $V_{G_L} = -5$ V/Tc = 175 °C (grey curve), to obtain the snappy condition passing from a current of 58 A to 54 A, it is necessary to increase the di_f/dt by about 40%. Therefore, the reduction in the current (−6.9%) is smaller than the di_f/dt increment, thus the overall effect is a Q_{rr} increment, accounting for the "valley".

5. Conclusions

The reverse recovery charge (Q_{rr}) at different operating conditions and the limit conditions at which snappy recovery occurs have been analyzed in this paper. More specifically, the analysis of the reverse recovery charge, Q_{rr}, revealed two unexpected phenomena at high temperatures: it decreases with increasing gate voltage; the higher the device threshold, the higher the Q_{rr}. TCAD-Silvaco simulations have shown that this is due to a displacement current flowing in the drift region due to the output capacitance voltage variation during commutation. From the analysis of the snappy recovery, it emerged that there is a minimum forward current slope, below which the reverse recovery cannot be snappy, even for a high current level. Once this current slope is reached, Qrr varies with the forward current only.

This analysis is useful in defining a set of conditions in order to be able to force or avoid snappy recovery occurrence. Although these results are noteworthy, further investigations on this topic are necessary. One interesting research path in this field is the development of models that help us better understand and explain the phenomena in other devices. Another is to provide formula of the reverse recovery loss and snappy conditions. From this perspective, it is necessary to check the reverse recovery response for each SiC MOSFET, since it depends on many parameters, on the technology structure (planar, trench, etc.) and the generation (on the market there are now devices of different suppliers belonging to the third or fourth generation, and typically, from one generation to the next one, there are modifications in technical properties).

The results of this work suggest that it is important to check static parameters as well as evaluate Q_{rr} trends and threshold limits of snappy recovery in real systems. This aspect is crucial in some applications, such as power modules for traction inverters where different SiC MOSFETs are connected in parallel, to ensure a balanced response during reverse recovery.

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Conflicts of Interest: Giuseppe Pennisi, Mario Pulvirenti, Luciano Salvo, Angelo Giuseppe Sciacca and Salvatore Cascino were employed by the company ST Microelectronics Co., Ltd. Antonio Laudani, Nunzio Salerno and Santi Agatino Rizzo declare that the research was conducted in the absence of any commercial or financial relationships that could be construed as a potential conflict of interest.

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