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Grid-Tied Single-Phase Integrated Zeta Inverter for Photovoltaic Applications

Anderson Aparecido Dionizio [1], Leonardo Poltronieri Sampaio [1,*], Sérgio Augusto Oliveira da Silva [1] and Sebastián de Jesús Manrique Machado [2]

[1] Electrical Engineering Department, Federal University of Technology—Paraná, Cornélio Procópio 86300-000, PR, Brazil; dionizio@alunos.utfpr.edu.br (A.A.D.); augus@utfpr.edu.br (S.A.O.d.S.)
[2] Electrical Engineering Department, Federal University of Technology—Paraná, Apucarana 86812-460, PR, Brazil; sebastiand@utfpr.edu.br
* Correspondence: sampaio@utfpr.edu.br

Abstract: Recently, the development of integrated inverters for photovoltaic systems has been widely performed to reduce overall system size, costs, and losses. Thus, integrated inverters have emerged as a prominent solution for replacing two-stage power conversion composed of a step-up converter and a voltage source inverter. Thereby, this paper proposes an integrated inverter topology for single-phase grid-tied photovoltaic systems. The proposed power converter, called a Single-Phase Integrated Zeta Inverter (SP-IZI), can boost the input voltage and inject a sinusoidal and regulated current into the mains with low harmonic distortion. The SP-IZI is based on integrating modified DC-DC Zeta converters, designed and controlled to operate in a discontinuous conduction mode, and presents similarities with the Modified Zeta Inverter (MZI). In this way, this paper compares the main parameters of both topologies and provides a complete study of the SP-IZI, involving both quantitative and qualitative studies as well as a small signals analysis. The feasibility and functionality of the proposed SP-IZI inverter are presented and evaluated through experimental results, which demonstrate that the SP-IZI presents the following advantages compared to the MZI: (i) the voltage in coupling capacitors is 13% lower; (ii) voltage stresses in switches and diodes are 40% lower; and (iii) static gain is similar to the traditional Zeta converter.

Keywords: DC-AC power conversion; integrated inverter; integrated zeta inverter; photovoltaic systems; zeta converter

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1. Introduction

Research and technological development involving renewable energies have been growing considerably in the past years [1–4]. This growth is mainly motivated by the necessity of expanding electricity generation and distribution by employing technologies that cause less environmental impact than traditional energy sources, such as those based on fossil fuels and mineral coal [3,5]. In this way, regulatory agencies are fundaments in regulating, inspecting, and promoting environmentally friendly electrical energy sources [6,7].

Particularly, photovoltaic (PV) systems can be widely used in various commercial/residential and industrial applications. However, PV panels present low efficiency, about 27% in the more efficient structures. Different materials have been used in PV panel building in the last years, reaching higher efficiency [8].

On the other hand, these sources produce direct current (DC) power, so it cannot be directly integrated into the conventional AC utility grid. Hence, it is necessary to make adequate the level and waveform of their voltages to achieve proper uses. Thus, the conditioning of this energy source can be performed using electronics-based power topologies to achieve DC-DC and DC-AC conversion [9–16].

Traditionally, a step-up DC-DC converter is associated with the voltage source inverter is performed to interface the PV system to the mains. This setup is characterized as a double-stage power conversion and is widely employed due to its simplicity. However, as disadvantages, this kind of conversion may present reduced efficiency, as well as a higher weight and size once a higher number of electrical and electronic components are needed [9,11,17–21].

Techniques to decrease issues in the DC-DC converter were proposed in [22,23]. In Refs. [22,23], a topology was suggested for PV applications that use multiple input sources and a single output; then, the circuit can operate with failure in some input sources. In addition, the converter structure can supply a higher or lower voltage in its output than the inputs. In Ref. [24], current and voltage oscillations in a PV generation connected to a single-phase utility grid were analyzed. The initial approach to reduce the oscillations is by using huge decoupling capacitors. However, an average current mode control is proposed for double-stage power conversion, reducing the second-order harmonic propagation.

A microinverter used to interface a PV module into the utility grid has been proposed in [25], which is deployed by the cascade association of a DC-DC flyback converter to the full-bridge inverter. Similarly, an association of an isolated DC-DC Zeta converter with multiple outputs, each connected to a voltage source inverter, is proposed in [26].

On the other hand, major research has been conducted to overcome the disadvantages mentioned above in the field of single-stage power conversion topologies [11–21]. The main advantage of the integrated inverter is its ability to perform the boost of the input PV voltage and simultaneously provide a regulated and controlled AC voltage or current in its output. Furthermore, in most cases, the integrated topologies employ fewer components and/or present a distinct topology configuration that leads to lower weight, size, and losses. However, combining the power stages and the presence of non-minimum phase characteristics can lead to significant difficulties in voltage and/or current control [27–29].

In Ref. [30], a submodule based on an isolated Ćuk converter has been proposed. The system analyzed includes a marine energy source, PV generation, battery storage, AC grid, and vessel supply. The main goal is to decrease dependence on fossil fuels in the shipping industry. The converter topology allows for bidirectional power flow and output voltage to be higher or lower than the input, as well as providing galvanic isolation.

In Ref. [31], an integrated topology based on a Zeta inverter is also proposed and designed to operate in continuous conduction mode (CCM) or discontinuous conduction mode (DCM). A feedback controller associated with a feedforward control loop and repetitive control was proposed to deal with different system dynamics once the converter operates in CCM and DCM. An integrated converter topology based on a DC-DC Ćuk converter presenting galvanic isolation and the capability to perform high voltage gains is proposed in [32]. On the other hand, the power converters presented in [33,34] have reduced switching devices. In Ref. [33], a microinverter is proposed based on the isolated DC-DC Zeta inverter. In Ref. [34], an inverter is shown derived from the Ćuk and Watkins-Johnson converter, which minimizes the problems related to parasite capacitances; it can operate either grid-tied or autonomously (off-grid). In addition, a buck–boost dual-leg-integrated step-up inverter for the AC microgrid is proposed in [35]. In this case, during one switching period, the topology presents four operation stages in each stage operation, where two switches are turned on while the other two remain turned off. Nevertheless, the inverter design can be complex. Considering the traditional step-up DC-DC converters, in Ref. [27], a family of integrated inverters is presented. This family of integrated inverters works with the same number of switching devices compared to the traditional two-stage power converters.

To improve the traditional boost inverter, a dual-input dual-buck inverter with integrated boost converters is proposed in [36]. The topology uses two integrated boost converters and two inverters' legs. Once the topology works symmetrically, an integrated boost and an inverter leg are used in the positive half-cycle output. In contrast, the other part of the topology is accountable for operating in the negative half-cycle.

In addition, integrated inverters also can be employed for three-phase grid-tied PV applications, which can step-up the input voltage and inject a three-phase sinusoidal current into the mains. The power from the PV array is transferred equally to three-phase mains. Therefore, this topology is commonly employed for higher power levels when compared with single-phase systems [21,27,37,38].

More recently, new topologies have been proposed, such as the Modified Zeta Inverter (MZI) in [39,40], which is based on the modified DC-DC Zeta converter. The MZI presents three operation stages during each switching period. However, its third stage differs from the conventional DC-DC converters operating at DCM. The currents through the input inductors from MZI present three steps. First, the current starts at zero and grows linearly to the peak value. In the second, it decreases linearly to zero. In the third, it is kept at zero.

On the other hand, the current through the output inductor acts as CCM. The current starts at a minimum value in the first operation stage and grows linearly to the maximum. After, the current decreases and reach the minimum value at the end of the switching period. Besides the distinct third operation stage, compared to conventional DC-DC converters, the voltages across some elements—such as the power switches, diodes, and coupling capacitors—can be higher and not easily determined.

This paper proposes an integrated inverter topology able to interface the PV array and the single-phase mains. The proposed topology combines the modified DC-DC Zeta converters, and is called a Single-Phase Integrated Zeta Inverter (SP-IZI). The SP-IZI can perform both the input voltage boosting and inject a sinusoidal current into the mains with low total harmonic distortion (THD). The entire analysis and development of the proposed SP-IZI are evaluated and validated from experimental results.

This paper is organized as follows: Section 2 describes the functionality, operation, and modeling of the proposed SP-IZI, while Section 3 compares the main differences between the proposed SP-IZI and the MZI. Section 4 presents and discusses the results obtained from experimental results. Finally, Section 5 presents the conclusions.

2. Functionality, Operation, and Modeling of the Proposed SP-IZI

As mentioned earlier, the proposed inverter can connect the PV array to the single-phase mains through an integrated converter topology. The system can simultaneously perform the DC PV-voltage boost while injecting a sinusoidal current into the mains by extracting the maximum energy available at the PV array, as illustrated in Figure 1.

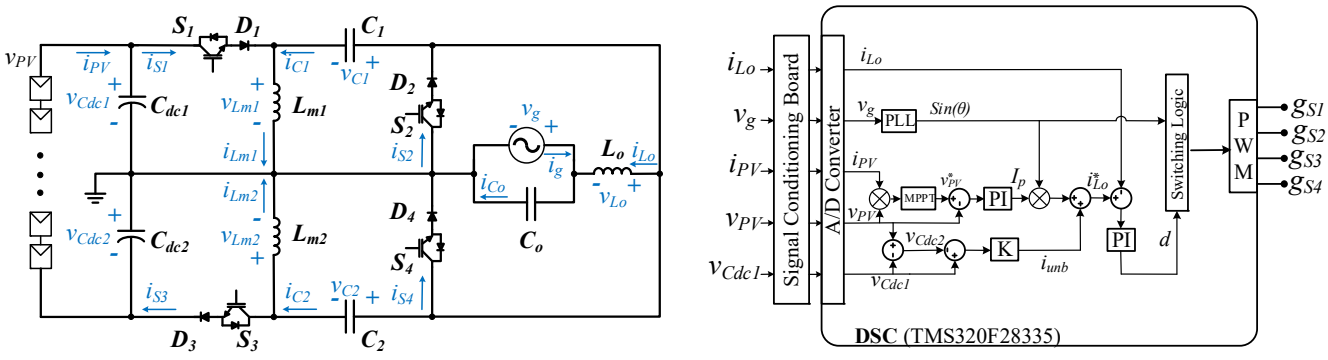


Figure 1. Scheme of the SP-IZI circuit: (**a**) electrical circuit; (**b**) control diagram block.

The SP-IZI is built by integrating modified DC-DC Zeta converters, each operating in a semi-cycle of the utility grid. The topology is designed to work in discontinuous conduction mode (DCM). In this operation mode, the static gain is linear. Thus, the proportional–integral controller gains can be easily tuned. The SP-IZI injects an active and synchronized current into the single-phase utility grid, attending to power quality standards and requirements [41,42]. The SP-IZI is controlled by employing a multiloop

control, in which the inner control loop regulates the injected current into the grid and is designed with a higher bandwidth than the outer loop. In contrast, the voltage control loop is set to be slower than the current control loop. It is responsible for maintaining the PV array voltage according to the reference provided by the MPPT algorithm. The SP-IZI control, the MPPT, and the PLL algorithms are addressed in Section 2.7.

2.1. Operation of the SP-IZI

The SP-IZI has three stages of operation during a switching period. In a simplified way, the division of the half-cycles of the utility grid voltage allows the topology to present the same operation stages as the traditional DC-DC Zeta converter. Figure 2 illustrates the three operation stages of the SP-IZI circuit.

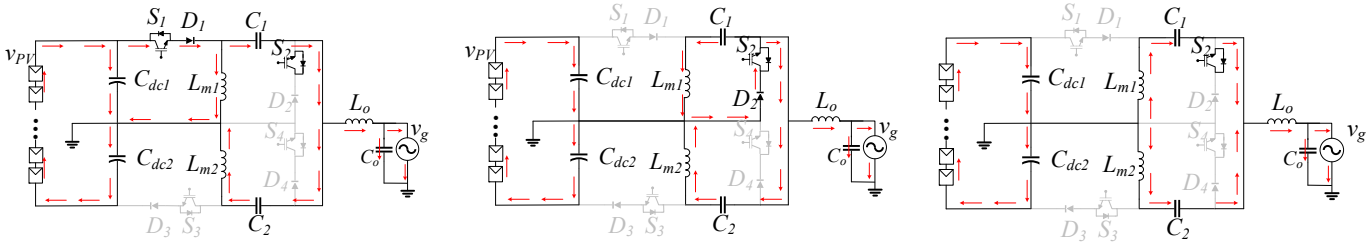


Figure 2. SP-IZI operation stages for the positive half-wave cycle of the mains: (**a**) D_aT_s; (**b**) D_bT_s; (**c**) D_cT_s.

Analyzing the positive half-wave cycle and disregarding the component losses, the switch S_1 is turned on in the first stage of operation (D_aT_s), and the switch S_2 is turned on during the entire positive half-wave cycle, but in this stage of operation, it is not sending current through the diode D_2, which is placed in series with switch S_2.

The voltage across the inductor L_{m1} is equal to the voltage across the capacitor C_{dc1}. Ideally, it represents half of the PV voltage amplitude ($v_{PV}/2$). At the same time, the inductor L_{m2} voltage is equal to half of the PV array voltage plus the sum of the voltage across the capacitors C_1 and C_2, such that $v_{Lm2} = v_{Cdc1} + v_{C1} - v_{C2}$. When $v_{C1} = v_{C2}$, the voltage across the inductor L_{m2} is equal to v_{Cdc1}. Furthermore, the output inductor (L_o) presents a voltage equivalent to the sum of the voltages across the capacitor C_{dc1}, capacitor C_1, and capacitor C_o, such as $v_{Lo} = v_{Cdc1} + v_{C1} - v_{Co}$. The current flowing through the capacitor C_1 is the sum of the currents that flow through the inductors L_{m2} and L_o. The current through the capacitor C_2 is equal to the inductor L_{m2} current for the entire positive half-cycle of the grid. This operating stage can be seen in Figure 2a.

The second operation stage (D_bT_s) initiates when the switch S_1 is turned off. Thus, the accumulated energy in the inductor L_{m1} is transferred to the capacitor C_1 through the switch S_2 and diode D_2.

The voltage across the inductor L_{m1} is the same as that of the capacitor C_1 ($v_{Lm1} = -v_{C1}$). The energy accumulated in the inductor L_{m2} is transferred to the capacitor C_2. Thus, the voltage across the inductor L_{m2} is the same as that of the capacitor C_2 ($v_{Lm2} = -v_{C2}$). Since the voltages across capacitors C_1 and C_2 are equivalent, the inductors L_{m1} and L_{m2} will be magnetized with the same ratio in D_aT_s and proportionally demagnetized in D_bT_s. For D_bT_s, the current through the capacitor C_1 is the same as in inductor L_{m1}. The voltage across the inductor L_o is equal to that of the capacitor C_o ($v_{Lo} = -v_{Co}$). This stage is visualized in Figure 2b.

The third stage (D_cT_s) starts when the currents through the inductors L_{m1} and L_{m2} decrease to their minimum values, and the sum of their currents cannot polarize the diode D_2 to operate in conduction mode. At this moment occurs the current change between the inductors. All the diodes are blocked in this stage, causing the current to flow only through the passive elements. Hence, the voltage across the inductors is nearly null, resulting in

voltage equality between the capacitors C_1 and C_2. This operation stage is visualized in Figure 2c.

By driving the switches S_3 and S_4, the operation analysis of the SP-IZI for the negative half-cycle of the grid voltage is performed similarly to the operation of the converter in the positive half-cycle.

2.2. Static Gain of SP-IZI Structure

From the description of the SP-IZI operation, it is possible to derive the voltage equation of the inductor L_{m1} during one switching period. Knowing the average voltage in the inductor is null in steady-state, the following relationship can be obtained:

$$V_{Lm1_{av}} = V_{dc1}D_{\mathrm{a}} - V_{C1}D_{\mathrm{b}} + (V_{C2} - V_{C1} + V_{Lm2})D_{\mathrm{c}} = 0 \tag{1}$$

The average voltage across the inductor L_{m2} is null and calculated as follows:

$$V_{Lm2_{av}} = (V_{dc1} + V_{C1} - V_{C2})D_a - V_{C2}D_b + (V_{Lm1} - V_{C1} + V_{C2})D_c = 0 \tag{2}$$

As analog from (1) and (2), the average voltage in the inductor L_{o} is derived as:

$$V_{Lo_{av}} = (V_{Cdc1} + V_{C1} - V_{Co})D_a - V_{Co}D_b + (V_{Lm2} + V_{C2} - V_{Co})D_c = 0 \tag{3}$$

Equaling (1)–(3), the result is that the average voltages across the three capacitors are the same, i.e., $V_{C1} = V_{C2} = V_{Co}$. Analyzing the third operation stage, the sum of the voltages across the inductors L_{m1} and L_{m2} is equal to the sum of the voltages across the coupling capacitors $V_{Lm1} - V_{Lm2} = V_{C1} - V_{C2}$, resulting in equality between L_{m1} and L_{m2} voltages. In this stage, the output inductor voltage also can be described as the sum of the voltages across the inductor L_{m1} and capacitors C_1 and C_o, resulting in $V_{Lo} = V_{Lm1} + V_{C1} - V_{Co}$. Since the average voltages in these capacitors are equal, the absolute voltages in L_{m1} and L_o must be nearly the same in the third operation stage. Therefore, the voltages across the three inductors in this stage are ideally null.

In the operation stage D_cT_S, considering the voltages across the inductors are null, the operation stages D_aT_S and D_bT_s can be related by:

$$V_{Cdc1}D_a = V_{C1}D_b \tag{4}$$

In the charging interval (D_a), the current through the switch S_1 is the sum of the three inductors' currents. As mentioned, the average voltages across the capacitors present the same value. Consequently, all inductors are charged with half of the input voltage during this stage.

The current through the switch S_1 flows only in the first operation stage. Considering the charge of the inductor, the average value of this current is calculated as follows:

$$I_{S1_{av}} = \frac{I_pD_aT_s}{2} = \frac{V_{cdc1}D_a2T_s}{2}\left(\frac{1}{L_{eq}}\right) \tag{5}$$

where I_p is the current peak in the semiconductors and L_{eq} is the parallel association of the inductors L_{m1}, L_{m2}, and L_o.

In Ref. [43], a converter modeling approach that uses an effective resistance (R_e) to represent the processed power was proposed. The power dissipated on this resistance is equivalent to the output power. In the SP-IZI, this power can be calculated by the product to half input voltage, or ideally V_{cdc1}, and the average current through the switch S_1. Thus, R_e is defined as:

$$R_e = \frac{2L_{eq}}{D_a{}^2T_s} \tag{6}$$

The proposed topology acts as an integrated inverter, injecting current into the utility grid. Therefore, the balance of power can be expressed as:

$$P_{in} = P_{out} = \frac{{V_{cdc1}}^2}{R_e} = \frac{{V_g}^2 P_{out}}{{v_g}^2} \tag{7}$$

The static gain is the relation between the output and input voltages, considering the voltage peak of the utility grid (V_p); using (6) and (7), the static gain as expressed as:

$$G_e = V_p \sqrt{\frac{1}{2R_e P_{out}}} = V_p D_a \sqrt{\frac{1}{4L_{eq} P_{out} f_s}} \tag{8}$$

where f_s is the switching frequency.

The voltage across the capacitor C_1 is nearly equal to the utility grid. Therefore, using (4) and (8), the second operation stage is determined as:

$$D_b = \frac{\sqrt{4P_{out} L_{eq} f_s}}{V_p} \tag{9}$$

2.3. Waveforms Concerning the Utility Grid

The SP-IZI operates as an integrated inverter that performs the interface between a PV array and the single-phase utility grid. The output current of SP-IZI is controlled to guarantee that a sinusoidal current is injected into the grid. Hence, each switching device of SP-IZI presents distinct modulation. Figure 3a shows the commutation signals used in SP-IZI for the entire grid voltage period.

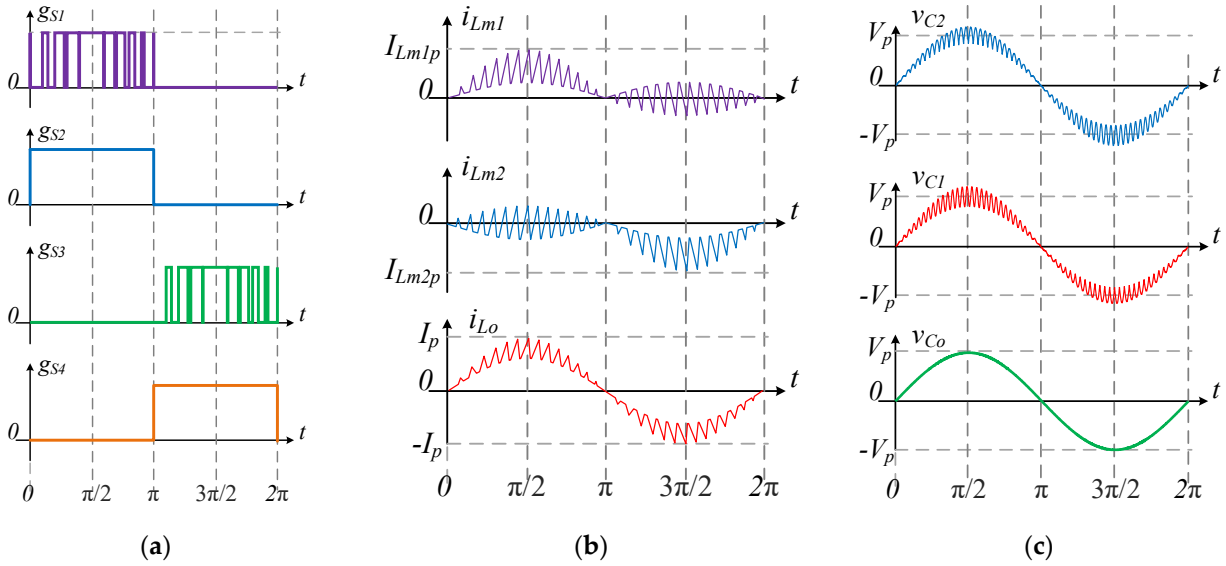


Figure 3. Waveforms for one period of the utility grid: (**a**) gate signals for the switches; (**b**) currents through the inductors; (**c**) voltages across the capacitors.

The voltage across the capacitor C_1 presents the same value as the utility grid but with some voltage ripple. Similarly, the capacitor C_2 also presents the same grid voltage waveform grid. Figure 3c shows the voltage waveforms of the capacitors C_1 and C_2 and the utility grid voltage waveform.

Considering the equal voltage across the capacitors C_1 and C_2, the resulting inductors' L_{m1} and L_{m2} voltages are the same. Thus, in each switching period, both inductors are magnetized and demagnetized with the same intensity, presenting the same current ripple.

On the other hand, during the whole positive half-wave cycle of the utility grid, the currents through the inductor L_{m2} and capacitor C_2 are the same, and the average capacitor current is null. Consequently, the average L_{m2} current also is null at this half-wave cycle. By symmetry of the topology, the average L_{m1} current is null at the negative half-wave

cycle. Figure 3b presents the current waveforms of the inductors for a complete utility grid period.

2.4. State-Space Model for the Inner Control Loop

Using the generalized switch-averaging modeling approach, the equations for the internal control loop in state-space is derived. The corresponding equations for the outer control loop are obtained, taking into account the power balance between the extracted PV array power and the injected power into the mains. Once the equations are obtained, the SP-IZI is analyzed for the operation in conjunction with the adopted MPPT and PLL algorithms.

During each switching period, the SP-IZI has three operating stages, D_aT_s, D_bT_s, and D_cT_s. Due to the symmetric operation of the proposed inverter, the same behavior for the positive half-wave cycle is equivalent to what occurs in the negative half-cycle. In this way, it is possible to simplify the converter structure for analysis such as the one acting in a half-cycle. It is noticed that, during a switching period, the current is divided between the inductors L_{m1} and L_{m2}, as compared to a conventional Zeta converter, where this current flows through the inductor L_m, which is equivalent to a parallel association of L_{m1} and L_{m2}. Once both inductors present the same inductance, it is possible to write $L_m = \frac{L_{m1}}{2}$. The current is also divided between capacitors C_1 and C_2, resulting in the coupling capacitor (C_a) for the conventional Zeta converter. The capacitor C_a is assumed to be the parallel between C_1 and C_2, and if $C_1 = C_2$, the equivalent capacitor is equivalent to $C_a = 2C_1$.

The average state-space model is widely employed for modeling dynamic systems by its simplicity. The state-space model can be obtained for the static converters operating in both CCM and DCM [43–47]. The SP-IZI presents the behavior as very close to the conventional Zeta converter operating in DCM. Thus, converter modeling is adopted as an equivalent model for the SP-IZI. The utility grid, v_g, can be represented as an input system in the matrix "B" in the state-space modeling. The voltage across the capacitor C_{dc1} also can be considered an input in this matrix. Furthermore, the line inductance (L_g) and resistance (r_g) between the inverter and the utility are also taken into account. These considerations for converter modeling ensure a better system response. Thus, Figure 4 presents the equivalent model used in the SP-IZI modeling.

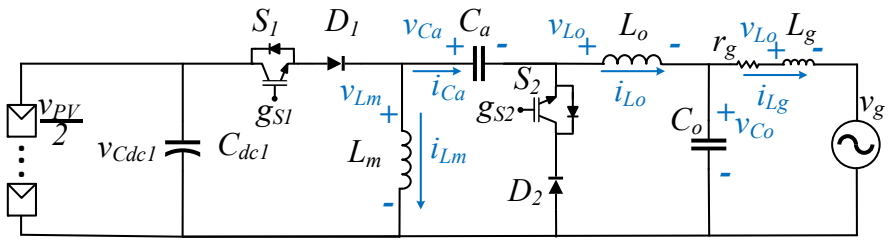


Figure 4. Equivalent circuit to the analysis of the SP-IZI.

In Ref. [33], the state matrix of the converter operating in DCM was adequate through a modification in the matrix concerning the inductor current to represent the system behavior in discontinuous operation.

In addition, a generalized switch-averaging technique is adopted in [31,47], which is associated with the average state-space model to overcome the problems of representing the dynamical characteristics of the converter operating in DCM.

The employed modeling is based on the linearization of the state variables around the quiescent operating point, in which small oscillations are considered in the mean value. Hence, a generic variable $\overline{x}$ is represented by a mean term (DC) plus a first-order AC term, $\overline{x} = X + \hat{x}$, with X representing the DC term and $\hat{x}$ the AC term. There are considerations that the DC terms are much greater than the AC terms, $|X|$" $|\hat{x}|$ [43].

The average state-space model is initially adopted for modeling the SP-IZI according to Equation (6).

$$\dot{\overline{x}} = MA_m\overline{x} + B_m\overline{u} \tag{10}$$

where $\overline{x}$ is the state vector, $\overline{u}$ is the input vector, A_m is the average state matrix for a switching period, B_m is the average input matrix, and M is the corrected matrix to DCM. The corrected matrix M can be obtained for the state-space averaging model of the SP-IZI operating in DCM as follows:

$$M = \begin{bmatrix} \frac{1-D_b}{D_a} & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 0 & 1 \end{bmatrix} \tag{11}$$

Performing the state-space averaging model and considering the adequacy matrix [see Equation (10)], the equivalent circuit representation for the SP-IZI presented in Figure 4 is determined as follows:

$$\begin{bmatrix} \dot{\overline{i}}_{Lm} \\ \dot{\overline{i}}_{Lo} \\ \dot{\overline{v}}_{Ca} \\ \dot{\overline{v}}_{Co} \\ \dot{\overline{i}}_{Lg} \end{bmatrix} \begin{bmatrix} 0 & 0 & a_1 & a_2 & 0 \\ 0 & 0 & a_3 & a_4 & 0 \\ \frac{D_b - D_b^2}{C_a D_a} & \frac{D_b - 1}{C_a} & 0 & 0 & 0 \\ 0 & \frac{1}{C_o} & 0 & 0 & \frac{-1}{C_o} \\ 0 & 0 & 0 & \frac{1}{L_g} & \frac{-r_g}{L_g} \end{bmatrix} \begin{bmatrix} \overline{i}_{Lm} \\ \overline{i}_{Lo} \\ \overline{v}_{Ca} \\ \overline{v}_{Co} \\ \overline{i}_{Lg} \end{bmatrix} + \begin{bmatrix} \frac{D_a}{L_m} & 0 \\ \frac{D_a}{L_o} & 0 \\ 0 & 0 \\ 0 & 0 \\ 0 & \frac{-1}{L_g} \end{bmatrix} \begin{bmatrix} \overline{v}_{Cdc1} \\ \overline{v}_g \end{bmatrix} \tag{12}$$

$$y = \begin{bmatrix} 0 & 1 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} \overline{i}_{Lm} \\ \overline{i}_{Lo} \\ \overline{v}_{Ca} \\ \overline{v}_{Co} \\ \overline{i}_{Lg} \end{bmatrix} \tag{13}$$

where $a_1 = \frac{-(L_m+L_o)D_b - L_m D_c}{L_m(L_m+L_o)}$; $a_2 = \frac{L_m D_c}{L_m+L_o}$; $a_3 = \frac{(L_m+L_o)D_a - L_m D_c}{L_o(L_m+L_o)}$; $a_4 = \frac{-(D_a+D_b)(L_m+L_o) - L_o D_c}{L_o(L_m+L_o)}$; and y represents the output vector.

If the equivalent circuit operates in CCM, the adequacy matrix has a unit value associated with eliminating the $D_c T_s$ operation step, which results in an averaging model also valid for the operation in CCM.

By manipulating (12) and (13), it is possible to determine the transfer function that relates the current in the inductor L_o to the duty cycle as follows:

$$G_{id}(s) = \frac{\hat{i}_{Lo}(s)}{\hat{d}(s)} = C\left(s - MA_m + \frac{B_d k_s M C_m}{1 - k_s E_d}\right)^{-1} + \frac{B_d k_c}{1 - k_s E_d} \tag{14}$$

where $k_s = [k_{id}\ k_{vs}]$ and the matrices B_d and E_d are defined in order to obtain the closed-loop system matrices as follows:

$$E_d = [C_1 - C_2] \begin{bmatrix} \overline{i}_{Lm} \\ \overline{i}_{Lo} \\ \overline{v}_{Ca} \\ \overline{v}_{Co} \\ \overline{i}_{Lg} \end{bmatrix} + [E_1 - E_2] \begin{bmatrix} \overline{v}_{Cdc1} \\ \overline{v}_g \end{bmatrix} \tag{15}$$

$$B_d = \left[A_1 - \frac{D_b}{D_b + D_c} A_2 - \frac{D_c}{D_b + D_c} A_3\right] \begin{bmatrix} \overline{i}_{Lm} \\ \overline{i}_{Lo} \\ \overline{v}_{Ca} \\ \overline{v}_{Co} \\ \overline{i}_{Lg} \end{bmatrix} + \left[B_1 - \frac{D_b}{D_b + D_c} B_2 - \frac{D_c}{D_b + D_c} B_3\right] \begin{bmatrix} \overline{v}_{Cdc1} \\ \overline{v}_g \end{bmatrix} \tag{16}$$

where A_1, A_2, and A_3 correspond to the respective state matrices for the passive elements during the operating stage D_a, D_b, and D_c; B_1, B_2, and B_3 are the input matrices

for the passive elements. The matrices C_1 and C_2 represent the output matrices of the generalized switch model, while E_1 and E_2 are the direct transition matrices of the generalized switch model. The matrix A_m is obtained by the operation stages averaging, i.e., $A_m = A_1D_a + A_2D_b + A_3D_c$. The same procedure step is also valid for obtaining the matrix C_m, i.e., $C_m = C_1D_a + C_2D_b + C_3D_c$.

2.5. Components Design

To guarantee the SP-IZI operates in DCM during all grid periods, the design of the components considers the voltage peak of the utility grid. However, the current injected into the grid presents a low ripple, and the output inductance is calculated as:

$$L_o = \frac{V_{cdc1} D_a T_s}{\Delta_{I_{Lo}} I_{Lo}} \tag{17}$$

where I_{Lo} is the average current during the voltage peak and $\Delta_{I_{Lo}}$ is the maximum ripple allowed.

The input inductors present a current ripple bigger than the average value and strongly influence the operation in the DCM. A maximum inductance can be obtained as follows:

$$L_{m1_{max}} = \frac{2V_p{}^2 L_0 (1 - 2D_a + D_a{}^2)}{4P_{out} L_o f_s - V_p{}^2 (1 - 2D_a + D_a{}^2)} \tag{18}$$

The output capacitance is calculated following a similar procedure commonly used for a buck converter and depends on the current and voltage ripple allowed, as obtained by:

$$C_o = \frac{\Delta_{I_{Lo}} I_{Lo}}{8 f_s \Delta_{V_{Co}} V_{Co}} \tag{19}$$

The coupling capacitances are designed in a range between two resonant frequencies, ωr_{min} and ωr_{max}. These capacitances are calculated as:

$$\left.\frac{1}{2\omega r^2}\right|_{\omega r = \omega r_{max}} < C_1 < \left.\frac{1}{2\omega r^2}\right|_{\omega r = \omega r_{min}} \tag{20}$$

After the design of the components are combined, the modeling presented in (14) can obtain the frequency response, as shown in Figure 5. There is a high similarity between the model and the circuit simulated in the software PSIM.

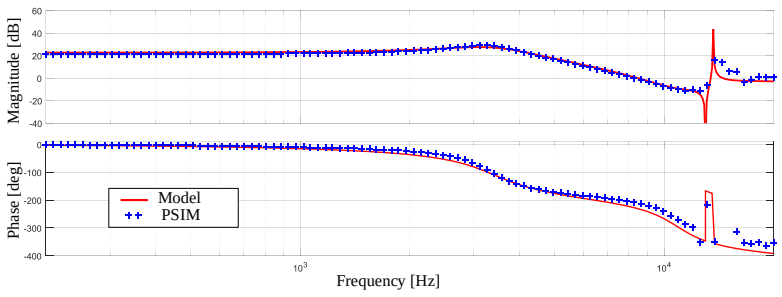


Figure 5. Bode diagram of the model and the SP-IZI.

2.6. Modeling of the Outer Control Loop

The outer voltage control loop is modeled considering the energy conservation between the PV array and the utility grid. Ideally, the energy extracted from the PV array is the same as that injected into the grid. As the output of SP-IZI is sinusoidal, the active power can be determined through the voltage and current magnitude peaks, V_p and I_p, respectively. In this way, the power balance is defined as follows:

$$v_{PV} i_{Cdc1} = \frac{V_p I_p}{2} \tag{21}$$

Replacing i_{Cdc1} for the ratio between the voltage across the capacitor C_{dc1} and the Laplace transform of the capacitor, applying small-signal perturbations, and posteriorly disregarding second-order terms as well as the oscillation in the grid, it is possible to find the transfer function that relates the PV array voltage to the grid current by (22).

$$G_{vi}(s) = \frac{\hat{v}_{PV}(s)}{\hat{i}_p(s)} = \frac{V_p}{2V_{PV}C_{dc1}s} \tag{22}$$

2.7. MPPT and PLL Algorithm

As is well-known, the PV array presents non-linear characteristics curves (power versus voltage and current versus voltage). In addition, the PV array depends on the climate conditions, such as solar irradiance and temperature. Therefore, using algorithms to perform the maximum power point tracking (MPPT) is mandatory to extract the total available power at the PV array. Hence, this paper adopts the traditional Perturb and Observe (P and O) to reach the maximum available capacity of the PV array [48–52].

A non-autonomous adaptative filter AF-αβ-pPLL technique is used in this paper for determining the synchronous unit vectors coordinates [sin(θ) and cos(θ)], which is detailed in [53]. The AF is responsible for extracting the fundamental component of the grid voltage. The adopted AF-αβ-pPLL is designed to deal with voltage disturbances, such as voltage sags/swells, voltage harmonics, phase-angle jumps, and frequency variations [53].

2.8. SP-IZI Control

The control of the SP-IZI is performed by a multiloop control as follows: (i) an inner current control loop controls the injected current into the grid (i_{Lo}); (ii) an outer voltage control loop controls the PV array (v_{pv}); and (iii) a maximum power point tracking (MPPT) algorithm extracts the maximum power available at the PV array measuring the PV array voltage (v_{pv}) and current (i_{pv}). Initially, the MPPT algorithm generates the reference voltage (v^*_{PV}) for the voltage control loop to extract the maximum PV array power. The voltage control loop's proportional–integral (PI) controller computes the peak current reference (I_p) needed to maintain the PV array voltage regulated at the reference provided by the MPPT. Thus, such peak current reference (I_p) is used to generate the current control loop's current reference (i^*_{Lo}), which is synchronized to the grid voltage (v_g) using a phase-locked-loop (PLL) technique, i.e., the peak current is multiplied by the sinusoidal ($sin(\theta)$) vector. In addition, considering possible imbalance between the voltages over the input DC-bus capacitors (C_{dc1} and C_{dc2}) can occur, a DC current (i_{unb}) is associated with the sinusoidal current reference ($I_p sin(\theta)$) to guarantee a balanced voltage between v_{Cdc1} and v_{Cdc2}. Finally, the current control loop's PI controller generates the duty cycle used in the switching logic to control the switching devices.

The proportional and integral gains of the PI controllers are tuned based on the procedure design proposed in [54]. The block diagram of the control diagram is presented in Figure 6a, while the block diagram of the signal logic adopted to control the switches of the SP-IZI is depicted in Figure 6b.

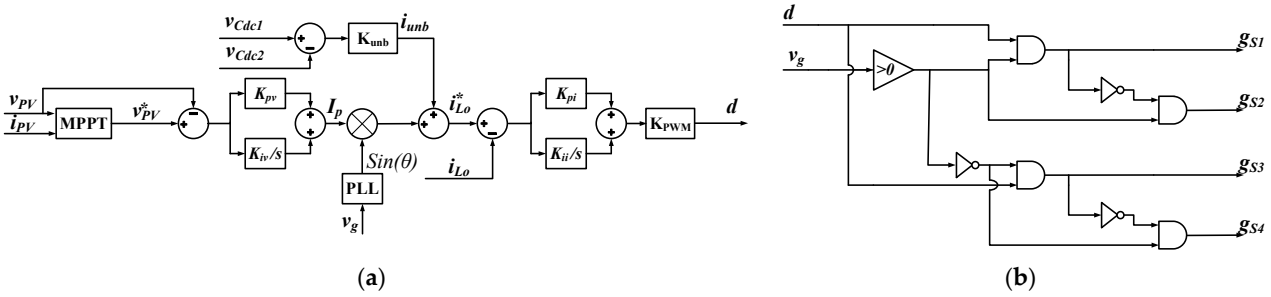


Figure 6. Block diagrams: (**a**) control diagram; (**b**) switching control logic.

3. Comparison between the SP-IZI and the MZI

The proposed SP-IZI operates similarly to the integrated inverters called MZIs [39,40]. In addition, accordingly to the characteristics presented by the SP-IZI, the following advantages are obtained when compared to the MZI: (i) the static converter gain in DCM is identical to the traditional DC-DC Zeta converter; (ii) it presents reduced voltage stress over the switches and diodes; and (iii) it can operate in an off-grid mode for a different type of load.

The MZI is based on the modified Zeta converter and controlled to inject a sinusoidal current into the utility grid. The topology operates in DCM. Therefore, a switching period is divided into three operation stages referred to as t_a, t_b, and t_c. Figure 7 presents the MZI.

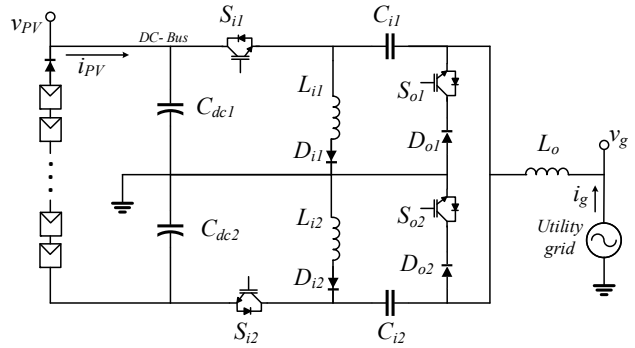


Figure 7. The electrical circuit of the MZI.

The diodes D_{i1} and D_{i2} in series with the inductors L_{i1} and L_{i2} prevent negative current during the third operation stage through the inductors mentioned. These diodes also prevent the current through all passive elements during the first and second stages, as in the SP-IZI.

According to the electrical circuit of the MZI and its operation, besides considering the peak amplitude of the grid, the gain of the inverter is determined as:

$$G_e = \frac{v_g}{V_{pv}} = \frac{{D_a}^2 + D_a D_b}{2D_b} \cdot \frac{D_a f_s L_i + D_a \sqrt{{L_i}^2 {f_s}^2 + \frac{2L_i {V_p}^2 f_s}{P_o}}}{4 f_s L_i} \tag{23}$$

where D_a and D_b represent the respective first and second operation stages during the peak voltage of the grid, f_s is the switching frequency, L_i is the input inductance, V_p is the peak voltage of the grid, and P_o is the output power.

The voltage across the capacitors C_{i1} and C_{i2} are distinct between the MZI and the SP-IZI or the conventional Zeta converter. In the MZI, these voltages are related to the first operation stage. In the SP-IZI, the voltage of the intermediate capacitor is similar to that of the utility grid. The voltage across the intermediate capacitors to the MZI is determined as:

$$V_{Ci} = \frac{V_{pv} d_a}{2 d_b} \tag{24}$$

According to (23), the first and second operation stages depend on the input inductance, switching frequency, grid voltage, and output power. Maintaining the output power and switching frequency as constant, in addition to considering the peak voltage of the utility grid, the voltages across the coupling capacitors (24) are related to the input inductance, in which lower values result in higher voltages. Conversely, high inductance values make the topology operate in CCM. Figure 8a presents the intermediate capacitors' average voltage dependence with the input inductance to the MZI and the voltage across the coupling capacitors to the SP-IZI.

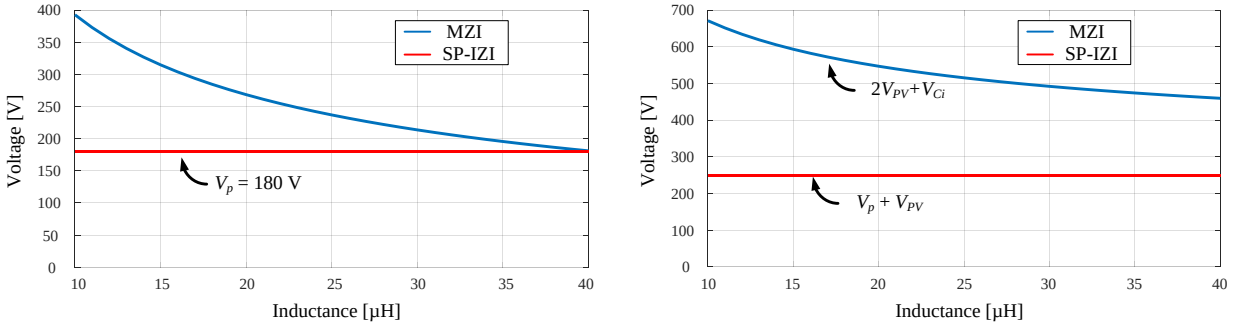


Figure 8. Voltage dependence to the MZI: (**a**) coupling capacitor average voltage; (**b**) maximum voltage switches.

Consequently, the maximum voltages across the switches S_{i1} and S_{i2} in the proposed inverter, MZI, depend on the input inductance and the voltage across the coupling capacitors. Thus, the voltages across these switches are described as $V_{Simax} = V_{Ci} + 2V_{PV}$. Figure 8b shows the maximum voltage across the switches S_{i2} and S_{i2} to the MZI and the S_1 and S_3 to the SP-IZI.

In brief, the voltages across the semiconductors are higher in the MZI than in the SP-IZI, which causes limitations in the operation range and power losses during commutation. Table 1 compares the main parameters of the MZI and the SP-IZI.

Table 1. Comparison between the main parameters of MZI and SP-IZI.

Parameters	MZI [39,40]	SP-IZI
Maximum coupling capacitors' voltage	$V_{Ci} = \frac{2V_g - V_{PV}D_a}{2D_a}$	$V_{Ci} = V_P$
Maximum switches voltage	$V_{si} = 2V_{PV} + V_{Ci}$ $V_{so} = 0.5V_{PV} + V_{CI}$	$V_{s1} = 0.5V_{pv} + V_p$ $Vs_2 = 0.5V_{PV} + V_P$
Maximum diodes voltage	$V_{Di} = -(1.5V_{PV} + V_{Ci})$ $V_{Do} = -(0.5V_{PV} + V_{Ci})$	$V_{D1} = 0.5V_{PV} - V_P$ $V_{D3} = -(0.5V_{PV} + V_P)$
RMS output inductor current	$I_{Lo} = Po/\sqrt{2}V_P$	$I_{Lo} = Po/\sqrt{2}V_P$
Input inductor peak current	$I_{Lmp} = V_{PV}D_aT_S/2L_i$	$I_{Lmp} = V_{PV}D_aT_S/L_m - I_{Lo}$

Based on the equations and the operational description of the SP-IZI using the MPP power in standard test conditions (STC), the theoretical values from the RMS currents through the semiconductors and inductors are calculated. In addition, the maximum semiconductors' and intermediate capacitors' voltages are determined. The MZI is also evaluated for the same conditions. Table 2 shows the main parameters of the adopted PV module. The theoretical and practical implementation have assumed eight series-connected PV array panels achieving a maximum nominal power of 432 Wp. Therefore, Table 3 compares the theoretical RMS values of the MZI and SP-IZI.

Table 2. Main specifications of the Kyocera KC 50 module in STC.

Parameters	Values
Maximum power (P_{MAX})	54 W
Maximum power voltage (V_{MPP})	17.4 V
Maximum power current (I_{MPP})	3.11 A
Open-circuit voltage (V_{OC})	21.7 V
Short-circuit current (I_{SC})	3.31 A

Table 3. Comparison between the main values of MZI and SP-IZI operating in STC.

Parameters	MZI [39,40]	SP-IZI
Maximum coupling capacitors' voltage	206.72 V	180 V
Maximum switches voltage	V_{si} = 485.12 V V_{So} = 276.32 V	V_{s1} = 249.2 V Vs_2 = 249.2 V
Maximum diodes voltage	V_{Di} = −415.52 V V_{Do} = −276.72 V	V_{D1} = −249.2 V_{D3} = −110.4 V
RMS output inductor current	3.439 A	3.394 A
Average input inductor current	3.11 A	2.87 A
RMS input inductor current	7.14 A	6.20 A
Average switches current	I_{si} = 3.11 A Iso = 1.536 A	I_{S1} = 3.09 A I_{S2} = 1.528 A
RMS switches current	I_{si} = 7.718 A I_{so} = 4.705 A	I_{S1} = 7.737 A I_{S2} = 5.237 A
Average diodes current	I_{Di} = 3.11 A I_{Do} = 1.536 A	I_{D1} = 3.09 A I_{D2} = 1.528 A
RMS diodes current	I_{Di} = 7.14 A I_{Do} = 4.705 A	I_{D1} = 7.737 A I_{D2} = 5.237 A

The SP-IZI presents current through all passive elements. Therefore, the semiconductors' currents are the sum of the inductors' currents, resulting in not much higher RMS values when compared to the MZI. Thus, these currents can cause conduction losses in the semiconductors. On the other hand, the currents through the inductors present lower values in SP-IZI.

4. Experimental Results

An experimental prototype was developed to evaluate the SP-IZI, as depicted in Figure 9. The experimental setup employs the discrete IGBT IRGP4650D (Infineon, Neubiberg, Germany) and 30ETH06 diodes (International Rectifier, El Segundo, CA, USA). The characteristics curves of the PV array were performed using a bidirectional PV array emulator IT6012C-800-50 (Itech, New Taipei City, Taiwan) in conjunction with the software SAS100L (Itech). The entire system was controlled using a digital signal controller (DSC), a TMS320F28335 (Texas Instruments, Dallas, TX, USA), in which the current and voltage quantities were measured by means of signal-conditioning boards that employ Hall-effect transducers (LEM, Geneva, Switzerland). The system's algorithms were embedded in the DSC. The experimental results were obtained by digital oscilloscope, the TPS2024 (Tektronix, Beaverton, OR, USA), while the power factor (PF) and total harmonic distortion were measured using the Power Quality Analyzer 43B (Fluke, Everett, WA, USA). Table 4 presents the main parameters employed in the experimental tests of the SP-IZI.

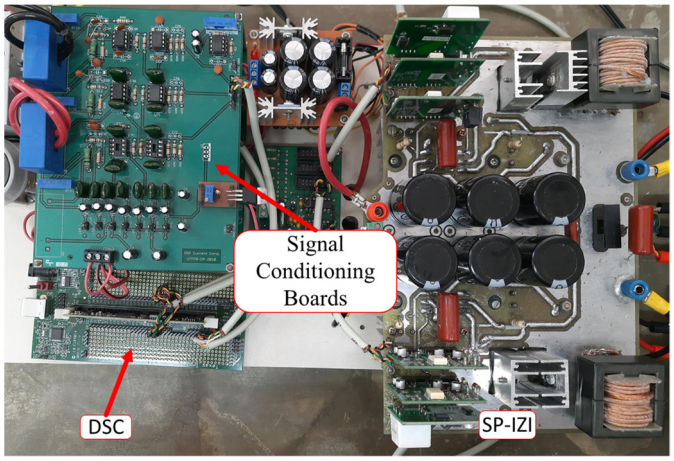


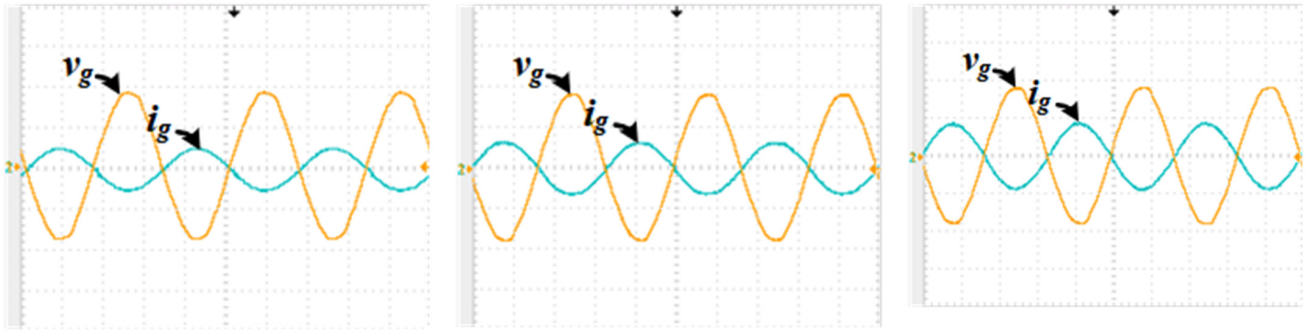
Figure 9. Experimental prototype of SP-IZI.

Table 4. Main SP-IZI parameters.

Parameters	SP-IZI
The nominal utility RMS voltage	V_o = 127 V
Nominal utility frequency	f = 60 Hz
Switching frequency	f_s = 50 kHz
Sampling frequency A/D converter	f_a = 60 kHz
Input DC-Bus capacitance	$C_{dc1} = C_{dc2}$ = 4500 µF
Nominal input DC-bus voltage	v_{PV} = 146.26 V
Input inductive filter	$L_{m1} = L_{m2}$ = 60 µH
Output inductive filter	L_o = 1.0 mH
Coupling capacitances	$C_1 = C_2$ = 1.0 µF
Nominal power	P = 432 W
Phase margin of the inner current control	P_{mi} = 76.8°
Crossover frequency of the inner current control	f_{ci} = 1220 Hz
Phase margin of the outer voltage control	P_{mo} = 80°
Crossover frequency of the outer voltage control	f_{co} = 10 Hz
PWM gain	K_{PWM} = 1/2999
Voltage PI controller gains	K_{pv} = 0.2157; K_{iv} = 1.1257
Current PI controller gains	K_{pi} = 20.826; K_{ii} = 1.5412 × 10^6
Unbalance gain	K_{unb} = 0.15
PLL PI controller gains	K_{PPLL} = 423.4; K_{iPLL} = 32234
Adaptive filter step size parameter (AF-pPLL)	μ_{AF} = 0.007
Sampling time (AF-pPLL)	60 kHz
Adaptive filter gain (AF-pPLL)	K_{AF} = 420

Firstly, the SP-IZI was evaluated for three different levels of solar irradiance employing the PV emulator, in which the PV array voltage was equal to 140 V. Hence, the peak amplitude of the inverter currents injected into the grid is described as follows: (i) Scenario 1: 2 A; (ii) Scenario 2: 3 A; and (iii) Scenario 3: 4.8 A.

Figure 10 shows the grid voltage and the current injected into the grid for the three evaluated scenarios. As noted, the grid-injected currents present sinusoidal waveforms in opposite-phase to the grid voltage for all the considered scenarios.



(**a**) (**b**) (**c**)

Figure 10. Experimental grid-injected current and grid voltage considering the three different scenarios (100 V/div, 5 A/div, 5 ms/div): (**a**) Scenario 1; (**b**) Scenario 2; (**c**) Scenario 3.

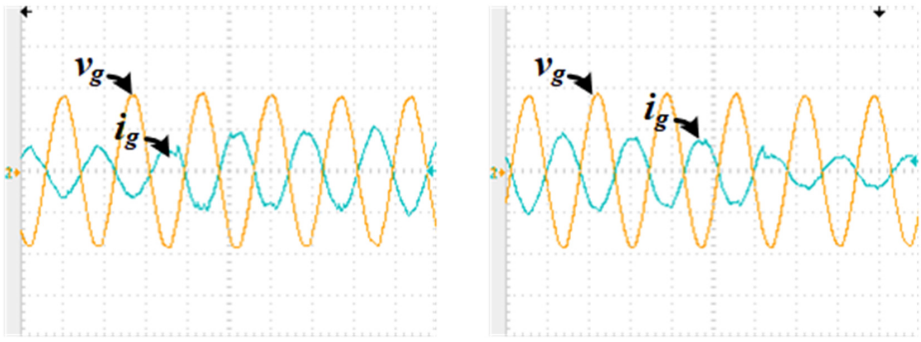
Figure 11 shows the total harmonic distortion (THD) for the three inverter currents shown in Figure 10. It can be observed that the SP-IZI currents are sinusoidal, meeting the requirements of the standards [41,42], i.e., the injected currents presented a maximum THD of around 3.3%, validating the feasibility and theoretical development of the proposed inverter.

(**a**) (**b**) (**c**)

Figure 11. THD of the current injected into the grid for the three evaluated scenarios: (**a**) Scenario 1; (**b**) Scenario 2; (**c**) Scenario 3.

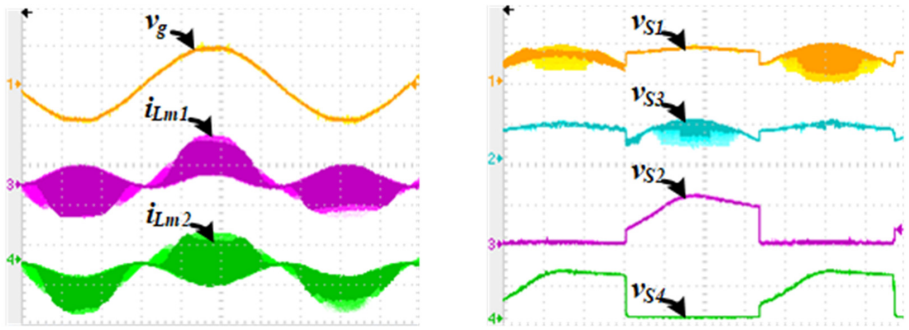
Figure 12 presents the dynamic performance of the SP-IZI considering changes in solar irradiance. The changes are performed from half of the power rate to nominal PV array power rate and vice versa (50% to 100% and 100% to 50%). As can be observed, the proposed SP-IZI acts very fast when abrupt solar irradiance changes occur.

The currents through the inductors L_{m1} and L_{m2} are presented in Figure 13a, while the voltages across the switches S_1, S_2, S_3, and S_4 are presented in Figure 13b. It can be noted that the experimental results presented in Figure 12 can be compared and evaluated to the theoretical development shown in Figure 3. These results demonstrated that the proposed SP-IZI operates following the developed mathematical equations and that the inverter is feasible and reliable.



(**a**) (**b**)

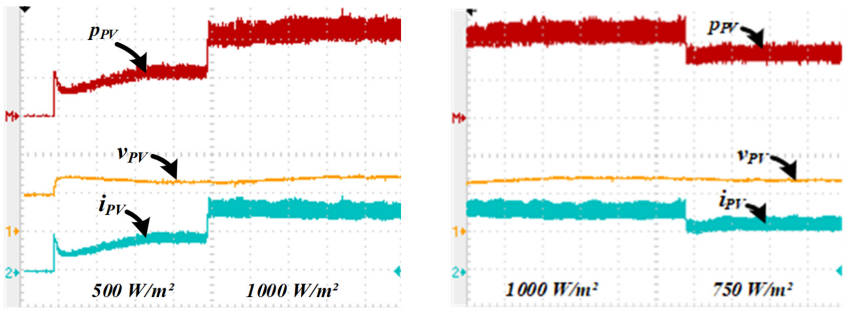
Figure 12. Experimental results for dynamic solar irradiance changes (100 V/div, 5 A/div, 10 ms/div): (**a**) transition from half to nominal PV array power rate; (**b**) transition from nominal to half of the PV array power rate.



(**a**) (**b**)

Figure 13. Experimental results (200 V/div, 10 A/div, 2.5 ms/div): (**a**) grid voltage and the current through the inductors L_{m1} and L_{m2}; (**b**) Voltages across the switches S_1, S_2, S_3, and S_4.

In STC, the performance of the P and O MPPT algorithm was evaluated considering the solar irradiance change from 500 W/m^2 to 1000 W/m^2 and from 1000 W/m^2 to 750 W/m^2, as shown in Figure 14. As observed, the P and O MPPT technique used in the SP-IZI can reach the maximum power point and acts very fast during abrupt solar irradiance changes. In addition, Figure 14 shows that the PV array voltage is below 160 V in all cases, while the grid peak voltage is near 200 V [see Figure 13a]. This demonstrates that the proposed SP-IZI can boost the input voltage and, simultaneously, injects in the grid a sinusoidal and regulated current into the utility with low harmonic distortion, as discussed above. Hence, all such results demonstrate that the proposed converter is useful and suitable for PV applications.



(**a**) (**b**)

Figure 14. Experimental results evaluating the P-and-O-based MPPT algorithm performance considering transitions in solar irradiance (100 V/div, 2 A/div, 200 W/div, 5 s/div): (**a**) 500 W/m^2 to 1000 W/m^2; (**b**) 1000 W/m^2 to 750 W/m^2.

5. Conclusions

This paper presented the implementation of an integrated inverter topology based on Zeta converters named SP-IZI. The proposed inverter increased the input voltage (PV array voltage) and injected a sinusoidal current into the grid with low total harmonic distortion.

The SP-IZI presented advantages compared to the MZI when both inverters were operating in DCM. The voltages across the semiconductors and coupling capacitors are lower and do not depend on the input inductance or the operation stages. The operation of the SP-IZI is similar to the conventional DC-DC Zeta converter, in which the third stage is well-defined. The SP-IZI presents the following advantages compared to the MZI: (i) the voltage in coupling capacitors is 13% lower; (ii) voltage stresses in switches and diodes are 40% lower; and (iii) static gain is similar to the traditional Zeta converter.

From the employed modeling technique, the SP-IZI transfer functions for the inner and outer control loops were derived. In addition, by the analysis of frequency response, it was possible to obtain the proportional and integral gains of the PI controllers.

Through experimental results, the effectiveness and feasibility of an SP-IZI were evaluated and demonstrated. In addition, simulation and experimental results corroborated the theoretical development.

As could be observed from the achieved results, the proposed SP-IZI can replace—with advantages—the traditional PV system constructed by the cascade association of a step-up DC-DC converter and a voltage source inverter.

6. Patents

This work resulted in a patent with the process number BR 10 2022 004213 6.

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Conflicts of Interest: The authors declare no conflict of interest.

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